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Gate capacitance model for the design of graphene nanoribbon array field-effect transistors

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In graphene nanoribbon (GNR) array field-effect transistors with sufficiently narrow ribbon widths and ribbon-to-ribbon distances, the gate capacitance and relevant carrier mobility are strongly affected by fringe field effects at the ribbon edges and the fringe fields between neighboring GNRs may overlap. To overcome the difficulties of predicting the channel properties of GNR array devices in design and characterization and of extracting accurate carrier mobility with complex fringe field effects, a simplified model for the prediction of gate capacitances in the GNR array channels of field-effect devices was developed. Numerical analyses were carried out, first, using the finite element method to understand how the gate capacitance of the GNR array channel is affected by changes in the configuration of the GNR arrays and the choice of gate dielectrics. Based on this analysis, a general model for determining the gate capacitance as a function of various configurations and material variables was formulated. This model was verified by performing additional finite element analyses and by making comparisons with previously reported experimental results. Good agreement among this data implies the generality of this model.

Introduction

Graphene has drawn significant interest as a potential alternative to silicon, which is used in current complementary metal-oxide-semiconductor (CMOS) technologies, for nanoelectronic applications, because of its extraordinary electronic properties, including high carrier mobility and tunable bandgap.[1-3] A two-dimensional monolayer graphene sheet intrinsically has a zero bandgap. It is, therefore, necessary to open and tune its bandgap by techniques including hydrogenation,[4] doping,[5] and lithographic patterning[6-8] for use in device applications. Among these methods, patterning the graphene into nanoribbons with sub-10-nm widths was suggested as a promising strategy based on ab initio calculations[9,10] and was verified experimentally.[6-8,11,12] In these experiments, the bandgap scaled inversely with ribbon width because of quantum confinement. Theoretical predictions show that field-effect transistors (FETs) employing graphene nanoribbons (GNRs) as a channel material can meet the requirements of next-generation devices.[3] The recent development of techniques used to achieve high-density aligned GNR arrays[13-15] may allow the creation of wafer-scale devices based on GNRs.

Understanding the key factors affecting carrier mobility in graphene is important for gauging and improving the performance of graphene-based electronic devices. Although the mobility in graphene sheets is extremely high, it decreases with decreasing ribbon width in GNRs.[3] In general, the scaling of the dimensions of a material causes a change in carrier transport, resulting from charge redistribution and edge/boundary scattering, thus affecting the mobility. The reduction of mobility in GNRs is mainly due to edge scattering and fringe field effects at the ribbon edges.[9,16] Particularly in GNR arrays, because both the ribbon width and the distance between GNRs are small, the fringe fields of individual GNRs may overlap (which does not occur for a single GNR). Consequently, complex fringe fields influencing the device performance will depend on both the channel dimensions such as ribbon width and ribbon-to-ribbon distance and the kind and thickness of the gate insulators.

Because the fringe field effect causes changes in the gate capacitance, and thus, the field-effect mobility of the GNR array channels, it is necessary to understand systematically how the gate capacitance changes with different configurations of GNR arrays when designing two-dimensional field-effect devices and extracting accurate carrier mobility. However, as yet, no general model is available to describe the effect of fringe fields on the gate capacitance because of the complex interference between fringe fields of individual GNRs in the array. Therefore, this study aims to develop a simple general model to predict the changes in the gate capacitance with different configurations and dimensions of GNR arrays and different kinds of gate insulator materials. Finite element (FE) analyses were carried out first; the results were summarized in a formula, which is a general capacitance

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model. The generality of this capacitance model has been verified with additional FE calculations and comparison with the experimental results in the literature.

Numerical modeling

For a single GNR channel, the fringe effect of the GNR can significantly affect the gate capacitance as the width of the GNR becomes sufficiently narrower than the thickness of the dielectric layer. In such a case, the effective gate capacitance, C_{tot}, of a single GNR channel consists of the fringe capacitance, C_f, and the parallel plate capacitance of the GNR, C_{2D}, as schematically illustrated in Fig. 1(a). Using the equivalent circuit representation, C_{tot} can be estimated via a semi-empirical model:[17]

$$C_{tot} = \varepsilon_{ox}\varepsilon_0\left\{\frac{\pi}{\ln[6(t_{ox}/W_{ch}+1)]W_{ch}} + \frac{1}{t_{ox}}\right\} \quad (1)$$

where ε_{ox} is the dielectric constant of the gate dielectric, t_{ox} is the thickness of the gate dielectric, W_{ch} is the width of the GNR channel, and ε_0 is the vacuum permittivity. This model cannot be used for a GNR array channel because the additional capacitance term, caused by the overlapping of the fringe fields of the adjacent GNRs in the trench regions between the GNRs, arises. The total capacitance is the sum of the parallel-plate capacitance, C_{2D}, the fringe capacitance contributed by the outermost GNR edges of the GNR array channel (the outermost fringe capacitance), C_{f1}, and the fringe capacitance contributed by the trench regions between the GNRs inside the GNR array channel (the inner fringe capacitance), C_{f2}, as illustrated in Fig. 1(b). In this case, it is not straightforward to estimate C_{tot} using a simple model like Eqn. (1) and a numerical tool such as the finite element method (FEM) can be a convenient means to estimate both C_{tot} and the component capacitances, C_{2D}, C_{f1}, and C_{f2}. In this study, an FE package, COMSOL, was used for this purpose. Fig. 1(c) shows the FEM model (mesh) of the GNR array FET used for the simulation. The FE model consists of a gate dielectric, a GNR array channel, and vacuum as measurement environment. The lengths of the GNRs were assumed to be 1 m. Therefore, the capacitances calculated in the FE analyses are given per unit length, with units of $F \cdot m^{-1}$. The geometric variables are the width of individual GNRs, w_{GNR}, and the distance between the GNRs, d_{inter}. If the channel width, W_{ch}, is fixed, the number of GNRs, N_{GNR}, and the number of the inter-GNR trench regions, N_d, will be automatically determined. The material variables are the thickness, t_{ox}, and the dielectric constant, ε_r, of the gate insulators. For a quantitative description of the changes in the total gate capacitance, C_{tot}, with different design variables, changes in the component capacitances, C_{2D}, C_{f1}, and C_{f2}, were considered as functions of the design variables, in the context of the equivalent circuit representation described in Fig. 1(b).

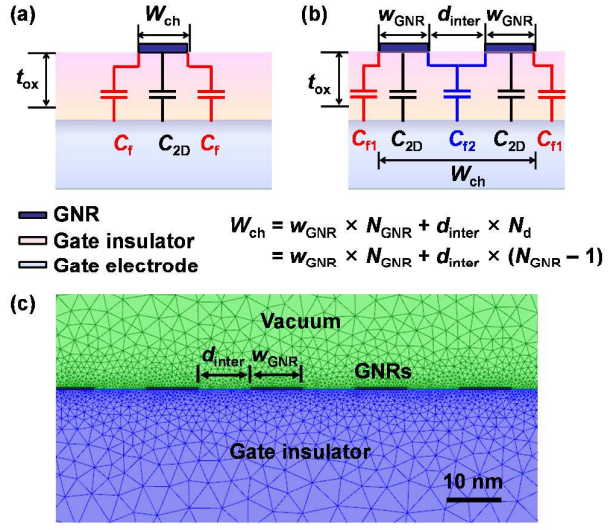

Fig. 1 Equivalent circuit representation of (a) a single GNR channel and (b) a GNR array channel for the estimation of gate capacitances and (c) the FEM model (mesh) for calculating the total gate capacitance of a GNR array FET.

Results and discussion

Numerical results

First, the effect of the geometric variables on the capacitances was investigated. Fig. 2(a) shows the changes in the component capacitances and total capacitance for different widths of GNR array channel, W_{ch}. In this case, the gate dielectric was assumed to be a 300-nm-thick SiO_2 layer. w_{GNR} and d_{inter} are both fixed at 10 nm; therefore, an increase in W_{ch} corresponds to an increase in the number of GNRs within the channel, N_{GNR}, and an increase in the number of inter-GNR trench regions, N_d (= N_{GNR} – 1). Both C_{2D} and C_{f2} increase linearly with increasing W_{ch} (= N_{GNR}). On the other hand, the change in C_{f1} with different values of W_{ch} appears to be logarithmic. C_{f1} increases relatively rapidly only for small values of W_{ch} (smaller than roughly 50 nm (inset of Fig. 2(a))); thereafter, the rate of increase becomes smaller with increasing W_{ch}. Consequently, C_{tot} is mainly influenced by C_{2D} and C_{f2}, whereas the effect of C_{f1} is limited, especially for large values of W_{ch}.

Fig. 2(b) shows the changes in the capacitances for different values of d_{inter}. In this case, W_{ch} and w_{GNR} were fixed at 4 μm and 10 nm, respectively, and only d_{inter} was varied. Therefore, as d_{inter} increases, N_{GNR} (and also N_d) will decrease. In this case, C_{f1} remains practically constant, regardless of the value of d_{inter}. Together with the results in Fig. 2(a), this result indicates that C_{f1} is primarily dependent on W_{ch}. C_{f2} increases with increasing d_{inter} and then decreases after reaching a maximum at d_{inter} = 70 nm. Additionally, the average inner fringe capacitance or inner fringe capacitance per inter-GNR trench, c_{f2} (C_{f2} divided by N_d), increases at a constantly decreasing rate as d_{inter} increases (inset of Fig. 2(b)). On the contrary, C_{2D} decreases with increasing d_{inter} because a larger d_{inter} value implies a smaller area fraction of GNR region for a fixed value of W_{ch}—in fact, the C_{2D} values in Fig. 2(b) divided by N_{GNR} (= N_d + 1) are almost constant. This result shows that the

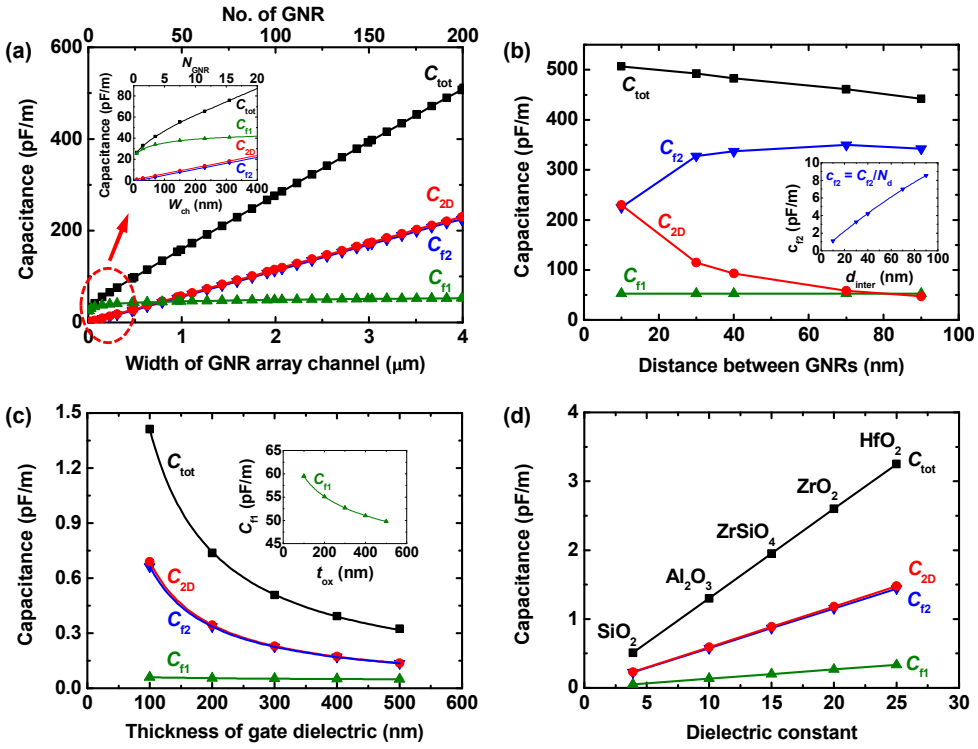

Fig. 2 Component and total gate capacitances of GNR array channels with: (a) different widths of GNR array channels, (b) different distances between GNRs, (c) different thicknesses of gate dielectrics, and (d) different dielectric constants of the gate dielectrics. The insets in (a) and (c) show enlarged plots. The inset in (b) shows the average inner fringe capacitance of the GNR array channels.

parallel plate capacitance of the GNR itself is independent of the channel geometry, unless W_{ch} is very small. As in the relation of W_{ch} and C_{tot} in Fig. 2(a), when d_{inter} varies, C_{tot} is mainly influenced by C_{2D} and C_{f2}.

Next, the material aspect of the changes in the capacitances is considered. When the thickness of the gate dielectric, t_{ox}, is varied for the SiO_2 gate dielectric and the GNR array consists of 200 GNRs with w_{GNR} = 10 nm and d_{inter} = 10 nm, the FEM predicts that all of the capacitance components will decrease as a power of t_{ox}, as shown in Fig. 2(c). In this case, while the exponents for C_{2D} and C_{f2} seem to be almost identical, that for C_{f1} is significantly smaller (inset of Fig. 2(c)). Thus, C_{tot} is again shown to be mainly affected by C_{2D} and C_{f2}. If the SiO_2 is replaced by an insulator material that has a higher dielectric constant and fixing t_{ox} at 300 nm for the same GNR array geometry, the FEM predicts that all of the capacitance components will increase linearly with the increasing dielectric constant, as shown in Fig. 2(d). That is, everything else being equal, the capacitances are affected only by the non-geometric parameter and the capacitances are proportional to the dielectric constant of the gate insulators.

Simplified capacitance model

Based on the numerical results shown in Fig. 2, the component capacitances—the parallel plate capacitance, C_{2D}, the outermost fringe capacitance, C_{f1}, and the inner fringe capacitance, C_{f2}—can now be described as functions of design variables in the formulations that follow. First, C_{2D}, which is the capacitance of the GNR body itself, is predicted to be proportional to $w_{GNR} \times N_{GNR}$—the total area of the GNRs—as seen in Figs. 2(a) and 2(b). It is, therefore, expressed as

$$C_{2D} = a_0 \times w_{GNR} \times N_{GNR} \quad (2)$$

where a_0 is the proportionality coefficient, which contains ε_0, ε_r, and t_{ox}.

Next, the outermost fringe capacitance, C_{f1}, is logarithmically proportional to the total channel width, as seen in Fig. 2(a). This capacitance is expressed as

$$C_{f1} = a_1 + b_1 \times \ln W_{ch} = a_1 + b_1 \times \ln(w_{GNR} \times N_{GNR} + d_{inter} \times N_d) \quad (3)$$

where the constant a_1 and the coefficient b_1 are determined by the material parameters, ε_0, ε_r, and t_{ox}, and $N_d = N_{GNR} - 1$.

Finally, the average inner fringe capacitance, c_{f2} (= C_{f2}/N_d), resulting from the overlap of the fringe fields of two neighboring GNRs, increases with the ribbon-to-ribbon distance, as shown in the inset of Fig. 2(b), yielding the relation:

$$c_{f2} = C_{f2}/N_d = a_2 \times d_{inter} + b_2 \times d_{inter}^2 \quad (4)$$

where the constant a_2 and the coefficient b_2 are determined by the material parameters, ε_0, ε_r, and t_{ox}.

In addition, all of the capacitance components are given by powers of t_{ox} for a given gate dielectric material (Fig. 2(c)); they show a linear dependence on ε_r for a given value of t_{ox} (Fig. 2(d)).

By fitting the numerical results to the formulae presented above with some trial and error, constants a_0 through b_2 and the exponents of the base t_{ox} were obtained. Subsequently, a

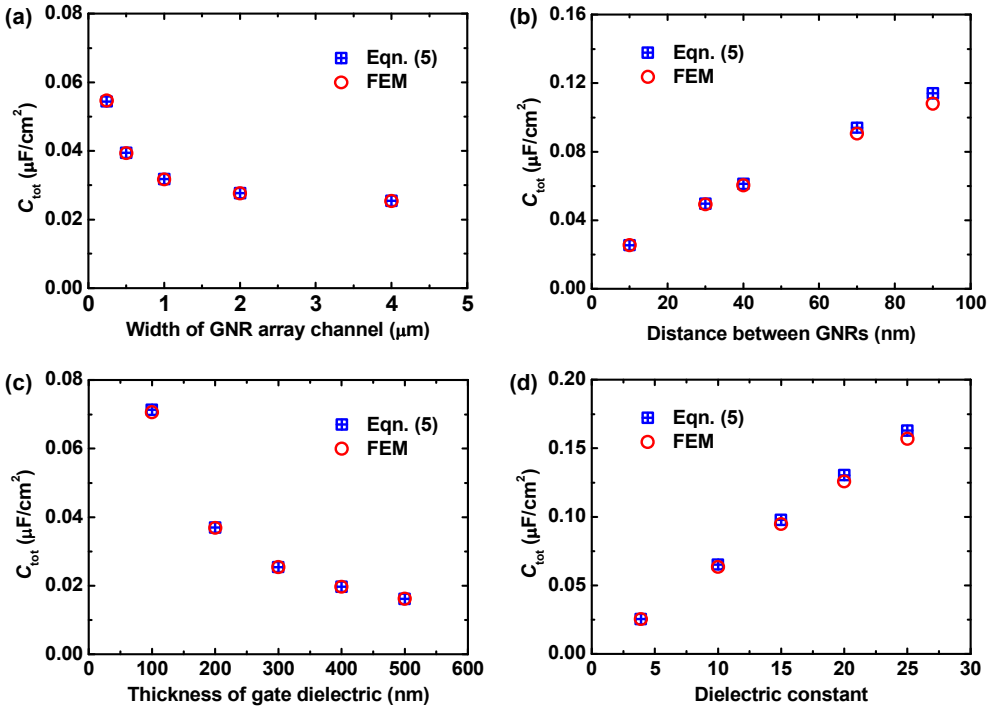

Fig. 3 Comparison of total gate capacitances predicted using Eqn. (5) and FEM, for GNR array channels with: (a) different widths of GNR array channels, (b) different distances between GNRs, (c) different thicknesses of gate dielectrics, and (d) different dielectric constants of the gate dielectric. The accuracy of the fitting coefficients and parameters in the simplified capacitance model of Eqn. (5) was assessed.

simplified capacitance model formula for the total capacitance, C_{tot}, was derived:

$$\begin{aligned} C_{tot} &= C_{2D} + C_{fl} + C_{f2} \\ &= \varepsilon_0\varepsilon_r\{w_{GNR}N_{GNR}/t_{ox} + [0.7 + 0.03\ln(w_{GNR}N_{GNR} + d_{inter}N_d)]/t_{ox}^{0.1} \\ &\quad + (d_{inter} - 1.25\times10^{-6}d_{inter}^2)N_d/t_{ox}\} \end{aligned} \quad (5)$$

For simplicity, in this formula, the constant, 0.7, the coefficients, 0.03 and 1.25 × 10^{-6}, and the exponents, 1.0 and 0.1, of the base t_{ox}, are chosen to be round numbers of the actual fitting parameters. Therefore, using Eqn. (5) to predict the gate capacitance may generate small errors. To assess whether the errors are acceptable, the C_{tot} values were calculated using Eqn. (5) and then compared to the FE solutions in Fig. 2, in terms of capacitance per unit area (square centimeter). As shown in Fig. 3, the total gate capacitances predicted using Eqn. (5) and FEM well coincide with tiny errors of 1.3±1.8%., and therefore, the use of round numbers in place of the actual fitting parameters in Eqn. (5) is justified.

Verification of the simplified capacitance model

In each numerical analysis to obtain the capacitance models of Eqns. (2) to (5), the component capacitances were described as functions of a single design variable while the other variables were fixed. One may, therefore, question the

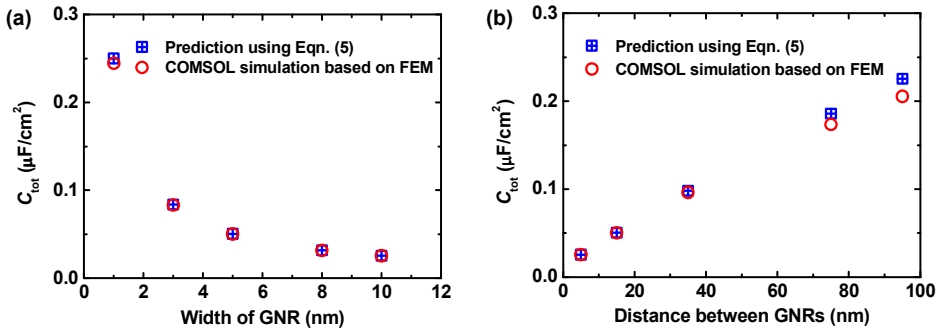

Fig. 4 Comparison of total gate capacitances of GNR array channels for: (a) different widths of GNR and (b) different distances between GNRs. These two cases were not considered in the derivation of Eqn. (5). However, the total capacitances predicted using Eqn. (5) agree well with the FEM simulation results, demonstrating the generality of the simplified capacitance model of Eqn. (5).

Table 1 Comparison of the experimental results in the literature and the field-effect mobilities predicted using the simplified capacitance model developed in this study.

GNR type	W_{ch} (μm)	w_{GNR} (nm)	d_{inter} (nm)	Reported μ_{FE} ($cm^2V^{-1}s^{-1}$)	Predicted μ_{FE} ($cm^2V^{-1}s^{-1}$)	Reference
Array	1	10	10	25	24	[13]
Single	40	40	-	100	102	[17]
Array	200	3	500	1800[†]	30	[18]

[†] This field-effect value was obtained on ignoring the fringe field contribution to the total gate capacitance.

generality of the simplified capacitance model. To verify whether the use of Eqn. (5) can be extended to other cases beyond those considered for Fig. 2 to derived itself, additional FEM simulations were carried out to obtain C_{tot} for the two cases of: i) combinations of changing w_{GNR} and d_{inter} with w_{GNR} + d_{inter} = 20 nm and a fixed W_{ch} value of 4 μm, and ii) changing d_{inter} with a fixed w_{GNR} value of 5 nm and a fixed W_{ch} value of 4 μm. At the same time, Eqn. (5) was used to calculate C_{tot} for these cases. Although these two additional cases had not been considered to derived Eqn. (5), once the C_{tot} values were calculated using Eqn. (5), the results agreed well with the FEM simulation results as shown in Figs. 4(a) and 4(b). This demonstrates that Eqn. (5) have general applicability.

The generality of Eqn. (5) was further evaluated by comparing the field-effect mobilities, μ_{FE}, reported in the literature[13,17] and the predicted μ_{FE} values based on the C_{tot} values estimated using Eqn. (5). As shown in Table 1, the mobilities predicted via Eqn. (5) are in good agreement with the previously reported values. In the last row in Table 1, there is a large discrepancy between the reported and predicted mobilities. In this case, the reported value was obtained without considering the effect of the fringe fields.[18] Such a marked difference is a clear indication that the fringe field has a significant effect on the total gate capacitance. This result is very important both when designing field-effect devices based on GNR arrays and when extracting accurate carrier mobility from the devices because the omission of fringe field terms leads to an overestimation of the field-effect mobility.

Conclusions

The GNR array channels of field-effect devices were treated as a circuit consisting of capacitors connected in parallel, while considering the interference between fringe fields of each GNR. Numerical analysis showed that the component capacitances of these GNR array channels were dependent on the configuration of the GNR arrays and the choice of gate dielectrics, which allowed the mathematical formulation of the component capacitances. Based on these results, a simple formula describing the gate capacitance of a GNR array channel was derived as a function of the GNR width, the numbers of GNRs and inter-GNR trench regions, the distance between GNRs, and the thickness and dielectric constant of the gate dielectrics. This model was verified numerically and experimentally, showing good agreement and implying its generality. This simplified capacitance model can be used not only to facilitate the estimation of channel properties in the design and characterization of the devices, but also to interpret experimental data and extract accurate carrier mobility.

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