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High-performance InGaZnO Thin-Film Transistor Incorporating a $HfO_2/Er_2O_3/HfO_2$ Stacked Gate Dielectric

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In this paper, a $HfO_2/Er_2O_3/HfO_2$ (HEH) stacked structure was developed as a gate dielectric for amorphous InGaZnO (α-IGZO) thin-film transistor (TFT) applications. Atomic force microscopy and X-ray photoelectron spectroscopy were used to study the morphological and chemical features of Er_2O_3 and HEH films. In comparison to the Er_2O_3 dielectric, the α-IGZO TFT device incorporating a HEH stacked dielectric exhibited a lower threshold voltage of 0.7 V, a higher I_{on}/I_{off} current ratio of 2.86×10^7, a larger field-effect mobility of 15.8 cm^2/V-s, and a smaller subthreshold swing of 101 mV/decade, suggesting a smooth surface at the dielectric-channel interface. Furthermore, the threshold voltage stability of α-IGZO TFT under positive gate voltage stress can be improved by using a HEH stacked structure.

Introduction

Amorphous indium gallium zinc oxide (α-IGZO) thin-film transistor (TFT) is a promising candidate for a switching element in flat, flexible, electric papers, and transparent display applications.[1] The silicon dioxide (SiO_2) is commonly used as a gate dielectric in α-IGZO TFTs.[2-3] However, due to its poor thermal conductivity,[4] the application of SiO_2 insulating layer in high-power and high-temperature logic devices is limited by the self-heating effect.[5] Therefore, the development of new insulating materials with good thermal conductivity and high dielectric constants has received much attention in recent years.[6-8] The search for suitable dielectric thin films at low temperatures has also been investigated for use in various display applications.[9-11] The most important criteria for a dielectric material are: a high band gap (>5 eV) and a favorable conduction or valence band offset (for n- and p-type semiconductors, respectively) to minimize the gate leakage current.[1, 12] Furthermore, the quality of the dielectric-semiconductor interface is a very important issue because the transistor performance can be very poor if the gate insulator with a rougher surface leads to excessive interface states.[12]

Rare-earth metal oxides (REOs) have been extensively studied because of their interesting properties, such as high dielectric constant, wide bandgap energy, high transparency, and high refractive index.[13-14] Erbium oxide (Er_2O_3) is one of the interesting REOs due to its multifunctionality in various fields of technology. Er_2O_3 has attracted considerable interest for applications in photonics, telecommunications and optics due to its photoluminescence and electroluminescence properties;[15] it can be used to substitute SiO_2 as the gate dielectric to suppress the gate leakage current with the scaling of complementary metal-oxide semiconductor (CMOS) devices because it possesses a combination of a large band gap (5–7 eV), a high dielectric constant (κ=~14) and high resistivity (10^{12}–10^{15} cm^{-3}).[16] Furthermore, its high chemical and thermal stabilities also makes an Er_2O_3 film as a protective and corrosion-resistant coating.[17] Mikhelashvili et al.[18] demonstrated that Er_2O_3 thin film showed a low gate leakge current and a high breakdown electric field. It also had a small hysteresis voltage and a low interface trap density in our previous report.[19] However, the hygroscopic nature of REO films can degrade their permittivity and surface morphology due to the formation of low-permittivity hydroxides.[20] To solve this issue, a triple layer dielectric structure was proposed to improve physical and electrical properties of both the gate/dielectric and the dielectric/α-IGZO channel.[21-23] The smooth surfaces are preferable regarding materials for TFT application because they generally provide higher carrier mobility, lower leakage current and better reliability.[24] Lee et al.[22] reported that α-IGZO TFT with $Al_2O_3/HfO_2/Al_2O_3$ gate dielectric had a smaller hysteresis width and lower subthreshold swing (SS) than that of HfO_2 dielectric. In this study, a novel $HfO_2/Er_2O_3/HfO_2$ (HEH) stacked structure was employed to improve interface properties of the dielectric/channel. We used atomic force microscopy (AFM) and X-ray photoelectron spectroscopy (XPS) to explore the surface morphologies and chemical compositions of Er_2O_3 and HEH films. In comparison with Er_2O_3 α-IGZO TFT, the HEH α-IGZO TFT device exhibited better electrical characterictics, such as a higher field-effect mobility (μ_{FE}), lower threshold voltage (V_{TH}), smaller (SS), and higher I_{on}/I_{off} current ratio. The stability of α-IGZO TFTs under positive gate bias stress (PBS) were also examined.

Experimental

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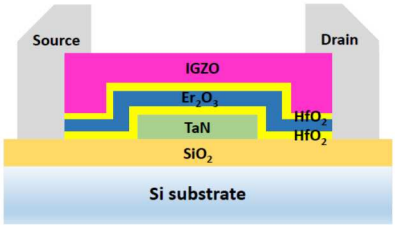

Fig. 1 Schematic diagram of the HEH stacked gate dielectric IGZO TFT device structure.

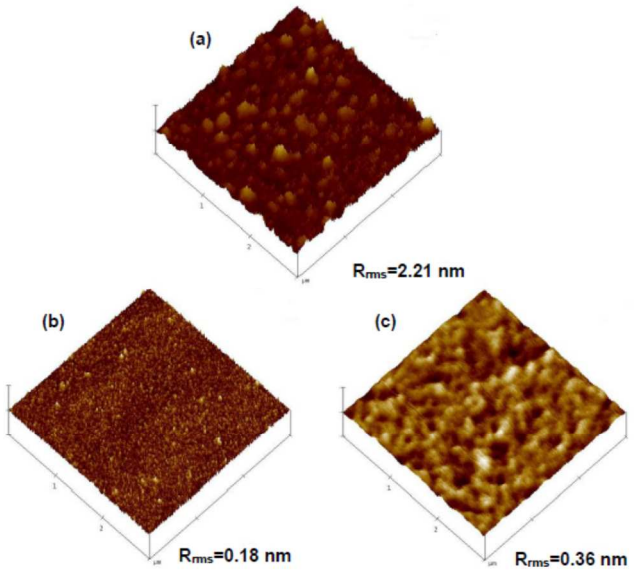

Fig. 2 AFM surface images of (a) Er_2O_3 (50 nm), (b) HfO_2 (6 nm), and (c) HEH (6 nm/38 nm/ 6 nm) dielectric films on the TaN/SiO_2.

Fig. 1 shows the cross section view of the HEH α-IGZO TFT device. The bottom gate staggered HEH α-IGZO TFTs were produced on the SiO_2/Si substrates. A 50-nm TaN film was deposited as a bottom gate through a reactive sputtering system. Then, a 6 nm HfO_2 film was grown by atomic layer deposition using tetrakis(ethylmethylamino)hafnium as the precursor and O_2 as the oxidizer at a temperature of 250 °C. A ~38 nm Er_2O_3 was deposited with sputtering from an Er target at room temperature, followed by furnace in O_2 ambient for 10 min at 300 °C. After the deposition of Er_2O_3 film, a 6 nm HfO_2 film was then grown to form a HEH sandwich stacked structure. The α-IGZO channel layer (~20 nm) was deposited on the HEH by using sputtering from a ceramic IGZO target (In_2O_3:Ga_2O_3:ZnO= 1:1:1) at room temperature. Subsequently, a 50-nm Al film is deposited by a thermal evaporation system and patterned for the source/drain (S/D) electrodes. The channel width/length (W/L) of TFT device was 100/10 μm. In

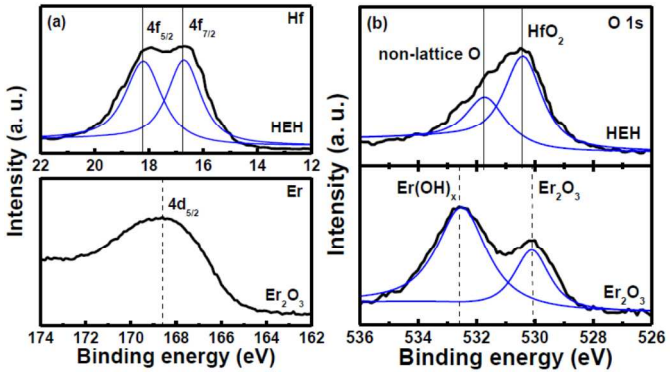

Fig. 3 (a) Er $4d_{5/2}$ and Hf 4f, and (b) O 1s energy levels in XPS spectra of Er_2O_3 and HEH dielectric films.

comparison with HEH α-IGZO TFTs, a ~50 nm Er_2O_3 gate dielectric was also fabricated to make α-IGZO TFTs.

The film composition of the dielectric films was investigated using XPS. The surface morphology and roughness of the films were analysed by AFM. The TFT characteristics and the PBS tests were performed at room temperature and in the dark using an Agilent semiconductor parameter 4156C. The V_{TH} is defined as the gate voltage (V_{GS}) when the normalized drain current (NI_{DS}=I_{DS}×L/W) reaches 1 nA. The SS was considered as the minimum value of $[d\log(I_{DS})/dV_{GS}]^{-1}$, where I_{DS} is the drain-source current. The μ_{FE} was extracted from the linear operation regime using the following formula[1]

$$\mu_{FE} = \frac{L \times g_m}{W \times C_{ox} \times V_{DS}} \qquad (1)$$

where g_m is the transconductance, V_{DS} is the drain-source voltage and C_{ox} is the gate capacitance per unit area.

Results and Discussion

Fig. 2 shows AFM surface images of the Er_2O_3, HfO_2 and HEH films on the TaN/SiO_2. The surface roughness of the Er_2O_3 film (2.21 nm) is higher compared with the HfO_2 film (0.18 nm). The surface roughness enhancement is a nonuniform moisture absorption of Er_2O_3, resulting in the nonuniform volume expansion of the film.[20] The cause of volume expansion is the density difference between $Er(OH)_x$ and Er_2O_3. The moisture absorption phenomenon is the reaction between the solid oxide (Er_2O_3) film and gaseous state water (H_2O) in air, which can be expressed as.[25]

$$Er_2O_3 + nH_2O_{(g)} \leftrightarrow Er_2(OH)_{2n} \qquad (2)$$

The Er_2O_3 film with a negative Gibbs free-energy value can cause a large moisture-absorption-reaction rate. In contrast, HfO_2 film possesses a positive Gibbs free-energy value to reduce the moisture-absorption-reaction rate. Therefore, the HEH film exhibits a smoother surface than the Er_2O_3 film, indicating that the HEH sandwich structure can suppress the moisture absorption of Er_2O_3 film.

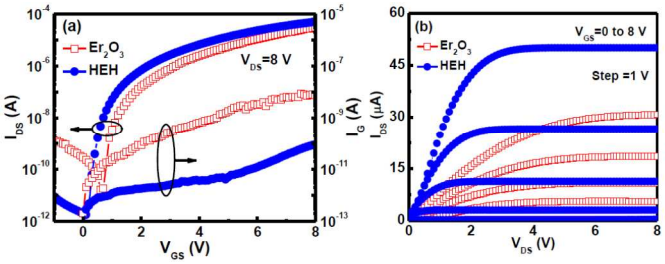

Fig. 4 (a) Transfer (I_{DS}-V_{GS}) and (b) output characteristics (I_{DS}–V_{DS}) of the Er_2O_3 and HEH IGZO TFT devices.

Fig. 3(a) shows the Er $4d_{5/2}$ and Hf 4f XPS spectra of Er_2O_3 and HEH dielectric films. The peak position of the Er $4d_{5/2}$ at 168.7 eV represented Er_2O_3,[26] while Hf $4f_{5/2}$ and $4f_{7/2}$ double peaks at 18.2 and 16.7 eV were assigned to HfO_2,[26] respectively. The O 1s spectra of Er_2O_3 sample in Fig. 3(b) can be deconvoluted to two chemical states: the low binding energy state at 530.1 eV can be related to O atoms in Er_2O_3[26] and the high binding energy state at 532.5 eV to O atoms in the $Er(OH)_x$. For HEH sample, the O 1s peaks at 530.4 and 531.7 eV represent the HfO_2[27] and non-lattice, respectively. The O 1s signal corresponding to $Er(OH)_x$ was a larger peak intensity than that of Er_2O_3, suggesting a high degree of the reaction between the water and Er_2O_3 causing hydroxide units to form in the Er_2O_3 film. On the contrary, no hydroxide peak was observed in the HEH sample. In addition, the O 1s peak corresponding to HfO_2 is larger intensity than that of non-lattice oxygen, possibly suggesting the formation of a stoichiometric HfO_2 film.

Fig. 4(a) shows the transfer characteristics (I_{DS}-V_{GS}) of the α-IGZO TFT devices incorporating Er_2O_3 and HEH gate dielectrics. The V_{TH} of the Er_2O_3 and HEH IGZO TFT devices is evaluated to be 1.16 and 0.7 V, respectively. The κ of the Er_2O_3 and HfO_2 dielectric films is determined to be ~14.1 and 10.7 from capacitance-voltage curves, respectively. The μ_{FE} of IGZO TFT devices incorporating Er_2O_3 and HEH gate dielectrics is 4.3 and 15.8 cm^2/V-sec, respectively. This high mobility is due to the smooth surface between the dielectric layer and IGZO channel, thus leading to less surface scattering at the dielectric-channel interface. Furthermore, the HEH TFT device has very low gate leakage current (I_{GS}~10^{-12}A) in the linear regime, while Er_2O_3 TFT is deteriorated by the increased I_{GS}. The I_{on}/I_{off} ratio of α-IGZO TFT devices fabricating Er_2O_3 and HEH gate dielectrics is 2.31×10^5 and 2.86×10^7, respectively. The SS value of the Er_2O_3 and HEH TFT devices is evaluated to be 268 and 101 mV/dec, respectively. The maximum states density (N_{it}) at the dielectric/channel interface of 5.46×10^{12} $cm^{-3}eV^{-1}$ for Er_2O_3 TFT and 1.01×10^{12} $cm^{-3}eV^{-1}$ for HEH TFT, were calculated by making the assumption that the interface states are independent of energy, using the following equation (3):[28]

$$N_{it} = \left(\frac{SS}{\ln 10}\frac{q}{kT} - 1\right)\frac{C_{ox}}{q} \qquad (3)$$

where q is the electronic charge, k is Boltzmann's constant, and T is the absolute temperature. The higher N_{it} of the Er_2O_3 TFT device suggests a larger interface trap densities at or near the Er_2O_3/IGZO interface. The output characteristics of typical α-IGZO TFT devices using Er_2O_3 and HEH gate dielectrics are presented in Fig. 4(b). It is clear that the driving current increases significantly for TFT using the HEH sandwich stacked structure. This result is attributed to the smooth surface at the dielectric/channel interface resulting in the higher mobility.

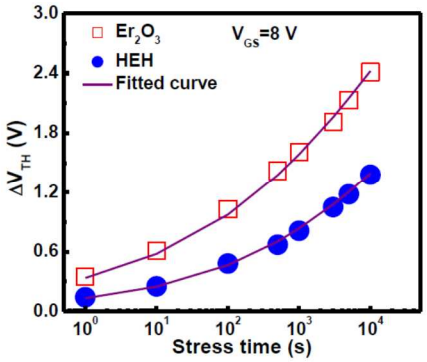

Fig. 5 Threshold voltage shift as a function of stress time for the Er_2O_3 and HEH IGZO TFT devices under PBS.

The device stability under operation is an important issue for the commercialization of α-IGZO TFT. PBS is one of the main factors which degrade the device performance as time passes. Fig. 5 shows the threshold voltage shift (ΔV_{TH}) as a function of stress time for the α-IGZO TFT devices fabricating Er_2O_3 and HEH gate dielectrics. The gate voltage stress was performed at V_{GS}=8 V for 10^4 s. The evolution of V_{TH} shift is found to fit the stretched-exponential equation as follows:[29]

$$\Delta V_{TH} = \Delta V_{TH0}\left[1 - e^{-\left(\frac{t}{\tau}\right)^{\beta}}\right] \qquad (4)$$

where ΔV_{TH0} is the ΔV_{TH} at infinite time, t is stress time, β is the stretched exponential exponent, and τ is the characteristic trapping time constant. This suggests that the V_{TH} instability is dominated by charge-trapping in the gate dielectric or at the interface of gate dielectric and IGZO channel.[30] The evolutions of threshold voltage under PBS well fit the stretched-exponential equation. The shift in V_{TH} is attributed to accumulated electrons near the dielectric–channel interface trapped by shallow acceptor-like trap states[31] or the oxygen molecular (negatively charged-oxygen) absorption in the IGZO channel caused the charge capture at the interface of dielectric and channel.[32] The high V_{TH} shift (2.41 V) of the Er_2O_3 TFT indicates that more electrons trapping near/at the Er_2O_3–IGZO interface, whereas the low V_{TH} shift (1.38 V) of the HEH TFT device suggests suppressed the trapped charge in the film because of a smooth surface at the dielectric-channel interface. In addition, the β value of the α-IGZO TFT device with Er_2O_3 and HEH gate dielectrics was extracted to be 0.25 and 0.29, whereas the τ value was 2.8×10^4 and 3.6×10^4 s, respectively.

Conclusions

In this study, we proposed a novel HEH stacked dielectric α-IGZO TFT device. The HEH stacked dielectric exhibited a smooth surface (from AFM) and no erbium hydroxide (from XPS). The α-IGZO TFT using a HEH stacked structure exhibited a lower V_{TH} of 0.7 V, a higher I_{on}/I_{off} ratio of 2.86×10^7, a larger μ_{FE} of 15.8 cm^2/V-sec, and a smaller subthreshold swing of 101 mV/dec, compared with that of Er_2O_3 dielectric. These results are attributed to the formation of a smooth surface at the dielectric-channel interface. In the case of α-IGZO TFT with HEH stacked structure, the device stability under PBS could be improved. It is expected that the HEH stacked

structure is a promising gate dielectric material to fabricate α-IGZO TFTs for future display applications.

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