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Improved Performance of Junctionless Tunnel Field Effect Transistor with Si and SiGe Hetero-Structure for Ultra Low Power Applications

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***Abstract*- In this paper, we present improved device characteristics of Junctionless Tunnel Field Effect Transistor (JLTFET) with Si and SiGe hetero-structure. Optimization of device is done for low power applications. Heterojunction engineering is done to optimize position of Si:SiGe junction. Subsequently, band gap engineering is incorporated using variations in, doping, gate work function, mole fraction of SiGe and dielectric constant. Comparison of optimized, hetero structure and silicon channel using numerical simulations indicates that I_{ON} increases from 0.12 to 15 µA/µm, I_{ON}/I_{OFF} from 4×10^6 to 3×10^9, subthreshold slope from 80 to 43mV/dec for 22nm channel with supply voltage of 0.7V.**

***Index Terms*- Junctionless Field Effect Transistors (JLFET); Tunnel Field Effect Transistor(TFET); Junctionless Tunnel Field Effect Transistor(JLTFET); SiGe; Hetero Junctionless Tunnel Field Effect Transistor(H-JLTFET)**

I. INTRODUCTION

Presence of two junctions in MOSFET causes size constraint and so its future. New perspective towards Lilienfeld's first transistor architecture [1] resulted in successful fabrication of a device which does not have any metallurgical junction thus solving the problem of constraint in geometry [2]-[8]. Junctionless FET (JLFET) could be used in applications such as SRAM, DRAM and Flash memory devices [9]-[11]. However OFF state current is significant in JLFET with less significant improvement in subthreshold swing which restraints it from vast applications. On the contrary, Tunnel Field Effect Transistors (TFET) are excellent for low power applications with very low leackage and low subthreshold slope[12] - [13]. However, their low I_{ON} restrained further high speed applications. There are various alternatives like germanium channel [14], III-V material channel [15] and strained silicon channel. However, OFF state drain side tunnelling is significant causing low current and current ON-OFF ratio in low band gap germanium, III-V materials have dielectric related issues and strained silicon has fabrication concerns.

Recently, Junctionless Tunnel Field Effect Transistor(JLTFET) has shown good ON state current and low subthreshold slope as blends benefits of JLFETs which causes high I_{ON} and TFETs which causes low subthreshold slope[16]-[20]. In this paper, we further improved characteristics with use of Si:SiGe heterojunction for Low Standby Power technology (LSTP) standards [21] of International Technology Roadmap for Semiconductors (ITRS) with fabrication ease. High band gap(1.11eV) Si is placed in drain side which generates weaker tunnelling in OFF state while low band gap(0.67eV) Ge strengths band to band tunnelling in ON state. Moreover, Si and SiGe heterojunction is widely accepted and it has one of the most workable process in hetero-structures. We performed heterojunction engineering to find the optimized position of hetero-junction. Following this characteristics are analysed with respect to variations in doping, work function, mole fraction of $Si_{1-x}Ge_x$ and dielectric. Drastic improvements are found with optimized hetero structure than Si-JLTFET. Finally, parasitic capacitances and unity gain frequency of device are extracted.

II. DEVICE AND SIMULATION CONDITIONS

A. Device Structure

Hetero Junctionless Tunnel Field Effect Transistor (H-JLTFET) does not contains any doping junctions as channel is uniformly n-type doped. Therefore, it is potential solution to the problem of random dopant fluctuations. H-JLTFET is structured using dual n^+ polysilicon control gate and dual p^+ polysilicon auxiliary gate at source side. The work function difference between control gate and channel causes intrinsic region using charge plasma concept while p^+ region is caused by auxiliary gate and channel work function difference resulting creation of p^+:i:n^+ regions. H-JLTFETs work on band to band tunnelling hence to implement higher I_{ON} and I_{ON}/I_{OFF} device with lower sub threshold slope, steeper energy bands have to be created with propinquity of bands in tunnelling region with higher band overlap.

Use of heterojunction of Si at drain side and SiGe at source side satisfies above conditions. Structure of Si:SiGe H-JLTFET is shown in Fig. 1 with heterojunction position, x_j at 34nm**.** Electron and hole concentration profile of Si:SiGe H-JLTFET is depicted in Fig. 2 as function of distance along the x-direction in ON state. The intrinsic region band energy shifts downward by applying sufficient positive gate voltage. This leads to p^+:n^+:n^+ regions from p^+:i:n^+ regions and hence making sufficient conditions for tunnelling. Device works on flat band when device is in ON state causing almost zero resistance while device is depleted of carriers in OFF state, giving no current. OFF state carrier concentration profile of proposed structure is shown in Fig.3.

Process attempts on Si: $Si_{1-x}Ge_x$ interface resulted significant progress and indicated it as a most suited potential candidate in hetero engineering [22]-[24]. $Si_{1-x}Ge_x$ source layer could be smoothly fabricated for x=0.15 to x=0.30. Higher mole fraction of Ge may lead to defects formation at the channel interface. Also, vertical hetero structures could be viable solution for fabrication of this device as vertical structures has resulted successful fabrication of many devices [23] - [29]. We have used HfO_2 as gate dielectric. It could be fabricated using atomic layer deposition (ALD) and through ALD, surface oxides are largely eliminated.

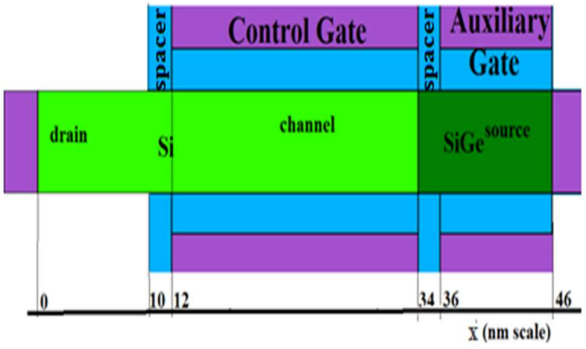

Fig. 1. Structure of Si:SiGe Hetero Junctionless Tunnel Field Effect Transistor (H-JLTFET) with heterojunction position, x_j at 34nm

B. Simulation setup

Simulations are done in SILVACO ATLAS 2D Device Simulator, using band to band tunnelling model (BBT) [30] for including effect of tunnelling. In BBT, we used non local models which are independent of electric field at individual mesh point and tunnelling current depends on the band structure along the cross section taken through the device[31]. As channel is heavily doped, Band Gap Narrowing (BGN) model has been added [31]. Other models include Shockley-Read-Hall (SRH) to model traps or defects[31]-[32], Schenk's Trap Assisted Tunnelling (TAT) model to account for electron tunnelling through the band gap via trap states[32] and Quantum Confinement (QC) model for interface trap effect and quantum confinement effect[31], [33] are also considered. Heavy doping and thin oxide are enough for creation of potential well in channel during inversion and therefore quantum confinement must be incorporated. Preset parameters used for device simulation of H-JLTFET as in Fig. 1 are tabulated in Table 1.

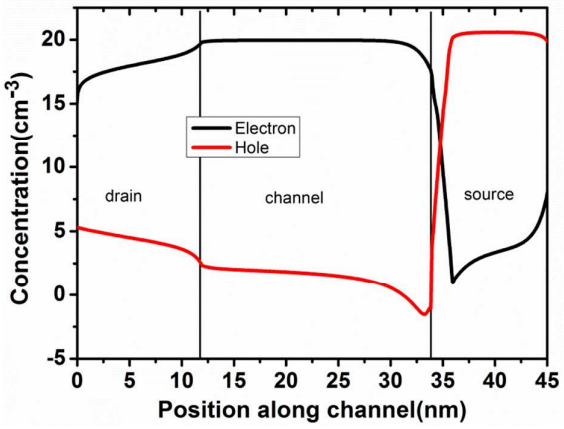

Fig. 2. Electron and hole concentration profile of Si:SiGe H-JLTFET as function of distance along the x-direction in ON state (V_{DS} = 0.7V, V_{GS} = 0.7V) at preset parameters

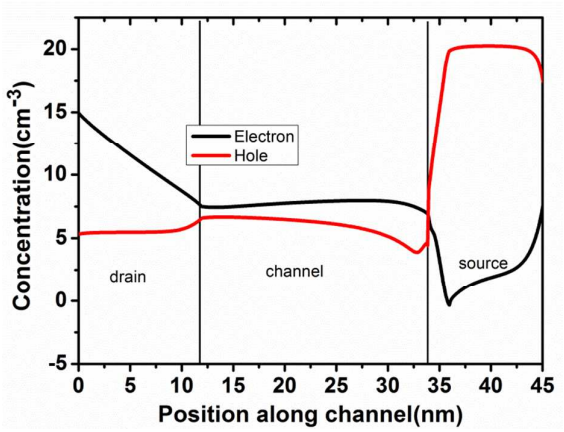

Fig.3. Electron and hole concentration profile of Si:SiGe H-JLTFET as function of distance along the x-direction in OFF state (V_{DS} = 0.7V, V_{GS} = 0V) at preset parameters

III. OPTIMIZATION OF H-JLTFET

Fig. 4 plots I_{ON} and I_{OFF} with respect to heterojunction position, x_j. As supply voltage is very low hence ON and some part of OFF state tunnelling occur in source region, contrary to TFETs where OFF state tunnelling mainly occurs in drain side. Therefore, variation in x_j across channel depicts smaller variation in ON and OFF currents till source region is covered by SiGe. Similarly, values of I_{ON}/I_{OFF} and subthreshold slope are finer with presence of SiGe at source side while they drop drastically in presence of larger band gap silicon material at source side. This is illustrated in Fig. 5. Two structures can be preferred from view of fabrication, first, Si:SiGe with hetero-junction, x_j at 34nm i.e. in situ SiGe source. There is no interaction of SiGe with gate dielectric and lesser region contains germanium which brings cost down. Second, homogeneous $Si_{1-x}Ge_x$ JLTFET structure which does not have any heterojunction. It works with problem of gate

insulator fabrication. Moreover, number of steps and power budget in process could be reduced because of absence of heterojunction. However, $Si_{1-x}Ge_x$ H-JLTFET exhibits lesser improvement in device performance when structural parameters are optimized. Furthermore, hetero-structure Si:SiGe has highly supressed tunneling between drain to channel than homogeneous SiGe device which brings very low leackage.

Table-1
Preset parameters for device simulation of H-JLTFET

Parameter	Value
Source/channel/drain doping (N_D) (Uniformly doped)	$1x10^{19}cm^{-3}$ (unless otherwise specified)
Effective Oxide Thickness(T_{OX})	2 nm
Control gate work function(Φ_G)	4.2eV (unless otherwise specified)
Auxiliary gate work function(Φ_S)	5.3eV
Gate Length (L_g)	22 nm
Hetero-junction position, x_j	34nm (unless otherwise specified)
Channel thickness(T_{ch})	5 nm
Supply voltage (V_{DD})	0.7V
Permittivity of Dielectric Material(ε_d)	25 (unless otherwise specified)
Spacers(low-k)	3.9
Mole fraction of $Si_{1-x}Ge_x$(x)	0.5 (unless otherwise specified)

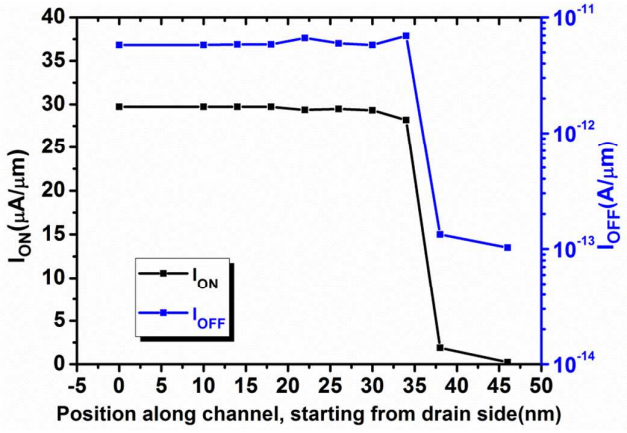

Fig. 4. ON and OFF state currents with respect to the position of hetero-junction, x_j of Si:SiGe H-JLTFET with V_{DD}=0.7V, Φ_G=4.2eV, ,ε_d=25, x=0.5 and $N_D=10^{19}cm^{-3}$

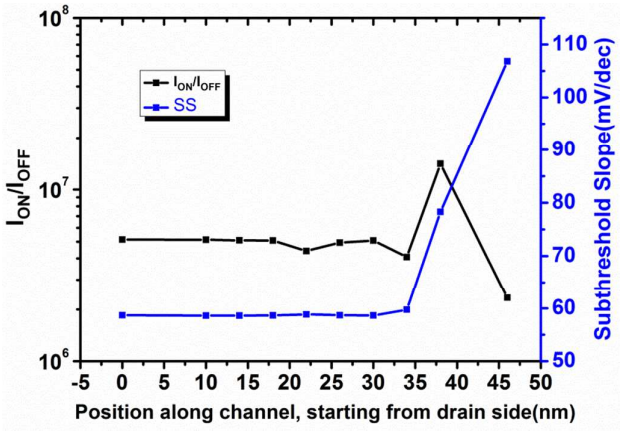

Fig. 5. I_{ON}/I_{OFF} and subthreshold slope with respect to the position of hetero-junction, x_j of Si:SiGe H-JLTFET with V_{DD}=0.7V, Φ_G=4.2eV, ε_d=25, x=0.5 and $N_D=10^{19}cm^{-3}$

Variation in concentration of dopant causes change in work function of semiconductor and hence energy band diagram of the device. Highest I_{ON}/I_{OFF} is obtained at channel doping, N_D of $10^{15}cm^{-3}$ as shown in Fig.6. Interestingly low process budget and low temperature process, intrinsic channel results highest ON and OFF state current ratio. However, at very high doping of 10^{19} energy band overlap increases causing higher I_{ON} and I_{OFF} and subsequently, lower I_{ON}/I_{OFF}. Reduction in workfunction of gate brings more electrons near surface. This results more band overlap bringing higher I_{ON} and I_{OFF}. Gate workfunction, Φ_G of 4.2eV yields highest I_{ON}/I_{OFF} . ON current and I_{ON}/I_{OFF} with work function of control gate material is shown in Fig. 7.

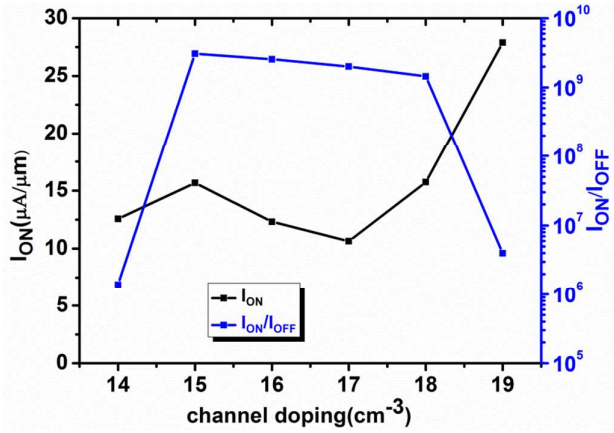

Fig. 6. ON current and ON and OFF current ratio versus channel doping with V_{DD}=0.7V, Φ_G=4.2eV, ε_d=25, x_j=34nm and x=0.5 for Si:SiGe H-JLTFET

One can increase current through increasing overlap region of bands. This can be done through higher mole fraction, x of germanium in source side $Si_{1-x}Ge_x$ which produces lower band gap near source side and turns higher drain current as shown in Fig. 8. However, fabrication of transistor with mole fraction, x higher than 0.5 carries issue of strain.

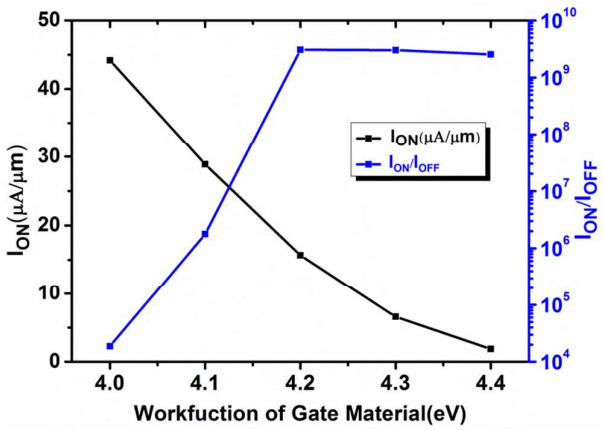

Fig. 7. ON current and ON and OFF current ratio versus work function of control gate material with V_{DD}=0.7V, N_D=10^{15}cm^{-3}, ε_d=25, x_j=34nm and x=0.5 for Si:SiGe H-JLTFET

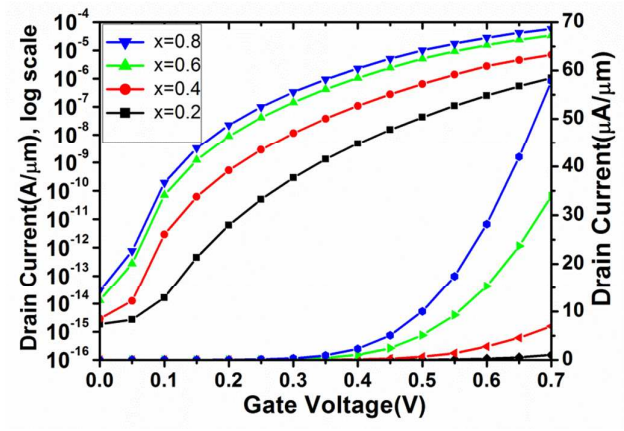

Fig. 8. Drain current versus gate voltage for varying mole fraction, x of $Si_{1-x}Ge_x$ with V_{DD}=0.7V, N_D=10^{15}cm^{-3}, Φ_G=4.2eV, ε_d=25 and x_j=34nm for Si:SiGe H-JLTFET

Substantial research has been done in dielectric materials for optimizing current [34] - [35]. Drain current is measured for four dielectrics namely $SiO_2(3.9), Si_3N_4(7), HfO_2(25)$and $TiO_2(80)$[36] – [37] as in Fig. 9. Increasing permittivity, increases ON state current and decreases OFF state current as gate control proliferates because of permittivity of dielectric. Consequently, I_{ON}/I_{OFF} rises along with significant improvement in subthreshold slope. I_{ON} and I_{ON}/I_{OFF} for TiO_2 are 125μA/μm and 9×10^9 respectively. There is more than 5×10^4 times improvement in I_{ON} for TiO_2 with reespect to SiO_2.

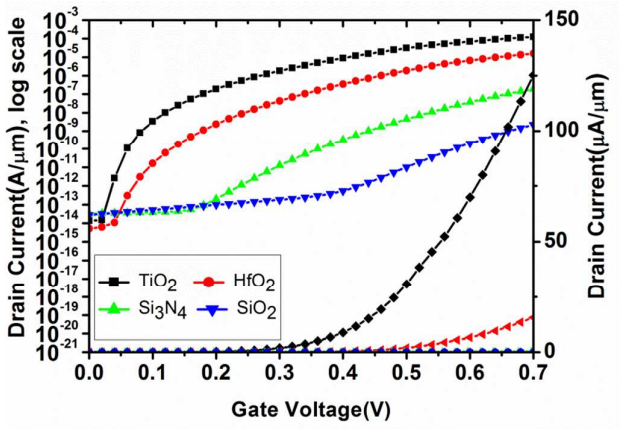

Fig. 9. Drain current versus gate voltage for varying permittivity with V_{DD}=0.7V, N_D=10^{15}cm^{-3}, Φ_G=4.2eV, x_j=34nm and x=0.5 for Si:SiGe H-JLTFET

IV. RESULTS AND DISCUSSIONS

Through variations of various device parameters, we found Φ_G=4.2eV, ε_d=25, x=0.5, x_j=34nm and N_D=10^{15}cm^{-3} result optimized device performance. However, above x=0.3 can create feasibility constraint of process. Therefore, till x=0.3 we can get performance improvement along with insignificant improvement in cost as we have removed doping junctions from structure. Transfer characteristic of proposed device is compared with Si JLTFET and $Si_{0.5}Ge_{0.5}$ JLTFET in Fig. 10. Clearly, Si:SiGe channel has much better transfer characteristics than Si and SiGe channels for low power applications. Si JLTFET has lower currents than SiGe JLTFET due to reduced band gap of $Si_{0.5}Ge_{0.5}$. ON state energy band diagram indicates reduced tunneling near source for silicon channel in comparison to Si:SiGe channel and thus following lower drain current. This is elaborated in Fig. 11. Comparison of deivce characterstics is done in Table. 2. Its evident from the table that hetro-structure and high-K dielectric materials improve the JLTFET performance drastically. Si:$Si_{0.5}Ge_{0.5}$ H-JLTFET with TiO_2 as gate dielctric provides best results with subthreshold slope as low as 23mV/dec. Subthreshold slope is calculated through following formula

$$\text{Average subthreshold slope (SS)} = \frac{V_t - V_{ref}}{\log\frac{I_t}{I_{ref}}} \qquad (1)$$

where I_t is taken as 10^{-7} A/μm. V_t is voltage at the point where current crosses 10^{-7} A/μm and V_{ref} is voltage at reference point. Clearly, from Table 2 we can conclude that H-JLTFET surpasses benchmark of ITRS' LSTP for 22nm technology and supply voltage of 0.7V.

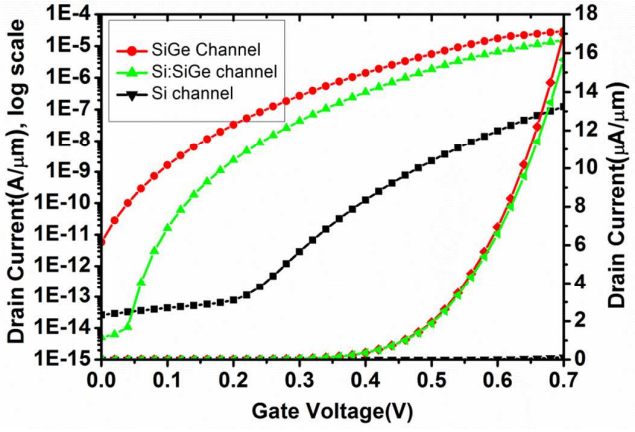

Fig. 10. Variation of drain current with gate voltage at V_{DD}=0.7V, $N_D=10^{15}cm^{-3}$, Φ_G=4.2eV, x_j=34nm, x=0.5 and ε_d=25 for SiGe JLTFET, Si:SiGe H-JLTFET and Si JLTFET

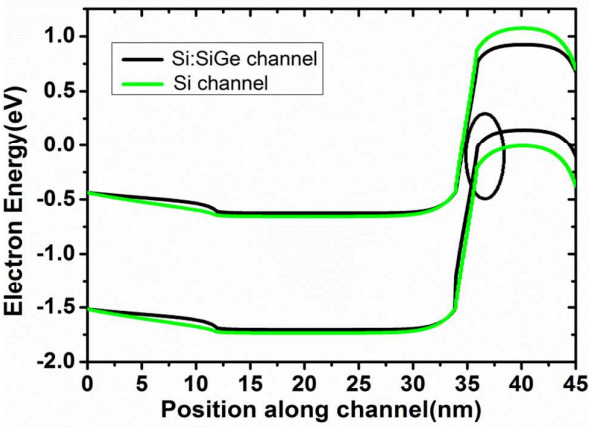

Fig. 11. ON state energy band diagram showing reduced tunneling near source for Si JLTFET in comparison to Si:SiGe H-JLTFET at V_{DD}=0.7V, $N_D=10^{15}cm^{-3}$, Φ_G=4.2eV, x_j=34nm, x=0.5 and ε_d=25

TABLE 2.
CHARACTERISTICS OF JLTFETS AND H-JLTFETS

	Si JLTFET (HfO_2, ε_d=25)	SiGe JLTFET (HfO_2, ε_d=25)	$Si:Si_{0.5}Ge_{0.5}$ H-JLTFET (HfO_2, ε_d=25)	$Si:Si_{0.5}Ge_{0.5}$ H-JLTFET (TiO_2, ε_d=80)
I_{ON}(μA /μm)	0.12	29.72	15.66	125.27
I_{OFF}(A /μm)	2.6×10^{-14}	5.8×10^{-12}	5.1×10^{-15}	1.35×10^{-14}
I_{ON}/I_{OFF}	4×10^{6}	5×10^{6}	3×10^{9}	9×10^{9}
SS(avg) (mV/ dec)	80	59	43	23

Capacitance between gate to source (C_{GS}), gate to drain (C_{GD}), gate to auxiliary gate(C_{GG1}), drain to source(C_{DS}) and drain to auxiliary gate(C_{DG1}) as a function of gate voltage at drain voltage of 0.7V are extracted and plotted in Fig.12. Here, 'G1' represents auxiliary gate. All the capacitances are extracted for the small signal of 0.01 V and frequency of 1MHz. Device approaches linear region with V_{GS} thus C_{GD} grows while C_{GS} decreases. Due to carrier concentration profile as in Fig.2 C_{GD} is higher than C_{GS}. Computation results maximum unity gain frequency, f_T of 4×10^9 at supply voltage. Unity gain frequency f_T, is compiled as a function of gate voltage at V_{DS}=0.7V in Fig. 13.

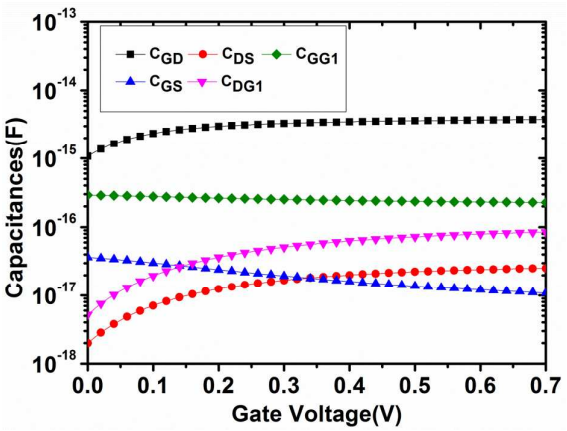

Fig. 12. Variation of capacitances, C_{GD}, C_{DS},C_{GS}, C_{DG1} and C_{GG1} with gate voltage at V_{DS}=0.7V for Si:SiGe H-JLTFET with ac freq=1MHz, small signal=0.01V, $N_D=10^{15}cm^{-3}$, Φ_G=4.2eV, x_j=34nm, x=0.5 and ε_d=25

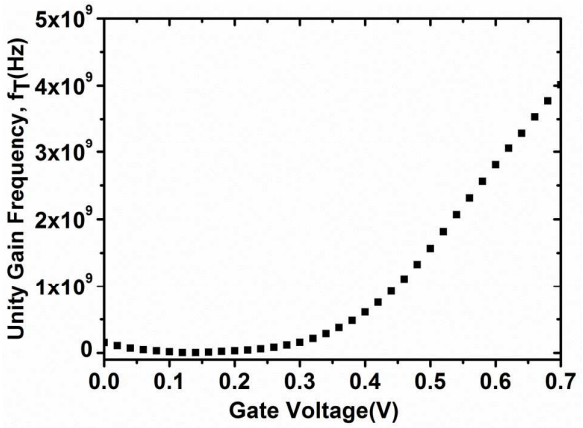

Fig. 13. Unity gain frequency f_T, as a function of gate voltage at V_{DS}=0.7V for Si:SiGe H-JLTFET with ac freq=1MHz, small signal=0.01V, $N_D=10^{15}cm^{-3}$, Φ_G=4.2eV, x_j=34nm, x=0.5 and ε_d=25

V. CONCLUSION

We can conclude that H-JLTFET exhibits tremendous characteristics for 22nm Low Standby Power technology(LSTP) standards of International Technology Roadmap for Semiconductors(ITRS) with fabrication ease as channel doping and dielectric oxide thickness were kept at 10^{15} and 2nm respectively. For 22nm channel, very low leakage current of ~ 10^{-15}A/μm and ON and OFF state current ratio of order of 10^9 at V_{DD} of 0.7V and dielectric constant of 25 are achieved. Furthermore, performance improves with very high-k dielectric, TiO_2 and H-JLTFET easily surpasses all standards of LSTP. Comparing this device data with recently developed structures, H-JLTFET is far ahead in terms of performance. Because of these exceptional characteristics for very small geometries at low voltage, H-JLTFET is a promising solution for low power applications.

REFERENCES

[1] J. E. Lilienfeld, "Method and apparatus for controlling electric current," *U.S. Patent* 1745175, 1930.

[2] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, " Nanowire transistors without junctions," *Nature Nanotech*, vol. 5, no.3, pp 225 – 229, 2010.

[3] C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge, "Junctionless multigate field-effect transistor," *Appl. Phys. Lett.,* vol. 94, no. 5, pp. 053511–053512, 2009.

[4] B. Soree, W. Magnus, and G. Pourtois, " Analytical and self-consistent quantum mechanical model for a surrounding gate MOS nanowire operated in JFET mode," *J. Comput. Electron,* vol. 7, no. 3, pp. 380–383, 2010.

[5] A. Kranti, C.-W. Lee, I. Ferain, R. Yu, N. D. Akhavan, P. Razavi, and J. Colinge, "Junctionless nanowire transistor: Properties and design guidelines," *Proc. 34th IEEE Eur. Solid-State Device Res. Conf.,* pp. 357–360, 2010.

[6] S. Gundapaneni, S. Ganguly, and A. Kottantharayil, "Bulk planar junctionless transistor (BPJLT): An attractive device alternative for scaling," *IEEE Electron Device Lett.,* vol. 32, no. 3, pp. 261–263, 2011.

[7] S. Gundapaneni, S. Ganguly, and A. Kottantharayil, "Enhanced electrostatic integrity of short channel junctionless transistor with high-κ spacers," *IEEE Electron Device Lett.,* vol. 32, no. 10, pp 1325–1327, 2011.

[8] Chi-Woo Lee, Isabelle Ferain, Aryan Afzalian, Ran Yan, Nima Dehdashti Akhavan, Pedram Razavi, Jean-Pierre, Lee Maltings, "Performance estimation of junctionless multigate transistors," *Solid State Elect.,* vol. 54, no. 2, pp. 97–103, 2010.

[9] S.-J. Choi, D.-I.Moon, S. Kim, J.-H.Ahn, J.-S.Lee, J.-Y.Kim, and Y.-K. Choi, " Nonvolatile memory by all-around-gate junctionless transistor composed of silicon nanowire on bulk substrate," *IEEE Electron Dev Lett.,* vol. 32, no. 5, pp. 602–604, 2011.

[10] C.-W. Lee, R. Yan, I. Ferain, A. Kranti, N. Akhvan, P. Razavi, R. Yu, and J. Colinge, "Nanowire zero-capacitor DRAM transistors with and without junctions," *Proc. 10th IEEE-NANO,* pp. 242–245, 2010.

[11] A. Kranti, C. Lee, I. Ferain, R. Yan, N. Akhavan, P. Razavi, R. Yu, G. A. Armstrong, and J. Colinge, "Junctionless 6T SRAM cell," *IET Electron. Lett.,* vol. 46, no. 22, pp. 1491–1493, 2010.

[12] K. Boucart and A.M. Ionescu, "Double gate tunnel FET high K gate dielectric," *IEEE Trans Electron Dev.,* vol. 54, no. 7, 2007.

[13]. M. T. Bjork, J. Knoch, H. Schmid, H. Riel, and W. Riess, "Silicon nanowire tunneling field-effect transistors," *Appl. Phys. Lett.,* vol. 92, no. 19, pp. 193504, 2008.

[14].D. Kazazis, P. Jannaty, A. Zaslavsky, C. Le Royer, C. Tabone, L. Clavelier, and S. Cristolovean, "Tunneling field-effect transistor with epitaxial junction in thin germanium-on-insulator," *Appl. Phys. Lett.,* vol. 94, 263508, 2009.

[15] Kartik Ganapathi, Youngki Yoon, and Sayeef Salahuddin, "Analysis of InAs vertical and lateral band-to-band tunneling transistors: Leveraging vertical tunneling for improved performance," *Appl. Phys. Lett.,* 97, 033504, 2010.

[16] Pranav Kumar Asthana, Bahniman Ghosh, Shiromani Bal Mukund Rahi and Yogesh Goswami, "Optimal design for a high performance H-JLTFET using HfO2 as a gate dielectric for ultra low power applications," RSC Advances,2014, DOI: 10.1039/C4RA00538D

[17] Ghosh, B.; Akram, M.W.: Junctionless Tunnel Field Effect Transistor," *IEEE Electron Device Lett.,* vol. 34, no. 5, pp. 584-586, 2013.

[18] Ghosh, Bahniman, Bal, Punyasloka and Mondal, Partha, "A junctionless tunnel field effect transistor with low subthreshold slope," *Journal of Comp. Elect.,* vol. 12, no.3, pp. 428-436, 2013.

[19] Punyasloka Bal, M. W. Akram, Partha Mondal, Bahniman Ghosh, "Performance estimation of sub-30 nm junctionless tunnel FET (JLTFET)," *Journal of Comp. Elect.,* 2013, DOI 10.1007/s10825-013-0483-6

[20] Punyasloka Bal, Bahniman Ghosh, Partha Mondal, M.W. Akram and Ball Mukund Tripathi: Dual material gate junctionless tunnel field effect transistor, accepted in Journal of Computational Electronics, Springer,10.1007/s10825-013-0505-4, 2013.

[21] Chenming Calvin Hu, " Modern Semiconductor Devices for Integrated Circuits," 1st ed., Pearson India, pp. 279-280, 2010.

[22] Konig, U. et al., "N- and p-type Si-SiGe hetero FETs," *IEEE Int. Symp. on High Perf. Electron. Dev. for Microwave and Optoelectronic Appl.*, vol. 8, pp. 1-7, 2000.

[23] M. Schmidt et al., "Si/SiGe Hetero-Structure Tunneling Field Effect Transistors with In-Situ Doped SiGe Source," *Int. Conf. on ULIS*, vol.13, 2012, 191 – 194,.

[24] Chao Wang,Stephen Y. Chou ,"Self-aligned fabrication of 10 nm wide asymmetric trenches for Si/SiGe heterojunction tunneling field effect transistors using nanoimprint lithography, shadow evaporation, and etching, " *J. Vac. Sci. Technol. B*, Vol. 27, No. 6, Nov/Dec 2009.

[25] Adrian M. Ionescu & Heike Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *nature*,doi:10.1038/nature10679.

[26] Davide Sacchetio, M. Haykel Ben-Jamaal, Giovanni De Michelil and Yusuf Leblebici, "Fabrication and Characterization of Vertically Stacked Gate-AIl-Around Si Nanowire FET Arrays," *Proc. of the 39th European Solid-State Dev. Res. Conf. (ESSDERC),* 2009.

[27]N. Shen, T.T. Le, H.Y. Yu, Z.X. Chen, K.T. Win, N. Singh, G.Q. Lo, and D.-L. Kwong, "Fabrication and Characterization of Poly-Si Vertical Nanowire Thin Film Transistor," *World Acad. of Sci, Eng. and Tech,* 57, 2011.

[28]T. T. Le, H. Y. Yu, Y. Sun, N. Singh, X. Zhou, N. Shen, G. Q. Lo, and D. L. Kwong, "High-Performance Poly-Si Vertical Nanowire Thin-Film Transistor and the Inverter Demonstration, " *IEEE Elec. Dev. Lett.*, vol. 32, no. 6, pp. 1102 – 1106, 2011.

[29] R. Yang et.al., "Two Dimensional Device Simulation and Fabrication of Mesa SOI Vertical Dual Carrier Field Effect Transistor with Effective Channel Length of 30nm for Switching ASIC and SOC*," 6th ASICON, vol.* 2, pp. 1102 – 1106, 2005.

[30]http://www.steeper-project.org/resources/Dissemination/Workshops/Sispad2010_Workshop/talk8_Palestri.pdf. asseccesd on 19 June,2013

[31] http://www.silvaco.com. accessed on 27 July,2013

[32] Schenk, A., "A model for the field and temperature dependence of SRH lifetimes in Silicon," *Solid-State Electron,* vol. 35, no. 11, 1585-1596, 1992.

[33] Hansch, W., Th. Vogelsang, R. Kirchner, and M. Orlowski, "Carrier Transport Near the Si/SiO2 Interface of a MOSFET," *Solid-State Electron.,* vol. 32, no. 10, pp. 839-849,1989.

[34] Katherine Boucart, "Simulation of Double-Gate Silicon Tunnel FETs with a High-k Gate Dielectric," ecole polytechnique federale de Lausanne, Switz. 2010, DOI:10.5075/epfl-thesis-4729.

[35] Costin Anghel, Prathyusha Chilagani, Amara Amara, and Andrei Vladimirescu, "Tunnel field effect transistor with increased ON current, low-k spacer and high-k dielectric," *Appl. Phys. Lett.,* vol. 96, pp.122104, 2010, DOI: 10.1063/1.3367880.

[36] J. Robertson, "High dielectric constant oxide," *Eur. Phys. J. Appl. Phys.,* vol 3, pp. 265–291, 2010.

[37] Minha Seo, Seong Keun Kim, Jeong Hwan Han and Cheol Seong Hwang, "Permittivity Enhanced Atomic Layer Deposited HfO2 Thin Films Manipulated by a Rutile TiO2," *Interlayer. Chem. Mater.,* vol. 22, no.15, pp. 4419–4425, 2010.

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