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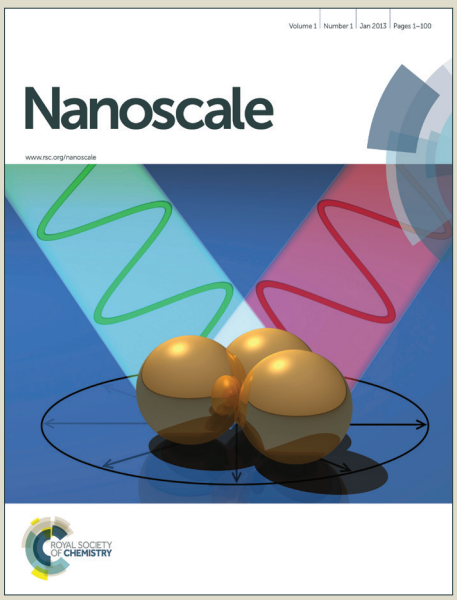

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Metal Assisted Anodic Etching of Silicon

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Abstract

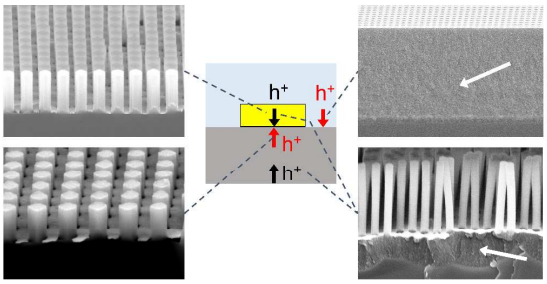
Metal assisted anodic etching (MAAE) of Si in HF, without H_2O_2, is demonstrated. Si wafers were coated with Au films, and the Au films were patterned with an array of holes. A Pt mesh was used as the cathode while the anodic contact was made through either the patterned Au film or the back side of the Si wafer. Experiments were carried out on P-type, N-type, P^+-type and N^+-type Si wafers and a wide range of nanostructure morphologies were observed, including solid Si nanowires, porous Si nanowires, a porous Si layer without Si nanowires, and porous Si nanowires on a thick porous Si layer. Formation of wires was the result of selective etching at the Au-Si interface. It was found that when the anodic contact was made through P-type or P^+-type Si, regular anodic etching due to electronic hole injection leads to formation of porous silicon simultaneously with metal assisted anodic etching. When the anodic contact was made through N-type or N^+-type Si, generation of electronic holes through processes such as impact ionization and tunnelling-assisted surface generation were required for etching. In addition, it was found that metal assisted anodic etching of Si with the anodic contact made through the patterned Au

film essentially reproduces the phenomenology of metal assisted chemical etching (MACE), in which holes are generated through metal assisted reduction of H_2O_2 rather than current flow. These results clarify the linked roles of electrical and chemical processes that occur during electrochemical etching of Si.

Keywords

Metal assisted anodic etching, external bias, silicon nanostructures, perforated Au film, etching without oxidants

TOC graphic



The electrochemical principles governing metal assisted chemical etching was investigated by subjecting P, N, P^+ and N^+ Si substrates to different locations of hole injections in metal assisted anodic etching.

Metal assisted chemical etching (MACE) has been the focus of much recent research, due to its flexibility in producing features such as high aspect ratio nanowires,[1, 2] nanopores,[3] tilted nanowires,[4] and spirals[5] in a simple and inexpensive wet etching process. Si nanostructures made using MACE have been incorporated into a wide range of devices, including devices for energy storage,[6-8] sensing,[9, 10] and advanced electronics.[11, 12]

In the MACE process, noble metals (e.g. Au, Ag, Pt) are used to localize etching of Si in the presence of a solution of HF and an oxidant, typically H_2O_2. It is generally accepted that this localized etching occurs because the metal catalyses the reduction of the oxidant to provide electronic holes that migrate from the metal to the Si to participate in the oxidation reaction that leads to Si etching.

There are two different Si nanowire morphologies generally observed when MACE is used, highly porous nanowires that are photoluminescent and solid nanowires. It has been found that the porosity of Si nanowires depends on many factors, including the resistivity of the wafer, oxidant type, and etchant composition. In general, highly doped Si wafers tend to form nanowires that are more porous than those formed in low to moderately doped N-type and P-type Si substrates, regardless of the oxidant type and concentration used.[13-15]

An alternative method of forming photoluminescent porous Si for optoelectronic devices, without nanowire formation, is to anodically etch Si in an electrochemical cell.[16, 17] Unlike MACE, anodic etching does not involve the use of an oxidant, but consists of an HF solution alone. Anodic etching also does not require a metal to act as a catalyst. In anodic etching, an electrical potential is applied to the Si using an external power supply, which drives electronic holes to the etchant/Si interface so that Si dissolution occurs. Holes are majority carriers in P-type Si, so they are readily available to cause etching under anodic bias. However, holes are

minority carriers in N-type Si, and thus, do not substantially contribute to Si dissolution under an anodic bias. Previous research have shown that porous Si cannot be formed from N-type Si, unless illumination or a high reverse bias are used to increase the hole concentration through electron-hole generation or breakdown.[18]

A few studies have combined MACE and anodic etching to produce Si nanowires. In these experiments, an external electrical bias is added to the traditional MACE process without eliminating the oxidant in etchant solutions. This external bias can provide an additional hole supply, leading to accelerated etching,[19, 20] or can be used to reduce lateral etching away from the metal coated area in conventional MACE.[21]

Nanowire and nanopore formation have also been shown to be possible by substituting the oxidant in MACE with an external bias.[22-24] However, these studies were relatively limited in scope and in some cases, the contribution of the external bias to the etching of the Si was not clear due to the use of Ag and Cu nanoparticles[22-23], which are known to dissolve in HF solution and etch Si when they re-precipitate, even in the absence of H_2O_2.[25] In addition, application of a bias to the metal in a conventional anodic etching configuration was not investigated in these studies.

Although MACE and anodic etching have both been widely used in research, the details of their etching mechanisms are not well understood.[26, 27] Indeed, researchers have acknowledged that a comprehensive study combining the electronic and chemical aspects of MACE is required to fully understand the etching mechanism.[22, 27]

For this reason, we have carried out experiments on metal assisted anodic etching (MAAE) of Si, using the two experimental configurations shown in Figure 1. Si substrates were coated with perforated Au films and subjected to anodic etching in a HF solution. Au is stable in

HF and does not dissolve and re-deposit during the etching processes[28, 29] (See Supplementary Information Section I). Also, besides anodic contact to the Si substrate (Fig. 1a), the use of a continuous, perforated film allows application of an anodic bias to the noble metal (Fig. 1b). This allows comparison and contrasting of the effects of hole generation at Au/Si interfaces and electrolyte/Si interfaces, and allows separate investigation of the effects that electronic and chemical processes have on the nanostructures formed in MAAE. This, in turn, provides insights into the mechanisms of MACE and conventional anodic etching.

Results and Discussion

A. Establishing the Schottky barrier heights

Based on the analysis of previous reports,[27, 29, 30] Metal Assisted Chemical Etching (MACE) of Si in HF takes place when electronic holes (h^+) are injected into the Si near the metal-Si interface (Fig. 2a). These holes then facilitate the reaction of Si with HF to form soluble SiF_6^{2-} in the following way:[30-33]

$$Si + 4HF + 4h^+ \rightarrow SiF_4 + 4H^+ \quad (1a)$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6 \quad (1b)$$

$$Si + 2HF + 2h^+ \rightarrow SiF_2 + 2H^+ \quad (2a)$$

$$SiF_2 + 2H_2O \rightarrow SiO_2 + 2HF + H_2\uparrow \quad (2b)$$

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \quad (2c)$$

The main difference between the series of reactions in (1) and (2) is that 4 holes are required to dissolve a single Si atom in reaction (1) whereas only 2 holes are required to do the same in

reaction (2). Previous studies[29, 30] have suggested that, generally, both reactions are involved in MACE, so the average number of holes required to dissolve a Si atom can range between 2 to 4.

Because most of the injected holes lie near the Au-Si interface for metal assisted chemical etching, the fastest dissolution of Si takes place under the metal. If a perforated Au film is used, the un-etched Si protrudes through the holes in the film, leading to the formation of Si nanowires.

In the process of metal assisted dissolution of Si described above, it should be noted that charge transfer takes place through two interfaces, the Au/Si interface and the etchant/Si interface. Therefore, the details of the electronic band structures of these two interfaces are required to quantitatively understand the etching process. Figs. 2b and 2c show examples of the general energy band diagrams for these two interfaces. It can be seen that they are basically Schottky junctions.[34, 35] Note that the axis for $Y = 0$ is arbitrarily fixed with respect to the Au/Si and etchant/Si interfaces, while $X = 0$ is fixed with respect to the Au/HF interface. This convention will be used throughout the rest of the paper.

In order to determine the Schottky barrier heights for each junction, we make use of the experimental J-V_a (current density vs applied voltage) trends obtained for various experimental configurations and samples, shown in Fig. 2d and 2e. The theoretical trends for currents passing through Schottky junctions with barrier heights of 0.76eV and 0.82eV (dashed lines) are also plotted in Fig. 2d, and are given by,

$$J = A^* T^2 e^{-\frac{B}{kT}} \left(e^{\frac{qV_a}{kT}} - 1 \right), \qquad (3)$$

where A^* refers to the Richardson's constant (120 A/cm^{2}K^2), T is the temperature, k is Boltzmann's constant, q is the elementary charge and V_a refers to the applied voltage (negative

for reverse bias and positive for forward bias). B refers to the Schottky barrier height and is represented by ϕ and ψ for the Au/Si and etchant/Si interfaces, respectively (Figs. 2b and 2c).

As can be seen in Fig. 2d, the J-V_a curves for all of the samples initially follow Eq. (3). However, as the values of J and V_a rise, the experimental trends deviate increasingly from the calculated trend. This is because, at large J, the J-V_a relationship becomes dominated by the resistance of the HF solution and the bulk Si instead of the interface[34]. This portion of the J-V_a trend is ohmic and thus, shows up as a curve in the semi-log graph shown in Fig. 2d. Nevertheless, the experimental J-V_a curves at small applied voltages conform to Eq. (3), and the experimental data can be fitted to evaluate the Schottky barrier height. From the data in Fig. 2d, we obtained a B value of 0.82eV for N-type Si with the Au anodic contact and 0.76eV for P-type Si, regardless of the anodic contact material (Au or Si).

For the case of N-type Si with a perforated Au anodic contact, a rectifying interface is formed.[36, 37] The applied voltage mainly drops across the Au/Si interface, and the main contribution to the Schottky barrier height, B, in this case, is ϕ_N (i.e. $B = \phi_N = 0.82$ eV). This value was confirmed with the Mott-Schottky plot for Au/N-Si (see Supplementary Information Section I), and is also in good agreement with previous reported[36, 37] Schottky barrier heights of 0.77 – 0.82 eV for Au/ N-type Si contact.

Au/P-Si forms an ohmic contact,[38] and therefore, the applied voltage is primarily dropped across the etchant/P-Si interface. As additional proof of this, the J-V_a characteristics for anodic etching of P-type Si in HF solution without the perforated Au was measured and from Fig. 2d and 2e, it can clearly be seen that the J-V_a characteristics for anodic etching of P-Si in HF with and without the perforated Au is the same. This implies that the etchant/P-Si interface is current limiting, and therefore $B = \psi_P = 0.76$eV. Unlike the case with Au/N-Si interface, however, we

were unable to verify this value with Mott-Schottky plots for the HF/P-Si interface as the standard reference electrodes of commercial electrochemical measurement systems, such as the porous glass plug, are susceptible to damage by the HF electrolyte. It should be noted, however, that the result is in reasonable agreement with the previous reported value of 0.62eV.[39, 40] Given that the band gap ($E_c - E_v$) of Si is 1.12eV, ϕ_P and ψ_N were found to be 0.3eV and 0.36eV, respectively.

To further verify the validity and reproducibility of the Schottky barrier heights derived from the J-V_a plots in this section, we have also performed the same experiments and analysis on Si samples coated with a perforated Pt film instead of an Au film (see Supplementary Information II). The Schottky barrier height obtained for the Pt/N-Si interface was 0.89 eV, which is well within the range of previously reported values[41, 42], and ψ_P = 0.77eV for the HF/Si interface, which is effectively the same value as that obtained through the J-V_a plots for the samples coated with a perforated Au film. These results, therefore, establish the trustworthiness of the Schottky barrier heights.

B. P-type Si (P-Si) substrates

When P-type Si substrates were subjected to electrochemical anodic etching, it was found that a minimum voltage of 0.3V was required before appreciable Si etching ($J \geq$ 1mA/cm^2) occurred, regardless of where the anodic contact was made (Fig. 2d and 2e). Once the applied voltage crossed this threshold, for the case in which the perforated Au was the anodic contact, the contrast in Fig. 3a suggests that the Si nanowires were solid, and the wires remained straight. However, when the contact was made through Si, two cases were observed. For V_a = 0.3V, the Si nanowires were similar to those obtained with the perforated Au contact, with no porous Si

formed under the perforated Au (Fig. 3b). However, if $V_a > 0.3$V, a thick layer of porous Si was found under the perforated Au film (Fig. 3c) and the Si nanowires were highly porous with rough sidewalls and more bending. (Fig. 3d).

It is also worth noting that in all cases, including results involving other types of Si substrates discussed in the following sections, the diameters of the nanowires correlate very well with the diameters of the holes in the perforated Au film. Any differences between the two dimensions cannot be easily resolved with SEM, like in the case of MACE Si nanowires[1, 29, 43, 44]. In addition, the etching is very uniform across the entire substrate (see Supplementary Information I).

To understand these results, it is necessary to turn to electronic band diagrams for the Au/Si and etchant/Si interfaces. The first observation to be made is that the Schottky barriers at the Au/Si and etchant/Si interfaces are different. With reference to Figs. 2b and 2c, with ϕ_N = 0.82eV, ϕ_P = 0.3eV, ψ_N = 0.36eV and ψ_P = 0.76eV, it can be seen that E_C for the Au/Si interface is pinned at 0.82eV above the E_F (Fermi level), and E_V is pinned at 0.3eV below E_F. For the etchant/Si interface, however, E_C is pinned at 0.36eV above the equilibrium E_F and E_V is pinned at 0.76eV below the equilibrium E_F. Therefore, at equilibrium, there will be band bending in the region where the Si under the Au joins the Si under the HF i.e. $X = 0$ (Fig. 4a). This bend at the Au/Si and the etchant/Si interfaces results in an electric field that will repel any hole attempting to diffuse from the Au/Si interface to the etchant/Si interface, unless the holes have sufficient energy to overcome the energy barrier, β (= 0.46eV for our experiments). In other words, excess holes injected in the Si will preferentially accumulate under the Au/Si interface as compared to the etchant/Si interface. This result is in line with those obtained from simulations conducted by Huang *et al*.[22]

Turning to the specific case of P-type Si with the perforated Au anodic contact, electronic holes could pass easily from Au to Si, since the interface is effectively ohmic with a low Schottky barrier of 0.3eV.[38] Thus, the applied voltage, V_a, is mainly dropped across the etchant/P-Si interface. An examination of the etchant/P-Si interface in Fig. 4b reveals that for $V_a = 0$, a potential barrier of $V_{bi} = \psi_P - (E_F - E_C)$ prevents significant hole current from crossing the interface and participating in the Si dissolution reaction. However, with the application of V_a, this potential barrier is reduced such that when $V_a \geq 0.34$V, $J \geq 1$mA/cm^2, based on computations from Eq. (1). This is in line with our observation from experiments that $J > 1$mA/cm^2 only when $V_a \geq 0.4$V (Fig. 2d and 2e).

Since the rate of Si dissolution was faster than the injection rate of holes,[29] the injected holes were not able to diffuse significantly away from the Au/Si interface before being consumed in reaction (1) or (2). In addition, the energy barrier, β, introduced by the perforated Au film at the surface of Si would have further discouraged the diffusion of holes away from the Au/P-Si interface. Therefore, the majority of the holes injected into Si through the perforated Au were involved in the dissolution of Si directly underneath the perforated Au, leading to a highly selective etching process which results in the solid nanowires seen in Fig. 3a.

The etching process described above is similar to that for MACE, with the difference being that the holes for MACE are produced by the reduction of H_2O_2, whereas the holes for MAAE are supplied by an external power source. It is, therefore, not surprising to find that the Si nanowires obtained in Fig. 3a resemble those obtained through MACE of Si.[27, 33, 45, 46]

Unlike the case of anodic contact through the perforated Au, when the anodic contact is made through the Si, holes are not supplied through the perforated Au mesh but through the bulk of the Si. As a result, the holes no longer need to pass through the Au/P-Si interface to enter the

Si substrate, but are free to move to the Au/P-Si interface and the etchant/P-Si interface from the backside of the substrate (Fig. 5). However, for a significant amount of holes to travel to the etchant/Si interface for the dissolution of Si, the applied voltage has to reduce the Schottky barrier, V_{bi}, substantially (Fig. 5a). As in the case of the perforated Au anodic contact, $V_a \geq 0.34$ V is required for $J \geq 1\text{mA/cm}^2$ to flow through the electrochemical etching circuit. This explains the experimental observation that $J \geq 1\text{mA/cm}^2$ when $V_a \geq 0.3$V for MAAE of P-Si substrates with anodic contact made through Si (Fig. 2d and 2e).

For the P-Si substrates used in this study, $V_{bi} = 0.46$V. Therefore, when $V_a = 0.3$ V, there is still a potential barrier of 0.16eV for holes to overcome to reach the etchant/Si interface (Fig. 5a). On the other hand, no barrier exists at the Au/Si interface (Fig. 5b). Therefore, for $V_a = 0.3$V, holes are attracted to the Au/Si interface and cause a higher etch rate for the Si under the perforated Au than in the regions where the Si is uncoated (Fig. 5c). Note that etching of the Si in the uncoated regions is essentially regular anodic etching, which leads to the formation of porous Si. Therefore, in this case, no porous Si formation is expected, which is in agreement with the morphology of the nanowires shown in Fig. 3b.

Once V_a reaches 0.4V (i.e. $V_a \geq V_{bi}$), the potential barrier at the etchant/P-Si interface is reduced to 0.06V, and there is no longer an energy barrier preventing holes from reaching the etchant/P-Si (Fig. 6a). Therefore, the etchant/P-Si interface, like the Au/P-Si interface (Fig. 6b), attracts holes and Si dissolution also takes place at the regions not covered by the Au (Fig. 6c). This effectively leads to regular anodic etching, and porous Si formation occurs in these areas.

As porous Si is formed, HF will permeate through the pores and new etchant/P-Si interfaces will form so that anodic etching continues. Because of the high resistivity of porous Si, most holes will not be able to reach the porous Si formed at the original etchant/P-Si interface to

cause complete dissolution of the porous Si there. Moreover, the formation of porous Si is isotropic and can eventually undercut the perforated Au. Therefore, as the porous Si grows thicker under the perforated Au, more and more of the applied voltage is dropped across the highly resistive porous Si layer, such that it eventually insulates the perforated Au, effectively ending the selective etching process that generates the nanowires (Fig. 6c).

In summary, for P-Si with anodic contact made through the Si substrate, an applied voltage of at least 0.3V is required to overcome the built-in potential barrier at the etchant/P-Si interface before Si etching occurs. For V_a = 0.3V, MAAE dominates over regular anodic etching and Si nanowires are formed with no porous Si regions underneath them. For $V_a \geq 0.4$V, however, MAAE and regular anodic etching compete, resulting in the formation of porous Si nanowires on top of a thick layer of porous Si.

C. N-type Si (N-Si) substrates

When MAAE was performed on N-type Si substrates, it was found that a much higher voltage was required to produce the same etching current density when the anodic contact was made through the Si rather than the perforated Au (Fig. 7a). The J-V_a plot for the case of Si anodic contact suggests that the etching current was produced by a voltage breakdown at the Au/N-Si interface. However, the breakdown voltage observed here is much lower than the value typically reported for Au/N-Si diodes (≈100V).[47] Nevertheless, the solid Si nanowires that formed in both cases exhibit similar characteristics of vertical and smooth sidewalls without any trace of a porous Si layer (Figs. 7b – 7d). At higher current densities, the N-Si nanowires fabricated using MAAE (anodic contact made through the Si) appeared to be more porous and mechanically weaker (Fig. 7e) than those fabricated at lower current densities.

Figure 8a shows that when the anodic contact is made through the perforated Au with the Au/N-Si interface forward biased, electronic holes can be readily injected into the N-Si from the perforated Au. Similar to the case with MACE (no external bias) and MAAE of P-Si (with a perforated Au anodic contact), the holes are concentrated under the perforated Au. When HF comes into contact with this thin layer of Si where the holes are concentrated, the holes will then travel to the etchant/N-Si interface (Fig. 8b) and participate in the Si dissolution reactions, bringing about highly selective etching of Si under the Au. This results in the N-Si nanowire morphology seen in Fig. 7b, which is very similar to the morphology observed for MACE and MAAE of P-Si (anodic contact made through the perforated Au).

When the anodic contact is shifted to the Si, the path that the holes take to the Au/N-Si and etchant/N-Si interfaces become less straightforward. Unlike the case with P-type Si, holes introduced from the backside of the Si would be eliminated through recombination with electrons in N-type Si before reaching the Au/N-Si or etchant/Si interfaces.[34] Instead, holes are injected into the interfaces when the applied voltage causes reverse-bias breakdown at the sharp edges of the Au coating due to electric field crowding,[48] as illustrated in Fig. 9a which depicts the field line concentration in the depletion region at the edges of the Au/N-Si interface. At a sufficiently large reverse bias, this strong asymmetric field strength at the edges of the Au film can reach the critical field strength of 10^5 V/cm required to cause breakdown[49] by impact ionization[34] (Fig. 9b) and cause sufficient holes to be generated near the Schottky interfaces for Si dissolution. This reverse-bias breakdown accounts for the observation that much higher voltages are required to obtain the same etching current density for Si anodic contact as compared to perforated Au anodic contact. The electric field crowding effect explains why the

breakdown voltages observed in our study are much lower than those commonly reported for Au/N-Si diodes.

Because of the band bending at the surface of the Si shown in Fig. 4a, most of the generated holes will be confined to the region of Si directly under the Au, so that preferential etching of N-Si under the perforated Au will take place. However, when the concentration of the generated holes is high enough, many holes will overcome the energy barrier, β, and diffuse from the Au/N-Si interface to the bare Si surface to cause porous Si formation there. For this reason, at high applied voltages, which lead to high concentrations of generated holes (reflected as high current density), the Si nanowires are more porous and mechanically weaker, as observed in Fig. 7e.

To test the proposed model, the breakdown voltages of the perforated-Au/N-Si and continuous-Au/N-Si interfaces in dry conditions (i.e. no HF) were investigated and compared. As can be seen in Fig. 10a, the perforated-Au/N-Si interface breaks down at lower voltages as compared to the continuous-Au/Si interface. This is because the perforated Au film has many more edges, causing it to be more susceptible to the field crowding effect.

To quantitatively account for MAAE in N-type Si, with the anodic contact connected through Si, we first assume that the rate limiting step in the etching process is the generation of holes through reverse bias breakdown and not the rate of Si dissolution through reactions (1) and (2). This assumption was previously shown to be valid in MACE[29] and will be validated later for MAAE of N-type Si using a Si anodic contact. Based on the model described above, the expected current injected per unit area at the Au/N-Si interface under reverse bias can calculated as[34]

$$J_0 = A^* T^2 e^{-\frac{B}{kT}}, \quad (4)$$

where

$$B = \phi_N - q\left[\frac{q\,|\,\xi_s\,|}{4\pi K_s \varepsilon_0}\right]^{\frac{1}{2}}. \quad (5)$$

The second term in Eq. (5) accounts for Schottky barrier lowering due to the image force[34] and K_s is the dielectric constant of the material (11.8 for Si), ε_0 is the permittivity of space (8.85 x 10^{-14} F/cm). ξ_s is the electric field strength at the surface of the Si ($Y = 0$) and is given by[34]

$$\xi_s = -\left\{\frac{2qN_D}{K_S\varepsilon_0}\left[\phi_N - \left(E_C - E_F\right) - V_a\right]\right\}^{\frac{1}{2}}, \quad (6)$$

where the current (J) due the breakdown, is given by[34]

$$J = \frac{1}{1-\left[\frac{|V_a|}{V_{BR}}\right]^g} J_0, \quad (7)$$

and where V_{BR} is the breakdown voltage and g is a constant. Both V_{BR} and g are empirically determined values[34]. Rewriting Eq. (7) in logarithmic form, we obtain

$$\ln\left(1 - \frac{J_0}{J}\right) = g \ln V_a - g \ln V_{BR}. \quad (8)$$

Figs. 10b and 10c show that the experimental trend for ln (1-J_0/J) vs ln (V_a) follows Eq. (8) very well except at high values of J and V_a, for which the resistances associated with the rest of the circuit (e.g. etchant, bulk Si etc.) distorted the J vs V_a trend to a linear relation[34] (Fig. 10c). From Fig. 10b, we were able to obtain g = 1.4 x 10^{-14} and V_{BR} = 8.5 V.

To further verify our analysis, we have also conducted the same experiments and analysis on Si samples coated with perforated Pt instead of perforated Au (see Supplementary Information Section II) and obtained V_{BR} = 5.6 V, which is in good agreement with the breakdown voltage of 5 V previously reported for Pt/N-Si interfaces subjected to electric field

crowding effects.[48] Moreover, it can be observed from Fig. 10c that the J-V_a trends do not vary significantly with the concentration of the HF solution for the range of V_a tested, suggesting that the rate limiting step is the hole generation process and not the dissolution process, which validates the assumption made above in development of the quantitative model.

D. Heavily doped P-type (P^+) and N-type (N^+) Si substrates

When P^+ and N^+ Si substrates were subjected to electrochemical anodic etching in HF with perforated Au anodic contacts, the results were similar to those previously obtained for lightly doped P-type and N-type Si substrates (Fig. 11). The only difference in this case was that the Si nanowires appeared to be more porous and were standing on top of a layer of porous Si. Given that this was seen for heavily doped substrates but not lightly doped substrates, even though the etching current density and voltage were similar for both, it follows that the formation of this porous layer was caused by material properties rather than process parameters.

It has previously been suggested that dopants in Si can cause defect sites[50] that lower the energy barrier for Si dissolution,[51] thereby leading to the formation of pores in the Si. In this case, it is not surprising to observe porous layers underneath the Si nanowires in MAAE, as heavily doped substrates have a much higher concentration of dopants as compared to lightly doped samples ($\approx 10^5$ times for the samples used in this study).

When the anodic contact was changed to Si, the morphologies of the nanostructures obtained on P^+ and N^+ Si were very different. For the case of P^+ Si, highly porous Si nanowires were obtained on a thick porous Si layer (Fig. 12a), while for N^+ Si, a thick porous layer was obtained with very short Si nanowires on top of it (Fig. 12b). These observations suggest differences in the mechanism of anodic etching of P^+ and N^+ Si substrates.

For P^+ substrates, anodic etching takes place because of the injection of holes from the contact into the Si. Much like the case of P-type substrates shown in Fig. 6c, because of the ohmic nature of the Au/P^+ and etchant/P^+ interfaces, the injected holes will cause regular anodic etching and MAAE to take place simultaneously. The end result is therefore similar for both cases, with the formation of porous P^+-Si nanowires and a porous layer underneath.

Unlike the case for P-type Si, however, holes can freely travel past the etchant/P^+-Si interface at all voltages and hence, there is no threshold voltage below which the formation of porous Si is suppressed (see Supplementary Information Section I). Once again, metal assisted anodic etching effectively ceases once the highly resistive porous Si reaches a thickness large enough to effectively insulate the Au/P^+-Si interface from the applied voltage.

In contrast, anodic etching of N^+-Si substrates depends on the surface generation of electron-hole pairs at the etchant/N^+-Si interface to provide the holes necessary for Si dissolution.[52, 53] This surface generation process incorporates tunnelling (Fig. 13a), as the energy required for an electron to jump from the valence band to the conduction band in this way is less than the band gap. As a consequence, the rate of surface generation can be much larger than the rate of the thermal generation in Si. However, since this process depends on tunnelling, substantial surface generation of holes, and therefore, anodic etching of Si in HF at low applied voltages, can only take place for N^+ substrates with doping concentrations above 10^{18}/cm^3.[53] Note that the J-V_a trend for electrochemical etching of N^+-Si is ohmic regardless of where the anodic contact is made, much like the case of P-Si and P^+-Si.

As in the case for N-type Si (Fig. 4a), the Au/N^+-Si interface provides a lower energy level for the surface generated holes to fall to, thus creating an electric field that sweeps the generated holes toward the Au/N^+-Si interface and enhancing the etching of Si under the Au, i.e.

MAAE. Unlike the case for N-type Si, however, the generation of holes does not take place at the edges of the perforated Au film (i.e. $X = 0$), where the newly created holes can be rapidly swept by the electric field to the Si under the Au, but takes place, instead, across the entire etchant/N^+-Si interface. Therefore, most of the generated holes will be consumed in the formation of porous Si (regular anodic etching) at the etchant/N^+-Si interface before they are swept to the Au/N^+-Si interface to be used in MAAE (Fig. 13b). The net result is, therefore, more rapid formation of porous Si through regular anodic etching, relative to the rate of metal assisted anodic etching. This, in turn, prevents significant nanowire formation (Fig. 13b).

It is also worth noting that the anodic etching rates of heavily doped Si substrates in HF at high current densities appear to be strongly dependent on the exposed crystallographic planes. As can be seen from Fig. 12, dendrite branching in <113> directions from a central <100> channel can be observed in the porous layer of the Si, and also in the Si nanowires. In addition, instead of obtaining Si nanowires, electrochemical anodic etching of N^+-Si was found to produce regular nanotubes/ nanorings (Fig. 12b). Dendritic porous Si structures have previously been observed for regular anodic etching of lightly doped N-type Si in an organic electrolyte using illumination on the backside of the wafer.[26] However, a linkage between this result and the result reported here is not clear. This is the first time that aligned dendritic structures have been found in Si nanowires formed using electrochemical etching of Si.

Conclusions

The formation of Si nanowires through the use of metal assisted anodic etching was investigated. Results obtained for varions substrate types and for anodic contact through perforated Au or through the silicon substrate are summarized in Table 1.

Using $J–V_a$ plots, the Schottky barrier heights of the Au/Si and etchant/Si interfaces were determined and energy band diagrams were constructed using the measured barrier heights. These, together with the observed morphologies of etched Si nanowires and substrates, were then used to show that mechanisms of electrochemical anodic etching of Si with the anodic contact made through the perforated Au is effectively the same as the mechanisms of the MACE process, regardless of the substrate doping type.

In these cases, holes required for Si dissolution reactions were injected into the Si via the perforated Au film, which led to them being concentrated directly under the perforated Au. As a result, the etch rate was much faster for Si under the perforated Au than in uncoated Si regions. Solid nanowires were obtained for lightly doped substrates (of either N or P type), and no porous Si layers were observed. Etching of heavily doped Si (of either N or P type) led to formation of porous nanowires on top of porous layers in the substrate.

In contrast, when anodic contact to P-Si was made through the Si, both regular anodic etching and MAAE took place. If the applied voltage was below a threshold voltage V_{bi}, MAAE dominated and relatively solid P-Si nanowires were obtained with little or no porous P-Si formed. However, if the applied voltage was above the threshold voltage, regular anodic etching and MAAE were concurrent and highly porous Si nanowires were formed on top of thick porous Si layers. It was argued that this happens below the threshold voltage, when the Au/P-Si interface was ohmic but the etchant/P-Si interface was not. If the applied voltage exceeds the threshold values, both interfaces become ohmic.

For N-Si, when the anodic contact was made through Si, solid nanowires formed with no porous Si underlayers, similar to the case when N-Si was etched with the anodic contact made through the perforated Au film. However, the formation mechanisms were different and it was proposed that the holes required for MAAE with Si anodic contact were generated when electric field crowding occurred at the edges of the perforated Au, causing reverse bias breakdown at relatively low applied voltages. Using standard analyses from semiconductor physics, the proposed model was shown to agree well with experimental data.

Results obtained for P^+-Si with anodic contact through the Si were the same as results for P-Si: porous Si nanowires formed over a thick porous Si layer. Unlike the case for P-Si, however, there was no threshold voltage below which MAAE could dominate over regular anodic etching, as both the Au/P^+-Si and etchant/P^+-Si interfaces were ohmic at all applied voltages.

Lastly, electrochemical anodic etching of N^+-Si with Si anodic contact led to formation of very short Si nanowires on top of a very thick porous Si layer, indicating that regular anodic etching dominated the etching process. It was argued that this is because the holes required for Si dissolution were generated at the etchant/N^+-Si interface and thus, most of them were consumed in the formation of porous Si before they could diffuse or drift to the Au/N^+-Si interface. This study shows that the morphology of the nanowires and the silicon layer underneath obtained through MAAE depends strongly on the site of hole injection and the electronic energy levels at the metal/Si and etchant/Si interfaces. Analyses of the effects of band structures at the Au/Si and etchant/Si interfaces can be used to explain the results of both MAAE and MACE, and create a unifed understanding of electrochemical etching in both cases.

Table 1: Overview of the nanostructure morphologies observed for each type of wafer and contact location.

Contact	Wafer type	Nanowires	Porous Layer	Source of h^+
Perforated Au	P (10-20ohm-cm)	Yes	—	External source through Au/Si interface Equivalent to MACE
	P^+ (0.005-0.01ohm-cm)	Yes	Yes	
	N (10-30ohm-cm)	Yes	—	
	N^+ (<0.005ohm-cm)	Yes	Yes	
Bulk Si	P (10-20ohm-cm)	Yes	Yes	External source through both Au/Si and etchant/Si interfaces Equivalent to MACE + Anodic Etching
	P^+ (0.005-0.01ohm-cm)	Yes	Yes	
	N (10-30ohm-cm)	Yes	—	Breakdown at Au/Si interface
	N^+ (<0.005ohm-cm)	—	Yes	Breakdown at etchant/Si interface

Materials and methods

Substrate preparation:

Four types of (100) Si wafers including P-type (boron-doped, 10-20 Ω·cm), P^+-type (boron-doped, 0.005-0.01 Ω·cm), N-type (phosphorous-doped, 10-30 Ω·cm) and N^+-type (Arsenic-doped, ≤0.005 Ω·cm) were used. The substrates were first coated with a 220nm BARLi anti-reflection coating (ARC) (AZ Electronic Materials), followed by e-beam deposition of a

20nm-thick SiO_2 layer. Then a 200nm-thick PFI-88 photoresist layer (Sumitomo Chemical Co.) was applied using spin-coating.

The trilayer stack was then exposed using Lloyd's mirror interference lithography[46]. The system uses a 325nm wavelength helium-cadmium laser. Two exposures at perpendicular angles were carried out to yield an ordered array of resist pillars, after which the wafers were developed in Developer CD 26 (DOW Chemical). All the wafers with patterned resist were then treated with a series of reactive ion etching recipes to transfer the pattern from the resist to the ARC layer[45].

20nm-thck Au films were then deposited onto the wafers using e-beam evaporation (Airco Temescal CV-8). After metal deposition, the remaining ARC posts were removed by immersing and sonicating the samples in heated N-methyl-2-pyrrolidone (NMP), leaving an Au film with a square periodic array of circular holes on top of the Si substrate. Ohmic contacts for P-Si and N-Si substrates were made using a thick layer (>100 nm) of Au and Al, respectively.

Etching and characterization: The samples were cut into $1\times1.5cm^2$ strips. A DC power supply (Agilent E3612A) was used to apply a bias during MAAE, and the *I-V* characteristics of the process were acquired. The etchant was composed of HF (49%, VWR) and de-ionized (DI) water. Unless indicated otherwise, the concentration of HF used was 4M and the total volume of the etchant was kept at 70mL. Experimental configuration in which the contact was made through the Si is shown in Fig. 1a. A platinum mesh is used as a counter electrode. The sample was sealed between a Teflon cell and a copper plate, with the Au-coated side of the wafer exposed to the etchant solution. The exposed area of the sample was $0.7cm^2$. The copper plate was

connected to the positive end of the power source, and the Pt counter electrode was connected to the negative end to complete the circuit.

The experimental configuration for contact through the perforated Au films is shown in Fig. 1b. The Si sample was suspended in the solution with an area immersed in the solution of approximately 0.7cm^2. An Au wire was fixed in place using a clip and was used to contact the patterned Au film, so that the electric current could only go through the Au on the top surface of the Si. After etching, the samples were removed from the etchant solution and rinsed with DI water multiple times before being dried using a nitrogen gun. SEM images were made using a Zeiss/Leo Gemini 982 SEM.

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Figure Captions:

Figure 1. (a) Set-up for MAAE with contact made through the Si (back side). (b) Set-up for MAAE with contact made through the perforated Au film (top side).

Figure 2. (a) Schematic diagram showing the injection of electronic holes from an Au coating into the Si, and how the holes participate in the etching of Si. Green arrows indicate hole current. The color scheme used to represent the different materials here will be employed throughout the rest of this report. (b) Energy band diagram for the Au/ N-Si interface. E_C, E_F and E_V refer to the conduction band edge, Fermi level and valence band edge, respectively. (c) Energy band diagram for the N-Si/ HF interface. (d) Semi-log plot showing fitted experimental trends (solid lines) and calculated trends (dashed lines) and (e) linear-linear plot of the experimental data, for the current density (J) vs. the applied voltage (V_a).

Figure 3. Representative SEM images showing the morphology of the nanowires obtained for electrochemical etching of P-type Si substrates. Please refer to the Supplementary Information Section I for additional images. The etch duration in each case was 10min. White solid arrow points to porous Si, white dashed arrow points to solid Si and the white dashed line demarcates the porous/ solid Si interface. The scale bar represents 1μm. Note that the entire Si layer underneath the nanowires shown in (d) is porous.

Figure 4. (a) Energy band diagram at the Si surface ($Y = 0$), showing band bending in Si at $X = 0$ (where the Au meets the HF). E_F here refers to the equilibrium Fermi level. The green arrow shows holes being repelled by the energy barrier, β (= 0.46eV). (b) Energy band diagram at the etchant/ P-Si interface before (solid lines) and after (dashed lines) the application of a positive

voltage, V_a, through the perforated Au film. Holes are initially repelled from the interface (red arrows) due to an energy barrier, V_{bi}, but after V_a is applied, they (green arrows) face no barrier.

Figure 5. Energy band diagrams at the (a) etchant/P-Si interface and (b) Au/ P-Si interface before (solid lines) and after (dashed lines) the application of a voltage of V_a (blue arrow). In this case, $V_a < V_{bi}$, the applied voltage at the etchant/P-Si interface is too low to overcome the energy barrier. As a result, holes injected through the bulk Si preferentially accumulate at the Au/P-Si interface and cause etching, as illustrated in (c).

Figure 6. Energy band diagrams at the (a) etchant/ P-Si interface and (b) Au/ P-Si interface, before (solid lines) and after (dashed lines) the application of a voltage of V_a (blue arrow) through the Si substrate ($V_a = V_{bi}$). Here, the applied voltage has overcome the energy barriers at the Au/ P-Si and etchant/ P-Si interfaces, and holes injected through the bulk Si can reach both interfaces. As a result, Si is etched under the Au and porous Si is also formed away from the Au, as illustrated in (c). Green arrows indicate the movement of the holes.

Figure 7. (a) J-V_a plot for MAAE of N-Si in 4M HF with the anodic contact made through the perforated Au and through the Si. (b) – (e) SEM images showing the morphology of the nanowires obtained for electrochemical etching of N-type Si substrates. The etching durations were (b) 10 min, (c) 10 min, (d) 10 min, and (e) 1 min. MAAE was the only etching mechanism operating, as no porous Si, an indication of regular anodic etching, can be observed. The scale bar represents 1μm.

Figure 8. (a) Energy band diagram showing that hole injection rate from Au to N-Si (green arrow) is higher when a positive voltage (blue arrow) is applied to the perforated Au. (b) Energy band diagram showing how holes transferred from the perforated Au in (a) are trapped at the etchant/N-Si interface near the Au, causing Si dissolution. (c) Schematic diagram showing the injection of holes into N-Si through the Au and how these holes lead to selective etching at the Au/N-Si interface.

Figure 9. (a) Schematic diagram showing the electric field crowding effect. The concentration of electric field lines is highest at the Au edges where breakdown occurs. (b) Energy band diagram showing hole generation by impact ionization breakdown when a sufficiently large positive voltage is applied to the N-Si substrate.

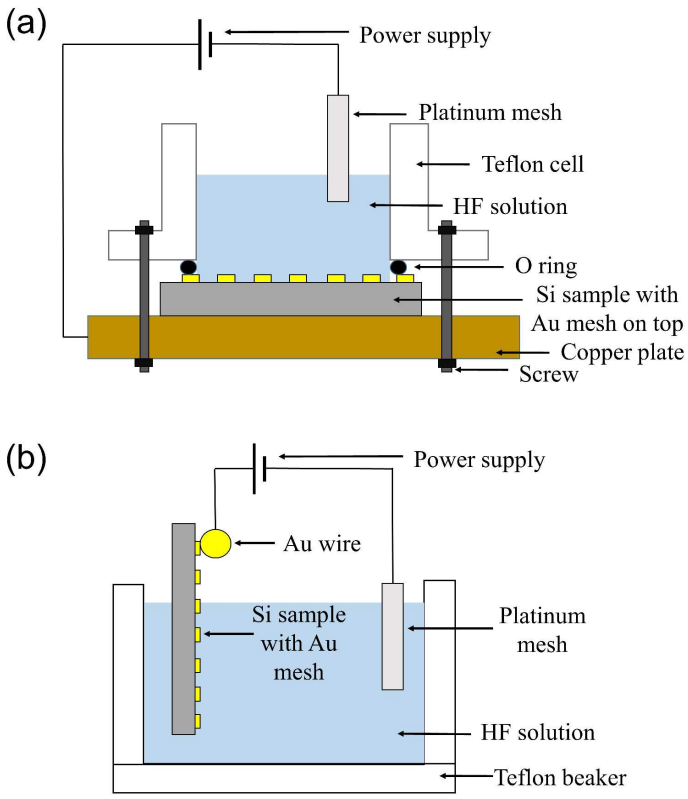
Figure 10. (a) J-V_a log-log plots for continuous-Au/N-Si and perforated-Au/N-Si interfaces. The best fit line is also shown for each trend. (b) Plot of ln $(1-J_0/J)$ vs ln $|V_a|$. (c) Calculated and experimental J-V_a plots for electrochemical etching of N-Si when the anodic contact was made through the Si substrate. The HF concentration was varied from 1M to 4M in the experiments.

Figure 11. Representative SEM images at different magnifications showing the morphologies of the nanostructures obtained for (a) P^+ and (b) N^+ Si substrates with the anodic contact made through the perforated Au. The current densities and durations of etching were (a) 12.5mA/cm^2, 10min and (b) 8mA/cm^2, 10min. White arrows indicate porous Si regions. The scale bars in (ai) and (bi) represent 1 μm, and those in (aii) and (bii) represent 500 nm. White arrows point to

porous Si, while the white dashed arrow points to solid Si. The dashed white line indicates the porous/ solid Si interface. In (b) all of the area shown under the wires is porous.

Figure 12. Representative SEM images at different magnifications showing the morphologies of the nanostructures obtained for (a) P^+ and (b) N^+ Si substrates with the anodic contact made through the Si substrate. The current densities and durations of etching were (a) 23mA/cm^2, 5min (bi) 23mA/cm^2, 5min and (bii) 28mA/cm^2, 5min. Yellow arrows point to a thin layer of anti-reflection coating on the Si nanowires that was not fully dissolved by the solvent NMP. The scale bars in (ai) and (bi) represent 1 μm while those in (aii) and (bii) represent 500 nm.

Figure 13. (a) Energy band diagram illustrating the process of surface generation of electron-hole pairs in N^+-Si by means of a tunnelling transition stage. Because this surface generation occurs at the etchant/N^+-Si interface, the majority of the holes are concentrated at the surface of the Si in contact with the HF, where they are consumed in porous Si formation, as illustrated in (b). As a result, little or no nanowire formation is observed.



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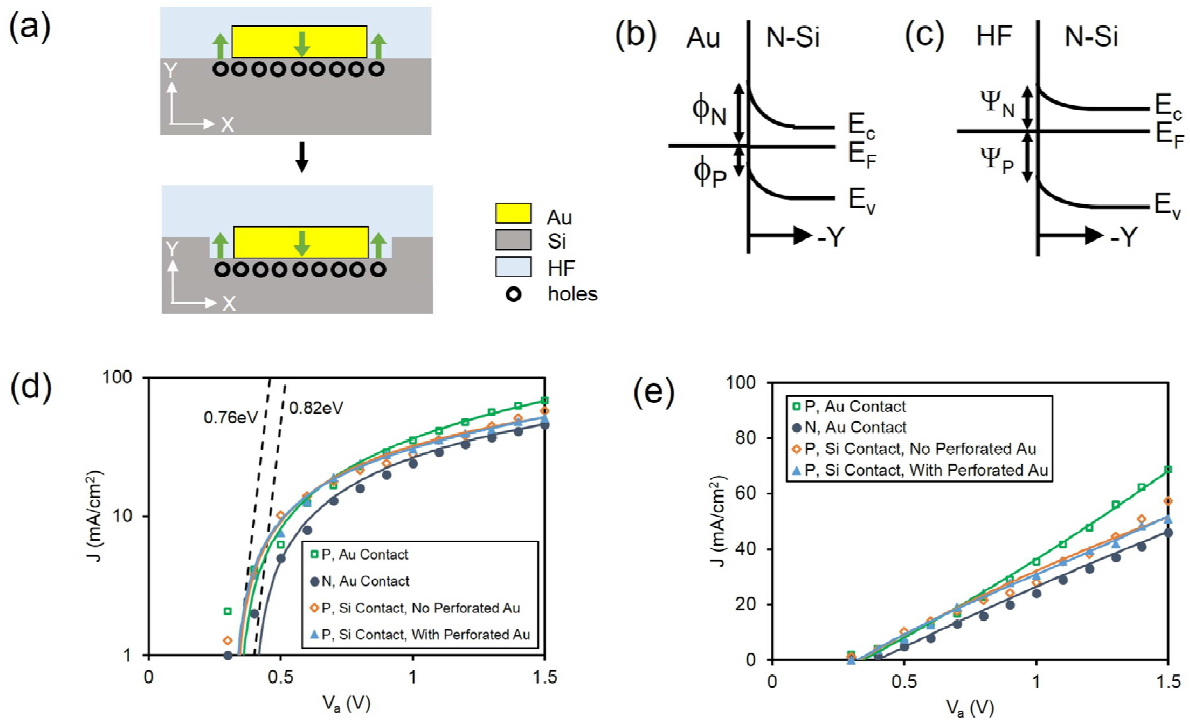

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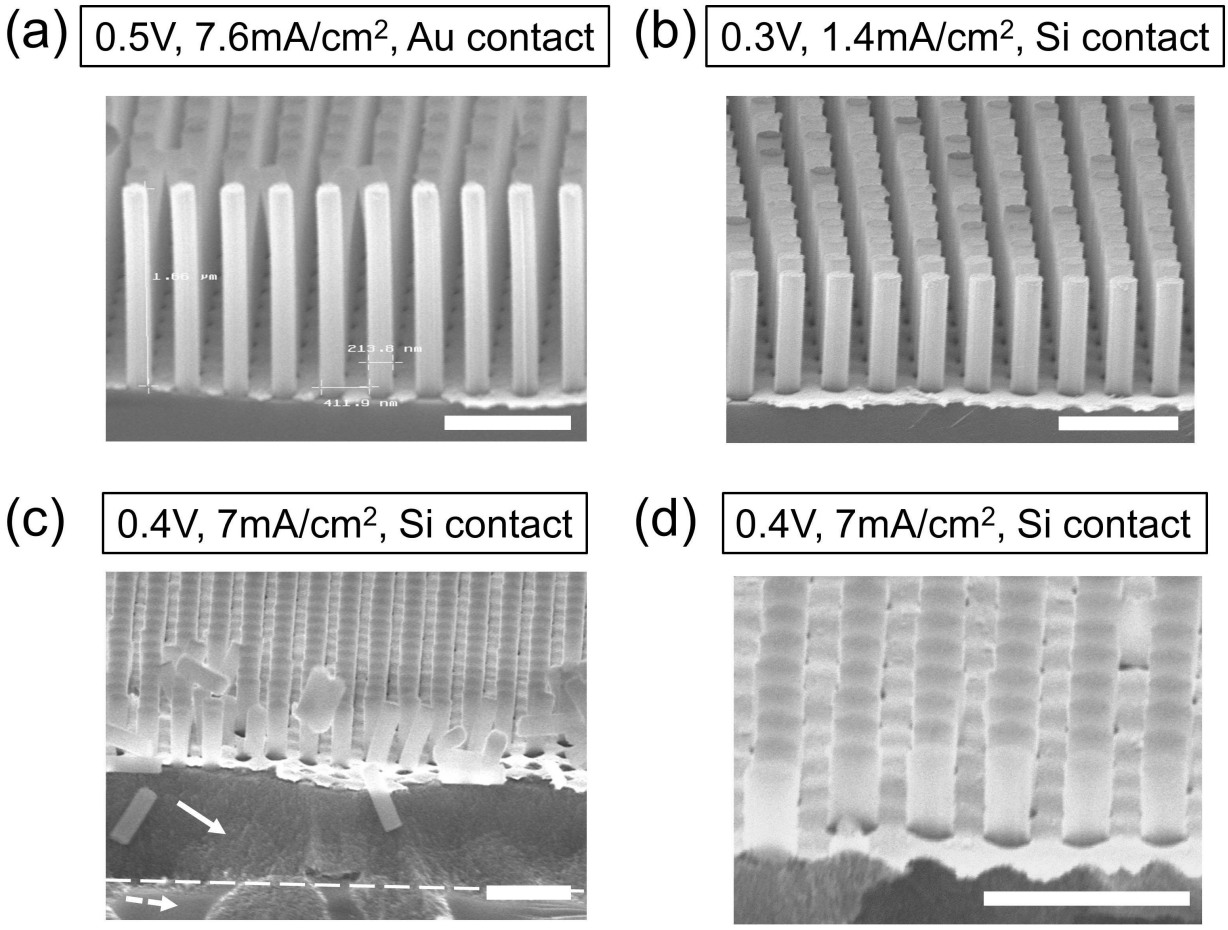

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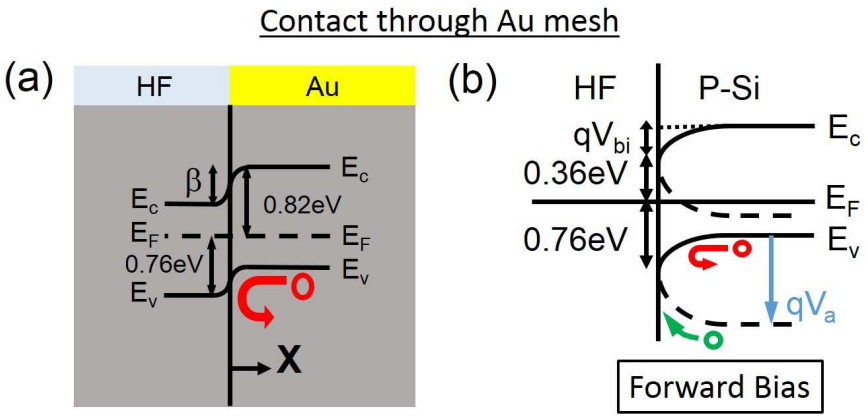

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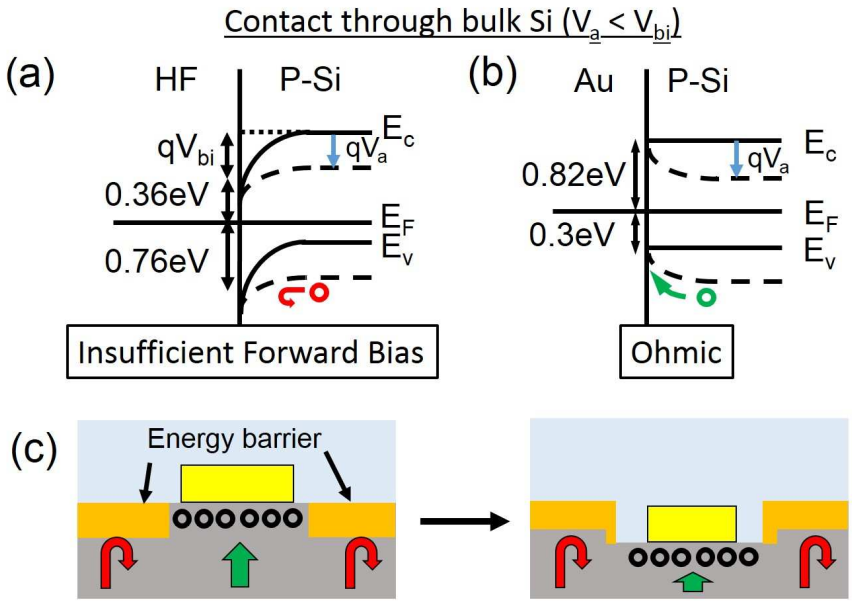

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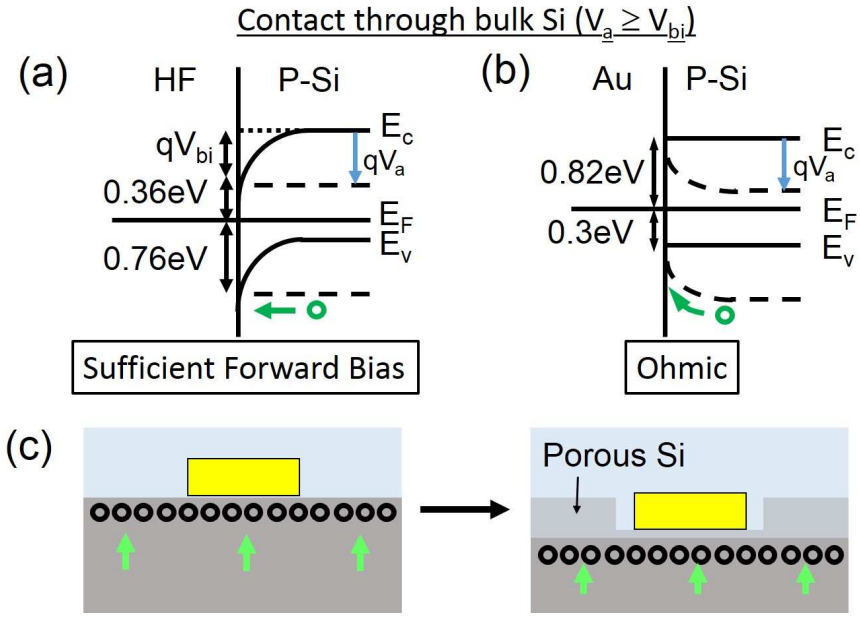

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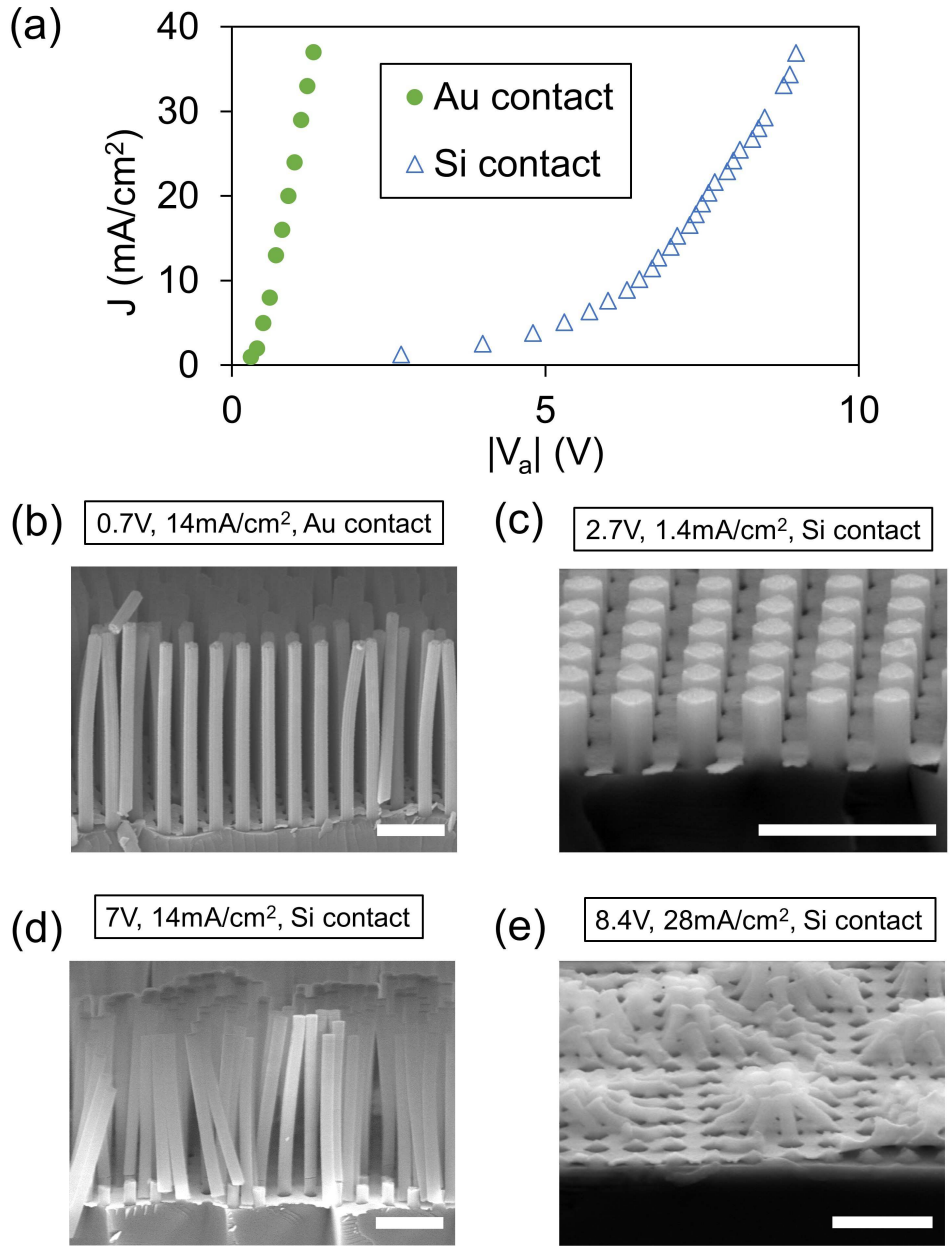

Figure 7. (a) J-V_a plot for MAAE of N-Si in 4M HF with the anodic contact made through the perforated Au and through the Si. (b) – (e) SEM images showing the morphology of the nanowires obtained for electrochemical etching of N-type Si substrates. The etching durations were (b) 10 min, (c) 10 min, (d) 10 min, and (e) 1 min. MAAE was the only etching mechanism operating, as no porous Si, an indication of regular anodic etching, can be observed. The scale bar represents 1μm.

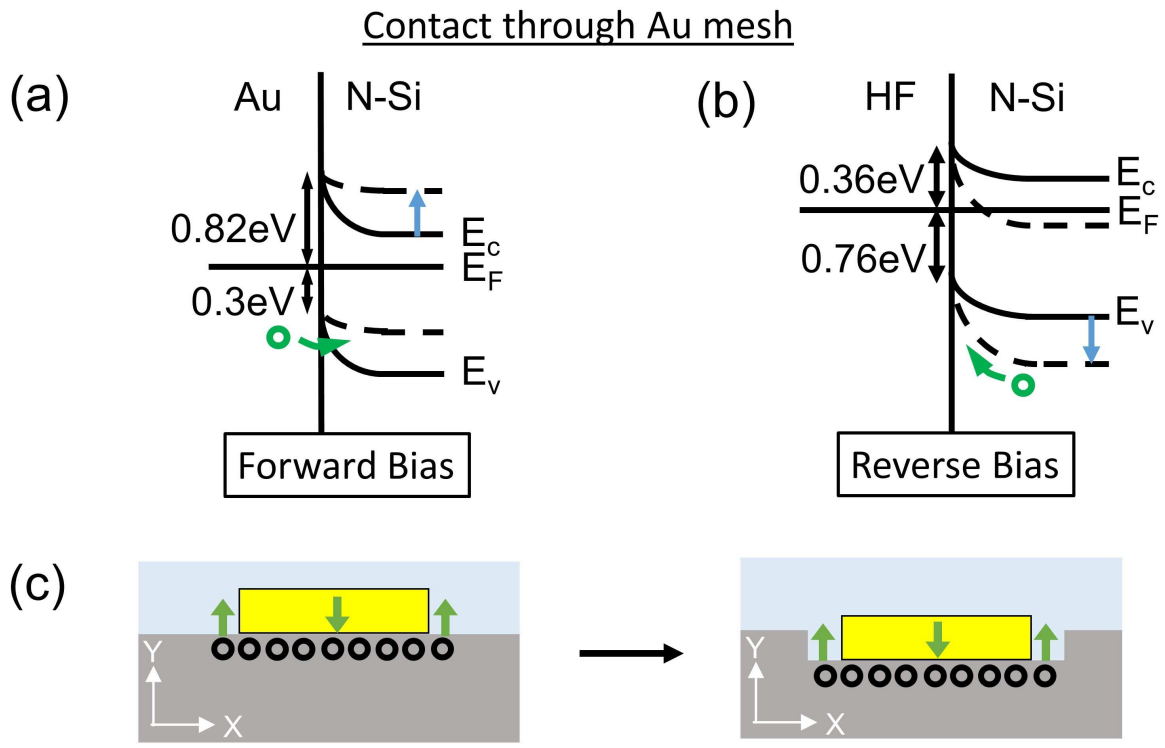

Figure 8. (a) Energy band diagram showing that hole injection rate from Au to N-Si (green arrow) is higher when a positive voltage (blue arrow) is applied to the perforated Au. (b) Energy band diagram showing how holes transferred from the perforated Au in (a) are trapped at the etchant/N-Si interface near the Au, causing Si dissolution. (c) Schematic diagram showing the injection of holes into N-Si through the Au and how these holes lead to selective etching at the Au/N-Si interface.

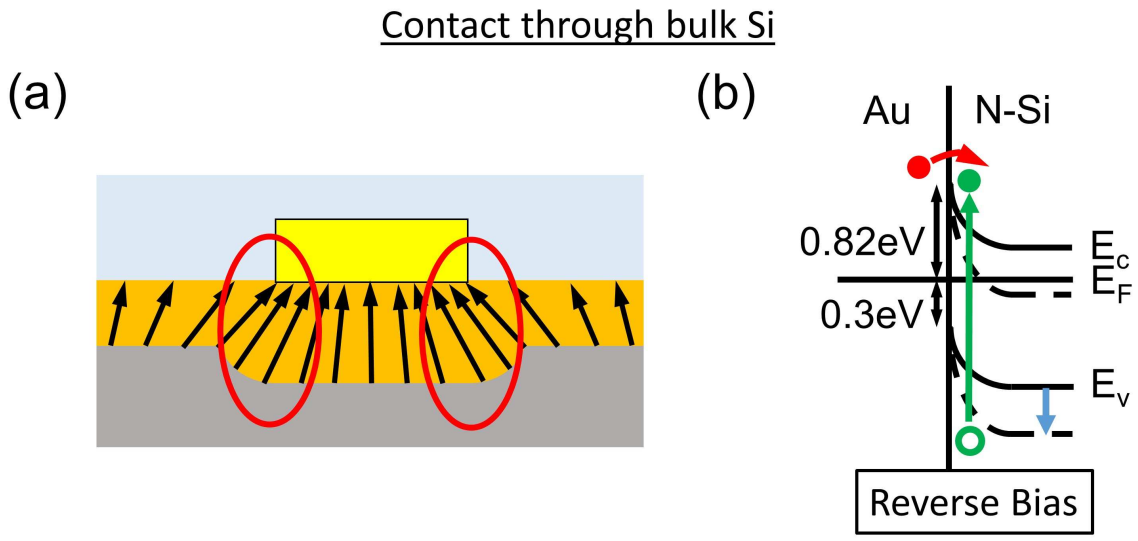

Figure 9. (a) Schematic diagram showing the electric field crowding effect. The concentration of electric field lines is highest at the Au edges where breakdown occurs. (b) Energy band diagram showing hole generation by impact ionization breakdown when a sufficiently large positive voltage is applied to the N-Si substrate.

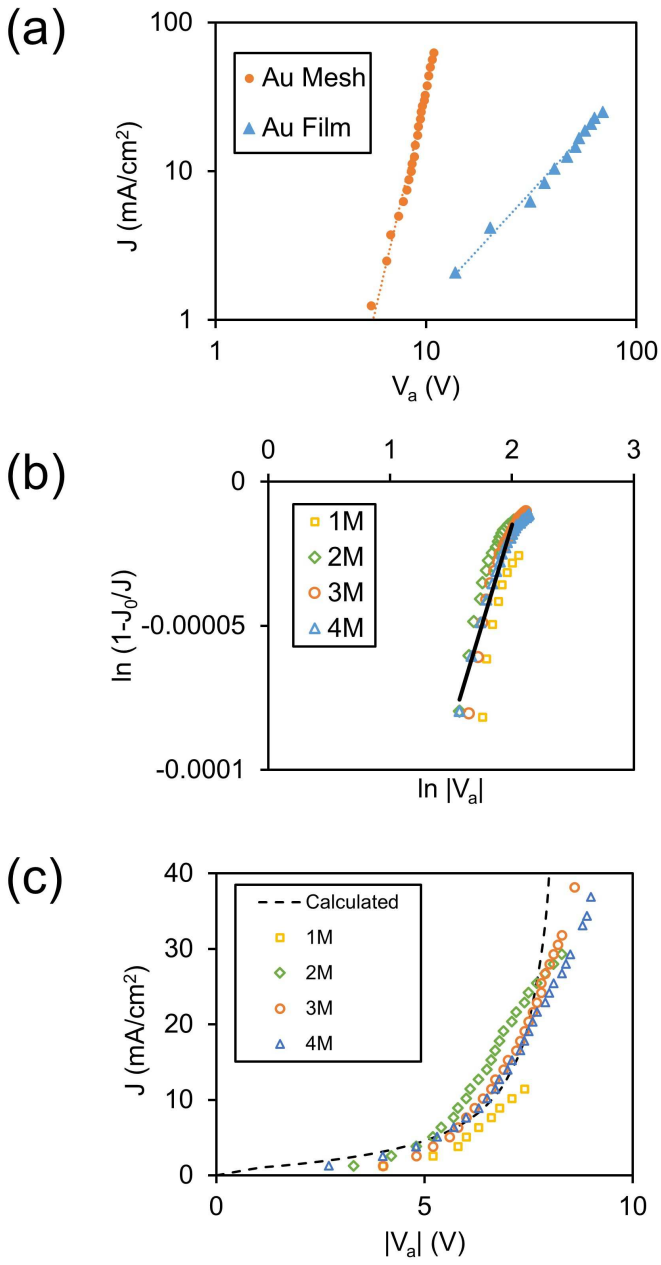

Figure 10. (a) J-V_a log-log plots for continuous-Au/N-Si and perforated-Au/N-Si interfaces. The best fit line is also shown for each trend. (b) Plot of ln $(1-J_0/J)$ vs ln $|V_a|$. (c) Calculated and experimental J-V_a plots for electrochemical etching of N-Si when the anodic contact was made through the Si substrate. The HF concentration was varied from 1M to 4M in the experiments.

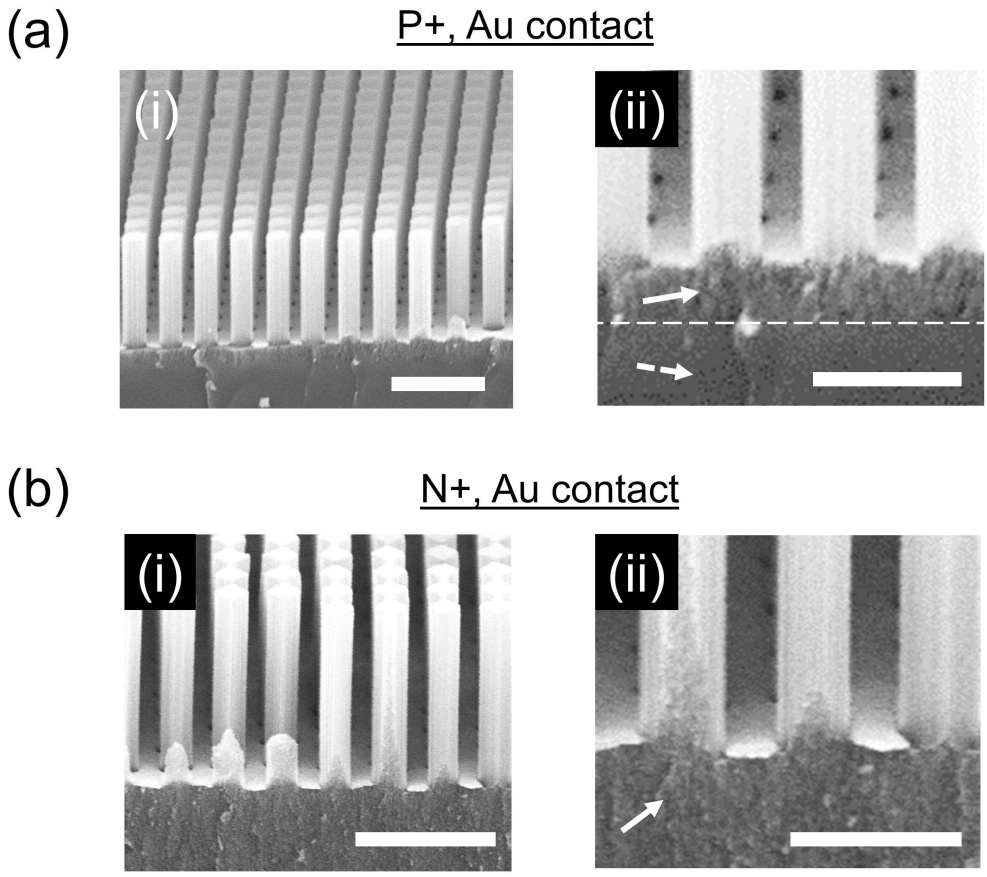

Figure 11. Representative SEM images at different magnifications showing the morphologies of the nanostructures obtained for (a) P^+ and (b) N^+ Si substrates with the anodic contact made through the perforated Au. The current densities and durations of etching were (a) 12.5mA/cm^2, 10min and (b) 8mA/cm^2, 10min. White arrows indicate porous Si regions. The scale bars in (ai) and (bi) represent 1 μm, and those in (aii) and (bii) represent 500 nm. White arrows point to porous Si, while the white dashed arrow points to solid Si. The dashed white line indicates the porous/ solid Si interface. In (b) all of the area shown under the wires is porous.

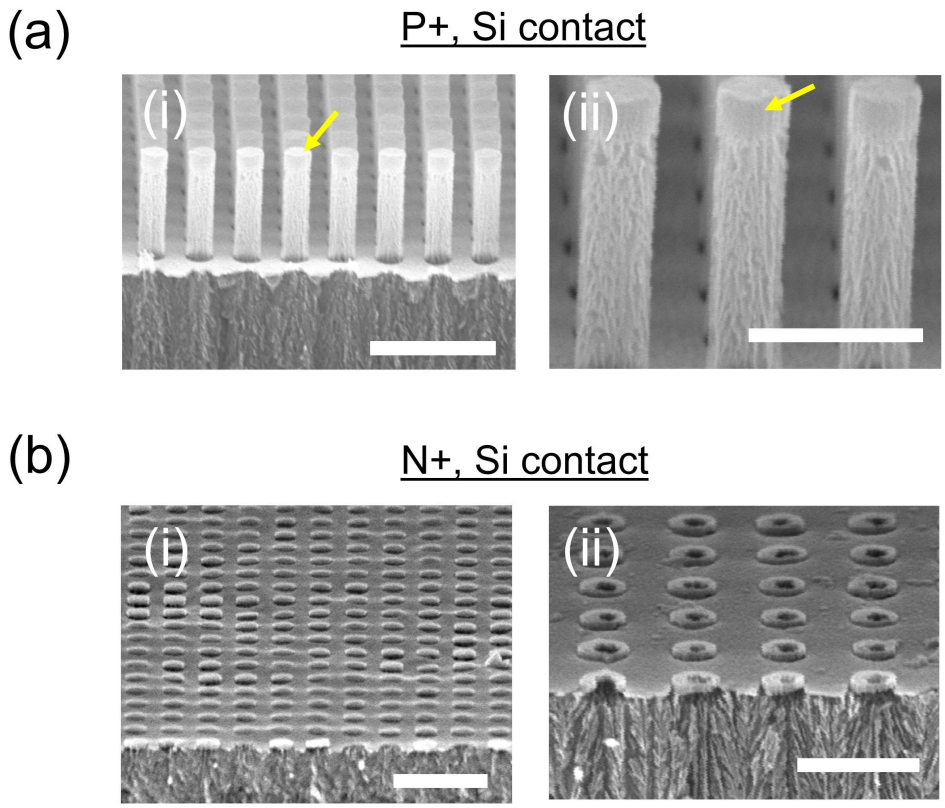

Figure 12. Representative SEM images at different magnifications showing the morphologies of the nanostructures obtained for (a) P^+ and (b) N^+ Si substrates with the anodic contact made through the Si substrate. The current densities and durations of etching were (a) 23mA/cm^2, 5min (bi) 23mA/cm^2, 5min and (bii) 28mA/cm^2, 5min. Yellow arrows point to a thin layer of anti-reflection coating on the Si nanowires that was not fully dissolved by the solvent NMP. The scale bars in (ai) and (bi) represent 1 μm while those in (aii) and (bii) represent 500 nm.

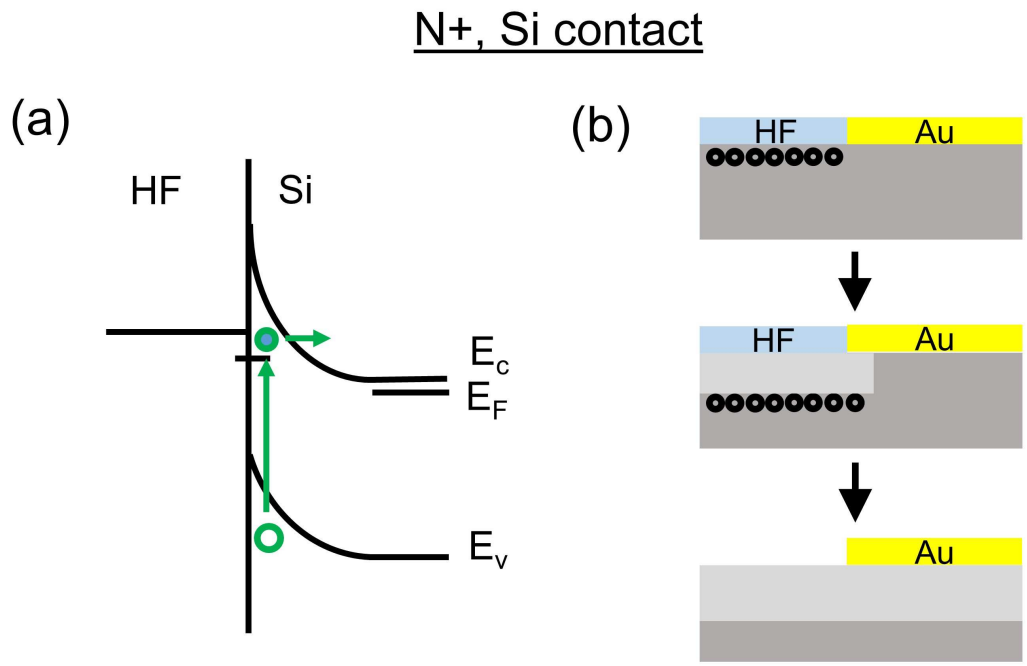

Figure 13. (a) Energy band diagram illustrating the process of surface generation of electron-hole pairs in N^+-Si by means of a tunnelling transition stage. Because this surface generation occurs at the etchant/N^+-Si interface, the majority of the holes are concentrated at the surface of the Si in contact with the HF, where they are consumed in porous Si formation, as illustrated in (b). As a result, little or no nanowire formation is observed.