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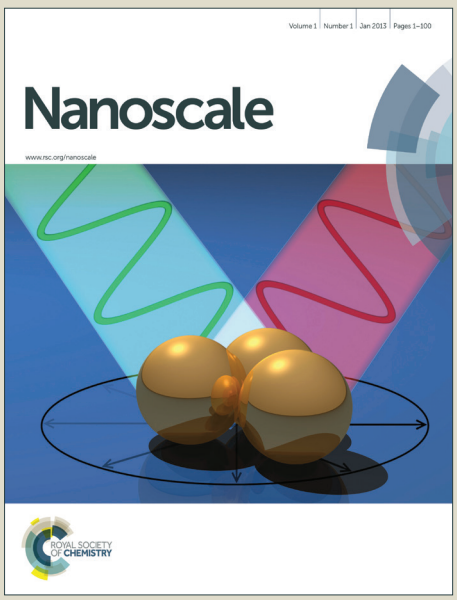

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Paper

The effects of shell layer morphology and processing on the electrical and photovoltaic properties of silicon nanowire radial p^+-n^+ junctions

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Single wire p^+-n^+ radial junction nanowire solar cell devices were fabricated by low pressure chemical vapor deposition of n^+ silicon shell layers on p^+ silicon nanowires synthesized by vapor-liquid-solid growth. The n^+-shell layers were deposited at two growth temperatures (650°C and 950°C) to study the impact of shell crystallinity on the device properties. The *n*-type Si shell layers deposited at 650°C were polycrystalline and resulted in diodes that were not rectifying. A pre-coating anneal at 950°C in H_2 improved the structural quality of the shell layers and yielded diodes with a dark saturation current density of 3×10^{-5}A/cm^2. Deposition of the *n*-type Si shell layer at 950°C resulted in epitaxial growth on the nanowire core, which lowered the dark saturation current density to 3×10^{-7}A/cm^2 and increased the solar energy conversion efficiency. Temperature-dependent current-voltage measurements demonstrated that the 950°C coated devices were abrupt junction p^+-n^+ diodes with band-to-band tunneling at high reverse-bias voltage, while multi-step tunneling degraded the performance of devices fabricated with a 950°C anneal and 650°C coating. The higher trap density of the 950°C annealed 650°C coated devices is believed to arise from the polycrystalline nature of the shell layer coating, which results in an increased density of dangling bonds at the p^+-n^+ junction interface.

Introduction

Radial junction silicon (Si) micro/nanowire array solar cells have been the subject of recent interest due to the potential advantages that they offer in terms of enhanced light trapping and improved carrier collection.[1-4] By separating light absorption from charge separation, the radial junction structure can reduce the requirements on Si purity without lowering solar energy conversion efficiency.[1] Additionally, employing the vapor-liquid-solid (VLS) technique for Si wire growth offers the possibility to fabricate radial junction devices on low cost substrates such as glass or plastic[5-6], thereby eliminating the use of thick, high purity crystalline Si substrates.[7-11]

The light absorption and collection advantages of wire array devices can be offset by their higher dark current, which arises from the large junction area compared to planar devices. The saturation current (I_0) in *p*-*n* junction diodes is given by $I_0 = A_j \times J_0$, where A_j is the junction area and J_0 is the saturation current density. For micro/nanowire array devices, the large A_j relative to the illuminated area, A_i, leads to an increase in I_0, which results in a reduction in the solar cell open circuit voltage (V_{oc}) because V_{oc} is proportional to $\ln(I_{ph}/I_0)$, where I_{ph} is the photogenerated current.[12] Consequently, to realize the benefits of the radial junction wire geometry, the junction region must contain a low density of traps and related defects to obtain a low I_0.[13]

Several methods have been used to fabricate Si-based micro/ nanowire *p*-*n* junction devices. Solar cells with V_{oc} in the range of 0.48V to 0.56V have been demonstrated by thermal diffusion of phosphorus into vertically aligned arrays of Si microwires fabricated by deep reactive ion etching (DRIE) or by VLS growth.[9-10, 14] Thermal diffusion produces high quality diodes because it places the *p*-*n* junction within the single crystal Si wire core. However, diffusion requires high processing temperatures of >950°C and is limited to the fabrication of simple *p*-*n* junctions. Radial junction devices with V_{oc} of 0.5 V to 0.6 V have also been demonstrated by plasma enhanced chemical vapour deposition (PECVD) of hydrogenated amorphous Si (*a*-Si:H) shell layers on Si micro/nanowires.[15-16] The *a*-Si:H layers are deposited at low temperatures of < 300°C and are effective at passivating the Si surface. However, the use of PECVD adds additional equipment and processing steps to the overall growth process. In contrast, low pressure chemical vapor deposition (LPCVD)

can be used to deposit Si shell layers in the same deposition chamber as nanowire growth. It also provides the flexibility to fabricate complex device structures such as *p*-*i*-*n* junctions and SiGe/Si heterostructures.[11, 17-21] In LPCVD growth, the crystallinity of the deposited Si layer is strongly dependent on growth rate, growth temperature and other process conditions and can range from amorphous to single crystal depending on the substrate and process conditions.[22] In addition, because the junction is located at the shell/core interface, metals and other impurities on the wire surface can degrade device performance.

This paper reports the effects of LPCVD growth temperature and wire surface pre-treatment conditions on the shell layer microstructure as well as the electrical and photovoltaic (PV) properties of individual radial p^+-n^+ junction Si nanowire devices. In contrast to earlier studies in which the Si nanowire core and shell layers were synthesized by LPCVD in the same growth chamber,[17-20] two separate CVD reactor chambers and processes were used to fabricate the *p*-type Si nanowire cores and *n*-type Si shell layers in this study due to dopant cross-contamination concerns that arose from the hot wall reactor configurations that were employed. Dark and light *I-V* characteristics were measured on these devices and reveal significant differences in the diode characteristics and solar energy conversion efficiency depending on the growth and processing conditions. Temperature-dependent dark *I-V* measurements were used to elucidate the role of the growth conditions on the dominant current transport mechanisms of the junction devices.

Experimental details

Nanowire synthesis

Intentionally doped *p*-type Si nanowires were first grown by the gold (Au)-catalyzed VLS technique on patterned Si(111) wafers. The pattern was composed of a square array of 80 nm thick Au catalyst particles that were selectively deposited within 1 μm diameter windows etched in a 100 nm thick SiO_2 layer at a pitch of 6 μm using a process described previously[23]. VLS growth was then carried out in a hot wall atmospheric pressure CVD reactor at 1050°C using $SiCl_4$ as the source gas in a H_2 carrier gas. The liquid $SiCl_4$ source was contained in a stainless steel bubbler that was held at -11.8°C and 1300 Torr. The flow rate of H_2 carrier gas through the bubbler was 80 sccm, which resulted in an inlet $SiCl_4$partial pressure of 9 Torr in the growth reactor. Intentional *p*-type doping of the Si nanowires was accomplished by adding 5 sccm of a trimethylboron (TMB) gas mixture (5000 ppm TMB in H_2). A total gas flow of 100 sccm was maintained by introducing an additional 15 sccm of H_2.

Metallic impurities such as Au form midgap trap states that act as highly efficient recombination centers for both holes and electrons, which degrade the performance of minority carrier *p*-*n* junction devices.[24] Therefore, the remaining Au present on the Si wire tip and surface after VLS growth was removed by first selectively etching the native oxide on the Si wire as well as the oxide pattern on the Si substrate in hydrofluoric (HF) acid for 5 minutes. The samples were rinsed in deionized water (DIW) and then placed directly into a commercial Au etch (Transene TFA) that was kept at a temperature of 40°C for 20 min to remove the exposed Au. Prior to shell coating, the wires were cleaned by immersing the sample in acetone, isopropyl alcohol (IPA) and DIW followed by a standard Si RCA cleaning process.[25] Next, the wires were thermally oxidized in dry O_2 for 2 hours at 1000°C to produce a 90 nm thick SiO_2 layer. The thermal oxide was selectively etched in HF and the oxidation process was repeated one more time using the same conditions. The second oxide layer was removed immediately prior to LPCVD of the n^+-Si shell.

Following synthesis, a portion of the *p*-type Si nanowires were removed from the growth substrate by mechanical agitation and released into the IPA solution. Individual wires were integrated into a test structure with multiple top electrodes defined by electron beam lithography for four-point resistance measurements. Field emission scanning electron microscopy (FESEM) measurements of the integrated Si nanowires showed that their diameter varied from 400nm to 620nm. The *p*-type Si nanowire resistivity determined from four-point resistance measurements was $(9.7\pm0.7)\times10^{-3}\Omega\cdot$cm, which corresponds to a *p*-type doping density of $\sim8\times10^{18}$cm^{-3} using the published hole mobility for high-purity crystalline Si.[26]

Radial p^+-n^+ junctions were fabricated by depositing *n*-type Si shell layers on the *p*-type Si nanowires before the wires were removed from the patterned growth substrate. The shell layers were deposited in a horizontal isothermal LPCVD system using 10% SiH_4 in H_2 as the precursor gas and 1% PH_3 in H_2 as the dopant gas. Immediately prior to loading into the N_2 purged LPCVD chamber, the samples were first cleaned by the RCA method and then dipped in HF for 1 min to selectively remove the thermal oxide and expose the crystalline Si nanowire surface. The *n*-type layer thickness and electron carrier concentration were calibrated by depositing a 1cm×1cm planar sapphire substrate in the same growth runs. Three different shell layer deposition conditions were used to study the effects of shell growth conditions on the structural and electrical properties of the radial junction devices.

The shell layer of the first sample (designated as Device A) was deposited at 650°C under a reactor pressure of 10 Torr with 200 sccm total flow, 2.5 sccm of SiH_4 and a PH_3/SiH_4 of 2×10^{-4}. The deposition time was 30 minutes which resulted in an *n*-type Si layer thickness of ~250 nm on the sapphire control sample. The shell layer of the second sample (Device B) was deposited at 950°C under 1 Torr reactor pressure with 200 sccm total flow, 2.5 sccm of SiH_4 and a PH_3/SiH_4 ratio of 5×10^{-3}. The deposition time was 3 minutes which resulted in an *n*-type Si layer thickness of ~280 nm on the sapphire. The shell layer of the third sample (Device C) was prepared by a two step process. The sample was initially heated to 950°C under 10 Torr pressure and 100 sccm H_2 for 20 minutes. The temperature was then reduced to 650°C and stabilized for 1 hour in H_2 flow, then a 650°C *n*-type Si thin film coating was applied with the exact same growth conditions as those for Device A. Room temperature Hall-effect measurements were carried out on the three thin films control samples deposited on sapphire. Electron concentrations of 2.1×10^{19}, 1.3×10^{19} and 1.8×10^{19}cm^{-3} were measured for samples grown under conditions designated as Devices A, B and C, respectively. The radial junction Si nanowires were removed from the Si substrate by mechanical agitation and released into IPA for structural characterization using transmission electron microscopy (TEM). TEM imaging and selected area diffraction (SAD) were performed in a JEOL-2010F field-emission TEM operated at 200kV.

Device fabrication and characterization

Single wire electrical test structures were fabricated using electric field-assisted assembly,[27] potassium hydroxide (KOH) selective etching to remove the *n*-type Si shell layer and contact

metal deposition. All devices were fabricated on heavily doped silicon substrates (*n*-type, resistivity<0.04Ω-cm) that were coated with 100 nm LPCVD silicon nitride. Interdigitated 50 nm thick silver electrodes were deposited for electric-field assisted assembly, which oriented and positioned single nanowires in lithographically-defined wells patterned in a sacrificial photoresist layer. Following nanowire assembly and removal of the photoresist, Ti(50nm)/Pd(600nm) contacts were patterned and deposited on the wires to serve both as contacts to the *n*-type Si shell layer and as anchors to hold the wires. The silver electrodes were then etched completely in Transene TFA gold etchant using a photoresist on the nanowire to protect the Ti/Pd contacts. An 80nm thick layer of silicon dioxide (SiO_2) was deposited by plasma-enhanced CVD (PECVD) and patterned as the hard mask to protect the *n*-type contacts and center segment of the wires during the KOH selective etching. The ends of the nanowires were then etched in 22.5% KOH solution at 65°C for 24 minutes, 23 minutes and 15 minutes for Devices A, B and C, respectively to remove the *n*-type shell and expose the p-type wire core. The etch rates of the *n*-type Si shell layers were found to vary depending on the growth conditions and doping level. Ti(50nm)/Pd(600nm) electrodes were then deposited on the exposed *p*-type core of the wires by evaporation and lift-off. *I-V* measurements were performed on all the single wire devices using an Agilent 4156B precision semiconductor parameter analyzer. A Lake Shore 331 temperature controller was used for variable temperature *I-V* measurement with liquid nitrogen. The photovoltaic performance of all of the single wire devices was also measured using a Keithley 6430 sub-fA remote source meter under 1-sun condition using a Class A AM 1.5G solar simulator.

Results and discussion

TEM images of the three types of radial p^+-n^+ junction nanowires are shown in Figure 1 along with their corresponding electron diffraction patterns. In all cases, the *p*-type Si nanowire core was found to be single crystal. The location of the shell/core interface is illustrated by dashed lines in the TEM images. As shown in Figure 1(b), the first type of wire with the *n*-type coating deposited at 650°C had a polycrystalline shell with a rough surface, which is expected for this low deposition temperature. The *n*-coating on the second type of wire that was synthesized at 950°C (Device B) deposited epitaxially on the *p*-type Si nanowire core, as shown in Figure 4-3(c). The third type of wire that included a 950°C anneal in H_2 prior to the 650°C also had a polycrystalline shell, as shown in Figure 4-3(d). However, the grain size of the shell layer was larger than the wire without the thermal pretreatment. In addition, the grains are better oriented with respect to the *p*-type Si core as indicated by the diffraction pattern in Figure 1(d) which contains more discrete diffraction rings than that of Figure 1(b). The TEM images were used to measure the thicknesses of the *n*-type Si shell layers for each of the device types. The average shell layer thicknesses measured on Devices A, B and C were 160±40 nm, 100±20 nm and 180±25 nm, respectively. It is interesting to note that the shell layers are ~30-60% thinner than the *n*-type Si layer thicknesses of 250 nm at 650°C and 280 nm at 950°C measured on the flat sapphire substrates grown under identical conditions. A similar reduction in growth rate was recently reported by Yoo et al. for silicon shell layers grown epitaxially on Si nanowire cores compared to growth on a large area silicon substrate.[28] The reduction in epitaxial growth rate was proposed to arise from enhanced surface desorption of SiH_4 near facet edges on nanowire sidewalls. A similar mechanism is believed to be responsible for the reduced shell layer growth rate in this study.

The electrical properties of the single wire devices were first characterized by room temperature *I-V* measurements between the *p*-type and *n*-type contacts and the radial p^+-n^+ junctions. Figure 2(a) shows the FESEM image of a fabricated radial p^+-n^+ junction nanowire device (Device B) in which n1 and n2 designate the contacts to the *n*-type shell and p1 and p2 designate the contacts to the *p*-type core. *I-V* measurements were taken between the contact electrode pairs p1-p2 (Figure 2(b)) and n1-n2 (Figure 2(c)) before and after rapid thermal annealing (RTA) in forming gas (4% H_2) at 300°C for 40 seconds. The *I-V* curves measured between n1 and n2 on the three device types were generally linear as-deposited due to the high doping density of the *n*-type Si shell layers and did not change significantly

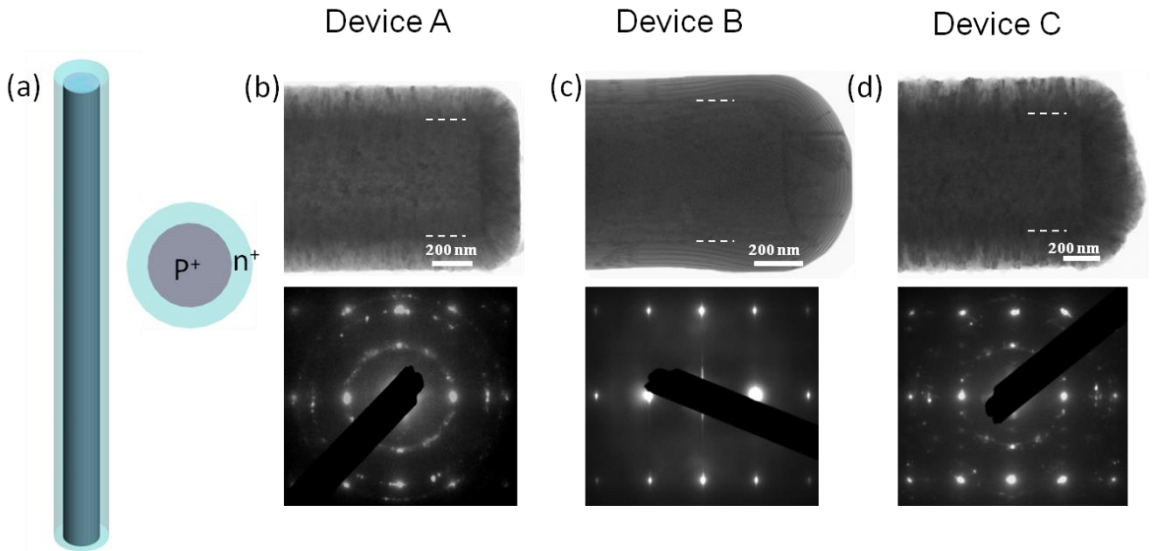

Figure 1 (a) Schematics of the core/shell (p^+/n^+) silicon nanowire structure. TEM images (top) and corresponding electron diffraction patterns (bottom) of diodes fabricated with (b) 650°C *n*-type Si shell layer coating (Device A); (c) 950°C *n*-type Si shell

layer coating (Device B) and (d) device fabricated with a 950°C anneal in H_2 prior to the 650°C *n*-type Si shell layer coating (Device C).

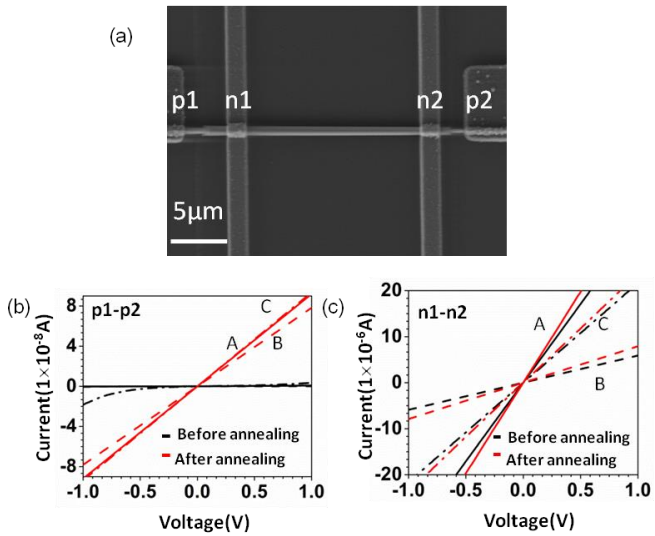

Figure 2 (a) FESEM image of a single nanowire device with four Ti/Pd contacts. p1 and p2 are in contact with p-type core, n1 and n2 are in contact with the n-type shell. Current-voltage(*I-V*) curves obtained across electrodes p1-p2 (b) and n1-n2 (c) of different types of devices.

after thermal annealing. The *I-V* curves measured between electrodes p1 and p2 on all three device types showed a higher resistance in the as-deposited state and non-linearity. After thermal annealing, however the resistance decreased significantly and the contacts exhibited Ohmic-like behavior.

Figure 3 shows the dark current density (*J*) in log scale as a function of voltage measured across the p^+-n^+ radial junctions of the three types of devices. For comparison, the *J-V* characteristics of a radial p^+-n^+ junction Si microwire array device formed by gas phase diffusion of phosphorus to form an n^+ shell into a *p*-type wire array fabricated by deep reactive ion etching of a crystalline p^+ Si substrate was also included.[14] Device A (with 650°C coating) behaves like a resistor rather than a rectifying junction, while Device B (with 950°C coating) and Device C (950°C annealing before 650°C coating) show current rectification with a rectification ratio greater than 100 at V=0.4 V. For forward bias voltages V < 0.2 V, the dark currents of Device B and Device C are mainly shunt leakage currents. The diode ideality factor of Device B varies from 1.6 to 2.0 for voltages between V=0.2 to 0.45V, which is range over which the shunt leakage and series resistance can be neglected. The ideality factor of Device C varies from 1.96 to 2.1 over the same voltage range. In contrast, the diffused p^+-n^+ junction has an ideality factor that ranges from 1.39 to 2 in the voltage range from 0.43V to 0.58V. These voltage ranges with ideality factors of ~2 can be modeled using the conventional double exponential *p-n* junction expression in which the non-ideal space-charge recombination current dominates.[29] The space-charge recombination current density is expressed as $J_r = qn_iW_d/2\tau$, where *q* is the charge of an electron, n_i is the intrinsic carrier density, W_d is the depletion region width and τ is the minority carrier lifetime. J_0 extracted from Device B, C and the diffused junction device are 2.59×10^{-7}A/cm^2, 3.27×10^{-5}A/cm^2 and 3.92×10^{-10}A/cm^2, respectively. The doping density of the core and shell of the coated devices are similar to that of the diffused device, so the larger J_0 of Devices B and C arises from the bulk electrical properties of the material and/or the junction interface. It is well known that gold, which was used as the catalyst for VLS growth of the *p*-type Si nanowire cores, forms deep level electronic states that reduce τ in bulk Si.

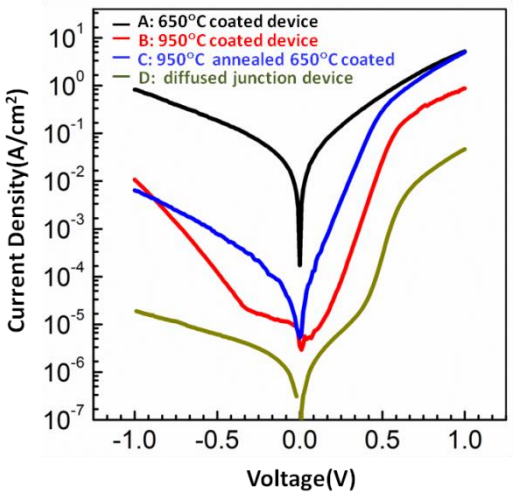

Figure 3 Semi-log plots of the dark current density-voltage(*J-V*) curves of the p^+-n^+ junction devices fabricated with n-type Si shell layers deposited by LPCVD under different conditions. The *J-V* curve from a diffused p^+-n^+ radial junction microwire (diameter of 8μm) array device is included for comparison.

Several studies have demonstrated that significant Au diffusion occurs along the outer surface of nanowires during the growth and subsequent cooling.[30-31] Consequently, the density of Au-related electronic states is expected to be highest near the surface of VLS-grown Si wires. The thermal oxidation/HF stripping process can effectively remove Au impurities and improve electrical and PV performance of radial *p-n* junction Si wire,[9] but it's not efficient enough to totally remove the contamination. Gold is still present in the wires, probably because of its strong diffusion during the oxidation step.[32] Bulk Au concentrations on the order of 1.7×10^{16} atoms/cm^3 have been measured by secondary ion mass spectrometry in Si wires grown by Au-catalyzed VLS growth. Assuming a similar Au impurity level in the *p*-type Si wires grown in this study, a minority–carrier recombination lifetime on the order of 3ns would be expected,[33] compared to ~3μs lifetimes typically obtained in *p*-type bulk silicon without Au impurities doped to a level of ~10^{18} cm^3.[34] So Au in the *p*-type silicon core is likely to be the reason for the larger current of Device B than the diffused junction device. Device C uses the same *p*-type wire core as Device B, consequently, the larger saturation current density of Device C may arise from additional traps introduced during the lower temperature n^+ shell deposition.

Temperature (*T*) dependent *I-V* measurements were also carried out on Devices B and C to identify the dark current mechanisms. The measured *I-V-T* curves of Devices B are shown in Figure 4(a). From the forward-biased region of Device B, the activation energy, E_a, for the $n \approx 2$ current mechanism in the diodes was obtained from an Arrhenius plot (Inset of figure 4(a)) of ln(I_0) versus 1000/*T*, where I_0 is dark saturation current, and $E_a = E_g/2$ for ideal recombination. The measured value for E_a is 0.49eV over the temperature range of 200K~300K for Device B. This value agrees well with $E_g/2$ = 0.56eV, showing the dark current is dominated by Shockley-Read-Hall (SRH) recombination through mid-gap states. For the range of T < 200K, the value of I_0 saturates, and is independent of temperature, suggesting that the dark current is dominated by tunneling. The reverse-biased current increases rapidly with bias at

higher voltage (V<-0.5V), and shows little temperature dependence. In this regime, the current is likely dominated by band-to-band tunneling (BTBT) current, which only has slight temperature dependence due to the temperature dependence of Si bandgap energy.[35] Figure 4(b) shows that the currents of Device B at V=-1V under different temperatures fit very

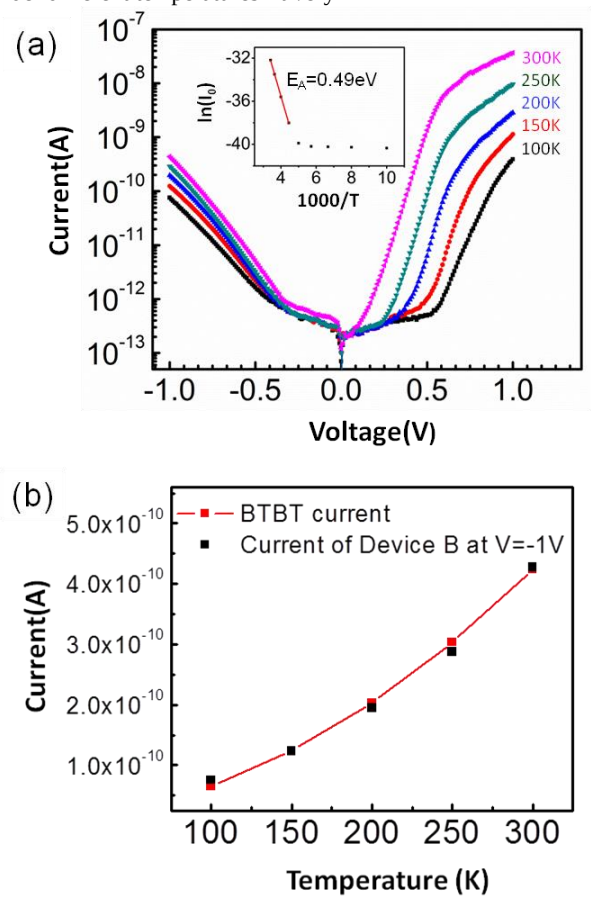

Figure 4 (a) Semi-log plot of variable temperature *I-V* curves of 950°C coated single wire device (Inset: Arrhenius plot of ln(I_0) versus 1000/T). (c) Current at bias V= -1V as a function of temperature. The red line with symbols is the calculated current using the BTBT current model and -1V.

well with the BTBT current model. These results indicate that Device B is a heavily doped abrupt junction with low interface state density.

The measured *I-V-T* curves of Device C are shown in Figure 5a. For Device C, the value of I_0 extracted from the $n \leq 2$ bias range decreases monotonically as the temperature is lowered, and the activation energy extracted from the Arrhenius plot (Inset of figure 5(a)) is 0.14eV, which is much smaller than $E_g/2$ = 0.56eV. A likely cause is that additional trap states with energies distributed throughout the bandgap are introduced during the shell coating, which results in an increase in the recombination current. Figure 5(b) is the Arrhenius plot of the reverse-biased current at V = -0.2, -0.5, -0.7 and -1V. For the low voltage region $|V|$ < 0.5V, the reverse current decreases exponentially with temperature at high temperatures. As the temperature is lowered, the junctions become temperature independent. This indicates that the reverse-biased current is composed of generation current and tunneling current components. As the temperature decreases, the generation current component decreases, and the tunneling current begins to dominate the reverse current. For the high voltage region $|V|$ > 0.5V, the reverse current has less temperature dependence. The dependence is not consistent with the pure BTBT current model, but may be explained by the multi-tunneling capture-emission model,[36] or multi-step trap-assisted tunneling model.[37-40] These data together with the small activation energy of reverse saturation current indicates that Device C has more trap states than Device B, which were likely introduced as a result of the low temperature n^+ layer coating.

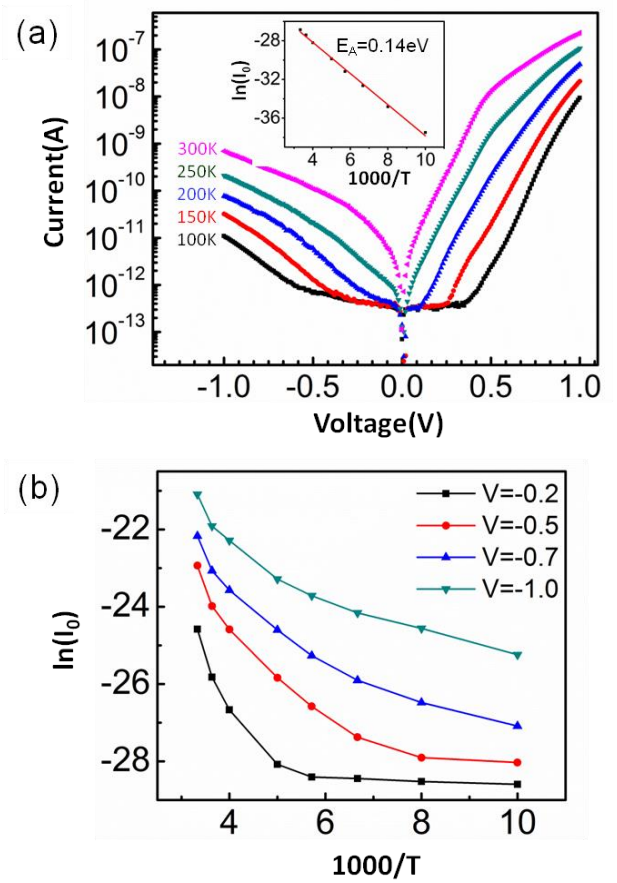

Figure 5 (a) Semi-log plot of variable temperature *I-V* curves of 950°C annealed 650°C coated single wire device (Inset: Arrhenius plot of ln(I_0) versus 1000/T). (b) Arrhenius plot of current as a function of temperature at bias V= -0.2, -0.5 -0.7 and -1V

The light current-voltage characteristics of device types B and C that exhibited current rectification were measured under 1 sun conditions (100mW/cm^2) using a Class A AM1.5G solar simulator, with current density (J) calculated using the projected NW area. The results are shown in Figure 6. The dimensions, series (R_s) and shunt (R_{sh}) resistances and solar cell parameters of the devices are listed in Table 1. Device B exhibits a larger V_{oc}, J_{sc} and *ff* than Device C (0.33V, 8.0 mA/cm^2 and 0.59 compared with 0.17V, 3.8 mA/cm^2 and 0.41), leading to the ~10 times greater energy conversion efficiency (1.6% compared with 0.27%). Device C which was fabricated using a 950°C anneal and 650°C coating temperature exhibits a significantly larger J_0 and smaller J_{sc} than Device B which was fabricated with an epitaxial Si shell deposited at 950°C. These results are consistent with the temperature-dependent *I-V* characteristics of the devices which indicated a higher density of trap states for Device C than Device B. The higher trap density of type C devices is believed to arise from the polycrystalline nature of the shell layer coating resulting in an increased density of dangling bonds at the p^+-n^+ junction interface. In addition, enhanced diffusion of impurities such as Au could occur along grain

boundaries in the polycrystalline shell leading to additional trap states compared to the epitaxial shell layer.

Conclusions

The effect of *n*-type shell LPCVD coating conditions on the structural and electrical properties of single wire radial p^+-n^+ junction solar cells was investigated. The shell layer morphology and pre-deposition

Device	Projected area (cm^2)	Junction area (cm^2)	J_0 (A/cm^2)	R_s (Ω)	R_{sh} (Ω)	J_{sc} (mA/cm^2)	V_{oc} (V)	*ff*	Efficiency η
B	4.04×10^{-8}	4.09×10^{-8}	2.59×10^{-7}	9.2×10^{6}	5.4×10^{8}	7.8	0.34	0.59	1.60%
C	4.70×10^{-8}	3.96×10^{-8}	3.27×10^{-5}	2×10^{6}	1.3×10^{9}	3.8	0.17	0.42	0.27%

Table 1 Diode and photovoltaic properties of single nanowire devices

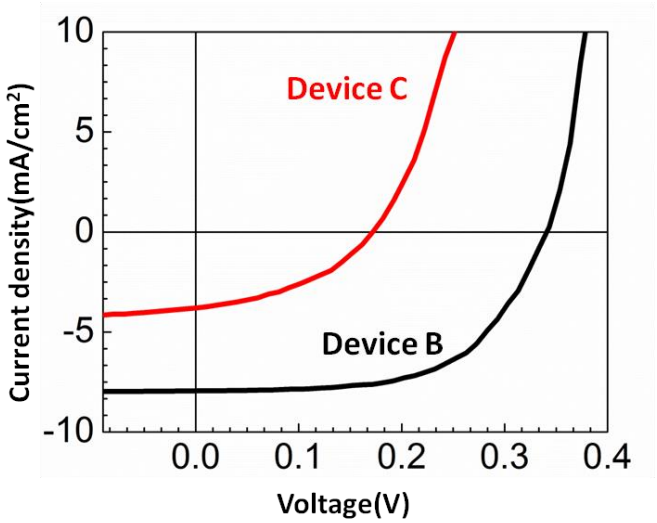

Figure 6 Light current density-voltage(*J-V*) plots of single wire p^+-n^+ junction Si nanowire devices with different n-type shell layer coating measured under 1-sun illumination.

annealing conditions were found to significantly impact the dark and light *I-V* characteristics of the devices. Higher deposition temperature (950°C) resulted in epitaxial growth of the n^+ shell on the p^+ core, and the resulting single wire device exhibited a low dark saturation current density (J_0=2.59×10^{-7} A/cm^2). Temperature-dependent *I-V* measurements show that the dark saturation current is mainly dominated by SRH recombination through mid-gap states, and the BTBT current at high reverse bias suggests Device B has a heavily doped abrupt junction. Under 1-sun AM1.5G illumination, the single p^+-n^+ junction nanowire device had J_{sc}~7.8mA/cm^2, V_{oc}~0.34V, *ff*~0.59 and η~1.60%. Reduced deposition temperature (650°C) resulted in a polycrystalline *n*-type shell, and the resulting devices did not exhibit current rectification or a light response. However, when the *p*-type Si nanowires were annealed at 950°C before the 650°C coating, the diodes exhibited current rectification but the dark saturation current density of 3.27×10^{-5} A/cm^2 was two orders of magnitude higher than the devices with the epitaxial n^+ shell. The device grown with a 650°C n^+ shell exhibited a J_{sc}~3.8mA/cm^2, V_{oc}~0.17V, *ff*~0.42 and η~0.27%. In this case, the *n*-type Si shell layer exhibited a granular texture, however, the grain size was increased and the film was more crystallographically oriented with respect to the *p*-type Si nanowire core compared to the device fabricated without the high temperature anneal step. Temperature-dependent *I-V* measurements showed that compared to the 950°C coated devices, additional trap states were introduced during the shell coating resulting in an increase in the recombination current, and the reverse current at high reverse bias is mainly due to multi-step trap-assisted tunneling current. For the low temperature coated devices, substantial improvements in electrical properties as well as solar cell efficiency can be realized by further reducing the traps at the junction interface and in the shell layer.

It should be noted that, in our study, high temperatures (≥950°C) were employed both for VLS growth of the *p*-type Si nanowire core and epitaxial growth of the *n*-type Si shell layer. Also, ex-situ removal of Au via wet etching and thermal oxidation and stripping was done before shell deposition. Nevertheless, it is possible to sequentially grow both the Si nanowire core and epitaxial Si shell layers by LPCVD at lower temperatures in the same reactor chamber using a cold wall reactor geometry and high vacuum conditions.[17-19] In addition, further reductions in the dark current and improvements in the photovoltaic properties would be expected in radial p^+-*i*-n^+ structures, however, it was not possible to obtain intrinsic Si layers in the hot wall LPCVD chamber that was employed in this study.

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Notes and references

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