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Charge transport and mobility engineering in two-dimensional transition metal chalcogenide semiconductors

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Two-dimensional (2D) van der Waals semiconductors represent the thinnest, air stable semiconducting materials known. Their unique optical, electronic and mechanical properties hold great potential for harnessing them as key components in novel applications for electronics and optoelectronics. However, the charge transport behavior in 2D semiconductors is more susceptible to external surroundings (*e.g.* gaseous adsorbates from air and trapped charges in substrates) and their electronic performance is generally lower than corresponding bulk materials due to the fact that surface and bulk coincide. In this article, we review recent progress on the charge transport properties and carrier mobility engineering of 2D transition metal chalcogenides, with a particular focus on the markedly high dependence of carrier mobility on thickness. We unveil the origin of this unique thickness dependence and elaborate the devised strategies to master it for carrier mobility optimization. Specifically, physical and chemical methods towards the optimization of the major factors influencing the extrinsic transport such as electrode/semiconductor contacts, interfacial Coulomb impurities and atomic defects are discussed. In particular, the use of *ad-hoc* molecules makes it possible to engineer the interface with the dielectric and heal the vacancies in such materials. By casting fresh light onto the theoretical and experimental works, we provide a guide for improving the electronic performance of the 2D semiconductors, with the ultimate goal of achieving technologically viable atomically thin (opto)electronics.

1 Introduction

Van der Waals (vdW) crystals represent a large family of materials that exhibit unique layered architectures, including graphite, metal oxides, chalcogenides, phosphates, cuprates, which differ on their chemical composition and crystal structure, leading to markedly different properties, *e.g.* their electronic characteristics can span from metallic to insulating. These materials all share a common feature—large interlayer vdW spacings and weak interlayer interactions, which results in peculiar mechanical properties like interlayer sliding and cleavability. In prehistory (the 4th millennium B.C.) graphite, the most widely known vdW material, was used as pottery paint. Nowadays it is still an unbeatable component for day-to-day applications as pencil cores, motor electrodes, and dry lubricants. The characteristic layered structure also endows vdW materials intriguing chemical and physical properties which make them the building blocks of choice for intercalation chemistry,[1] energy storage,[2] and superconductivity.

Remarkably, the structural anisotropy allows for mechanical exfoliation of vdW crystals down to the atomic scale.[3–5] The

two-dimensional (2D) vdW flakes such as monolayers of metal chalcogenides represent the thinnest manifestation of stable materials that exhibit an energy bandgap. Following the success of graphene,[6,7] the research endeavor on the 2D vdW semiconductors rapidly increased.[8–36] The concurrence of several unique properties, including the atomic thickness, sizable bandgap, high carrier mobility and absence of dangling bonds, and the fast-growing synthesis techniques[37–78] pave the way towards revolutionary applications, such as ultimate atomically-thin-body field-effect transistor (FET),[79–82] stacked vdW superlattices and heterojunctions,[83] valleytronics,[84–89] and novel flexible and transparent electronics and optoelectronics.[90–99] Here we will focus on the role of 2D vdW crystals as electroactive channels in FETs and, more specifically, on the factors influencing the electronic performances of the atomically-thin-body FETs and the devised strategies to improve them.

In fact, one of the prime interests in 2D crystals rests in their potential as conduction channels in digital circuits beyond silicon. The characteristic FET scaling length is derived as $\lambda = \sqrt{t_s t_{ox} \varepsilon_s / \varepsilon_{ox}}$,[100] where ε and t are electrical permittivity and thickness, and the subscripts s and ox denote semiconductor and oxide dielectric. The thinner the FET channels, the smaller and faster the FETs will be.[101–103] Given the material physical limitation (such as surface roughness control) and production yield, the thickness of silicon channels can hardly be less than 5 nm,[104] be-

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ing much larger than the atomic scale. Exploiting 2D vdW semiconductors as FET channels would enable further device miniaturization after silicon.[105,106]

It is noteworthy that the 2D planar structure also offers full compatibility to conventional semiconductor processing such that they can be perfectly carved for making highly ordered FET arrays, being a critical factor rivaling the 1D nanostructures. The third figure of merit of the vdW semiconductors is the self-saturated nature of the surfaces which, in principle, contain no dangling bonds and are free of the composition fluctuation at the channel/dielectric interfaces, making them immune to the notorious 'sixth-power law' mobility degradation[107] due to surface roughness (*i.e.* interface asperity) that occurs in non-vdW superlattices and silicon.[108,109] The chemical stability is the fourth advantage which makes them stand out over other semiconductor membranes carved from 3D materials (*e.g.* silicene[110] and germanene), which degrade rapidly in ambient conditions. In contrast, most vdW crystals are stable in air; some of them like graphite and molybdenite exist as minerals in nature.

In the framework of post-silicon microelectronics, a great attention was initially devoted to the metallic graphene for its ultrahigh carrier mobility[3] rather than the 2D vdW semiconductors.[4,111] It was then realized that it would be extremely difficult to use graphene for any digital application due to the absence of a bandgap, despite sustained efforts on bandgap and device engineering.[112–125] Renewed interest on 2D vdW semiconductors arose in 2011 when Kis *et al.* reported high carrier mobility in monolayer MoS_2 FETs.[81,126]

As far as the FET performance is concerned, one of the essential figures of merit is the field-effect mobility (μ_{FE}), which determines how fast a charge can move through a semiconductor or a metal under the effect of an external electric field. For 2D materials, where surface and bulk structurally coincide, a major yet not fully unanswered question is why in such atomically thin semiconductors carrier mobility undergoes degradation[4,111] unlike in the corresponding bulk systems,[127] in spite of the immunity to the surface roughness scattering. It appears obvious that the full exposure of the lattice atoms to the environment can lead to strong carrier scattering and lower carrier mobility. In order to find out new strategies for improving carrier mobility, in-depth and quantitative answers to the thickness dependence of electronic performances are highly desirable.

Several theoretical studies were performed to cast light onto the charge transport behavior of the 2D vdW semiconductors. Kaasbjerg *et al.* extensively investigated the role of lattice phonons in MoS_2 monolayers and predicted an intrinsic transport mobility of $\sim 410\,cm^2V^{-1}s^{-1}$ at room temperature.[128,129] Jena *et al.* first considered the scattering generated by long-range Coulomb impurities in multilayer MoS_2.[130] Li *et al.* addressed the role of the channel thickness in carrier scattering by considering various scattering mechanisms and ascribed the interfacial impurity scattering as the origin of the strong thickness dependence of mobility.[131] Alongside phonons and Coulomb impurities, Ma *et al.* were the first to consider the role of remote interface phonons, located in the dielectric, on the electronic behavior and identified the implications of using high-κ dielectric in the atomically-thin-body

FET.[132] The above works represent the theoretical framework of this review. On the other hand, a notable experimental effort was devoted to improving the mobility of the 2D vdW flakes by i) eliminating adverse extrinsic factors to attain material characteristics close to their intrinsic behavior, and ii) upon strain engineering to gain extra performance enhancement. To date, dramatic progress has been achieved on the first route in particular through contact optimization and carrier scattering suppression.

The review will discuss the origin of the high thickness dependence of electronic performance exhibited by 2D vdW semiconductors, providing a theoretical insight and summarizing the devised strategies to minimize its effect. A brief introduction is first given in section 1 to illustrate the advantages and current hurdles in using the 2D vdW semiconductors as the active layer in FET devices. Section 2 outlines the material parameters regarding the electronic behavior, including band structure, carrier effective mass, and lattice phonons. In order to provide the reader with information on the typical electronic properties of MX_2 flakes, section 3 gives an exhaustive list of the values of carrier mobility measured so far, together with fabrication and measurement details. The extrinsic and intrinsic factors responsible for the charge transport behavior are outlined in section 4, shining light onto the origin of the dependence of the electronic performances on thickness. Section 5 describes various physical and chemical strategies on mobility engineering developed in recent years, followed by the state-of-the-art performance achieved after the mobility engineering. Section 6 presents the experimental standards one should follow to avoid experimental traps and unintentional errors, which are neglected in some literature. Finally, a summary and outlook on the above-mentioned research field are given that are meant to suggest new avenues to minimize the charge scattering while paving the way towards chemical strategies to be adopted.

2   Basic material properties

The term *chalcogen* was proposed around 1930 by Werner Fischer to denote the elements of Group 16. The use of such a term was approved in 1938 by the Committee of the International Union of Chemistry (later IUPAC).[133] It was then widely accepted that the elements sulfur, selenium, and tellurium are named chalcogens whereas their compounds chalcogenides. A large number of chalcogenides exhibit a layered structure and lend themselves to the application as the conduction channels in FETs.

In this section we outline the material parameters pertinent to electronic transport behavior in 2D vdW semiconductors, including crystal structure, phonon vibration mode, band structure, carrier effective mass, and electrical permittivity. Special attention is paid to the variation of these parameters with reducing material thickness, which may lead to mobility change.

2.1   Atomic structure

The metal chalcogenides chemical composition discussed in the review can be described by the formula MX_2 (M=Ti, Zr, Hf, V, Nb, Ta, Cr, Mo, W, Pt and X=S, Se, Te). Figure 1a displays the location of these elements in the element periodic table. The layered
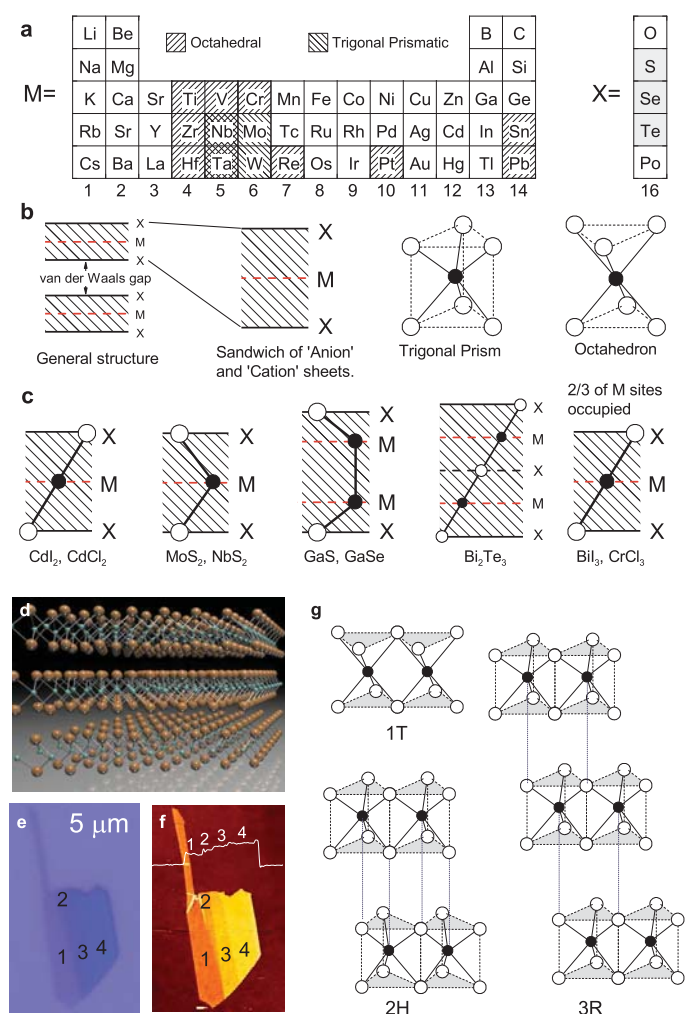
Fig. 1 (a) Element periodic table showing the metal and chalcogen elements that form the MX_2 type van de Waals crystals. The shadows indicate the structure coordination of the crystals (octahedral or trigonal prismatic). Reproduced with permission from ref. 1, copyright 1978, Elsevier Ltd. (b) The two basic trigonal prismatic and octahedral coordination units for the MX_2 crystals. (c) Cross-sectional (along $11\bar{2}0$ plane) atomic coordination for the MX_2 chalcogenides and other typical van de Waals crystals. Panels (b) and (c) are reproduced with permission from ref. 8, copyright 1969, Taylor & Francis Ltd. (d) Three-dimensional schematic representation of a typical 2H-MX_2 structure with the chalcogen atom X in yellow and the metal atom M in cyan. (e) and (f) show optical and corresponding AFM images for a MoS_2 flake with consecutive thickness values from 1 to 4 layers. Panels (e) and (f) are reproduced with permission from ref. 134, copyright 2012, American Chemical Society. (g) Schematic arrangements of sandwich units for the typical three phases of MoS_2 crystals: 1T (tetragonal symmetry, one layer per repeat unit, octahedral coordination), 2H (hexagonal symmetry, two layers per repeat unit, trigonal prismatic coordination), and 3R (rhombohedral symmetry, three layers per repeat unit, trigonal prismatic coordination). The dotted vertical lines indicate the alignments of interlayer M and X atoms.

structure originates from the stacking of hexagonally packed X–M–X trilayer sandwich units. The metal and chalcogen atoms are covalently bonded as individual 'tricomponent' (trilayered) sandwich units while the different sandwich units are held together by

weak vdW force, resulting in a remarkably easy mechanical cleavage. In compliance with the terminology used in literature, we call an individual 'tricomponent' sandwich unit as a MX_2 monolayer. Within each layer, the atoms are arranged in configuration of either trigonal prism or octahedron (Fig. 1b), resulting in different lattice symmetries. It is worth noting that the layered structure is not only limited to the dichalcogenides composed of transition metal elements; some non-transition metal (*e.g.* Ga, In, Bi, Sn, Pb) chalcogenides and halides also show layered structures. Figure 1c illustrates some examples of monochalcogenides, trichalcogenides and halides that also possess a layered structure. Notably, Bi_2Se_3 and Bi_2Te_3 are well-known topological insulators.

Due to compositional variation, the MX_2 family covers a wide range of electronic properties, spanning from those of an insulator like HfS_2, to semiconductors like MoS_2 and semi-metals like WTe_2 and TeS_2, way down to true metals like NbS_2 and VSe_2.[8] In this review article we focus our attention on semiconductors with bandgap around 1–2 eV. As a prototype MX_2 semiconductor, we will especially concentrate on the structure and properties of MoS_2 layers. Figure 1d shows the atomic structure for typical 2H-phased MoS_2. It exists in nature as the mineral *molybdenite* and can be easily mechanically exfoliated into few-layer flakes. Figures 1e and 1f illustrate the optical and atomic force images for an exfoliated MoS_2 flake with consecutive numbers of layers (NL, N is an integer) from 1 to 4. In fact, MoS_2 has three different structural phases: 1T (tetragonal symmetry), 2H (hexagonal symmetry) and 3R (rhombohedral symmetry), as illustrated in Fig. 1g. Among them, the 2H and 3R phases are semiconducting while the 1T phase is metallic. Phase change can occur under external stimuli[135,136] or chemical treatment,[137–139] for example, by soaking in n-butyl lithium MoS_2 can undergo phase change from semiconducting 2H to metallic 1T phase. The phase change induced property change has been employed to reduce the contact resistance, as will be discussed in section 5.

2.2 Lattice phonon modes

In elastic materials the lattice phonon is a collective atom displacement with atoms vibrating around their equilibrium positions. Such a displacement can modify the carrier pathway in two ways: 1) deformation of the local lattice potential, and 2) formation of electric fields due to polarizability and piezoelectricity of lattices. These two scattering mechanisms will be discussed in section 4.2. Lattice phonons have a thermal origin and exist at non-zero temperatures; hence, unlike other scattering centers phonon is an intrinsic scattering factor.

The phonon modes of bulk MX_2 vdW crystals have been fully investigated in the 1970–80s. Related information such as symmetry representation, vibration mode, and optical activity are well documented in literature.[141–151] Taking advantage of the capacity to reduce the thickness of the crystal, new information such as frequency shift[152] and excitation of new phonon modes[153,154] have been acquired in recent years.

According to the energy-momentum (ω-k) dispersion relations, phonons are categorized into two types: acoustic ($\omega \propto k$ at $k \approx 0$) and optical ($\omega \approx$ constant), which represent the relative motion
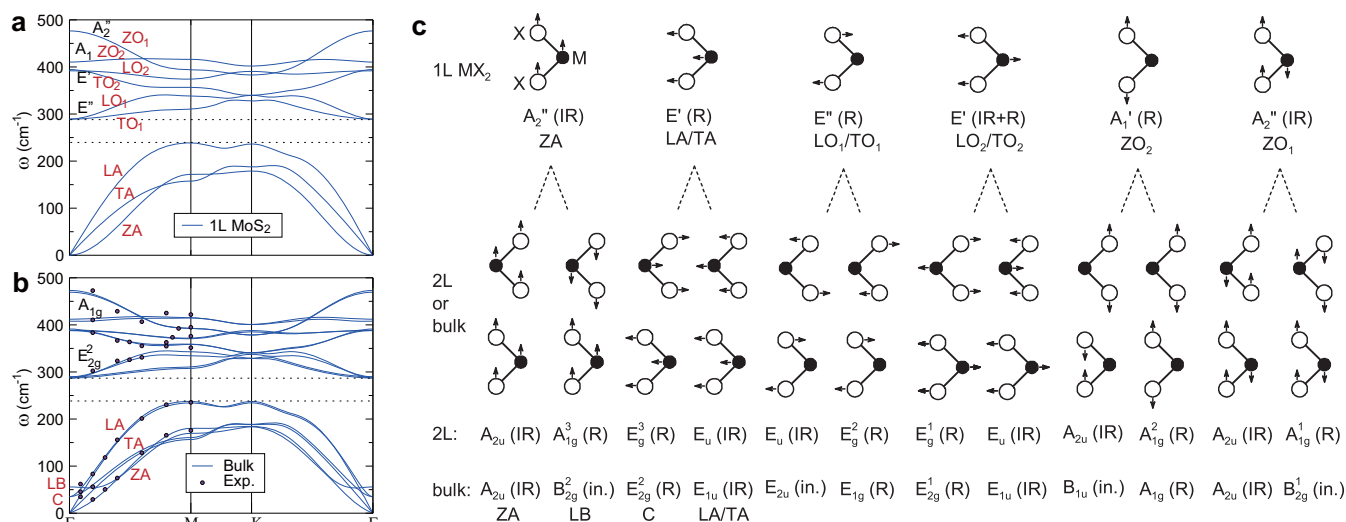
Fig. 2 Calculated phonon dispersion curves for (a) 1L and (b) bulk MX$_2$. The dots in (b) are the data from inelastic neutron scattering experiments. Panels (a) and (b) are reproduced with permission from ref. 140, copyright 2011, American Physical Society. (c) Vibration modes, symmetry representation, and optical activities (Raman: R; Infrared: IR; inactive: in.) of the lattice phonons for 1L, 2L and bulk MX$_2$. There are 6 optical and 3 acoustic branches in the 1L flake while the numbers of optical branches increase to $3\times6-3=15$ for 2L and bulk samples, due to the doubling of the numbers of atoms in unit cells. Note that the low-frequency LB and C modes are of optical characteristics although they share quite close dispersion behavior to the 3 acoustic modes at high wavenumbers. Reproduced with permission from ref. 35, copyright 2015, Royal Society of Chemistry.

Table 1 Relevant phonon symmetry representation and optical activity (Raman: R, Infrared: IR, and inactive: in.) of single-layer (point group D_{3h}), bilayer (point group D_{3d}), and bulk (point group D_{6h}) MoS$_2$. Vibration direction is along the azimuth axis of the unit cell. Phonon frequencies (ω_{MoS_2}) are calculated values. Reproduced with permission from ref. 140, copyright 2011, American Physical Society.

D_{3h}	D_{3d}/D_{6h}	Activity	Direction	Atoms	ω_{MoS_2} (cm^{-1})	
A_2'' (IR)	A_{2u}/A_{2u}	IR	z axis	Mo+S	0.0	0.0
	A_{1g}^3/B_{2g}^2	R/in.				55.7
E' (R)	E_g^3/E_{2g}^2	R	xy plane	Mo+S	-	35.2
	E_u/E_{1u}	IR				-
E'' (R)	E_u/E_{1u}	IR/in.	xy plane	S	289.2	287.1
	E_g^2/E_{1g}	R				288.7
E' (IR+R)	E_g^1/E_{2g}^1	R	xy plane	Mo+S	391.7	387.8
	E_u/E_{1u}	IR ($\boldsymbol{E}\perp z$)				391.2
A_1 (R)	A_{2u}/B_{1u}	IR/in.	z axis	S	410.3	407.8
	A_{1g}^2/A_{1g}	R				412.0
A_2'' (IR)	A_{2u}/A_{2u}	IR ($\boldsymbol{E}\|z$)	z axis	Mo+S	476.0	469.4
	A_{1g}^1/B_{2g}^1	R/in.				473.2

phase for adjacent atoms. A simple rule to discern the phonon feature, for instance in a 1D diatomic chain, is that the optical modes are produced when two adjacent atoms move against each other (out-of-phase), while the acoustic modes are produced when they move together (in-phase). Figures 2a and 2b show the calculated dispersion relations for MX$_2$ monolayer and bulk, respectively. Specifically, for monolayer MX$_2$ one unit cell comprises one X–M–X sandwich with 3 atoms and thus there are 9 phonon modes (3 acoustic and 6 optical modes). The numbers of atoms in the unit cell increases to 6 for bulk and, accordingly, the numbers of optical modes increases to 15.
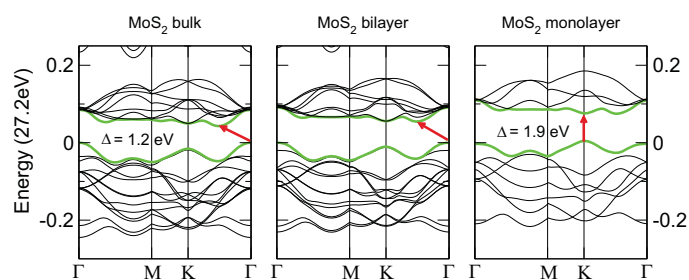
Figure 2c illustrates the schematic atomic vibration modes, optical activities (Raman, infrared, or inactive, abbreviated here as R, IR and in., respectively), and acoustic/optical features for the monolayer (1L), bilayer (2L) and bulk MoS$_2$. Lattice vibration modes are normally classified according to the irreducible representation of the crystal symmetry. For few-layer flakes, the symmetries differ if the flakes have an odd or even number of layers. The odd numbered flakes have a point group symmetry of D_{3h} owing to the presence of the horizontal reflection plane (σ_h) that passes through the transition metal atom (M). The corresponding representation is $\Gamma= 2A_2''+A_1'+2E'+E''$,[155,156] where one A_2'' and one E' are acoustic modes, another A_2'' is IR active, A_1' and E'' are R active, and another E' is both R and IR active, as shown in Fig. 2a. In contrast, due to the presence of the inversion symmetry, the symmetry of the even numbered flakes is D_{3d} with the representation: $\Gamma= 3A_{1g}+3A_{2u}+3E_g+3E_u$,[157,158] where one A_{2u} and one E_u are acoustic modes, the other A_{2u} and E_u are IR active, and A_{1g} and E_g are R active.

For bulk MX$_2$, the point group symmetry is enhanced to D_{6h} due to the gain of translational symmetry along the z axis.[157] The lattice vibrations at Γ point is: $\Gamma=A_{1g} + 2A_{2u} + 2B_{2g} + B_{1u} + E_{1g} + 2E_{1u} + 2E_{2g} + E_{2u}$,[141,156] where one A_{2u} and one E_{1u} are acoustic modes, A_{1g}, E_{1g}, and E_{2g} are R active, another A_{2u} and E_{1u} are IR active, and B_{2g}, B_{1u}, and E_{2u} are optically inactive. Here the modes denoted by the letter "E" are doubly degenerate in the xy plane. For the sake of clarity, Table 1 also lists the crystal symmetry, vibration mode, and Raman frequency for the 1L, 2L and bulk MoS$_2$.

2.3 Band structure and electrical permittivity

When compared to bulk materials, the band structures of 2D materials are considerably modified owing to the quantum confinement effect. The energy-momentum relation (of electrons) and even the positions of band edges can be altered that can lead to a fundamental change of physical properties such as carrier ef-

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Fig. 3 Band structures of bulk, bilayer, and monolayer MoS$_2$. The top of valence band and bottom of conduction band are highlighted in green. The red arrows indicate the smallest value of the bandgap (direct or indirect) for a given thickness. Adapted with permission from ref. 159, copyright 2011, American Physical Society.
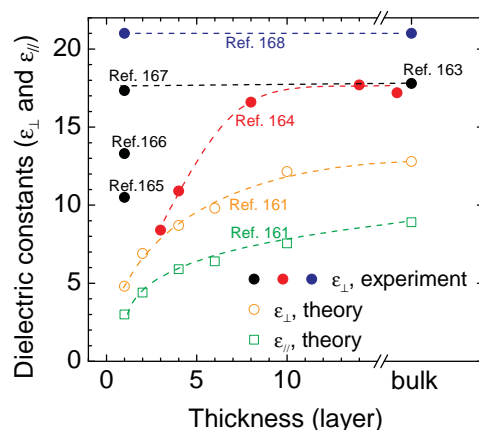
Table 2 Calculated the hole and electron effective masses (in unit of electron mass m_e) at the high symmetry points. Reproduced with permission from ref. 160. Copyright 2012, American Physical Society.

Type	Symmetry point	Bulk	2L	1L
hole	Γ	0.711	1.168	3.524
	K	0.625	0.628	0.637
electron	midpoint of Γ–K	0.551	0.579	0.569
	K	0.821	0.542	0.483

Fig. 4 Theoretical and experimental values of dielectric constants for MoS$_2$ at different thicknesses. While most theoretical calculations favor the increasing trend of dielectric constant with increasing thickness, there are controversies in experiments on the trend of dielectric constant with thickness.

fective mass and dielectric constant, which requires a special attention when comparing the performances of the same material measured at different thicknesses.

In particular, two aspects are closely related to the charge transport. First, the bandgap magnitude determines the height of the Schottky barrier at the semiconductor/electrode interface. Carrier injection into monolayer is more difficult than into bulk owing to a broader bandgap. Second, the effective mass m^* directly reflects the intrinsic mobility following the equation $\mu \propto 1/m^*$. Kuc *et al.* calculated the band structures for MoS$_2$ with different thickness values from 1L to bulk and systematically revealed the influence of thickness on the position of band edges as well as the size of bandgap.[159] Figure 3 shows the band structures of bulk, 2L and 1L MoS$_2$, with the band edges of the valence and conduction bands indicated by arrows. For 2L and bulk MoS$_2$ the conduction band minimum and the valence band maximum are located at the Γ point and a midpoint between K and Γ, respectively. Both of them shift to the K point for the 1L MoS$_2$. The energy-momentum relations at different values of the momentum are not necessarily the same and thus the shift in the conduction band minimum may change the carrier effective mass and the intrinsic mobility. Table 2 lists the thickness modulated carrier effective mass values in MoS$_2$ calculated by Yun *et al.*[160] Evidently, the electron effective mass is reduced from 0.551 to 0.483 m_e where m_e is the electron mass. The slight reduction of carrier effective mass is favorable to achieving high mobility.

Also, reducing thickness by exfoliating the top layers changes the electrostatic surroundings of the remaining low lying layers and, consequently, may alter the carrier screening and electrical permittivity (dielectric constant, ε), forming a third way to modify charge transport. Figure 4 summarizes theoretical and experimental values of dielectric constants for MoS$_2$ at different thick-

nesses. Monotonic thickness dependence of ε can be traced. Using first-principle calculations, Kumar *et al.* theoretically studied the influence of thickness on the dielectric properties (in-plane $\varepsilon_\parallel$ and out-of-plane dielectric constant, $\varepsilon_\perp$) of Mo and W based chalcogenides.[161] In their calculation, both $\varepsilon_\parallel$ and $\varepsilon_\perp$ decrease as thickness reduces. For instance, $\varepsilon_\perp$ of MoS$_2$ is reduced from 12.8 to 4.8 when thinned from bulk to monolayer. However, it should be noted that even for a specific sample large discrepancies still exist among different theoretical research groups, which results in tremendous variation in adopting the ε value when calculating the field-effect mobility. Taking the 1L MoS$_2$ as an example, Yoon *et al.* use 3.3 in their non-equilibrium Green's function calculation,[162] while Li *et al.* adopt 17.8 following the value of bulk,[131] and Ma *et al.* employ 7.6.[132] Therefore, more accurate measurements or techniques that can lead to more reliable permittivity information need to be developed.

The electrical permittivity can be determined experimentally by optical absorption and reflection techniques.[163–168] Several groups have measured the ε in thick MoS$_2$ with different thicknesses. The data from Yim *et al.*[164] seems to support the reducing trend of ε upon reducing thickness as predicted theoretically by Kumar *et al.*, but the magnitudes are generally higher. On the other hand, owing to the influence of surface adsorbate layers on the ultrathin samples (*e.g.* water and chemical residues on substrates), inconsistent experimental results were reported for the monolayer MoS$_2$, with the real part of static ε varying from 10.5 to 21.[164–168] Among them, Li *et al.* measured a $\varepsilon_\perp$ value of 17.3 in monolayer MoS$_2$,[167] being quite close to the bulk value of 17.8 reported by Hughes *et al.*[163] If these values are reliable, it would imply no variation of the dielectric permittivity with reducing the thickness. This conclusion is further supported by the optical reflectance measurements from Heinze *et al.* where they observed nearly similar $\varepsilon_\perp$ between bulk and monolayer in all the visible regime for four types of MX$_2$ (MoS$_2$, MoSe$_2$, WS$_2$, WSe$_2$).[168] As it will be discussed in section 4, ε determines the polarization function as well as the frequency and the coupling intensity of the

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surface polar phonon, which is an essential parameter for studying the carrier scattering mechanisms. Reliable information on electrical permittivity is instrumental to gain more accurate understanding on the electronic transport behavior.

3 Electronic performance at early time (with slight or without mobility engineering)

For 2D chalcogenides, their charge transport behavior is more susceptible to lattice defects and external surroundings (*e.g.* gaseous adsorbates from air and trapped charges in substrates) due to the fact that surface and bulk coincide. In experiment, a wide distribution of carrier mobility exists as a result of varied sample quality and measurement conditions. Table 3 lists typical carrier mobility values of MX_2 chalcogenides reported in recent years. In order to find out the relationship between carrier mobility and extrinsic factors (contact quality, densities of charged impurities and structural defects), the detailed device information, when available, are all reported, including preparation methods (exfoliated or synthesized), channel thickness, contact metals, thermal annealing condition (*in situ* or *ex situ*, gas environment, temperature, and duration), interface surroundings, and measurement environment.

Table 3 Carrier mobility values of 2D chalcogenides with slight or no mobility engineering, roughly listed in ascending orders of preparation method (mechanically exfoliated or synthesized) and channel thickness (numbers of layers NL or nanometers), and in a descending order of room temperature mobility.

Channel material	Channel thickness	Contact & doping	Thermal annealing	Dielectric & encapsulation	Measurement pressure	μ near RT cm^{2}V^{-1}s^{-1}	μ at LT cm^{2}V^{-1}s^{-1}	γ value near RT	Ref. no.
MoS_2	1L	Au		TG:Al$_2$O$_3$		80 (?)			93
MoS_2	1L	Ti	in. 0.7Pa 300°C 1h	TE:Si$_3$N$_4$	humidity	71.8 (?)			169
MoS_2	1L	Au		BG:SiO$_2$		64	147 (6.5 K)		170
MoS_2	1L	Au	ex. Ar/H$_2$ 200°C 2h + in. 120°C 12 h	BG:SiO$_2$	~0.13mPa	59[4W]			171 / 171
MoS_2	1L	Ti	ex. Ar/H$_2$ 350°C 3h	BG:SiO$_2$	~0.13mPa	~20[Hall]	250 (4 K)	1.7	172
MoS_2	1L	Au/IL	ex. 200°C 2h	TG:IG	vac.		230 (10 K)	1.22	173
MoS_2	1L	Mo	147°C 2h	BG:Al$_2$O$_3$		11–13			174
MoS_2	1L	Ti	ex. vac. 200°C	BG:SiO$_2$→BN		0.5→7.6–12			175
MoS_2	1L	Au	ex. N$_2$ 250°C 1h	BG:SiO$_2$		~1			176
MoS_2	1L	Au	ex. N$_2$ 250°C 1h	→BG:BN		→~10			176
MoS_2	1L	Ti		BG:SiO$_2$	vac.,	1.1–10			169
MoS_2	1L	Cr		suspended	~0.13mPa	0.9			177
MoS_2	1L	Cr		BG:SiO$_2$	~0.13mPa	0.1			177
MoS_2	1L	Cr		suspended		0.05			178
MoS_2	2L	Ti	in. 120°C 20h	BG:SiO$_2$	~0.13mPa	~80[Hall]	375 (3 K)	1.1	172
MoS_2	2L	Au	ex. 200°C 2h	TG:IG	vac.		450 (2 K)	1.9–2.9	173
MoS_2	2L	Ti	no	BG:SiO$_2$	vac.	35			179
MoS_2	2L	Au	ex. Ar/H$_2$ 200°C 2h + in. 120°C 12 h	BG:SiO$_2$	~0.13mPa	33[4W]			171 / 171
MoS_2	2L	Au	ex. N$_2$ 250°C 1h	BG:BN		~27			176
MoS_2	2L	Au		TG:Al$_2$O$_3$		27			93
MoS_2	2L	Ti	ex. vac. 200°C	BG:SiO$_2$		~7			175
MoS_2	2L	Ti	ex. vac. 200°C	→BG:BN		→24			175
MoS_2	2L	Mo	147°C 2h	BG:Al$_2$O$_3$		11–14			174
MoS_2	2L	Au	ex. N$_2$ 250°C 1h	BG:SiO$_2$		~3.5			176
MoS_2	2L	Ti	in. vac. 77°C	BG:SiO$_2$	~0.13mPa	4			180
MoS_2	2L	Ti	ex. Ar/H$_2$ 400°C	BG:SiO$_2$	air	0.12			180
MoS_2	2–3L	Au→1T	no	BG:SiO$_2$	air	19→46			137
MoS_2	2–3L	Au→1T	no	TG:HfO$_2$	air	3.5→12.5			137
MoS_2	2 nm	Sc		BG:SiO$_2$		26			181
MoS_2	3L	Au	ex. 200°C 2h	TG:IG	vac.	65–95	820 (2 K)	1.9–2.4	173
MoS_2	3L	Ti		TG:IL	~0.13mPa	63			182
MoS_2	3L	Ti	ex. vac. 200°C	BG:SiO$_2$		~9			175
MoS_2	3L	Ti	ex. vac. 200°C	→BG:BN		→45			175
MoS_2	3L	Au	ex. Ar/H$_2$ 200°C 2h + in. 120°C 12 h	BG:SiO$_2$	~0.13mPa	36[4W]			171 / 171
MoS_2	3L	Mo	147°C 2h	BG:Al$_2$O$_3$		~27			174
MoS_2	3L	Ni		TG:ZrO$_2$		25			183
MoS_2	3L	Permalloy	in. 87°C 2h	BG:SiO$_2$	vac.	~27 (200K)	~54 (2 K)	~0.6	184
MoS_2	3L	Ni		TG:IG		12			185
MoS_2	3L	Au		TG:Al$_2$O$_3$		10			93
MoS_2	3–5L	Cr		TG:Y$_2$O$_3$/HfO$_2$		47.7±11.9			186
MoS_2	3–5L	Cr		TG:Al$_2$O$_3$/HfO$_2$		37.4±11.4			186
MoS_2	3–5L	Cr		TG:MgO/HfO$_2$		15.9±7.2			186
MoS_2	4L	Mo	147°C 2h	BG:Al$_2$O$_3$		22–26			174
MoS_2	4L	Ti	ex. vac. 200°C	BG:SiO$_2$		~5			175
MoS_2	4L	Ni		BG:SiO$_2$	vac.		310 (1K)		187
MoS_2	5L	Mo	147°C 2h	BG:Al$_2$O$_3$		25–26			174

MoS_2	5L	Ti	ex. vac. 200°C	BG:SiO_2		$\sim$15			175
MoS_2	5L	Ti		BG:SiO_2	$\sim$0.13mPa	$\sim$5 (295K)	$\sim$0.3 (140 K)		182
MoS_2	5L	Ti		TG:IL	$\sim$0.13mPa	$\sim$100 (180K)	$\sim$220 (77 K)	1	182
MoS_2	6L	Au	no	BG:SiO_2	vac.	49			179
MoS_2	6L	Ti	no	BG:SiO_2	vac.	42			179
MoS_2	5 nm/7L	Ti		BG:SiO_2	$\sim$0.13mPa	$\sim$75 (295K)	$\sim$180 (140 K)		182
MoS_2	5 nm	Ni or Au	no	BG:SiO_2		28			188
MoS_2	5–6 nm	Ni		BG:SiO_2	vac.	24			187
MoS_2	8nm	Ti		BG:SiO_2	$\sim$0.13mPa	$\sim$40 (300K)	$\sim$390 (77 K)	1.7	182
MoS_2	8nm	Ti		TG:IL	$\sim$0.13mPa	$\sim$160 (100K)	$\sim$390 (77 K)	1.2	182
MoS_2	$\sim$10 nm	Sc		BG:SiO_2		184			181
MoS_2	$\sim$10 nm	Ti		BG:SiO_2		125			181
MoS_2	$\sim$10 nm	Ni		BG:SiO_2		36			181
MoS_2	$\sim$10 nm	Pt		BG:SiO_2		21			181
MoS_2	10 nm	BLG	in. 200°C 3h	TG:BN		26, 33(no Rc)			189
MoS_2	10 nm	Ti		TG:IL		44[Hall] (220 K)			190
MoS_2:p						86[Hall] (220 K)			190
MoS_2	11 nm	Ti		BG:SiO_2		8.4			191
MoS_2	11 nm	Ti		TG:Al_2O_3		9.8			191
MoS_2	1–17 nm	Cr	as-fabricated	suspended	vac.	0.01–46			192
MoS_2	1–17 nm	Cr	ex. Ar/H_2 200°C 1h	suspended	vac.	0.5–105			192
MoS_2	12 nm	Ti	ex. Ar/H_2 200°C 2h	BG:SiO_2	vac.(PPMS)	$\sim$150[4W]			193
MoS_2	12 nm	Ti	ex. Ar/H_2 200°C 2h	BG:SiO_2	vac. (PPMS)	91			193
MoS_2	13 nm	Co→1nmTiO_2		BG:SiO_2	vac.	12→76			194
MoS_2-M	1L	Ti/Au		BG:SiO_2	ambient[RT]	3–37[all]	90–110 (90 K)	1.6	78
MoS_2-M	1L	Ti/Au		BG:SiO_2	vac.[Low T]	25–35[best]			78
MoS_2-C	1L	Ag		DE:Si_3N_4	$\sim$0.13mPa	24	58 (77 K)	0.65	195
				TG:HfO_2					195
MoS_2-C	1L	Ti		BG:-SH	<1.3mPa	13			196
MoS_2-C	1L	Ti	200°C	TG:Al_2O_3		11±3			197
MoS_2-S	1L	Cr		BG:SiO_2		7 (2–12)			75
MoS_2-C	1L	Ti		TG:HfO_2		6, 30[band]	1.3, 13[band] (50 K)		198
MoS_2-C	1L	Ti	ex. Ar/H_2 350°C 2h	BG:SiO_2		3.6	$\sim$3.6 (90 K)		74
MoS_2-C	1L	Ti		BG:-NH2	<1.3mPa	3.6			196
MoS_2-C	1L	Ti		BG:SiO_2	<1.3mPa	1.9			196
MoS_2-A	1L	Ti		BG:SiO_2	$\sim$1.3mPa	1.2			52
MoS_2-C	2L	Ti	ex. Ar/H_2 350°C 2h	BG:SiO_2		8.2	$\sim$8.2 (90 K)		74
MoS_2-C	2–3L	1T MoS_2	no	BG:SiO_2	air	24→56			138
MoS_2-C	3L	Ti	ex. Ar/H_2 350°C 2h	BG:SiO_2		15.6	$\sim$15.6 (90 K)		74
MoS_2-C	5.7 nm	Ti/Ni		BG:SiO_2		9.9			199
MoS_2-C	70 nm	Ti/Ni		BG:SiO_2		42			199
$MoSe_2$-C	1L	Ti	ex. vac. 120°C 2h	BG:SiO_2		50			61
$MoSe_2$	few nm	Ni		BG:SiO_2	$\sim$13μPa	$\sim$40	180 (78 K)	2.1	200
$MoSe_2$	7 nm	Ti		BG:SiO_2		$\sim$200 (275 K)	$\sim$150 (h)		201
$MoSe_2$	:p 7 nm	Ti	+ in. 120°C 24h	BG:SiO_2		$\sim$150 (275 K)			201
$MoSe_2$	10–12 nm	Ti		BG:SiO_2	$\sim$0.13mPa	$\sim$110	500 (100 K)	1.2	202
$MoSe_2$	20 nm	Ti[BC]	ex. N_2 400°C 2h	BG:SiO_2			$\sim$20		203
$MoSe_2$	5–14 nm	Ti		BG:SiO_2	$\sim$0.13mPa	$\sim$50	600 (77 K)	1.7	202
$MoTe_2$:p	2L	Ti	ex. Ar/H_2 250°C 2h in. 120°C 24h	BG:SiO_2	vac. (PPMS)	11			204 204
$MoTe_2$:p	3L→7L	Ti	ex. Ar/H_2 250°C 2h + in. 120°C 24h	BG:SiO_2	vac. (PPMS)	20→27			204 204
$MoTe_2$:p	3L	Ti		BG:SiO_2	vac.	0.3			205
$MoTe_2$	3L	Ti		BG:SiO_2	vac.	0.03			205
$MoTe_2$	8 nm	Ti		TG:IL	vac.	30 (270K)			206
$MoTe_2$:p	8 nm	Ti		TG:IL	vac.	5 (270K)			206
$MoTe_2$:p	30L	Ti	ex. Ar/H_2 300°C 3h	BG:SiO_2	vac.	6.4			207
WS_2	1L	Au	ex. Ar/H_2 200°C 2h + in. 120°C 24h	BG:SiO_2	vac. (PPMS)	$\sim$50±7	140 (7 K)	0.73	208 208
WS_2	1L	Au	ex. Ar/H_2 200°C 2h	TG:IL	<0.13mPa	19 (240K)			209
WS_2:p	1L	Au	ex. Ar/H_2 200°C 2h	TG:IL	<0.13mPa	12 (240K)			209
WS_2	1L	Cr	in. current	BG:SiO_2	vac.	0.23			210
WS_2	2L	Au	ex. Ar/H_2 200°C 2h + in. 120°C 24h	BG:SiO_2	vac. (PPMS)	$\sim$30	>300 (5 K)	1.75	208 208
WS_2	2L	Au	ex. Ar/H_2 200°C 2h	TG:IL	<0.13mPa	44 (230K)			209
WS_2:p	2L	Au	ex. Ar/H_2 200°C 2h	TG:IL	<0.13mPa	43 (230K)			209
WS_2	4L	Cr	in. current	BG:SiO_2	vac.	17			210
WS_2	4L	Cr	in. current	BG:BN	vac.	80			210
WS_2	few nm	Ti		BG:SiO_2	vac.	16			92
WS_2	$\sim$7 nm	Au	ex. Ar/H_2 200°C 2h	BG:SiO_2		80	250 ($\sim$3.5 K)	1.15	211
WS_2:p	20–60 nm	Ti		TG:IL	<0.13mPa	60–100			212

WS$_2$	20–60 nm	Ti		TG:IL	<0.13mPa	20–60			212
WS$_2$-C	1L	Ti	ex. N$_2$ 200°C 5h	BG:SiO$_2$	vac.	15–24			72
WS$_2$-M	1L	Ti/Au		BG:SiO$_2$	ambient	~5^{median}			78
WS$_2$-M	1L	Ti/Au		BG:SiO$_2$	ambient	18^{best}			78
WS$_2$-A	1L	Ti		BG:SiO$_2$	~1.3mPa	0.01			52
WS$_2$-C	7.5 nm	Au	Ar/H$_2$ 200°C 2h	BG:SiO$_2$		234			211
WS$_2$-C	8 nm	Au	Ar/H$_2$ 200°C 2h	BG:SiO$_2$		~250	~70(3.5 K)	1.15	211
WSe$_2$:p	1L	Ni		TG:IG		90			59
WSe$_2$	1L	Ni		TG:IG		7			59
WSe$_2$:p	1L	Pd	in. vac. 80°C	TG:IL	vac.	180 (250K)	255 (4 K)		213
WSe$_2$	1L	Pd	in. vac. 80°C	TG:IL	vac.	30 (250K)	160 (4 K)		213
WSe$_2$	1L	Pd	in. vac. 80°C	TG:IL	vac.	30 (250K)	100^{Hall} (4 K)		213
WSe$_2$:p	2L	SLG		TG:BN		45			214
WSe$_2$	2L	SLG		TG:BN		34			214
WSe$_2$:p	3L	Cr/Pd/IL		DE:BN	vac.	>600^{Hall} (220K)			215
WSe$_2$	3L	Au		TG:ZrO$_2$		110			183
WSe$_2$	few nm	Au		BG:SiO$_2$	vac.	82			92
WSe$_2$	6 nm	Gr./IL		TE:BN	~0.13mPa	~200 (160 K)	~330 (77 K)		216
WSe$_2$:p	6 nm	Gr./IL		TE:BN	~0.13mPa	~200 (160 K)	~270 (77 K)		216
WSe$_2$	7 nm	Gr./IL		TE:Al$_2$O$_3$	~0.13mPa		~130 (77 K)		216
WSe$_2$:p	7 nm	Gr./IL		TE:Al$_2$O$_3$	~0.13mPa		~57 (77 K)		216
WSe$_2$	8 nm	Gr./IL		TG:IL	~0.13mPa		~250 (77 K)		216
WSe$_2$:p	8 nm	Gr./IL		TG:IL	~0.13mPa		~110 (77 K)		216
WSe$_2$:p	8 nm/12L	Ti	ex. Ar/H$_2$ 200°C 2h	BG:SiO$_2$	vac. (PPMS)	150	550 (<50 K)		217
WSe$_2$	8 nm/12L	Ti	ex. Ar/H$_2$ 200°C 2h	BG:SiO$_2$	vac. (PPMS)	300	665 (100 K)		217
SnS$_2$	1L	Ti		TG:Al$_2$O$_3$	~1.3mPa	50			218
SnS$_2$	15 nm	Cr		BG:SiO$_2$	0.13–1.3mPa	0.8	0.1 (100K)		219

Abbreviation and note.
C: Chemical Vapour Deposition (CVD), A: Atmospheric Pressure CVD (APCVD), M: Metal-Organic CVD (MOCVD), S: sputtering
p: p-type conduction, NL: number of layers (N is an integer)
ex.: *ex situ*, in.: *in situ*, vac.:vacuum, PPMS: Physical Property Measurement System, RT: room temperature, LT: low temperature
BG: bottom gated, TG: top gated, DE: double-side encapsulated, BC: bottom contacted, IL: ionic liquid, IG: ionic gel, Gr.: graphene
+ (annealing): *in situ* annealing is also used besides *ex situ* annealing.
X→Y: Experimental condition (or mobility) changes from X to Y.
?: Mobility value deserves to be checked due to top/bottom gate coupling.

In spite of the mobility variation, some tendencies can still be singled out. First, the quality of the contact plays a crucial role. High mobility is often seen in samples with appropriate annealing and/or work function matching by suitable electrodes. It is worth noting that devices operated by high-capacitive ionic liquid/gel normally exhibit higher mobility than those gated by common oxide dielectrics. This behavior can be attributed to the improved carrier injection at high carrier density. Second, thicker samples (below ~10 nm) normally show higher mobility, as a result of protection effect of the outer layers to external scattering centers. Third, the electronic characteristics are temperature dependent, indicative of the important role played by lattice phonons and/or other thermally related scattering factors.

3.1 Thickness dependence

The trace of dependence of field-effect mobility on thickness was observed already in 2005 when the MX$_2$ monolayers were first prepared by mechanical exfoliation.[220] A low mobility range from 0.5 to 3.0 cm^{2}V^{-1}s^{-1} was reported for MoS$_2$ and NbSe$_2$, showing about two orders of magnitude lower than the corresponding bulk materials. By collecting more data on a broad thickness range, a deeper understanding of the charge transport mechanism was put forward. Figure 5 shows a schematic measurement configuration in a bottom-contact FET and the values of carrier mobility at different semiconductor thicknesses.[131,175] In scandium

(Sc) contacted MoS$_2$ samples, Appenzeller *et al.* first reported a parabolic-like mobility dependence on thickness, with the highest mobility of 180 cm^{2}V^{-1}s^{-1} obtained at around 10 nm.[181] Later, Li *et al.* focused the attention to the few-layer regime (Figs. 5a–5b) and reported mobility varying from 10 to 50 cm^{2}V^{-1}s^{-1} in Au or Ti contacted samples while the thickness changed from 1 to 5 layers (Fig. 5d).[131] Similar monotonic decrease of mobility with reducing thickness was also confirmed by Hone *et al.* on samples supported by SiO$_2$ and hexagonal boron nitride (hBN) dielectrics (Fig.5e).[175] The origin of the thickness dependence is rather complex. As will be discussed in section 4.2.1, one of the main reasons is the interfacial Coulomb impurity,[131] which is also an extrinsic scattering factor to be suppressed for achieving high channel mobility.
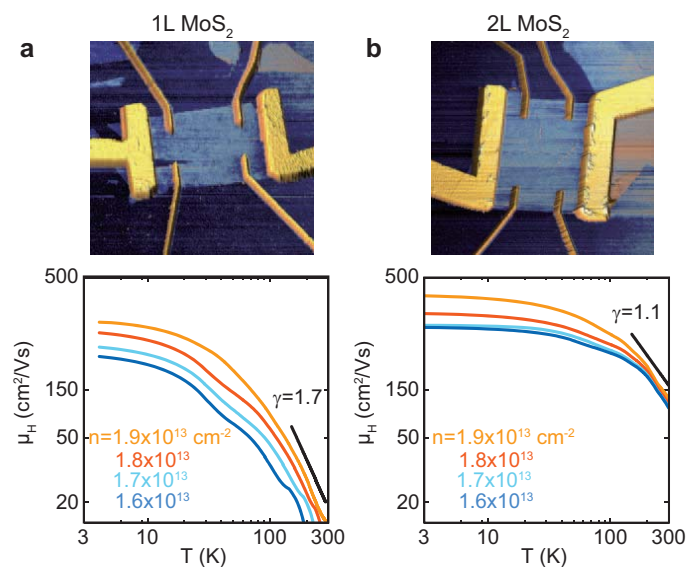
3.2 Temperature dependence

Alongside the thickness dependence, temperature (T) is a powerful parameter whose tuning allows for exploring the intrinsic carrier scattering mechanisms due to lattice phonons, because the phonon number depends highly on temperature. In contrast, other scattering mechanisms such as Coulomb impurity and atomic vacancy possess a moderate or weak dependence on temperature where temperature mainly embodies its effect through tuning the carrier screening ability and the carrier distribution near the Fermi level.

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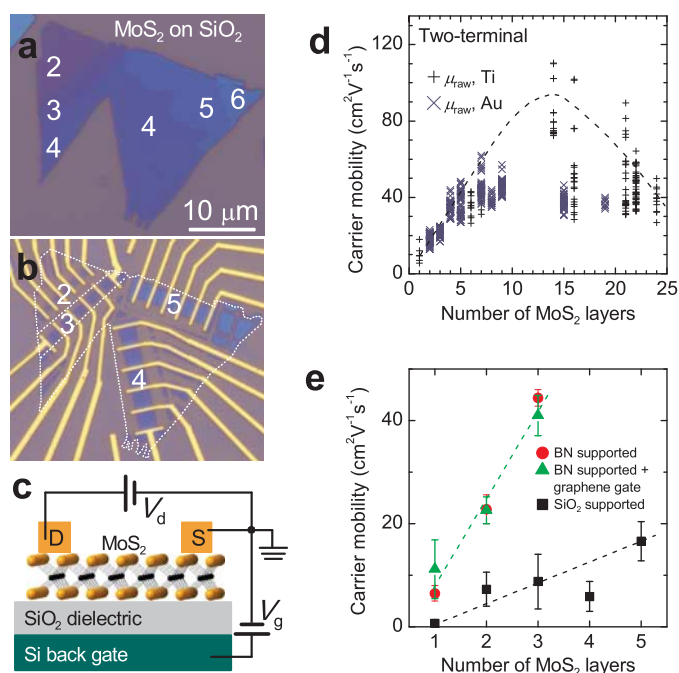
Fig. 5 (a) and (b) Optical images for as-transferred MoS$_2$ flakes with consecutive numbers of layers from 2 to 6 and corresponding FETs with bottom SiO$_2$ as gate dielectric. (c) Schematic diagram for the back-gated MoS$_2$ FETs. (d) and (e) Dependence of carrier mobility on thickness in MoS$_2$ FETs. Panels (a)–(d) are reproduced with permission from ref. 131, copyright 2013, American Chemical Society. Panel (e) is reproduced with permission from ref. 175, copyright 2013, American Chemical Society.


Fig. 6 Dependence of Hall mobility (μ_H) on temperature for (a) monolayer and (b) bilayer MoS$_2$ FETs after long-time thermal annealing at different carrier densities. Top panels are the color-enhanced AFM height images for the corresponding devices. Bottom panels are the mobility data and the power-law temperature fitting near room temperature. Reproduced with permission from ref. 172, copyright 2013, American Chemical Society.

Several theoretical studies have been carried out to investigate the intrinsically phonon-dominated mobility dependence on temperature, which predict a power-law relation between mobility and temperature $\mu \propto T^\gamma$ with γ being a parameter dependent on the phonon type. In high-quality bulk, Fivaz and Mooser predicted γ values of ~ 2.6, ~ 1.6, and 1 for homopolar optical, polar optical and acoustic phonons, respectively.[127] They determined that the homopolar optical phonons are the primary scattering centers in most MX$_2$ chalcogenide crystals. For MoS$_2$ monolayer, in contrast, Kaasbjerg et al. showed that the scattering around room temperature is co-dominated by the deformation potential of optical phonons (see LO$_2$/TO$_2$ and LO$_1$/TO$_1$ modes in Fig. 2a) and the Fröhlich interaction (polar optical phonons, see LO$_2$/TO$_2$ modes in Fig. 2a), which gives rise to $\gamma \sim 1.69$.[128] The acoustic phonons ($\gamma = 1$) become leading at temperatures lower than 100 K.

Experimentally, however, there have been no reports showing 2D vdW samples that can reach the intrinsic phonon-limited transport regime and exhibit the predicted γ values. As can been seen in Table 3, the measured γ values range broadly from 0.56 to 2.85 near room temperature, implying the existence of other scattering mechanisms that deviate the anticipated γ values from pure phonon scattering. In high-quality 1L MoS$_2$ samples with mobility of 60–70 cm^{2}V^{-1}s^{-1}, Hersam et al. extracted a low γ value ~ 0.62,[221] being much smaller than 1.69. They attributed the

deviation to the presence of remote phonons from underlying oxide substrates and the effect of contact resistance. A close result ($\gamma = 0.72$) was observed by Wang et al. in their high-quality vacancy healed 1L MoS$_2$ samples.[222] In another study on super-clean hBN encapsulated MoS$_2$, Hone et al. reported high γ values of 1.9 for 1L and 2.5 for 2L samples.[223] All the experimental data indicate that at room temperature the charge transport in 2D vdW semiconductors is not dominated by lattice phonons.

This conclusion is further corroborated by the absolute magnitude of mobility. The theoretically predicted room-temperature mobility limited by phonons amounts to 410 cm^{2}V^{-1}s^{-1} for 1L MoS$_2$. Figure 6 shows the Hall mobility versus temperature for 1L ($\gamma = 1.7$) and 2L ($\gamma = 1.1$) MoS$_2$ measured by Jarillo-Herrero et al. Although they observed $\gamma = 1.7$ in long-time in situ annealed 1L MoS$_2$,[172] appearing to match the theoretical prediction, the absolute value of mobility is only 20 cm^{2}V^{-1}s^{-1}, i.e. it is much lower than the predicted value. Hitherto, this high theoretical value has never been reached experimentally (See Table 3), indicating that there is still large room for mobility improvement if the extrinsic scattering centers can be effectively suppressed or minimized.

3.3 Dependence of electronic phase on carrier density

The layered MX$_2$ chalcogenides exhibits a rich phase diagram depending on carrier density (n_{2D}) as a result of complicated electron-electron interaction. Figure 7 shows the results on carrier density by Iwasa et al. who first investigated the electronic behavior of 20 nm thick MoS$_2$ over a wide range of n_{2D} through ionic liquid gating. With this, an extremely high n_{2D} value up to 10^{14} cm^{-2} is reached such that the superconducting phase can be accessed. As shown in the phase diagram
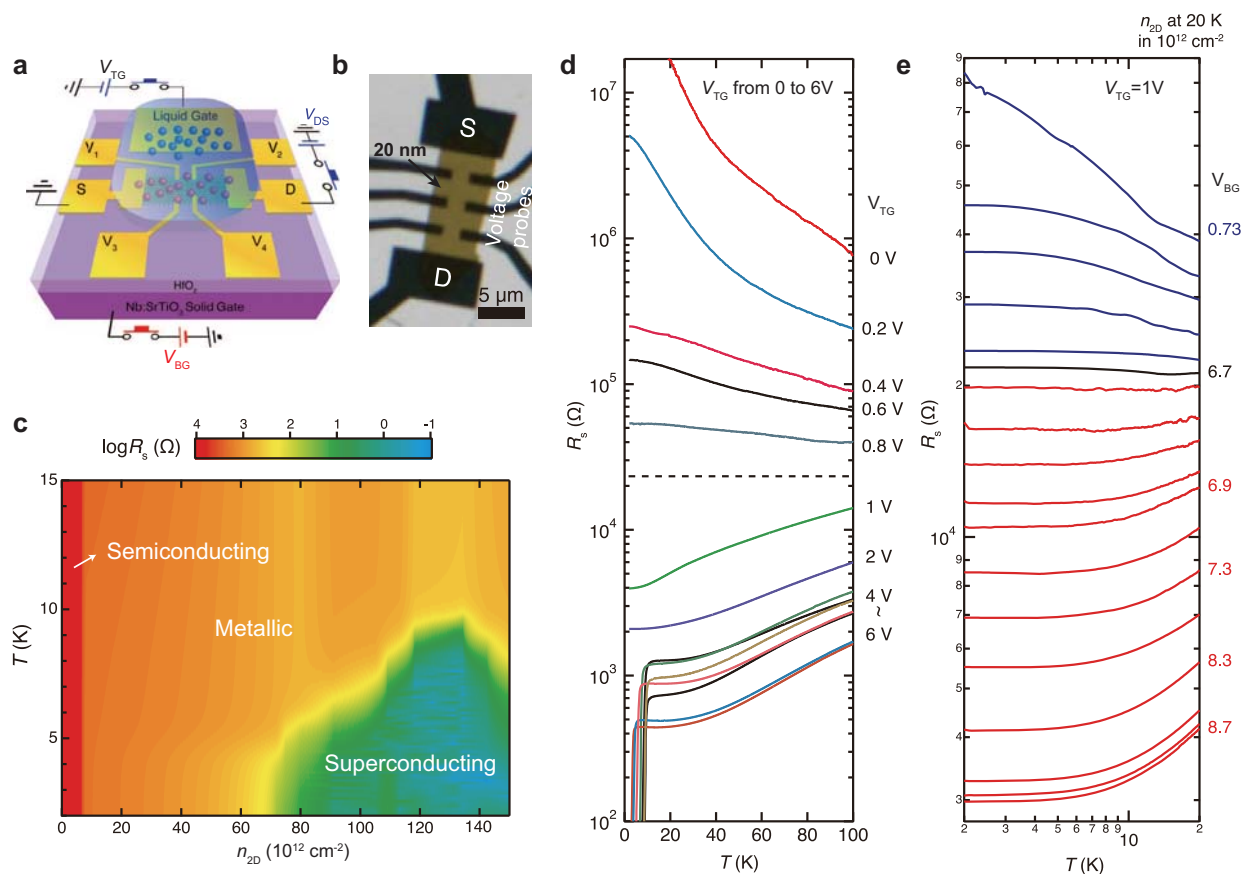
Fig. 7 (a) Schematic and (b) optical images for an ionic liquid gated (TG) MoS_2 FET. (c) Phase diagram showing the evolution of electronic phases as a function of carrier density n_{2D}. (d) Temperature dependence of the channel sheet resistance R_s at different V_{TG} gate biases ranging from 0 to 6 V (indicated on the right). (e) Temperature dependence of R_s at $V_{TG} = 1$ V and different V_{BG} showing a metal-insulator transition at $n_{2D} = 6.7 \times 10^{12}$ cm^{-2}. For each V_{BG}, the corresponding n_{2D} is determined by Hall measurement at 20 K. Reproduced with permission from ref. 224, copyright 2012, American Association for the Advancement of Science.

(Fig. 7b), the thick MoS_2 flake exhibits a semiconducting (insulating) phase as $n_{2D} < 6.7 \times 10^{12}$ cm^{-2}, a metallic phase from 6.7×10^{12} to 6.8×10^{13} cm^{-2}, and a domelike superconducting phase as $n_{2D} > 6.8 \times 10^{13}$ cm^{-2}. The critical density for the insulator-metal transition $n_{2D} = 6.7 \times 10^{12}$ cm^{-2} corresponds to a sheet resistance $R_s = 21.7$ kΩ per square (Fig. 7d), which is close to the quantum resistance h/e^2 and is consistent with metal-insulator transition found in other 2D systems.

The metal-insulator transition was soon confirmed in the monolayer MoS_2 samples.[82,172,173,222,225] However, the superconducting phase is absent,[173,225] indicating the detrimental role played by the interfacial impurities that are strong enough to destroy the electrostatic surrounding required to form the superconducting cooper pairs.

The semiconducting regime with medium n_{2D} is critical for FET applications. In this regime, the variation of carrier density has two opposite effects to the channel mobility. On the one hand, high n_{2D} is beneficial for screening the interfacial impurity potential that increases mobility. On the other hand, high n_{2D} also increases the carrier energy such that they are interacted with high-energy scattering centers, which may reduce mobility.[131] Hence, there is normally an optimized carrier density for achieving the

best carrier mobility.

In very low n_{2D} regime, some groups reported a hopping-like transport behavior,[221,226,227] which was interpreted that most carriers are filled into the band tails where carriers are highly localized. Another possible explanation to this behavior is the presence of large contribution of the contact resistance, which becomes increasingly important at low temperature and produces the artificial behavior of $\ln\sigma \sim T^{-1/3}$ since most reports of hopping transport behavior are observed in two-terminal devices.[221,222,226] No trace of hopping behavior was seen in the devices with a four-terminal measurement where the contact contribution is eliminated.[82] Instead, only thermal activation behavior was observed in this regime.

4 Factors related to electronic transport

The carrier mobility of bulk MX_2 chalcogenides can reach ~ 200 cm^{2}V^{-1}s^{-1} at room temperature.[127] Last section showed that most 2D MX_2 chalcogenides exhibit reduced mobility in comparison with their bulk phase. To develop technologically viable 2D semiconductors, especially for the atomically-thin-body FETs, it is highly desired to unravel the origin of such adverse thickness dependence.

It is well known that silicon shows thickness dependence below ~4 nm with a power-law thickness scaling behavior ($\mu \sim t^{-6}$),[107,109] as a result of the inevitable compositional transition from SiO_2 dielectric to Si channel, *i.e.* the issue of surface roughness (SR). However, this factor can be confidently ruled out in case of 2D vdW semiconductors because of the atomically well-defined interlayer interfaces. Studies indicate that there are two aspects responsible for the thickness dependence in the 2D vdW semiconductor:[228] 1) carrier injection at the electrode/channel contacts, and 2) carrier scattering mechanism within the conduction channels.

4.1 Electrode/semiconductor contacts
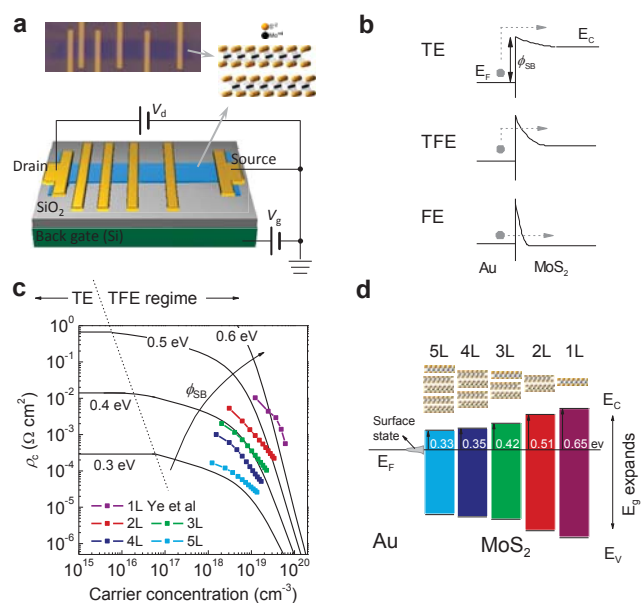
Fig. 8 (a) Schematic diagram and real optical image for the geometry of transfer line measurement. The inset shows the atomic structure of MoS_2.(b) Schematic band alignments between Au electrode and channel MoS_2 and the evolution of the three carrier injection mechanisms from low to extremely high carrier densities: thermal emission (TE), thermal field emission (TFE), and field emission (FE). The difference among the three injection mechanisms lies in the width of interfacial barrier which changes with the carrier density in channels. (c) Comparison of the room temperature contact resistivity (solid dots) with theoretical calculation of TE and TFE conduction mechanisms to extract injection barrier height (ϕ_{SB}). (d) Evolution of energy level alignment at the Au/MoS_2 interfaces as MoS_2 thickness reduces from 5 to 1 layer. Adapted with permission from ref. 229, copyright 2014, American Chemical Society.

Contact issue is ubiquitous at all metal/semiconductor interfaces due to the formation of interfacial Schottky barriers which blocks efficient carrier transfer. Figure 8 shows related studies on the contact resistance for MoS_2. Strictly speaking, the contact does not affect the intrinsic carrier mobility in semiconductors; this unfavorable effect can be ruled out by employing a transfer-line method or four-terminal measurement (Fig. 8a). However, the practical FETs collect current with two electrodes (source and drain). In most cases, the field-effect mobility μ_{FE}, defined as

the derivative of drain current to gate bias, is used to evaluate the channel performance. Normally the contact resistance does not depend on gate bias as strongly as channel resistance, the presence of contact resistance thus leads to underestimation of semiconductor performance when adopting μ_{FE} as the criterion.

4.1.1 Schottky barrier and Fermi pinning

A Schottky barrier (ϕ_{SB}) often forms at the metal/semiconductor interfaces due to the difference of chemical potentials and mismatch of energy levels of the two contacting components. This understanding leads to an empirical rule by reducing the barrier through matching the energy levels of contacting materials. In solid-state physics, low work function metals are expected to inject effectively electrons into n-type semiconductors while metals which possess a high work function are normally employed for p-type semiconductors. Note that the barrier heights for electron and hole injection are normally different, depending on the exact alignment of the energy levels. The carrier conduction type (electron: n-type or hole: p-type) in semiconductor and the practical magnitude of interfacial barrier are determined by the smaller barrier.

However, the actual injection barrier height is also governed by the effect of Fermi level pinning due to the presence of interface states of semiconductors. The pinning effect is more pronounced when the channels becomes atomically thick because the density of interface states enhances considerably. The barrier height ϕ_{SB} is proportional to the potential difference of the energy levels Δu, expressed as $\phi_{SB} = \beta \Delta u$ with β a coefficient between 0 and 1, representing the strong and weak pinning limits, respectively.[230]

It is widely accepted that the electrode/semiconductor contacts play a crucial role in the overall device performance. In early time, the variation of barrier width upon applying gate bias has ever been suggested as the current switching mechanism in FETs with nanostructured channels (*e.g.* carbon nanotube FETs).[231] Transistors operated under this switching mechanism are termed as 'Schottky barrier transistors'. At low carrier density the injection is dominated by a thermal emission process, while the injection becomes thermal-field emission (thermally assisted tunneling) or even field-emission (direct tunneling) at high carrier density, as shown in Fig. 8b.

Such a switching mechanism has also been proposed on monolayer MoS_2 FETs where a faster variation is observed in contact resistance than channel resistance in the sub-linear conduction regime.[232] It is found later, however, that the influence of contact resistance also depends highly on channel thickness and channel length. The contact may not dominate in FETs with a long channel length. In another report on mechanically exfoliated bilayer and hexalayer MoS_2 samples, Chen *et al.* reported that the contact resistance comprises only 5–20% of the total channel resistance,[179] indicating that the heights of contact barriers are smaller in thick flakes.

Furthermore, for the few-layer thick 2D semiconductors, the contact barrier height can be modified by the quantum confinement effect through the change of semiconductor bandgap.[233] To address this issue, Li *et al.* performed a systematic thickness scaling study on the Au/2D MoS_2 contacts using the transfer line

method to extract the area normalized contact resistivity (ρ_c) for each MoS$_2$ layer.[229] For MoS$_2$ thinner than 5 layers, the contact resistivity sharply increases with reducing MoS$_2$ thickness, as a consequence of bandgap expansion (Fig. 8c). Figure 8d plots a full evolution diagram of energy level alignment to elucidate the thickness scaling effect. The interfacial potential barrier is varied from 0.3 to 0.6 eV with merely reducing MoS$_2$ thickness. The thickness-dependent barrier height for charge injection is one of the reasons responsible for the field-effect mobility degradation in the ultrathin flakes. Hence, optimizing the contact quality is crucial for improving the mobility of the two-terminal FETs with 2D semiconductor channels.

4.1.2 Current crowding effect
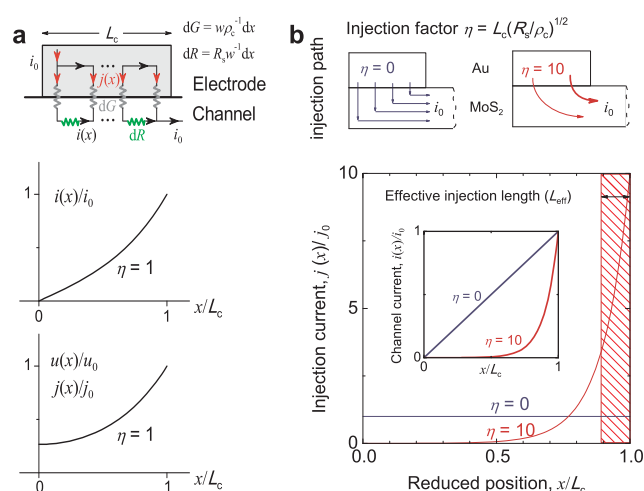
Fig. 9 (a) Resistor network model for analysing the distributions of injection current along a probe/channel stack. Top: Current injection path and distribution of impedance elements at the probe/channel interface (modeled as dG) and in the channel (modeled as dR). Bottom: Plots for lateral channel current $i(x)$, vertical interfacial potential $u(x)$ and injection current density $j(x)$ at $\eta = 1$. (b) Comparison for two extreme cases of $\eta = 0$ and 10. Reproduced with permission from ref. 229, copyright 2014, American Chemical Society.

At electrode/semiconductor contacts, current is not injected uniformly along the entire contact length (L_c) but rather concentrates at the two near-end edges of the two injection contacts, which is called 'current crowding effect'. It is important to understand this effect if one needs to compromise the contact length and area occupancy of electrodes in a limited chip area during device design. We discuss it here as basic knowledge aiming to emphasize some experimental standards for four-terminal measurements, as will be seen in section 6.2.

For 2D channels, the vertical current injection path at the electrode/channel interface and the lateral current distribution in the channels can be analytically solved via a resistor network model,[234] in which the electrode/channel stack is divided into infinite resistor and conductor elements. Figure 9a shows the schematic distribution of the impedance elements at the contact interface d$G = \rho_c^{-1}w$dx and in the channel d$R = R_s w^{-1}$dx, where R_s, ρ_c, w, and x denote the channel square resistivity, area contact

resistivity, channel width, and channel coordinate, respectively. It has been derived that the lateral channel current $i(x)$, vertical interface potential $u(x)$, and vertical injection density $j(x)$ satisfy the relations below[234]

$$i(x) = i_0 \frac{\sinh(\eta x/L_c)}{\sinh(\eta)} \quad (1)$$

$$u(x) = i_0 \frac{\sqrt{R_s\rho_c}}{w} \frac{\cosh(\eta/L_c)}{\sinh(\eta)} \quad (2)$$

$$j(x) = u(x)/\rho_c \quad (3)$$

where $\eta = L_c/L_T$ is the injection factor, and $L_T = \sqrt{\rho_c/R_s}$ is the transfer length, which is a characteristic length for current injection phenomena. In particular, R_c, R_s, and ρ_c are linked by
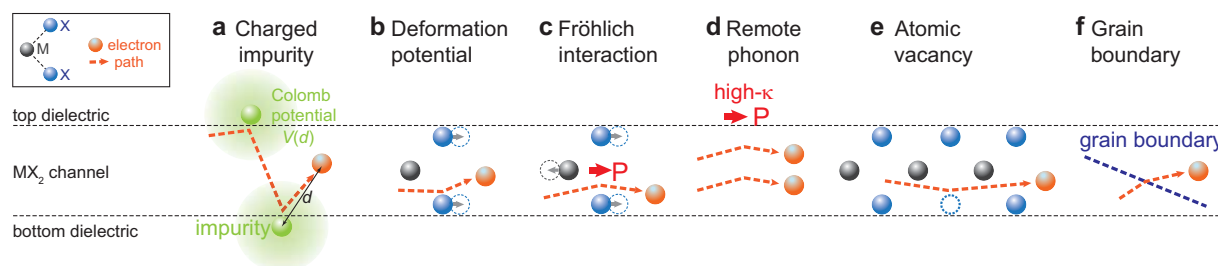
$$R_c w = \sqrt{R_s\rho_c} \coth\eta. \quad (4)$$

According to Eqs. (1)–(3), the carrier injection at contact is governed by the η factor which is a function of L_c, ρ_c, and R_s. Figure 9a depicts an illustrative distribution of $i(x)$, $u(x)$, and $j(x)$ at $\eta = 1$. Apparently, the injection is rather asymmetric along the x axis. To deepen our understanding, Fig. 9b plots two extreme cases for $\eta = 0$ and 10. As $\eta = 0$ (e.g. in presence of a superconducting channel with $R_s = 0$ or a bad contact with $\rho_c \to \infty$), the current is uniformly injected along the entire channel. At $\eta = 10$ (e.g. in case of a wide electrode with large L_c or small ρ_c), the crowding behavior is aggravated and half of the current is injected from ~10% portion from the side. For typical MoS$_2$ devices η is in the range of 2–5 depending on gate bias.

In device physics, one can use the transfer length $L_T = \sqrt{\rho_c/R_s}$ to estimate the minimum electrode length (few times of L_T) that enables efficient current injection. For Ti contacted 1L MoS$_2$, Ye et al. estimated L_T is 1.26 μm at 0 V gate bias and drops to 0.63 μm at high gate biases.[232] They suggested that the contact length should be at least 1 μm (1.5 L_T) to guarantee good contact at device on state. In contrast to the shrinking tendency with increasing gate bias, Chen et al. observed an L_T behavior increasing with elevating gate bias in their few-layer samples.[179] It increases from 20 to 80 nm for Ti/2L MoS$_2$ contact, from 50 to 180 nm for Ti/6L MoS$_2$, and from 30 to 200 nm for Au/6L MoS$_2$. Independently, Li et al. extracted L_T from 200–400 nm for thermally annealed Au contacted few-layer MoS$_2$ (2–9 L).[229] It seems that the contact length depends highly on the semiconductor thickness and whether the samples are undergone annealing treatment. For most appropriate annealed devices, contact length would not be a limit to MoS$_2$ performance since most devices employ electrode longer than 500 nm (limited by lithographic resolution).

4.2 Carrier scattering mechanisms

In this subsection, we give a fundamental introduction to the main scattering mechanisms in semiconductors, including Coulomb impurities, lattice phonons and remote interfacial phonons. Figure 10 schematically depicts the carrier scattering processes where the orange balls and dashed arrows represent the carriers and their transport paths, respectively. The change in the direction of carrier path results in a scattering event. The common

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Fig. 10 Schematic diagrams of leading carrier scattering mechanisms in 2D MX_2 channels. The black and blue balls denote the M and X atoms, respectively. The orange balls and corresponding arrows denote the electrons and their paths in the channels. (a) Charged interfacial impurities at both the top and bottom channel surfaces. The green balls and the outer surroundings denote the impurities and corresponding scattering potential $V(d)$. (b) Deformation potential of phonons due to atom vibration. (c) Fröhlich interaction due to polar optical phonons. The red arrow denotes the oscillating polar electric field induced by the polar optical phonon. (d) Remote interface phonon from dielectric. The red arrow denotes the polar phonon in the top dielectric. (e) Atomic vacancies (dashed circle) which tend to form in both natural and synthetic chalcogenides. (f) Grain boundaries (dashed line) which are typically present in synthetic chalcogenides.

method to calculate the scattering rates for each mechanism is to solve the Boltzmann transport equation within the relaxation-time approximation. To this end, one has to derive the scattering matrix elements M_{2D}, electron polarization function for the 2D channels ε_{2D}, and configurative form factor $\Phi(q,t)$ according to the device configuration. Here, we will summarize the main theoretical results and show the derived calculating formulae without dealing with the derivation. For the detailed theoretical analyses, we recommend the readers refer to related literature.[235–238]

4.2.1 Interfacial impurities
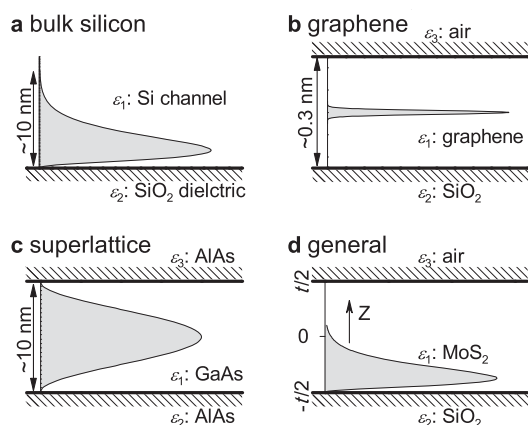
Fig. 11 Schematic diagrams of dielectric environments and carrier distributions for different FET configurations. (a) Bulk silicon: one boundary which produces only one image charge.[238] (b) Graphene: negligible thickness in the middle channel ($t \sim 0.3$ nm) that enables the approximation of a simple pulse-like carrier distribution.[239,240] (c) Superlattice: symmetric dielectrics and trigonometric carrier wavefunction.[109,241] (d) A general FET with complicated device configuration: 1) two channel boundaries which can produce infinite image charges when considering charge-charge interaction; 2) a lopsided carrier distribution which leads to complicated configurative form factors $\Phi(q,t)$ in scattering matrix elements M_{2D} and electron polarization function ε_{2D}. Reproduced with permission from ref. 131, copyright 2013, American Chemical Society..

In 2D systems, carriers are within a confined space and the Coulomb/charged impurities (CIs) are randomly distributed at
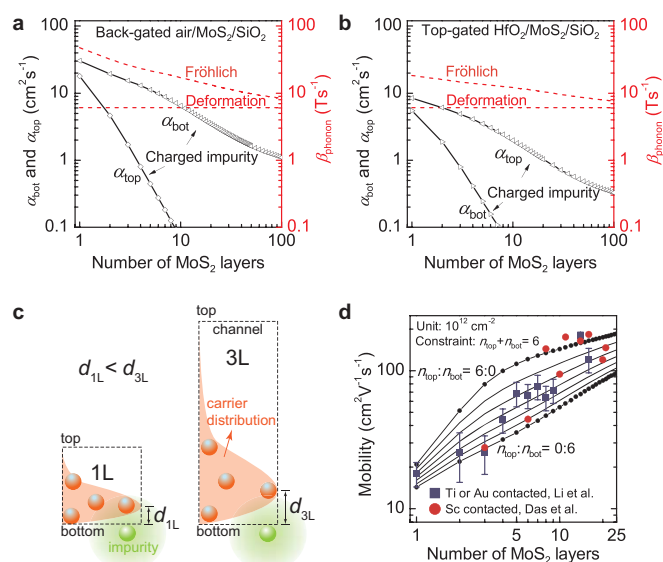
Fig. 12 (a) and (b) Calculated Coulomb impurity scattering coefficients at the top and bottom channel surfaces (α_{top} and α_{bot}) for different channel thickness. For comparison, the scattering rates of phonon deformation and Fröhlich interaction (β_{phonon}) are also plotted on the right longitudinal axis in red. (a) is for back-gated air/MoS_2/SiO_2 and (b) for top-gated HfO_2/MoS_2/SiO_2 FETs. (c) Schematic diagram for the origin of dependence of impurity scattering intensity on channel thickness. The underlying nature is the variation of interaction distance (d_{NL}) between the impurities and the channel carriers as channel thickness changes. For instance, for the 1L and 3L MoS_2 samples $d_{3L} > d_{1L}$ and hence the scattering rate is lower in the 3L sample (*i.e.*, carrier mobility is higher). (d) Comparison between the experiment and calculation based on impurity and phonon scattering. Reproduced with permission from ref. 131, copyright 2013, American Chemical Society.

the channel/dielectric interface. Each point impurity imposes its scattering potential $V(d)$ to channel carriers via the long-range Coulomb interaction. Figure 10a schematically shows two point impurity located at the top and bottom channel surfaces and the evanescent scattering potential around them. The interaction distance between a point impurity and a conduction electron is d. With the advent of silicon FETs,[238] superlattice,[109,241] and graphene,[239,240] it is proved that the randomly

distributed Coulomb impurities are one type of leading scattering mechanisms. In comparison with silicon FETs, where impurities come mainly from the residual metals ions and unsaturated silicon bonds at the channel/dielectric interfaces, the sources of the Coulomb impurities in 2D semiconductors are much richer. Additional impurities such as gaseous adsorbates and chemical residues can also be introduced during device fabrication. The 'dirty' surface condition is one of the main reasons for the low mobility in 2D vdW crystals.

While the theoretical calculations on various symmetric systems (*i.e.* superlattices, graphene, and silicon FETs) have been performed, the calculation on a generalized asymmetric system remains invalid. As mentioned, the challenging parts are the derivations of scattering matrix element M_{2D}, configurative form factor $\Phi(q,t)$, and carrier polarization function ε_{2D} according to the exact device configurative parameters (*i.e.*, carrier distribution, symmetry of dielectric surroundings, and channel thickness). In most symmetric systems, the three terms can be analytically expressed,[109,238–241] while they are only numerically solvable for complex systems.[130]

Figure 11 depicts the difference for four device configurations. Here we use ε_i (i= 1, 2, 3) to denote the dielectric constants for different layers of channel and dielectrics. For superlattice with a periodic structure of two semiconductor layers (Fig. 11c), one often adopts a symmetric carrier distribution (trigonometric) and a dielectric environment ($\varepsilon_2 = \varepsilon_3$). For graphene (Fig. 11b), the thickness of channel (0.35 nm) is negligible which enables the use of a pulse-like (δ function) to represent the carrier distribution. In general, the high symmetries exhibited enable analytic expression for the three factors of M_{2D}, ε_{2D}, and $\Phi(q,t)$. The situation is difficult in case of silicon FETs (Fig. 11a) because it involves many configurative asymmetries. Upon adopting an empirical form of carrier distribution, analytic forms for the three items can still be reached.[238] Nevertheless, none of the three device configurations is suitable for the generalized MoS$_2$ FET since it possesses a finite channel thickness (non-negligible thickness), asymmetric dielectric environments (*i.e.*, $\varepsilon_2 \neq \varepsilon_3$), and lopsided carrier distribution (close to the gated dielectric). Compared to silicon, the MoS$_2$ FET has one more top dielectric needed to be considered.

Jena *et al.* are the first to calculate the scattering of charged impurities in 2D MoS$_2$ FETs.[130] They achieved the carrier distribution in multilayer MoS$_2$ by numerically solving the Schrödinger-Poisson equation. Such a treatment, albeit accurate, requires a case-by-case calculation for each channel thickness or gate bias because any variation of them would change the carrier distribution. Later on, they did an analogue simplification to graphene for calculating monolayer MoS$_2$ with adopting zero channel thickness and symmetric carrier distribution.[132]

To combine accuracy and convenience, Li *et al.* employed a phenomenological method by adopting the carrier distribution from silicon FET.[131] In their calculation they strictly considered the configurative parameters of devices, including non-zero channel thickness, asymmetric surroundings, positions of interfacial impurities. This method allowed them, for the first time, to shed light onto the dependence of mobility over the full range thickness. In their calculation, the impurity scattering rate can be expressed as

a linear combination of the contributions from the top and bottom channel surfaces as

$$\tau_{CI}^{-1} = \alpha_{bot}(t)n_{bot} + \alpha_{top}(t)n_{top} \tag{5}$$

where the subscript bot/top denotes the bottom/top interface, t, and n are the channel thickness and density of impurity, and α is the scattering coefficient calculated. They compared the scattering rates for impurities located at bottom and top surfaces, as well as the dependence of the scattering rates for different scattering centers (including lattice phonons) on channel thickness. The scattering coefficients α_{bot} and α_{top} versus channel thickness for back-SiO$_2$-gated and top-HfO$_2$-gated FET configurations are given in Figs. 12a and 12b, respectively.

Two major pieces of information can be understood. First, the impurity scattering from the interface of gated dielectric is stronger than the ungated interface as a result of distribution unbalance of carriers upon applying gate bias. For the monolayer MoS$_2$, the scattering from charged impurity would outperform that from phonons if the gated interface had impurity density higher than $\sim 2 \times 10^{12}$ cm^{-1}. Second, the impurity scattering is considerably enhanced in extremely thinned channels, resulting from the reduction of interaction distance (d_{NL}) between impurities and carriers. As an example, Fig. 12c shows the carrier distribution and the interaction distance d_{1L} and d_{3L} for the back-gated 1L and 3L FET channels, respectively. The carriers in the thinner 1L channel are located closer to the gated bottom dielectric due to electrostatic equilibrium, resulting in a smaller d_{1L} than d_{3L}. Since scattering potential $V(d) \propto d^{-1}$, the scattering intensity on the thin channels is stronger than on the thick ones. Therefore, the variation of interaction distance with channel thickness is the direct origin for the dependence of carrier mobility on thickness.[131] Figure 12d compares the experiment and calculation of the mobility values at different thicknesses. Reasonable agreement is reached in terms of the thickness dependence.

Based on the above results, a general conclusion can be drawn that it is crucial to achieve clean channel interfaces in order to realize high mobility in the extremely thinned 2D semiconductors. Specific strategies will be discussed in section 5.2.

4.2.2 Deformation potential

In semiconductors the lattice potential determines the band structure. The atomic displacement (a) due to lattice phonon forms a perturbation to band edges. Lattice phonons can scatter off the electron waves through the potential deformation, as shown in Fig. 10b. For acoustic phonons, adjacent atoms move in the same direction and the modification of interatomic distance $\delta A \propto \delta a$, with A the interatomic distance in equilibrium. Hence the shift of band edges can be written as $\delta E = \Xi \cdot \delta a/A$ in a linear approximation, where Ξ is the deformation potential of acoustic phonons. For optical phonons, adjacent atoms move in the opposite direction and $\delta A \propto a$. Thus energy shift can be expanded as $\delta E = D_0 a + D_1 \cdot \delta a/A$ with D_i the i-th order deformation potential.

Phonon scattering depends highly on temperature because the number of phonons follows the Bose-Einstein distribution $N_q =$

Table 4 Physical parameters of lattice phonons for monolayer MoS_2. The Γ/K subscript on the optical deformation potentials indicate couplings to the intra/intervalley phonons. Reproduced with permission from ref. 128, copyright 2012, American Physical Society.

Parameter	Symbol	Value
Lattice constant	a	3.14 Å
Ion mass density	ρ	3.1×10^{-7} g/cm^2
Effective electron mass	m^*	0.48 m_e
Valley degeneracy	g_v	2
Effective layer thickness	σ	5.41 Å
Piezoelectric constant	e_{11}	3.0×10^{-11} C/m
Transverse sound velocity	c_{TA}	4.2×10^3 m/s
Longitudinal sound velocity	c_{LA}	6.7×10^3 m/s
Acoustic deformation potentials		
TA	Ξ_{TA}	1.5 eV
LA	Ξ_{LA}	2.4 eV
Optical deformation potentials		
TA	$D^1_{K,TA}$	5.9 eV
LA	$D^1_{K,LA}$	3.9 eV
TO	$D^1_{\Gamma,TO}$	4.0 eV
TO	$D^1_{K,TO}$	1.9 eV
LO	$D^0_{K,LO}$	2.6×10^8 eV/cm
Homopolar	$D^0_{\Gamma,HP}$	4.1×10^8 eV/cm
Phonon energies		
TA	$\hbar\omega_{K,TA}$	23 meV
LA	$\hbar\omega_{K,LA}$	29 meV
TO	$\hbar\omega_{\Gamma,TO}$	48 meV
	$\hbar\omega_{K,TO}$	47 meV
LO	$\hbar\omega_{\Gamma,LO}$	48 meV
	$\hbar\omega_{K,LO}$	41 meV
Homopolar	$\hbar\omega_{HP}$	50 meV

$1/[\exp(\hbar\omega/k_B T) - 1]$, where $\hbar\omega$ is the phonon energy. The expressions of phonon scattering rates and related physical parameters for monolayer MoS_2 have been derived by Kaasbjerg *et al.* [128,129] Table 4 summarizes the phonon parameters required in the calculation. To account for the screening effect, Jena *et al.* included the electron polarization function ε_{2D} in the calculation. Hence the scattering rate due to deformation potential of the acoustic phonon is written as [132]

$$\frac{1}{\tau_{ac}} = \frac{\Xi_{ac}^2 k_B T m^*}{2\pi\hbar^3 \rho_s v_s^2} \int_{-\pi}^{\pi} \frac{(1 - \cos\theta)}{\varepsilon_{2D}^2}, \tag{6}$$

where k_B, T, and $\hbar$ are the Boltzmann constant, temperature, and Planck constant, respectively, and θ is the elastic scattering angle from the initial momentum k to the final momentumto k', and ε_{2D} is the electron polarization function in the 2D semiconductor. The meanings and values of other parameters related to MoS_2 are listed in Table 4. Similarly, the scattering rate of the polar phonons is given by [132]

$$\frac{1}{\tau_{op}} = \frac{\Theta[E_k - \hbar\omega_{op}^\nu]}{\tau_{op}^+} + \frac{1}{\tau_{op}^-}, \tag{7}$$

$$\frac{1}{\tau_{0\text{-}ODP}^\pm} = \frac{D_0^2 m^* (N_q + \frac{1}{2} \pm \frac{1}{2})}{4\pi\hbar^2 \rho_s \omega} \int_{-\pi}^{\pi} \frac{(1 - (k'/k)\cos\theta)\mathrm{d}\theta}{\varepsilon_{2D}^2}, \tag{8}$$

$$\frac{1}{\tau_{1\text{-}ODP}^\pm} = \frac{D_1^2 m^* (N_q + \frac{1}{2} \pm \frac{1}{2})}{4\pi\hbar^2 \rho_s \omega} \int_{-\pi}^{\pi} \frac{q^2 (1 - (k'/k)\cos\theta)\mathrm{d}\theta}{\varepsilon_{2D}^2}. \tag{9}$$

where $\Theta[]$ is the step function, E_k is the carrier energy at mo-

mentum k, ω is the phonon frequency, and $q = 2k \cdot \sin(\theta/2)$ is the scattering vector. The superscript $+$ and $-$ represent scattering processes with absorbing and releasing a phonon, respectively. The subscripts 0 and 1 denote the zeroth- and first-order optical deformation potential, respectively.

4.2.3 Fröhlich and piezoelectric interactions

In compound semiconductors like GaAs and all MX_2 chalcogenides, dipole moments forms between adjacent cation and anion due to the polar nature of the chemical bonds. Deformation of the lattice by polar phonons perturbs the dipole moment between atoms which results in an electric field that is coupled to carriers, as shown in Fig. 10c. Polar optical phonon scattering, known as Fröhlich interaction, is normally strong near room temperature. In contrast, the polar acoustic phonon scattering, known as piezoelectric interaction, is typically weak. [129]

The scattering rate for Fröhlich interaction is given by [132,242]

$$\frac{1}{\tau_{LO}^\pm} = \frac{e^2 \omega m^*}{8\pi\hbar^2} \frac{1}{\varepsilon_0} \left(\frac{1}{\varepsilon_1^\infty} - \frac{1}{\varepsilon_1^0} \right) (N_q + \frac{1}{2} \pm \frac{1}{2})$$

$$\int_{-\pi}^{\pi} \frac{1}{q} \Phi(q,t) \frac{(1 - (k'/k)\cos\theta)\mathrm{d}\theta}{\varepsilon_{2D}^2} \tag{10}$$

where e and ε_0 are the elementary charge and vacuum permittivity, respectively, the superscripts of 0 and ∞ in the permittivity denote the static and high-frequency values, respectively, and $\Phi(q,t)$ is the thickness-dependent configurative form factor. A simplified version of $\Phi(q,t)$ for monolayer channels (within zero-thickness approximation) is available in ref. 240. A strict solution for a generalized FET configuration can be found in refs. 131 and 228.

Kaasbjerg *et al.* derived the scattering matrix element for the piezoelectric interaction in 2D MoS_2, [129]

$$\left| M_{PE}^{q\lambda} \right| = e_{11} eq/\varepsilon_0 \times \mathrm{erfc}(q\sigma/2) |A_\lambda(\mathbf{q})| \tag{11}$$

where $M_{PE}^{q\lambda}$ is the independent component of the piezoelectric tensor of the 2D hexagonal lattice, e_{11} is the piezoelectric constant, erfc() is the complementary error function, σ is an effective width of the electron wave functions, and $A_\lambda(\mathbf{q})$ is the anisotropy factor that accounts for the anisotropic angular dependence of the piezoelectric interaction. Within the long-wavelength approximation, the high-temperature relaxation time for piezoelectric scattering can be calculated together with the acoustic phonon scattering as [129]

$$\frac{1}{\tau_{PE}} = \frac{1}{\tau_{ac}} \times \frac{(e_{11}e/\varepsilon_0)^2}{2\Xi_{ac}^2}. \tag{12}$$

4.2.4 Remote interfacial phonons

Electrons in semiconductors, especially in the inversion layer of electrically gated FET channels, can excite phonons in the surrounding dielectrics via long-range Coulomb interactions, if the dielectrics support polar vibrational modes, as shown in Fig 10d. They are long recognized as 'remote interface phonons' (RIP) or 'surface optical phonons' (SOP) and exist in dielectrics near the inversion layers in silicon [243,244], organic FETs, [245–247] and graphene. [248–253] The RIP scattering may not be a significant scat-

Table 5 RIP modes for commonly used dielectrics.

Dielectric	ε_{ox}^0	ε_{ox}^∞	ω_{RIP}^1	ω_{RIP}^2
SiO_2	3.9	2.5	55.6	138
BN	5.1	4.1	93.1	179
AlN	9.1	4.8	81.4	88.5
Al_2O_3	12.5	3.2	48.2	71.4
HfO_2	22	5.0	12.4	48.4
ZrO_2	24	4.0	16.7	57.7

tering mechanism in low-field transport or in FETs using low-κ dielectrics, but it can become important at high fields,[253] large inversion densities or high-κ dielectric surroundings, as pointed out by Moore *et al.*[243,244] Experimental studies on organic FETs indicate that the use of high κ dielectric degrades FET carrier mobility.[245–247] Table 5 lists the RIP modes for commonly used dielectrics, which are useful for theoretical calculation and device design.

On the assumptions of zero thickness for 2D channels and semi-infinite for dielectrics, the electron-RIP coupling parameter is

$$F_v^2 = \frac{\hbar\omega_{RIP}^v}{2S\varepsilon_0}\left(\frac{1}{\varepsilon_2^\infty+\varepsilon_3^\infty}-\frac{1}{\varepsilon_2^0+\varepsilon_3^\infty}\right) \tag{13}$$

where ε_i ($i=1,2,3$) denotes the dielectric constants for different layers of channel and dielectrics as shown in Fig. 11, and

$$\omega_{RIP}^v = \omega_{TO}^v\left(\frac{\varepsilon_2^0+\varepsilon_3^\infty}{\varepsilon_2^\infty+\varepsilon_3^\infty}\right)^{1/2}. \tag{14}$$

The scattering rate due to RIP can be written as[132]

$$\frac{1}{\tau_{RIP}^\pm} = \frac{32\pi^3 e^2 F_v^2 m^* S}{\hbar^3 a^2}\left(N_q+\frac{1}{2}\pm\frac{1}{2}\right)$$

$$\int_{-\pi}^{\pi}\frac{1}{q}\left(\frac{\sinh(aq/2)}{4\pi^2 q+a^2 q^3}\right)^2\frac{(1-(k'/k)\cos\theta)\mathrm{d}\theta}{\varepsilon_{2D}^2}. \tag{15}$$

The significant room-temperature RIP scattering rate for high-κ dielectric in monolayer MoS_2 FETs poses a challenge to the dielectric screening engineering advocated,[81,241] which is oriented to enhance carrier mobility. We will elaborate this issue in section 5.3.

4.2.5 Atomic and structural defects

Atomic and structural defects can create midgap energy states or highly localized band tails and considerable affect charge transport in semiconductors. There are many different types of defects, ranging from spatially extended structures (*e.g.*, grain boundaries, dislocations, and precipitates), to pairs and complexes, to isolated vacancies or impurities. The theoretical and experimental studies on the defects are very active in the field of electronic band structure calculation[254–262] because defect chemistry brings about industrial applications. For instance, the sulfur vacancies in MoS_2 enable its use as chemical catalysis for desulfurization in petrochemistry[263,264] and water splitting.[265–268]

The defect scattering is normally not considered in high-quality superlattices and silicon FETs,[238] because the very low density

causes negligible scattering rates relative to other mechanisms. However, the defect density is by no means low in the 2D vdW crystals. Figure 13 show the structures and corresponding formation energies of different atomic defects in MoS_2. The sulfur vacancies have a rather low formation energy of $\sim$1.6 eV, hence the anion vacancies tend to form in chalcogenides, just like in oxides (*e.g.* ZnO), which is presumably a strong scattering source when the sample quality is not sufficiently high.

High-resolution TEM experiments revealed the presence of large amounts of point defects and grain boundaries in natural and synthesized MoS_2.[227,262,270,271] It is found that the structures of dominant defects correlate closely with material growth methods. For samples prepared by mechanical exfoliation and chemical vapor deposition (CVD), sulfur vacancy defects with one (denoted as V_S, Fig. 13a) or two (V_{S2}) S atoms absent are frequently observed, while the dominant defects for the physical vapor deposited (PVD) samples are antisite defects with one Mo atom replacing one (Mo_S, Fig. 13e) or two (Mo_{S2}, Fig. 13g) S atoms.[271] The density of sulfur vacancy can reach $(1.2\pm0.4)\times10^{13}$ cm^{-2} in exfoliated and CVD samples, corresponding to a surprisingly high atomic percentages of 0.4%. Undoubtedly, atomic defects would play an important role in carrier scattering, if such high-level defects are present in device channels.

Wang *et al.* attributed the presence of sulfur vacancies as the reason for the hopping transport behavior observed in low carrier density regime.[227] The short-range vacancy scattering is also proposed as one of the scattering mechanisms in the CVD MoS_2 flakes by Eda *et al.*[225] With long-time *in situ* thermal annealing to minimize contact resistance, they estimated a high room-temperature mobility of 45 cm^{2}V^{-1}s^{-1} and an intrinsic mobility of 58 cm^{2}V^{-1}s^{-1} after deducting the effect of short-range vacancy scattering. Since the anion vacancies could be the leading scattering centers, vacancy repair is expected to improve device performance.

Hitherto, there has been no theoretical work on the vacancy scattering in 2D vdW semiconductors. However, one can quickly grasp its basic characteristics by looking through previous works on their bulk[272,273] and 2D analogue graphene.[274,275] Unlike Coulomb impurity scattering, vacancy scattering is a kind of short-range interaction with interaction range comparable to the lattice spacing (Fig. 10e). In this case, the scattering potential can be treated as a δ function.[275] The scattering matrix in low-energy regime becomes dispersionless on energy for 2D semiconductors because the Fourier transformation of the real space δ potential is a constant in the reciprocal momentum space, which results in a constant scattering matrix. Hence, the scattering rate of atomic vacancies is independent on carrier density, manifested itself as a resistivity background as in graphene.[274] In addition the vacancy scattering in 2D systems should be weakly dependent on temperature or channel thickness because the defect density is independent on these two parameters. It would reduce the temperature dependence of mobility and the temperature exponent γ, once vacancy scattering becomes important. In this sense, the low γ values ($\sim$0.7) observed in clean samples[221,222] is likely indicative of the emergent dominance of vacancy scattering. Overall, it is expected that defect scattering would become paramount in
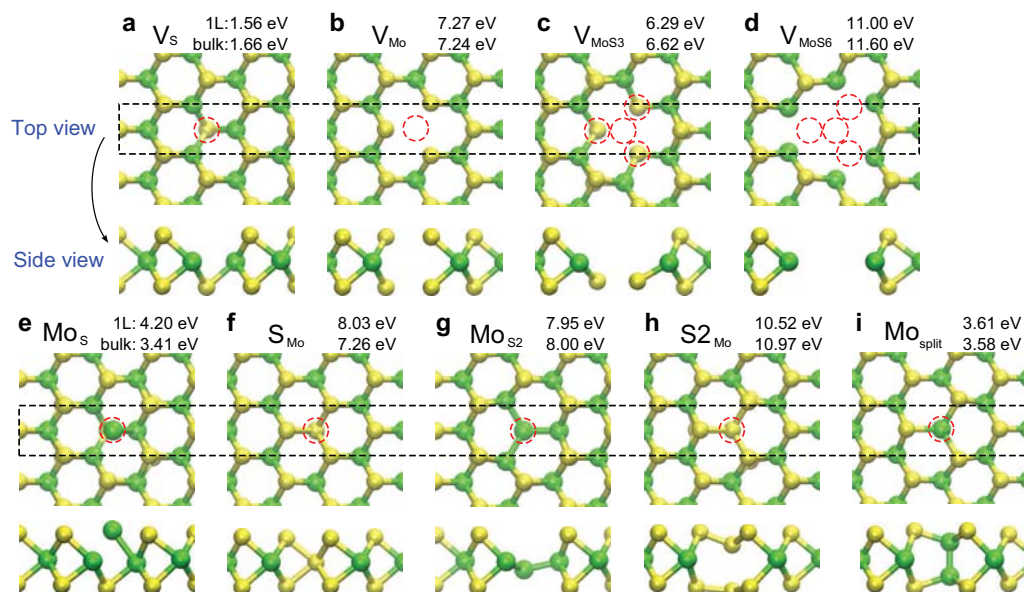
Fig. 13 Optimized atomic structures and formation energies for different defects in MoS_2 monolayer (1L) and bulk. (a)–(d): vacancies, (e)–(h):antisites, (i) Mo-Mo split interstitial defect. Dashed circles (red) denote the position of the defect. Owing to a rather low formation energy of $\sim$1.6 eV, sulfur vacancies tend to form in MoS_2. Reproduced with permission from ref. 269, copyright 2015, American Physical Society.

very clean samples or at low temperature when Coulomb impurity and phonon scattering rates are low.[223]

Grain boundary is another typical form of defect commonly present in synthesized samples. Figures 14a–14f show two types of grain boundaries (the mirror and title type), as seen by optical microscopy and photoluminescent mapping.[270,276,277] An important question for device applications is whether these grain boundaries disrupt or modify electronic transport. Hone *et al.* compared the electronic transport properties of exfoliated and synthesized MoS_2 flakes with room temperature mobilities from 1 to 8 $cm^2V^{-1}s^{-1}$.[270] They found that device performance strongly depends on the boundary type as well as current flow direction. The mirror twin boundary has little effect on channel conductivity when current is perpendicular to boundary and, surprisingly, it slightly increases the on-state conductivity by when current flows in parallel (Fig. 14g). This observation suggests that the few-atom-wide twin boundaries, although still semiconducting, have similar conductivity of pristine MoS_2. In contrast, the tilt boundary generally degrades the device performances to large extent in any current directions (Fig. 14h). A wide variation of the conductance (5–80%) is observed among devices, implying a complicated dependence of electronic structure at boundaries on the tilt angle and atomic structure.[278]

4.2.6 Other scattering mechanisms

Besides above mechanisms, other scattering factors such as electron-electron collision and surface corrugation could also be a correction the overall electronic performance. It is noteworthy that all the above mechanisms are discussed within the assumption of low-energy, intraband approximation and they are suitable only for the transport behavior at low fields. More complicated scattering processes including interband scattering under high electrical and magnetic fields are beyond the scope of this
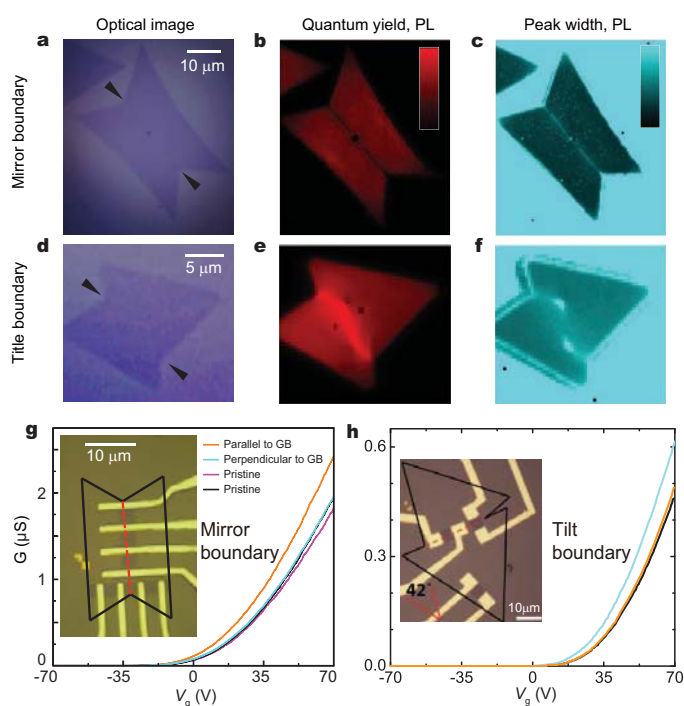
Fig. 14 Optical and electronic properties of mirror and tilt boundaries in synthesized MoS_2 flakes. (a)–(c) Optical measurements of a MoS_2 flake containing a mirror twin boundary. (d)–(f) Corresponding measurements for a MoS_2 flake containing a tilt boundary. Panels (a) and (d) are optical images; Panel (b), (c), (e), and (f) are colour plots of photoluminescence. Panels (g) and (h) show the transfer curves of four FETs fabricated from the MoS_2 flakes with mirror and tilt boundaries in the insets. Reproduced with permission from ref. 270, copyright 2013, Nature Publishing Group.

review and will not be discussed here.

5 Mobility engineering strategies and state-of-the-art performance

5.1 Contact optimization

It is well known that the presence of contact resistance strongly limits the current carrying capacity in FETs. The contact resistance for 2D chalcogenides ranges from 10–$100\,\mathrm{k\Omega\cdot\mu m}$ at Au/MoS$_2$ contacts[229] to $\sim 1\,\mathrm{k\Omega\cdot\mu m}$ with graphene/2L WSe$_2$ contacts.[214] These values are at least 1–2 orders higher than the requirement of the deep-nanometer technological node in semiconductor industry. Hence, optimizing the electrode/channel contacts is highly desired.

Figure 15 summarizes the mobility engineering strategies devised for contact optimization. Thermal annealing is traditionally used to reduce contact resistance. This technique is particularly necessary and effective for the 2D chalcogenide FETs. Jarillo-Herrero et al. found that large contact resistance is the main reason for the low field-effect mobility in thermally untreated 2D FETs.[172] A huge drop in contact resistance, with 2 orders of magnitude in monolayer and more than 1 order of magnitude in bilayer MoS$_2$ devices, was observed after long-time (12 h), low-temperature (120 °C) in situ thermal annealing (Fig. 15b). Remarkably high room temperature mobility values of 20–50 and 80–150 cm^{2}V^{-1}s^{-1} were observed in monolayer and bilayer MoS$_2$, respectively. In their experiment, low annealing temperature was used likely because of the safety limitation of test cables and cryostat, which, however, favorably prevents the decomposition of MoS$_2$ during annealing and the creation of sulfur vacancies, a kind of short-range carrier scattering center. The similar behavior has been observed in CVD MoS$_2$ samples by Eda et al.[225] and 1L WS$_2$ samples by Kis et al.[208] (Fig. 15a). Figure 15c shows the real-time monitor of the mobility evolution with annealing time for the 1L WS$_2$ sample under both two-terminal and four-terminal measurement. After a long annealing time of 150 h, the mobility extracted by four-terminal method remains 2-fold higher than that extracted by two-terminal method, suggesting that the contact issue, though largely reduced, cannot be completely eliminated by thermal annealing.

Energy level matching between electrodes and semiconductors was also employed to improve the field-effect mobility. The height of the contact barrier is highly related to the work function of metal electrodes, as shown in inset of Fig. 15d. The metal Sc, with a low work function of 3.5 eV which is close to the electron affinity of MoS$_2$ $\sim$4.0 eV, is found to form electrically transparent interface with thick MoS$_2$.[181] The mobility reaches 180 cm^{2}V^{-1}s^{-1} in $\sim$10 nm MoS$_2$ devices. The pinning coefficient is estimated to be 0.1, as compared with $\sim$0.3 in bulk silicon, suggesting the presence of extremely strong pining effect in the 2D semiconductors due to the full exposure of channel surfaces. Nevertheless, the energy level matching with Sc electrode seems an effective way to improve mobility for thick channels but to be much less influential for ultrathin samples. The carrier mobility was found to sharply drop to 25 cm^{2}V^{-1}s^{-1} in $\sim$2 nm MoS$_2$, indicating a more complicated behavior in the ultrathin regime. This can be ascribed to

the expansions of bandgap and contact barrier due to quantum confinement (Fig. 8d). Owing to the upshift of conduction band in the few-layer MoS$_2$, electrodes with lower work functions are required to match the high-lying conduction band.

Graphene is also explored as a contact material to chalcogenides because it is a unique Dirac metal whose work function can be broadly tuned upon applying gate voltage.[216,223,281,282] In particular, graphene contacted MoS$_2$ shows extremely high low-temperature mobility when encapsulated by clean BN.[223,282] The devices with graphene contacts will be discussed in section 5.5.

Besides the empirical strategy, band structure calculation is also used to understand the interface physics to facilitate contact design between metal and monolayer WSe$_2$ (Figs. 8e–8g). Calculations based on ab initio density functional theory (DFT) indicate that using d-orbital electron abundant transition metals as contacts like Ag and Ti are beneficial to form better electron injection into WSe$_2$ because the d-orbitals in these metals can hybridize with the d-orbitals in the Se and W atoms (Fig. 8h).[279] A considerably high carrier mobility of 142 cm^{2}V^{-1}s^{-1} is measured in thermally annealed Ag contacted monolayer WSe$_2$ samples in vacuum environment.

Apart from the rational choice of contact metals, contact doping by gas molecules or alkali metals is also developed as a chemical strategy to optimize contact quality.[183,280] By introducing highly active electron donor NO$_2$ to form heavily doped contact areas (Fig. 15i), Javey et al. observed a high mobility of 250 cm^{2}V^{-1}s^{-1} in top ZrO$_2$ gated, Pd contacted p-type monolayer WSe$_2$ FETs (Fig. 15j).[280] They carefully compared the device current before and after NO$_2$ doping and about 3 orders of magnitude enhancement in device current was observed (Fig. 15k), indicating the critical role of contact in achieving high device performance. Additionally, they observed a high mobility of >110 cm^{2}V^{-1}s^{-1} in a potassium doped 3L WSe$_2$ FET.[183]

For the same reason, ionic liquid gating is used for contact engineering.[215,216] This is because the injection of charges is assisted by high carrier density in channels near the metal/semiconductor contacts, which largely decreases the width of the injection barrier. As a result, carrier injection from the source/drain contacts is controlled by tunneling instead of by the over-the-barrier thermal activation process (Fig. 8b). Zhou et al. reported a high electron and hole mobility of $\sim$200 cm^{2}V^{-1}s^{-1} at 160 K and at $\sim$300 cm^{2}V^{-1}s^{-1} at 77 K in 6 nm WSe$_2$.[216] Similarly, Jarillo-Herrero et al. achieved a low contact resistance of <330 $\Omega\cdot\mu$m and a high mobility of $\sim$600 cm^{2}V^{-1}s^{-1} at 220K in 3L WSe$_2$.[215]

Artificial engineered phase change has also been developed to increase contact quality.[136–138] For chalcogenides, different atomic structures and phases may exhibit distinct electronic properties. Typically, the 2H phase of MoS$_2$ is metallic while the 1T phase is semiconducting. After replacing the 2H phase with the 1T phase, Chhowalla et al. observed a $\sim$5-fold decrease of contact resistance from 1.1 to 0.2 k$\Omega\cdot\mu$m at zero gate bias,[137] a value comparable to the source/drain parasitic resistance in silicon FETs (290 $\Omega\cdot\mu$m and $\Omega\cdot\mu$m for planar and SOI low standby power CMOS, respectively). As a result, the carrier mobility increases from 19 to 46 cm^{2}V^{-1}s^{-1}. Direct doping and metallization at contacts is a promising way to achieve technologically vi-

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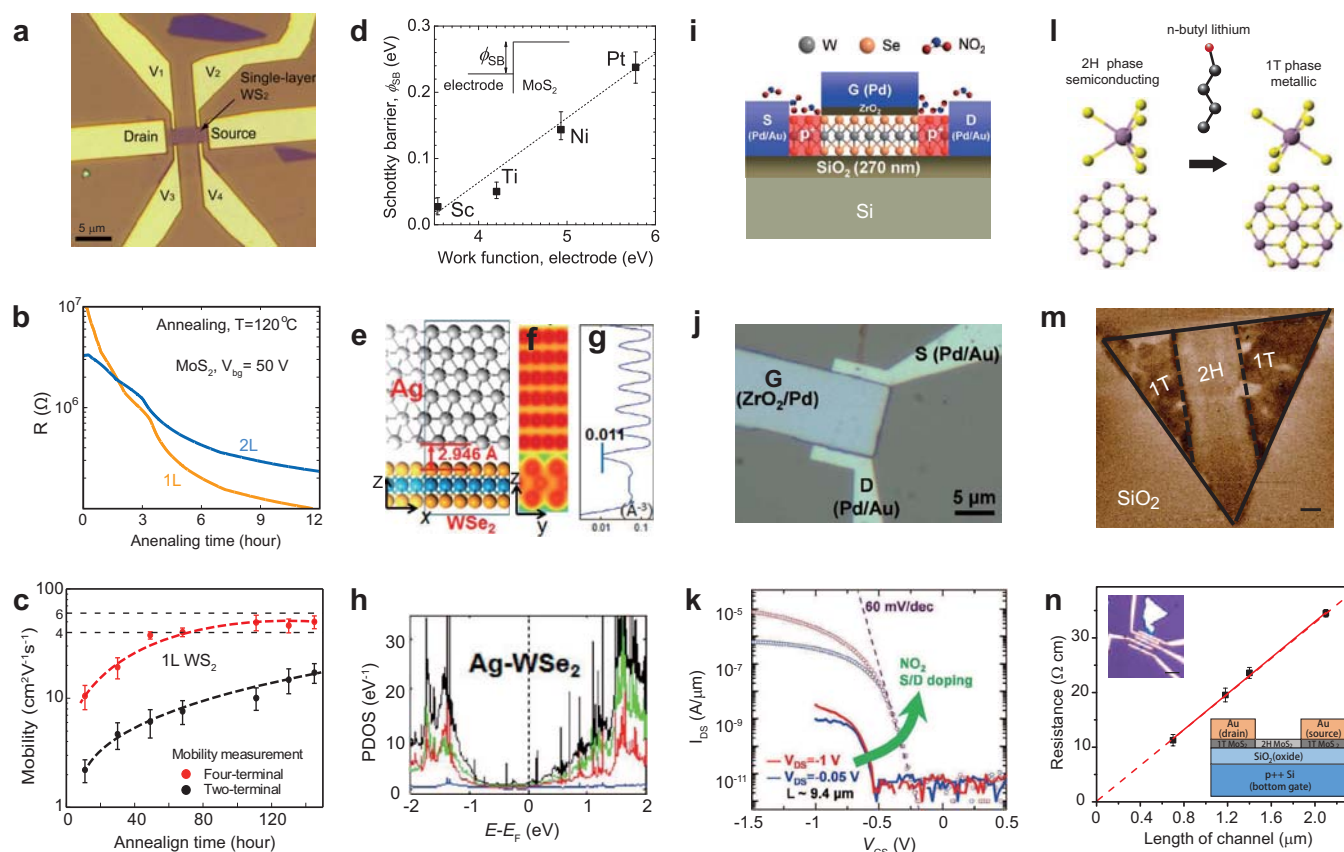
Fig. 15 Mobility engineering for contact optimization. (a)–(c) Thermal annealing. (a) Optical image of 1L WS_2 four-terminal measurement geometry which can be used to estimate the contact quality. (b) Evolution of contact resistance at Ti/MoS_2 interface with time under 120 °C thermal annealing up to 12 h. (c) Mobility comparison for 1L WS_2 under different wiring methods (two-terminal and four-terminal), showing that the contact resistance is difficult to be eliminated since the difference of mobility values under the two wiring methods exists all the time (up to 150 h annealing). (d) Energy level matching, which shows that electrodes with low work functions in general lead to low contact barrier to n-type semiconductors. Adapted with permission from ref. 181, copyright 2013, American Chemical Society. (e)–(h) Orbit hybridizing engineering. (e) Side view of the relaxed contact regions at the WS_2/ Ag (111) interface. (f) and (g) show the contour plot of the spatial electron density and the average line electron density, respectively. (h) Partial density of states (PDOS) the $Ag-WS_2$ system. Hybridization states occur at the contacts which are beneficial for carrier transfer. (i)–(k) Contact doping engineering. (i) Schematic diagram for using NO_2 gas to dope the channel edges in vicinity of contacts. (j) Optical device image with top ZrO_2/Pd gate stacks. (k) Comparison of channel current before and after NO_2 doping. (l)–(n) Phase change engineering. (l) Atomic phase change of MoS_2 from 2H to 1T structure after soaking in n-butyl lithium. (m) Electrostatic force microscopy phase image of a 1L MoS_2 nanosheet showing the difference between locally patterned 2H (bright colour) and 1T (dark colour) phases. The scale bar is 1 μm. (n) Transfer line plot for the 1T phase contacted MoS_2 channels. The intercept is close to zero, indicating the contact resistance is very small. Panels (a) and (c) are reproduced with permission from ref. 208, copyright 2014, American Chemical Society. Panel (b) is reproduced with permission from ref. 172, copyright 2013, American Chemical Society. Panels (e)–(h) are reproduced with permission from ref. 279, copyright 2013, American Chemical Society. Panels (i)–(k) are reproduced with permission from ref. 280, copyright 2012, American Chemical Society. Panels (l)–(n) are reproduced with permission from ref. 137, copyright 2014, Nature Publishing Group.

able 2D FETs.

5.2 Reduction of impurity scattering

Before discussing the technical routes, we first remark on the origins of the Coulomb impurities and corresponding experimental evidence, which may help to understand the nature behind. Figure 16a schematically displays the sources of Coulomb impurities at the both interfaces of the FET channels, including gaseous adsorbates (*e.g.* humidity and oxygen molecules), unsaturated chemical bonds/groups at dielectric surface, and chemical residues during device fabrication. It has been pointed out

that the device current is higher in vacuum than in ambient measurement environment (Fig. 16b).[180,221] The gaseous adsorbate such as humidity and oxygen molecules[169,180,283] which results in charge transfer to channel are believed to be an important Coulomb impurity source. The second impurity source can be attributed to chemical residues introduced during device fabrication, as evidenced by the increase in channel current in both exfoliated and CVD devices after performing long-time thermal annealing under ultrahigh vacuum.[172,225] The dangling bonds, hydroxyl groups and charged ions in the surface of dielectric[284] are believed to be the third type of impurity source since a remarkable current increase is observed in suspended MoS_2 channels by
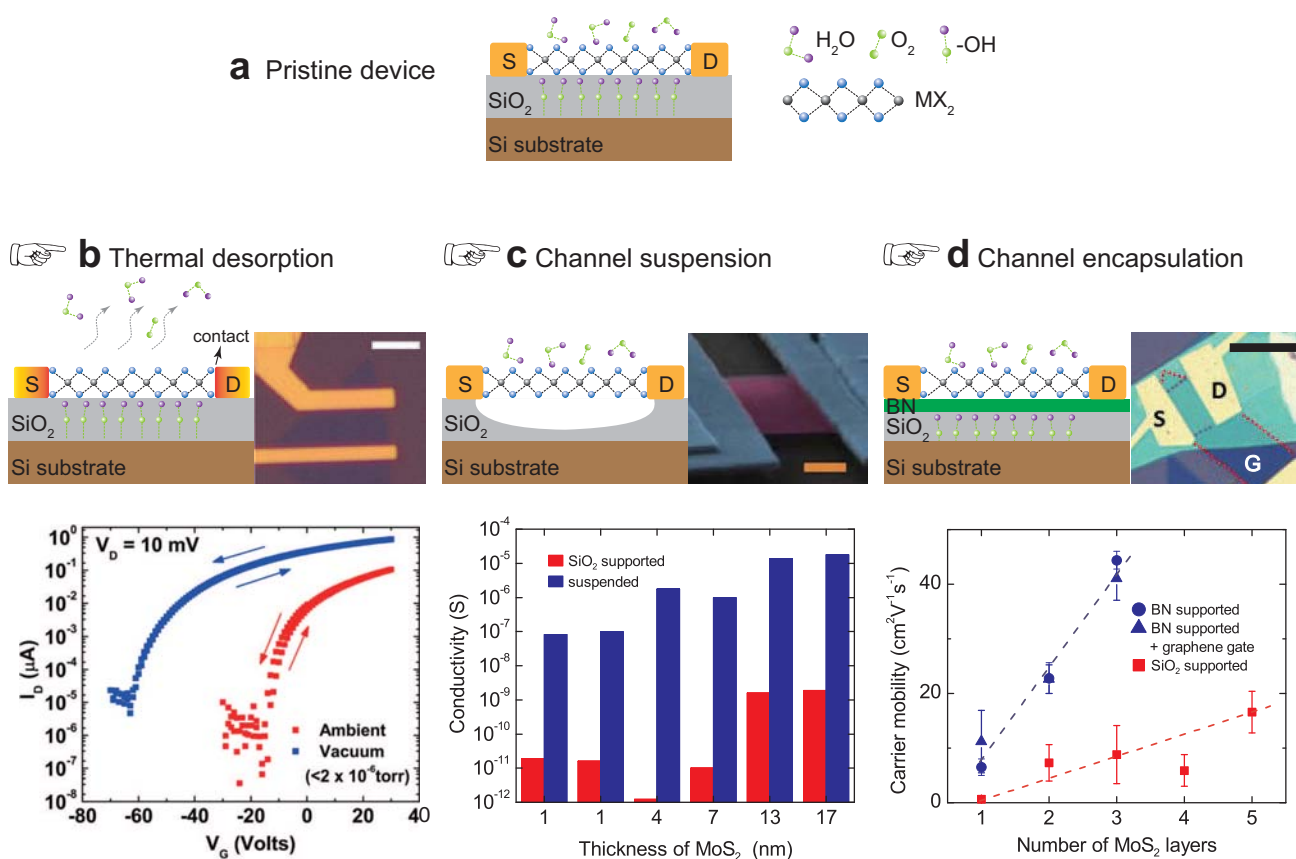
Fig. 16 Mobility engineering for interfacial impurity suppression. (a) Schematic diagram for a pristine SiO_2 back-gated FET consisted of a 2D MX_2 channel. The main Coulomb impurities arise from the molecular absorbates on the top channel surface and the dangling bonds and hydroxyl group (–OH) on the bottom channel surface (*i.e.* channel/dielctric interface). Three techniques are developed to suppress the impurity sources: (b) thermal desorption at ultrahigh vacuum, (c) channel suspension to remove the bottom impurities, (d) channel encapsulation by clean dielectrics such as boron nitride or polymers (*e.g.* PMMA). In each panel from (b) to (d), the schematic techniques, typical device images, and corresponding effects on performance are illustrated. Panel (b) is reproduced with permission from ref. 221, copyright 2013, American Institute of Physics. Panel (c) is reproduced with permission from ref. 192, copyright 2015, Institute of Physics, UK. Panel (d) is reproduced with permission from ref. 175, copyright 2013, American Chemical Society.

etching out the underlying SiO_2 dielectric (Fig. 16c). [177,178,192]

Figure 16b–16d show the main three schemes developed to suppress the Coulomb impurity sources including 1) thermal desorption at ultrahigh vacuum (Fig. 16b), 2) channel suspension to remove the bottom impurities (Fig. 16c), and 3) channel encapsulation by clean dielectrics such as the vdW dielectric hexagonal boron nitride (hBN) and hydrophobic polymers (*e.g.* PMMA) (Fig. 16d, only encapsulation at the bottom side is shown).

Thermal desorption is proven one of the most effective methods to improve mobility in chalcogenide. In the high vacuum measurement (2×10^{-6} Torr), Hersam *et al.* observed the highest room-temperature mobility of 60–70 $cm^2V^{-1}s^{-1}$ for pristine (neither encapsulated nor suspended), two-terminal (mobility underestimation due to contact resistance) 1L MoS_2, [221] demonstrating that the gaseous adsorbates are one of the leading scattering centers. Here, it deserves to note the different roles played by the annealing surroundings. Annealing *ex situ* can only influence the contact quality while *in situ* vacuum annealing can further remove gaseous adsorbates. In addition, an ultrahigh vacuum and long-time treatment is particularly critical to complete the adsor-

bate desorption. [172,208]

Among the three schemes to suppress interfacial impurities, the first and third are technological viable but the second one is only of scientific interest since a suspended channel would cause severe issues in mechanical stability. Besides, the channel suspension scheme on 2D chalcogenides seems not as successful as graphene. Naively, one expects suspended devices to have higher mobility, due to removal of substrates that introduce trapped charges and other scattering centers. However, the electronic performance of most suspended 1L MX_2 flakes fabricated to date remains much lower than SiO_2 supported samples. [177,178,192] One possible explanation is the higher chemical activity of MX_2 chalcogenides than graphene in the substrate etchant which produces new scattering sites on channels after dielectric etching treatment. [192] Additionally, the general worse contact in chalcogenides devices could be another factor in limiting the performance of suspended MX_2 flakes. Recently, Lau *et al.* investigated the effect of thermal annealing condition on the suspended MoS_2 samples and they showed remarkable increase in mobility from 46 to 105 $cm^2V^{-1}s^{-1}$ for a 17 nm thick sample. [192]

Channel encapsulation is always a challenging task due to either the incompatibility of encapsulation materials to processing (*e.g.* PMMA) or the complexity in fabrication (*e.g.* hBN). Nonetheless, interface engineering via channel encapsulation has been applied to fabricate high-performance MoS$_2$ FETs. By placing multiple MoS$_2$ flakes on PMMA dielectric and using four-terminal measurements, Fuhrer *et al.* demonstrated a high mobility value of $\sim$500 cm^{2}V^{-1}s^{-1} in $\sim$50 nm MoS$_2$.[285] With a similar dielectric material, Hu *et al.* observed a room-temperature mobility of 1055 cm^{2}V^{-1}s^{-1} in back-gated multilayer InSe,[286] being an extremely high value comparable to silicon.

The atomically flat vdW dielectric hBN, which is free of dangling bond and thus is in principle free of trapped charges, has proven to be beneficial for graphene electronics.[287–289] It is naturally introduced into the chalcogenide devices. Kim *et al.* first adopted hBN as dielectric layer in MoS$_2$ FETs.[175] An order of magnitude enhancement in field-effect mobility, from 0.5 to 7.6 cm^{2}V^{-1}s^{-1}, is observed in the hBN supported monolayer MoS$_2$ FETs, as compared with the conventional SiO$_2$ supported devices. A high mobility of $\sim$45 cm^{2}V^{-1}s^{-1} is measured in a trilayer device. By comparing the mobility trend versus channel thickness, the authors pointed out that there is likely a remarkable contribution from the electrode/channel contacts that limit the mobility because contact resistance decreases with increasing channel thickness. Independently, Tsukagoshi *et al.* also fabricated hBN supported MoS$_2$ FETs and observed similar behavior of mobility enhancement and thickness dependence.[176] Moreover, they studied the temperature dependence and revealed that the clean hBN dielectric can suppress the carrier traps at channel/dielectric interface, which converts the carrier transport in monolayer MoS$_2$ from hopping to thermal activation mode. Besides MoS$_2$, other MX$_2$ chalcogenides were also explored. The mobility enhancement from 17 to 80 cm^{2}V^{-1}s^{-1} is observed in 4L WS$_2$ after replacing the underlying dielectric from SiO$_2$ to clean hBN.[210]

5.3 Dielectric screening versus RIP scattering

Since Coulomb impurity is one of the main scattering mechanisms in FETs, a dielectric engineering, *i.e.*, employing high κ dielectrics, was proposed to be a strategy to reduce the Coulomb impurity scattering to carriers for the reason that the elevated permittivity of dielectrics is expected to enhance the screening ability to the adverse scattering potentials from internal and external Coulomb impurities.[241] This strategy would be justifiable, if the adopted high κ dielectrics do not bring remote interfacial phonons, and appears working on 2D chalcogenides with low initial mobility. A noticeable performance enhancement was observed in monolayer MoS$_2$ and SnS2 flakes,[81,218] with carrier mobility increasing from few to $\sim$50 cm^{2}V^{-1}s^{-1}.

In fact, there is a growing controversy on the exact role of the dielectric environment in suppressing carrier scattering. Early on, it was found that high-κ dielectrics lead to low carrier mobility in FETs made of silicon and organic materials because of the carrier scattering of polar phonon at the channel/dielectric interfaces.[243–247] In high-quality graphene, Geim *et al.* also pointed

out that screening of Coulomb impurities by high-κ dielectrics has little effect on mobility.[290] The same is also true in chalcogenides. Several groups confirmed that the introduction of high-κ dielectrics deteriorates, rather than improves, the mobility of high-quality chalcogenide devices.[137,216] In MoS$_2$ FETs with high initial mobility, Liao *et al.* recently observed a mobility degradation of 30-50% in top HfO$_2$ gated MoS$_2$, as compared with back SiO$_2$ gated devices.[291] Conversely, when dielectrics without available RIP modes are used such as polymer parylene, 2–3 fold enhancement in mobility, from $\sim$50 to 100–150 cm^{2}V^{-1}s^{-1}, was observed in 10 nm MoSe$_2$ samples.[202] All the experimental observations can be well explained by taking into account the adverse RIP scattering accompanied by the use of high-κ dielectrics. Ma and Jena *et al.* found that a FET can gain additional mobility enhancement from dielectric screening when the average permittivity of the top and bottom dielectrics is smaller than a critical value of 10.[132] The adverse RIP scattering would outperform and degrade mobility once the average permittivity is higher than the critical value.

In this sense, the early observation of mobility enhancement after high-κ dielectric deposition in devices with low initial mobility is likely due to the facts below: 1) improvement of device contact by thermal annealing during the time-consuming atomic layer deposition (ALD) process for the high κ dielectrics; 2) reaction and cleaning effect on the surface gaseous adsorbates (humidity and oxygen, which are one of the main Coulomb impurity source) with the ALD precursors; 3) encapsulation of the conduction channels and consequent insulation from external surroundings.

5.4 Atomic vacancy healing

Apart from the long-range charged impurities, short-range scattering factors such as anion vacancy in chalcogenides is also likely one of the leading carrier scattering mechanisms. Hence, it is desired to repair them with a chemical approach based on interface and molecular engineering when contact optimization and impurity scattering are already well addressed.

Figure 17 show a typical vacancy healing scheme assisted by interface engineering on dielectric and/or semiconductor with designed functional molecules. Due to the full exposure of sulfur planes, a post molecular surface modification and healing becomes realistic. By introducing a long-chain molecule with chemical group at one end attaching to SiO$_2$ and the other end modifying MoS$_2$ channel, one can form self-assembly monolayer (SAM) at the surface of 'dirty' SiO$_2$ dielectric (Fig. 17a). Lou *et al.* intentionally modified the chemical surroundings of the conduction channels in FETs with a series of designed SAMs.[196] The higher mobility of $\sim$18 cm^{2}V^{-1}s^{-1} was observed in the thiol group (–SH) contacted MoS$_2$ channels than those contacted by other groups of –OH, –SiO$_2$, –CF$_3$, –CH$_3$ and –NH$_2$ (Fig. 17b), due partially to the vacancy repair effect. They concluded that the mobility improvement is a combined effect of interface-related effects of charge transfer, built-in molecular polarities, varied densities of defects, and remote interfacial phonons.

Later on, with a double-side encapsulation of MoS$_2$ channels by
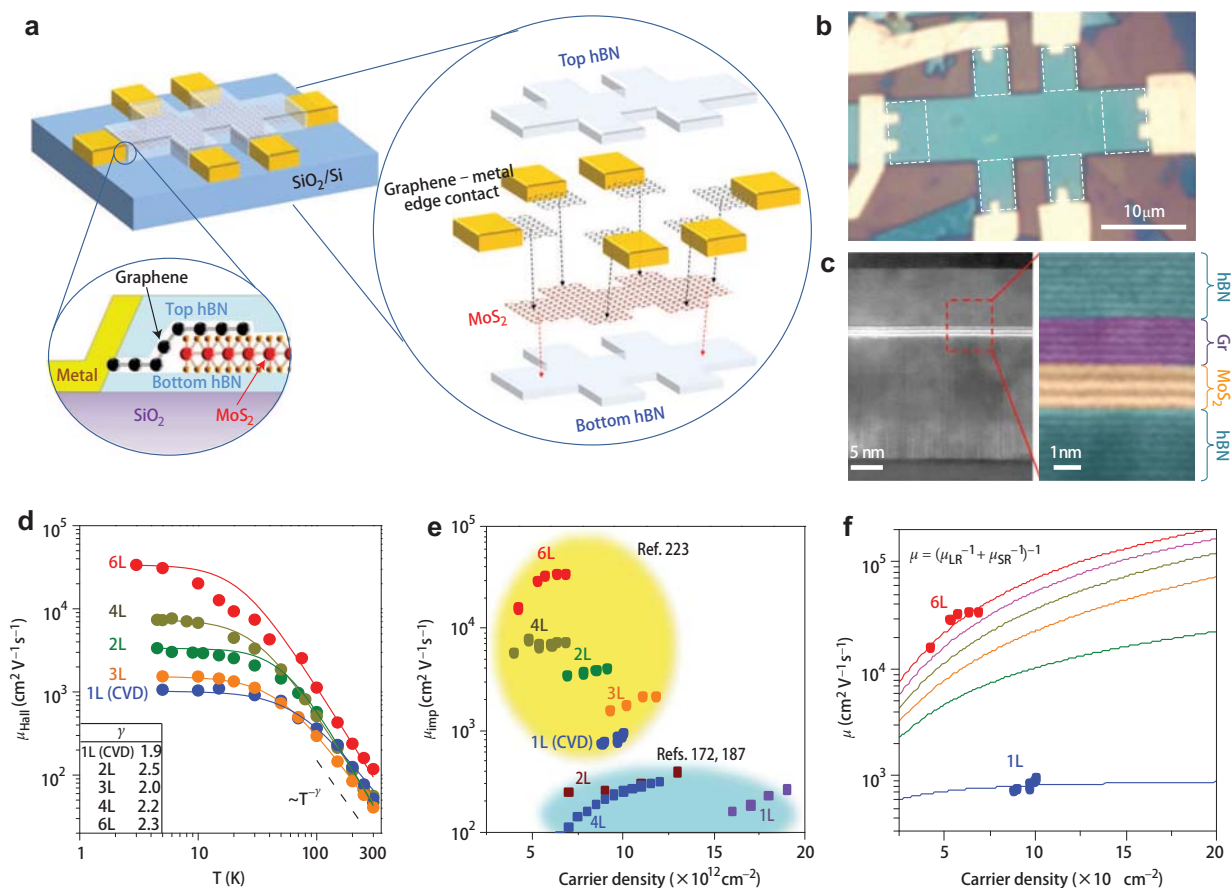
Fig. 18 A typical case with combined schemes of mobility engineering. (a) Schematic of the hBN-encapsulated MoS$_2$ multi-terminal device. The exploded view shows the individual components that constitute the heterostructure stack. Bottom: Zoom-in cross-sectional schematic of the metal-graphene-MoS$_2$ contact region. (b) Optical microscope image of a fabricated device. Graphene contact regions are outlined by dashed lines. (c) Cross-sectional TEM image of the fabricated device. The zoom-in false-colour image clearly shows the ultra-sharp interfaces between different layers (graphene, 5L; MoS$_2$, 3L; top hBN, 8 nm; bottom hBN, 19 nm). (d) Hall mobility of hBN-encapsulated MoS$_2$ devices (with different numbers of layers of MoS$_2$) as a function of temperature. The solid fitting lines are drawn by a combined phonon and impurity scattering model. As a visual guide, the dashed line shows the power law $\mu \sim T^{-\gamma}$, and fitted values of γ for each device are listed in the inset table. (e) Impurity-limited mobility (μ_{imp}) as a function of the MoS$_2$ carrier density. For comparison, previously reported values from MoS$_2$ on SiO$_2$ substrates (refs. 172 and 187) are plotted. (f) The solid lines show the theoretically calculated mobility including both long-range (LR) impurity scattering and short-range (SR) defect scattering based on Matthiessen's rule, $\mu^{-1} = \mu_{LR}^{-1} + \mu_{SR}^{-1}$, as a function of carrier density for 1L to 6L MoS$_2$. Experimental data are shown as solid circles. Reproduced with permission from ref. 223, copyright 2015, Nature Publishing Group.

thiol group ended (3-mercaptopropy)trimethoxysilane molecules and appropriate thermal healing, Wang *et al.* achieved a record high room-temperature mobility of 80 cm^{2}V^{-1}s^{-1} in monolayer MoS$_2$.[222] By comparing the high-resolution TEM images for the healed and untreated samples (Figs. 17e and 17f), they revealed that that the density of sulfur vacancies is largely reduced in the healed samples. Meanwhile, a remarkable enhancement in the room-temperature and low-temperature mobility is achieved in the double-side treated samples when compared with the single-side treated or untreated samples. Based on the observation and theoretical calculation, they attributed the large performance improvement as the healing effect on sulfur vacancy by the thiol group during thermal treatment. It worth noting that the above result is not merely a simple vacancy healing effect for the reasons below. Large suppression of Coulomb impurities and trap densities are simultaneously seen in their analysis, indicating the existence of cleaning effect on the channel interfaces after applying the SAM. In other word, the SAM layers can act the same role as hBN encapsulation to isolate the external Coulomb impurity scattering. It would be more reasonable to ascribe the mobility enhancement to the synergetic effects of the interface cleaning and the vacancy healing. Anyway, the proposed molecular healing strategy is a very promising technique to propel the 2D vdW semiconductors to their performance limit.

Apart from the iso-elemental repair technique, Soe *et al.* also proposed a novel healing technique of surface laser passivation by using a hetero-element of oxygen.[292] The basic concept is to passivate the chalcogen vacancies by adsorbed oxygen atoms which can, meanwhile, suppress the midgap states and repair the material electronic structure. They demonstrated that this technique can enhance the conductivity of monolayer WS$_2$ by 400 times and the photoconductivity by 150 times.

Table 6 The state-of-the-art carrier mobility values in 2D chalcogenide MoS_2 and WSe_2.

Channel material	Channel thickness	Contact & doping	Thermal annealing	Dielectric & encapsulation	Measurement pressure	μ@RT cm^{2}V^{-1}s^{-1}	μ@LT cm^{2}V^{-1}s^{-1}	γ value near RT	Ref. no.
MoS_2	1L	Gr.	No	DE:BN	vac.	~100	328 (1.9 K)	1.2	282
MoS_2	1L	Ti/Pd	ex. 350°C	DE:SAM	~1.3 mPa	81	>300 (10 K)	0.72	222
MoS_2	1L	Ti/Pd	in. 77°C	DE:SAM	~1.3 mPa	81	>300 (10 K)	0.72	222
MoS_2	1L	Au	No	BG:SiO$_2$	<0.3 mPa	60-70	~110 (~5 K)	0.62	221
MoS_2-C	1L	Gr.		DE:BN	vac.	~50	1020 (~4K)	1.9	223
MoS_2-C	1L	Au	in. 120°C	BG:SiO$_2$	vac. (PPMS)	45	~500 (10 K)	0.62	225
MoS_2	2L	Gr.		DE:BN	vac.	~40	~4000 (~4K)	2.5	223
MoS_2	3L	Gr.		DE:BN	vac.	~40	~2000 (~4K)	2	223
MoS_2	4L	Gr.		DE:BN	vac.	~55	~7000 (~4K)	2.2	223
MoS_2	5L	Gr.	No	DE:BN	vac.	<100	1300(~10 K)	N.A.	282
MoS_2	6L	Gr.		DE:BN	vac.	~120	34000 (~4K)	2.3	223
WSe_2	1L	Ag	in. 170°C	BG:SiO$_2$	<0.1 mPa	140	N.A.	N.A.	279
WSe_2:p	1L	Pd+NO$_2$	N.A.	TG: ZrO$_2$	<0.1 mPa	250	N.A.	N.A.	280

Abbreviations and notes are same as Table 3.
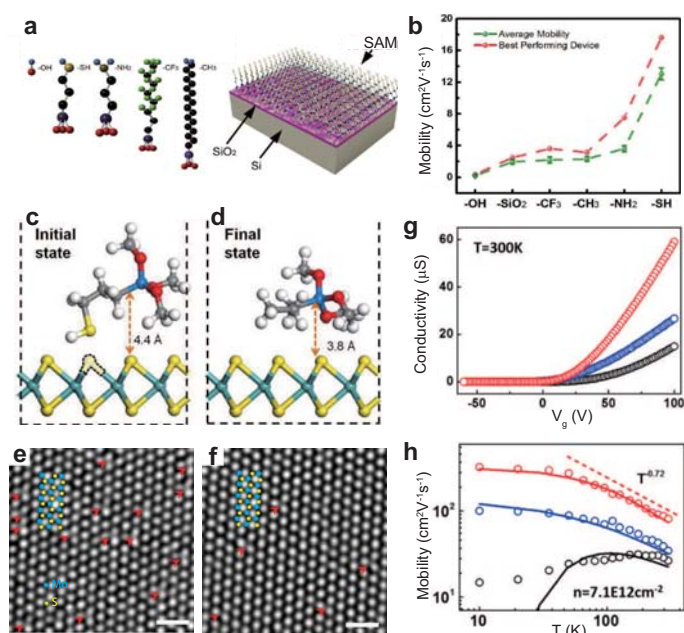
Fig. 17 Mobility engineering for atomic vacancy healing. (a) Schematic molecules which can form self assembly monolayer (SAM) onto SiO$_2$ substrates. (b) Comparison on the MoS$_2$ mobility modified by different surfacial chemical groups present at the SiO$_2$ dielectric after SAM modification. Panels (a) and (b) are reproduced with permission from ref. 196, copyright 2014, American Chemical Society. (c) and (d) show the calculated molecular reaction and layout before and after sulfur vacancy healing. (e) and (f) are the corresponding high-resolution TEM images for (c) and (d) to evaluate the effect of vacancy healing. (g) Comparison of room-temperature conductivity of samples under different heling conditions. Black: pristine, blue: one-sided vacancy healing, red: double-sided vacancy healing. (h) Temperature dependence of mobility for corresponding samples shown in (g). Panels (c)–(h) are reproduced with permission from ref. 222, copyright 2014, Nature Publishing Group.

5.5　state-of-the-art performance

We have showed that the optimization of an individual aspect leads to improved mobility. The highest device performance is attained when multiple schemes are employed. Very recently, Hone *et al.* carefully tackled both the issues of interfacial impurity and channel/electrode contact with a combined 'hBN encapsulation + graphene contact' scheme, as shown in Fig. 18. A superclean interfacial condition is achieved by using a dry transfer method where the MoS$_2$ channel is encapsulated by high-quality vdW hBN dielectrics that act as excellent channel isolator to external Coulomb impurity sources. Furthermore, graphene is used as the contact to channels, which reduces contact considerably. Hall geometry is adopted in the characterization to further eliminate contact issue. With the delicate experimental design, they observed a record high low temperature (<5 K) mobility from 1000 to 34000 cm^{2}V^{-1}s^{-1} for 1L–6L MoS$_2$.[223] A high room temperature mobility from 45 to 120 cm^{2}V^{-1}s^{-1} is also achieved. They conclude that the interfacial scattering centers, including both long-range Coulomb impurities and short-range defects are the limiting scattering mechanisms in the high-quality 2D samples, rather than the scattering centers within the bulk. A ultralow interfacial impurity density of 6×10^9 cm^{-2} is fitted for their superclean samples.

While the above results are extracted from the four-terminal measurement, Duan *et al.* recently confirmed the presence of high performance in the two-terminal measurement, *i.e.* in the practical FET device configuration, with the similar 'hBN encapsulation + graphene contact' scheme. They reported a record high RT mobility of ~100 cm^{2}V^{-1}s^{-1} and low-T mobility of >300 cm^{2}V^{-1}s^{-1} in hBN sandwiched monolayer MoS$_2$.[282] Impressively, extremely high low-temperature two-terminal field-effect mobility of 1300 cm^{2}V^{-1}s^{-1} was observed in multilayer samples.

So far, the highest room temperature mobility has been achieved in 1L MX$_2$ chalcogenides is in WSe$_2$ with a value of 250 cm^{2}V^{-1}s^{-1}. In this case, synergetic engineering on contact optimization by NO$_2$ doping and channel encapsulation by ZrO$_2$ top dielectric was employed. To gain a quick on the state-of-the-art carrier mobility results achieved to date, Table 6 summarizes the works with notably high mobility. Apparently, multiple schemes of mobility engineering are used for most of them, pointing out a clear direction for performance optimization and device design.

6　Experimental traps and standards

Modern sciences are highly developed and involve interdisciplinary research activities. As for the research field of 2D vdW

crystals, numerous chemists, physicists and materials scientists participated into this extremely active subject and stimulated inspirations. However, the lack of solid training on a specific field tends to cause low-level mistakes. Here we would like to point out some apparent 'traps' and emphasize some basic experimental standards one should follow.
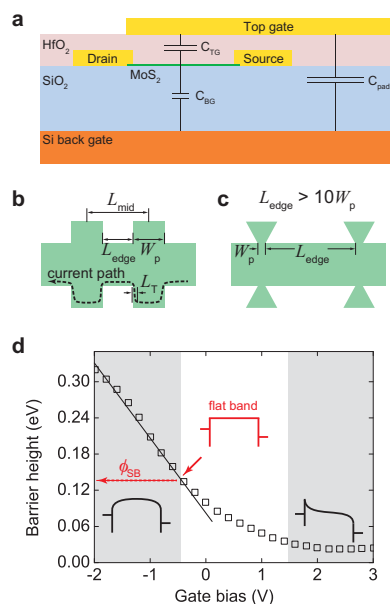
Fig. 19 (a) Layout of capacitance distribution in a dual-gate FET. Reproduced with permission from ref. 126, copyright 2013, Nature Publishing Group. (b) A typical four-terminal geometry with a comparable edge distance (L_{edge}) to the width of voltage probe (W_p), which may cause large overestimation in mobility due to the current crowding effect in the inner voltage probes. (c) A standard four-wire geometry in which $L_{edge} > 10\, W_p$ such that measurement error can be controlled less than 10%. (d) Extraction barrier height ϕ_{SB} at the flat band condition. Reproduced with permission from ref. 181, copyright 2013, American Chemical Society.

6.1 Mobility overestimation in dual-gated structure

A common trap in early time is the mobility overestimation in a dual-gated FET structure, pointed out by Fuhrer and Hone.[126] Figure 19a illustrates the layout of capacitance for a dual-gated FET geometry. The capacitive coupling between the back and top gates through the large measurement pads of the top gate can lead to a significant deviation of the back-gate capacitance from its nominal parallel-plate value. In a typical device with a thin (few tens nm) high-κ top-gate dielectric, 300 nm bottom gate dielectric, and $\sim(100\,\mu\text{m})^2$ measurement pads, $C_{pad} \gg C_{TG} \gg C_{BG}$. If the device is characterized by sweeping the back gate with floating the top-gate electrode, then the effective back-gate capacitance $C = C_{BG} + (C_{TG}^{-1} + C_{pad}^{-1})^{-1} \approx C_{TG}$. Neglecting this coupling would lead to a mobility overestimation by a factor around C_{TG}/C_{BG}. This hidden trap has led to mobility overestimation in several early reports.[81,106,181,293] As suggested by Fuhrer and Hone,[126] the correct measurement method for the dual-gated FET structure is to sweep one gate while grounding the other one such that removing the capacitive coupling effect.

6.2 Four-terminal measurement

It is often to adopt the four-terminal geometry in electronic characterization to rule out the contact issue, which may also produce experimental artifacts in some cases. The size of the exfoliated 2D vdW flakes is typically small, which often restricts one to define a long enough distance between the inner voltage collection probes. Figure 19b shows a typical four-terminal layout used in experiment with comparable probe width and probe distance, which would cause large experimental error. Normally one defines the channel length by calculating the distance between the midpoints (L_{mid}) rather than between the near edges (L_{edge}) of the voltage probes. As will be seen, (L_{edge}) is slightly shorter but more close to the realistic channel length in most cases. Large mobility overestimation ($\sim$2 folds) would arise if the probe width (W_p) is comparable to L_{edge}, as shown in Fig. 18b.[193,223]

Taking into account the current crowding effect discussed in section 4.1.2, the real channel length should be $L_{edge} + 2L_T$, where L_T is the transfer length. L_T is typically in range of about 20–600 nm (dependent on channel thickness and gate bias) for the Au or Ti contacted MoS$_2$ MoS$_2$[179,232] and it is expected to be much smaller if considering the smaller ρ_c for the graphene/MoS$_2$ contacts.[223] Since $L_T < L_{edge}$, a more accurate channel length should be L_{edge} rather than the normally used L_{mid} ($\sim$2 L_{edge} if $W_p \sim L_{edge}$). In a standard four-terminal measurement, the ratio of L_{edge} to W_p should be greater than 10 to guarantee an experimental error within 10%, as shown in Figs. 19c and 6a.

6.3 Barrier height extraction by thermionic emission

It is frequent to estimate the contact barrier height by using the thermionic emission theory

$$I_{DS} = AT^2 \exp\left(\frac{q\phi_{SB}}{k_B T}\right)\left(1 - \exp\left(\frac{qV_{DS}}{k_B T}\right)\right), \qquad (16)$$

which enables an Arrhenius plot $\ln I_{DS} = \ln(AT^2) + q(\phi_{SB} - V_{DS})/(k_B T)$ to extract the barrier height at large V_{DS}. For the two-terminal FETs, the basic assumptions which validate the use of the Arrhenius plot to extract barrier height are: 1) contact dominates the overall device current; and 2) Thermally assisted tunneling current is negligible. The verification of the two assumptions has been neglected in a large number of reports. For instance, the derivation of a negative barrier height of -5.7 meV at the permalloy/MoS$_2$ contacts contradicts the first assumption and thus is unreliable.[184] It is well known that the barrier is effective for carrier blocking only when it is higher than $3k_BT$. If the extracted barrier height is smaller than $3k_BT$, $\sim$ 80 meV at RT, one has to consider the validity of the original assumptions.

It has been shown that for general long-channel MX$_2$ devices the contact resistance comprises 10–20% of the total resistance,[179] indicating the inapplicability to apply this method in most devices. To make the first assumption valid, one has to use an ultrashort channel (e.g. 50 nm long) such that the contact resistance exceeds the channel resistance. Another way to avoid the first assumption is to directly use the net contact results extracted from the four-terminal[223,294] or transfer-line measurement[229] (Fig. 8a).

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In addition, the current injection is controlled by two components: thermionic and tunneling. The ratio between them varies with the carrier density (*i.e.* gate bias). At high carrier density, the channel current actually comprises a high ratio of the tunneling current, which would lead to underestimation of barrier height by using the Arrhenius plot. One may also notice that the extracted barrier value highly depends on gate bias, a signature of the involvement of tunneling current (since it is gate-bias dependent). In this sense, the extracted barrier value at the high current regime can at most be viewed as an effective parameter.

In order to suppress the tunneling component, one has to tune the device to the flat band condition. Figure 19d shows the extracted harrier height versus gate bias. Apparently, the presence of tunneling current results in underestimation of the barrier height. As suggested by Appenzeller *et al.*,[181] a more accurate way is to plot the effective barrier height versus gate voltage and extract the turning point between the sublinear and linear regime. The value at the turning point can be more reliably adopted as the barrier height than those extracted in the conventional way.

7   Summary and outlook

The last few years have witnessed the significant progress on the electronic performance of 2D vdW semiconductors. With fundamental understanding in the transport physics and developing delicate mobility engineering strategies, their room temperature mobility increases rapidly from few to few hundred $cm^2V^{-1}s^{-1}$. While most mobility engineering efforts are devoted to device fabrication that rely on physical methods (*i.e.*, thermal annealing, energy level matching, hBN encapsulation, graphene contact), the chemical strategies concerning interfacial and molecular engineering remains highly unexplored.

Interface modification by growing self-assembled monolayers (SAMs) on dielectric supports[196,222] is a very promising method to create structurally well-defined surfaces with controlled chemical and physical properties like composition, surface energy, hydrophobicity, etc. The use of silane chemistry allows to chemisorb alkyl substituted molecules on SiO_2 or other oxide dielectrics and to have an atomically smooth SAMs surfaces as *ad-hoc* support for the 2D channels in the interelectrodic channel, which is expected to minimize the density of interfacial impurities and thus the extrinsic impurity scattering. Besides, by virtue of the molecular design and engineering, more advanced functional molecules and convenient defect healing techniques are to be exploited, in order to repair the high-density chalcogen vacancies in the channels. The importance of molecular engineering is also reflected by the requirement for degenerate doping at contact area. A long-term stable doping onto the ultrathin channels is the key for realizing practical high-performance devices. In the framework of holistic mobility engineering strategies, we expect that the electronic performance of the 2D vdW semiconductors will be further propelled to the level of their intrinsic behavior. In the regards, the molecular and interfacial chemistry is a key direction to be exploited for realizing the atomic electronics.

We then remark on the potential of 2D chalcogenides in the atomic electronics in terms of the electronic performance. In deeply downscaled bulk silicon FETs, the channels are heavily doped to reduce the depletion length and thus the channel mobility degrades accordingly due to the scattering from high-density dopants insides. The hole and electron mobility is only about $200–300\,cm^2V^{-1}s^{-1}$.[295] In FETs made of ultrathin 2D channels, they operate in a fully depleted mode and only lightly doping is required. No considerable mobility degradation is expected to occur. From the point view of engineering, any 2D semiconductors could be electronically favorable in constructing FETs if the mobility is higher than or approaches the value of heavily doped silicon FETs. Recently a high hole mobility of $250\,cm^2V^{-1}s^{-1}$ has been reached in monolayer WSe_2 at room temperature,[280] indicating that the 2D semiconductors are electronically promising for next-generation microelectronics.

Apart from the applications in integrated circuits, the constant improvement on mobility would also benefit the 2D vdW semiconductors for other applications where the thickness of monolayer is not necessarily required, such as for the radio frequency circuits and the driving FET arrays in flat-panel displays.[130] For instance, from multilayer MoS_2 flakes it is easy to achieve a high mobility of $100\,cm^2V^{-1}s^{-1}$ that is generally higher than the prevailing amorphous silicon, InGaZnO,[296–299] and actively developed organic materials.

Furthermore, the elevated electronic performance would be favorable for broad potential applications in optoelectronics such as monolayer light emitting diodes, photodetectors and gas sensors. In general, higher mobility would allow for higher operating current and device performance. In particular if molecules with self-assembly ability on the vdW semiconductors can be developed, novel superlattices with periodic molecule/vdW material structure and designed functions would be possible. In this sense, the mobility engineering can extend the application fields of the 2D vdW semiconductors. With constant mobility and molecular engineering, we believe that the 2D vdW would generate numerous novel applications in near future.

In conclusion, we reviewed recent progress on the charge transport properties of FETs based on 2D chalcogenide semiconductors, in particular by unraveling the role of thickness on their carrier mobility. We discussed the physical origins and strategies devised for mobility engineering, with the ultimate goal of developing device with performance beyond the state-of-the-art. Specifically, various Coulomb impurities including gaseous adsorbates, dangling bonds/chemical groups of dielectric and other surficial residues are the main scattering centers. Contact quality also plays a role as crucial as Coulomb impurities that affects mobility. Besides, vacancy healing could be used as an additional strategy to further improve device performance when both the contact and interface surroundings are optimized. The synergistic improvement of fundamental physico-chemical properties of 2D chalcogenides (chemical composition, spatial distribution and nature of structural and electronic defects, etc) and their interfacing with chemically optimized dielectric supports and functionalized electrodes (to suppress scattering centers, to tailor their environment, and to optimize contact resistance via lowering injection barrier), is the best solution to improves carrier mobility. We conclude that all the above adverse transport factors have to be optimized or suppressed in order to achieve technologically vi-

able atomically thin body FETs and other novel (opto)electronic devices. The review sheds an in-depth light onto the charge transport behavior of the 2D semiconductors and would guide future performance optimization and device design.

Acknowledgments

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