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A Study of Interfacial Resistive Switching Mechanism by Proton Exchange Reactions on SiO_x layer

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Fei Zhou,[a] Yao-Feng Chang,[a] Ying-Chen Chen,[a] Xiaohan Wu, [a] Ye Zhang,[a] Burt Fowler[a] and Jack C. Lee [a]

In this work, we investigated SiO_x–based interfacial resistive switching in planar metal-insulator-metal structures using physical/chemical/electrical analyses. This work helps clarify the interfacial reaction process and mechanism in SiO_x, and also shows the potential for high temperature operation in future nonvolatile memory applications.

Scaling down the size of conventional memory devices becomes increasingly difficult as physical limits are approached.[1] New resistive switching materials and devices (resistive random access memory, RRAM) are attractive candidates for nonvolatile memories due to their 3D integration structure, excellent scalability and reduced power consumption during memory operations. Transition metal oxides including TiO_2, NiO_x, Ta_2O_5, and organic materials have been investigated and show excellent resistive switching performance.[1-6] Recent studies report that resistive memories can be built solely from the suboxide of SiO_2, a well-studied material that has long been used in semiconductor technology.[7] Recently, Yao *et al.* have reported SiO_x-based resistive switching in vacuum, indicating that this traditionally passive material can be converted to an active memory element controlled by external electrical activation.[8] Robust nonvolatile memory properties of SiO_x RRAM have been reported, including high on/off ratio (~10^5), fast switching (~100ns) and good endurance (~10^4 write-erase cycles).[9,10] These characteristics and good compatibility with the existing metal-oxide-semiconductor (MOS) manufacturing process make SiO_x a very promising resistive switching material for RRAM applications.[1-6] SiO_x-based RRAM was previously characterized using vertically-stacked structures over a temperature range from 220K to room temperature.[11] However, similar data for planar device structures at high temperature are missing in the literature, and additional physical, chemical and electrical analyses are required to confirm the resistive switching mechanism. Specifically, the only high temperature measurement reported was related to the retention characteristics, where devices were not resistively switched.[12] Interfacial surface analytics and high temperature (180°C) switching characteristics are crucial in understanding both switching mechanisms and possible device degradation. Note that one of the difficulties to conduct such high temperature measurements is that SiO_x RRAM switching requires an oxygen-free ambient,[13] where even trace amounts of oxygen disables the switching operation. Such oxygen-free ambient is often achieved using a vacuum chamber, which has a working temperature upper limit of only 100°C. Because nitrogen is an inactive gas, we used nitrogen ambient to achieve the oxygen free environment instead of vacuum. It was previously demonstrated that nitrogen has little effect on switching characteristics of SiO_x RRAM.[13] In this work, we built a high temperature test platform based on a probe station with nitrogen purging capability to ensure the necessary oxygen-free ambient for device switching. Our characterization of SiO_x RRAM at high temperature indicates excellent performance under elevated temperatures up to 180°C. The results demonstrate that switching reactions in SiO_x are maintained at high temperature without any dramatic reliability issues. The results also help clarify that the initiation of switching events are consistent with electron tunneling mechanisms.

The fabrication process is similar to the MOS structure device.[9-13] It starts with BOE cleaning of undoped p-type silicon wafer, followed by deposition of SiO_x layer using evaporation. The major difference lies in the formation of top electrodes and the device structure. Then E-beam lithography and Lift Off Resist (LOR) were used to form top electrodes by lifting off a 100nm thick Chromium (Cr) layer. The Cr layer was deposited using e-beam evaporation. The electrodes are designed to consist of two 100μm×100μm contact pad for probe contacts, a narrow connection region of 1um width and a gap region of varying gap distance from 40nm to 70nm. The top view and side view of the Cr electrodes are shown in Figure 1 (a). After the fabrication,

[a] *Microelectronics Research Center, Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, Texas 78758 USA.*
† F. Zhou and Y. F. Chang contributed equally to this work.

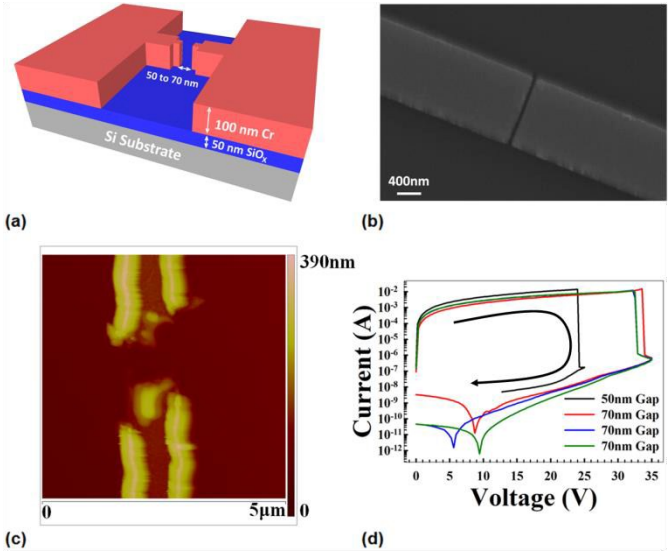

Figure 1. (a) Tilted view structure of planar SiO_x based RRAM device. (b) SEM image (top view) of as-fabricated planar device at gap region. (c) AFM image (top view) of planar device at gap region. (d) Pre-Forming I-V curves showing electric induced Joule heating breakdown behavior. Arrows indicate voltage sweep directions.

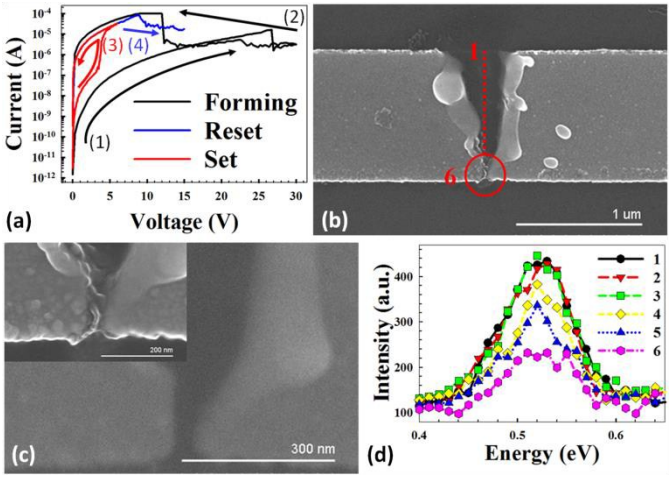

Figure 2. (a) Forming ((1), (2)), Set (3) and Reset (4) I-V curve for planar device. Arrows indicate voltage sweep directions. (b) Top view SEM image of the gap region between two adjacent Cr electrodes on a formed planar SiO_x based RRAM device. EDS probe sites #1-6 locations shown and labeled. (c) Magnifying red circle region in (a) by bright field (inset) and dark find images. (d) Intensity of X-ray signals around oxygen Kα energy level (0.525eV) for different probe sites.

Scanning Electron Microscopy (JEOL S-5500 STEM) and Atomic Force Microscope (AFM) images were obtained on as-fabricated devices and on devices after electroforming, respectively. The gap region between the Cr electrodes and the gap region after electroforming are shown in SEM and AFM images (both top view) in Figure 1 (b) and Figure 1 (c). Lake Shore Cryotronics vacuum probe chamber and Agilent B1500A device analyzer were used to electroform devices and measure the DC I-V response in vacuum (< 1 mTorr). After electroforming, all RRAM devices were switched 50 cycles between a High Resistance State (HRS) and Low Resistance State (LRS) to ensure selection of a device with robust switching performance and to make sure that any observed degradation of resistive switching (RS) characteristics under elevated temperature were not due to inadequate electroforming. "Set Voltage" is defined as the voltage where the transition from HRS to LRS occurs in the *I-V* curve. For planar metal-insulator-metal devices, the transition from LRS to HRS is not an abrupt current level change. Therefore, "Reset Voltage" is defined as the voltage where the current reaches the maximum value. The definitions of "LRS Current" and "HRS Current" are the measured current at 1 V bias for each state.

With this device design, the two electrodes are effectively placed on the surface of SiO_x layer with a spacing of 40nm to 70nm. The probe electrode area (length × width) is 100μm×100μm; middle extended electrode area is 10μm×10μm; gap electrode area is 10μm×1μm (Figure 1 (a)). During the measurement, one of the electrodes was biased with positive voltage and the other is grounded. Such a configuration limits the electroforming/resistive switching region to the gap between the adjacent electrodes. However, the measured data shows that most of the two adjacent electrodes are actually not electrically isolated. This was attributed to the two adjacent Cr electrodes contacting each other due to imperfect lift off at the gap region between the Cr electrodes. As a result, very high voltage double sweeps (0 V to 35 V and back to 0 V) were needed to induce localized Joule heating at the contact point and cause the breakdown of the Cr connections between the two electrodes. *I-V* plots of Pre-Forming process for planar devices with varying Cr electrode spacing are shown in Figure 1 (d), in which the burn-off process can be observed. The conduction current between the two adjacent Cr electrodes was initially following an Ohmic conduction behavior and suddenly decreased from mA level down to μA level at ~ 30 V. After the Cr burn-off, the planar devices were electroformed using a double sweep method. Unlike the electroforming procedure described in our previous reports,[9-13] where consecutive voltage single sweeps were used, the electroforming procedure used here was to apply only one voltage double sweep to electroform the device. As shown in Figure 2 (a) (black curve), a forward/reverse voltage sweep from 0 to 30 V is applied to electroform the planar device. During the forward sweep (0 V to 30 V), the current abruptly decreased at 27 V, and then began to fluctuate near the 10^{-6} A level. Such abrupt change marked the beginning of the electroforming process. During the reverse sweep (30 V to 0 V), the current initially fluctuated near the 10^{-6} A level, then increased to 10^{-4} A, indicating the completion of the electroforming process. This increase of conduction current/decrease of resistance during the reverse sweep of voltage is unique to SiO_x based RRAM, and is called the "Backward Scan Effect".[14] The forming voltage can be reduced by D_2 annealing and SiOx composition modulation by Plasma-enhanced chemical vapor deposition (PECVD) process.[15] In Figure 2 (a), resistive switching characteristics are also shown, Set process in red and Reset process in blue.

Following electroforming of the planar device, scanning electron microscopy (JEOL S-5500 STEM) was performed and shows the top-down view of a "burn-off" planar device

structure (Figure 2 (b)). From top-view SEM image, it was observed that the gap region between adjacent Cr electrodes, shown as red circle in Figure 2 (b) and inset of Figure 2 (c), and also, by examining the dark field image, the gap region can be clearly identified (about 30nm) due to the compositional difference (Cr and SiO_x), as shown in Figure 2 (c). Energy Dispersive X-ray Spectroscopy (EDS) was performed at the gap regions of electroformed planar devices, following the direction and sequences indicated in Figure 2 (b), as shown in Figure 2 (d). The EDS equipment used in this work was JEOL S-5500 STEM, with 25 keV accelerating voltage. The oxygen characteristic peak at 0.525eV (Kα) was chosen to qualitatively estimate the amount of oxygen atoms at different locations of the gap region.[15] For the case of EDS data collected on electroformed device, as the probe site scans though the gap region, a localized probe site with significantly lowered X-ray intensity was identified (20~40% lower intensity compared with as-fabricated regions outside of metal line, confirmed by three devices). This contrast of intensity trend suggests that the forming process of planar SiO_x based RRAM device is related to localized deficiency of oxygen atoms.

A Cascade Femto Guard probe station with temperature controlled by a Textronix 110 controller was used as the high temperature measurement platform. The electroformed samples were first placed on the probe station chuck; then the probe station chamber was purged with nitrogen continuously throughout the measurements. Once an oxygen-free ambient is achieved, a HP4156B semiconductor parameter analyzer controlled by Labview software was used to measure DC I-V response at the following temperatures, 20°C, 60°C, 100°C, 140°C, and 180°C. For each temperature condition, a dwelling time of 5mins was used so that the indicated temperature reflected the true device temperature. DC I-V data for each temperature condition were collected in both progressive and retrogressive ways (e.g. from 20°C to 180°C and back to 20°C) so that any degradation effects due to accumulated thermal stress are averaged-out. Device performance and resistive switching parameters were extracted for all samples to capture the high temperature RS characteristics of SiO_x-based RRAMs. In order to reduce high temperature voltage stress on the switching dielectric layer, the maximum DC voltage applied to switch devices was intentionally reduced from 8V (used for device cycling in vacuum at room temperature) to 5V when in 1 atmosphere nitrogen and at high temperature. Therefore the HRS was achieved using a DC voltage sweep from 0V to 5V, whereas a DC voltage sweep from 0V to 3.5V was used for LRS. After each Set and Reset operation, DC I-V characteristics of LRS and HRS were measured, respectively. It is observed that SiO_x based RRAM is able to perform resistive switching operation even at 180°C while maintaining a LRS/HRS ratio > 1 order of magnitude (read at 1V). This demonstrates that the defects responsible for RS are thermally stable throughout the measured temperature range.

Previous reports on SiO_x based RRAM hypothesized a thermal induced filament rupture process as the switching mechanism

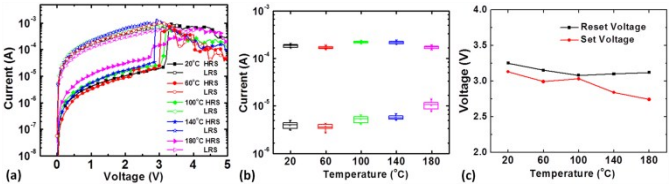

Figure 3. (a) I-V plots for SiOx–based RRAM device in both HRS and LRS switching at 20°C, 60°C, 100°C, 140°C and 180°C. (b) Effects of temperature on HRS and LRS current of SiO_x RRAM device. (c) Effects of temperature on Set Voltage and Reset Voltage of SiO_x RRAM device.

for the device Reset operation.[16] Such an explanation is intuitively plausible for two reasons. Firstly, the unique unipolar behavior of SiO_x based RRAM where the Set voltage is smaller than or equal to the Reset voltage suggests that the Reset operation is associated with higher thermal energy. Secondly, many resistive switching materials such as Ag, Cu and Al_2O_3 exhibit similar "Joule Heating" Reset behavior.[17] However, the high temperature RS data challenge this hypothesis. The thermal induced rupture hypothesis predicts that the thermal energy required to rupture the filament would decrease as ambient temperature increases, therefore the corresponding Reset voltage would also decrease. But such a trend is not observed in the RS characteristics of measured devices (Figure 3 (a)); the measurement results suggest that a heat-induced Reset mechanism may not be an accurate model for SiO_x RRAM. Key switching parameters such as HRS/LRS current, and Set/Reset voltage were plotted versus temperature in Figure 3 (b) and (c). Two high temperature effects were observed. First, as the temperature increased, the HRS currents steadily increased while the LRS currents stayed about the same, and the On/Off ratio consequentially decreased. Second effect of high temperature was the steady decrease of Set voltage as the temperature increased, while the Reset voltage stayed about the same.

We believe both phenomenon arise directly from the physical defects involved in charge transport and device switching. Within the framework of our working hypothesis of device operation, defects within the switching region of the filament transform between two defect types: a hydrogen bridge defect (Si-H-Si), known as an electrically-conductive defect; and a hydrogen doublet defect (H-SiSi-H or 2Si-H), a non-conductive defect. Transformations between these two defect types only requires the addition or removal of a single hydrogen atom. It is well known that water molecules in weak ionic media will "uptake" a free proton to form H_3O^+.[15,16] Then, when the local charge environment becomes negative, the H_3O^+ will release the proton for reaction with the negative charge, making water the logical choice for a defect that will store and release a proton to accommodate the defect transformations. In this hypothesis, the H_3O^+ and Si-H-Si defects are present when the defect pair is conductive, and H_2O and H-SiSi-H are present when the defect pair is nonconductive. It may be noted that the H_2O molecule readily reacts with the SiO_2 network to form the stable 2Si-OH defect. The total number of these defect pairs within the filament's switching region is determined during

electroforming, and should stay about constant during switching. A LRS occurs when most of the defect pairs in the switching region transform into the H_3O^+/Si-H-Si configuration, whereas most defects transform to H_2O/2SiH when programed to the HRS. As Reset voltage increases, a larger percentage of the defects are converted to nonconductive H_2O/2SiH and the HRS current decreases by orders of magnitude as compared to LRS current. This effect is known as Reset stop voltage effect, as discussed thoroughly in a previous report.[13]

The high temperature effects shown in Figure 3 can be explained using our SiO_x resistive switching model. As described in a previous report,[18] the Set transformation from hydrogen doublet to hydrogen bridge (HRS to LRS) is modelled as being initiated by trap-assisted tunneling (TAT) through 2Si-H defects. The threshold voltage for TAT depends on the energy level difference between occupied and unoccupied states of 2Si-H, which is ~ 2.4 eV,[15,16] in good agreement with the previously-measured minimum Set transition of 2.45 V.[19] As TAT current through the 2Si-H defect increases to above some threshold, a hydrogen atom is desorbed (as a proton) from one of the Si-H groups to form Si-H-Si. The released proton then reacts with H_2O to form the H_3O^+/Si-H-Si complex. At elevated temperature, the effective tunneling distance is reduced and phonon-assisted tunneling current such as TAT increases. Therefore, less potential energy in the form of applied bias will be needed to induce the Set transition. As a result, the Set voltage is expected to decrease as temperature increases, as observed in Figure 3 (c).

On the other hand, the Reset mechanism is modelled as being initiated by a Fowler-Nordheim (FN) tunneling event,[14] where electrons tunnel from hydrogen bridge defects into H_3O^+ defects. The H_3O^+ defect is expected to have an energy level very near the SiO_2 conduction band, which is approximately 2.5 eV above the hydrogen bridge conduction band.[15] Therefore, a bias voltage of at least 2.5 V must be applied before FN tunnelling occurs. When an electron tunnels into the H_3O^+ defect, a proton is released and becomes available to react electrochemically with a negative-charged bridge defect in a well-understood exothermic reaction that releases ~ 3 eV.[15] The result is transformation to the H_2O/2Si-H complex. As Reset voltage continues to increase, more FN electrons can tunnel into H_3O^+ defects to drive the Reset transformation, thus providing a natural explanation for the stop voltage effect.[13] Since FN tunnelling has no strong temperature dependence, the Reset voltage is not expected to depend on temperature. As shown in Figure 3 (c), the Reset voltage stays about the same as temperature increases from 20°C to 180°C.

Some potential problems for operating SiO_x RRAM at elevated temperatures include smaller on/off ratio and potential misreads due to HRS current increase. But higher temperature also reduces energy consumption by decreasing Set voltage, which may further allow reduction of stop voltage, depending on the on/off ratio required by the sensing circuit. In this work, a stop voltage of 5V was used to maintain an on/off ratio of at least 1 order. Despite these potential issues, this paper shows the potential for use of SiO_x RRAM in extreme environments. It may be noted that very few material systems have demonstrated reproducible resistive switching at 180°C.[20]

In conclusion, SiO_x RRAM was fabricated in a planar structure, with EDS analysis suggesting that electroforming and resistive switching in SiO_x is related to localized oxygen deficiency. Robust resistive switching was achieved for temperatures as high as 180°C, showing the potential for use of SiO_x RRAM in high temperature applications. Reset characteristics at high temperature help rule-out a Reset mechanism based on Joule heating. Temperature effects were observed that HRS current increases and Set voltage decreases as the temperature increases. This is believed to be an intrinsic characteristics of SiO_x RRAM switching elements, namely hydrogen doublet and hydrogen bridge defects. The phenomenon can be explained by a thermally assisted tunneling mechanism which transforms more hydrogen doublet defects to hydrogen bridge defects at elevated temperature.

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