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**A low-temperature formation path toward high efficiency Se-free
 $\text{Cu}_2\text{ZnSnS}_4$ solar cells fabricated through sputtering and sulfurization**

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Abstract

A novel low temperature $\text{Cu}_2\text{ZnSnS}_4$ (CZTS) formation path using co-sputtered SnS_2 -ZnS-Cu precursors was employed for CZTS solar cell fabrication, which led to cell with power conversion efficiency of 8.58%, a big step forward from the previous record 6.77% reported by Katagiri *et al.* for this kind of solar cell. This method consists of a low-temperature annealing stage for CZTS phase formation followed by a short high-temperature annealing stage for grain growth and secondary phase removal. The employment of SnS_2 as a precursor makes CZTS phase can readily form at low temperature when SnS_2 has not dramatically decomposed into volatile SnS. The two stage process wisely separates the phase formation and crystal coalescence, which makes the fabrication of CZTS film be more controllable. Furthermore, the demonstration of the low temperature formation path provides new opportunities to fabricate high efficiency, cost-effective and environmental friendly CZTS solar cells on low weight and flexible substrates such as polyimide.

Keywords: CZTS, co-sputtering, low temperature formation, X-ray diffraction

1. Introduction

Kesterite $\text{Cu}_2\text{ZnSnS}_4$ (CZTS) thin film solar cells have attracted considerable interests in the last decade¹⁻³ and have shown potential to replace its well-developed predecessor $\text{Cu}(\text{In,Ga})\text{Se}_2$ solar cell with earth-abundant and environmentally friendly raw materials. Many fabrication processes have been developed for CZTS solar cells, including vacuum processes such as co-evaporation⁴⁻⁷, sputtering/sulfuration or selenization⁸⁻¹⁴ and non-vacuum processes such as electroplating^{15,16}, sol-gel¹⁷, nanocrystal^{18,19}, spray-printing^{20,21}, and solution-based methods²². Although so far the most successful fabrication process for CZTS solar cells is the hydrazine solution method which leads to a record power conversion efficiency (PCE) of 12.6%²³, it incorporates the element selenium which deviates the optical bandgap from ideal value 1.5 eV^{24,25} and raises cost and abundance concerns. Note that they are usually called $\text{Cu}_2\text{ZnSn}(\text{S,Se})_4$ (CZTSSe) to distinguish from the Se-free CZTS absorbers. Until now, the best performing Se-free CZTS cells were produced by vacuum process. In 2013, Shin *et al* reported a record CZTS device fabricated by co-evaporation with a PCE of 8.4%⁶. And Katagiri *et al* achieved a record cell with a PCE of 6.77% through sputtering/sulfuration in 2008¹³.

In spite of the progresses in CZTS device fabrication techniques, there emerged several challenges that impede the further improvements of device performance. For most reported high-efficiency studies, CZTS was formed at annealing temperatures higher than 500°C^{8-13,26-33}. At such temperatures, SnS becomes volatile and is constantly lost to the environment. This will push the CZTS formation reaction backwards, decomposing CZTS into binary

secondary phases³⁴. Providing high vapor pressure of S₂ and SnS, or increasing the overall chamber pressure by employing excess inert gases could partially solve this problem^{34,35}. However, these methods shift the thermodynamic equilibrium and resulted in unwanted MoS₂ layer. It was supported by theories that the formation of CZTS quaternary phase is energetically favorable at lower temperatures³⁶. Unfortunately, this fact did not receive enough attention since the small crystal size leads to defects that are detrimental to the device performance.

In this work, we present a formation path by combining both low-temperature and high-temperature annealing for co-sputtered SnS₂-ZnS-Cu precursor to address the aforementioned challenges. Although two-stage annealing process was employed in fabricating CIGS or CZTS absorbers previously^{37,38}, the main purpose of the short low temperature annealing is to make metal alloys more mixable or more ready to react into binary compounds. Through our method, as named Low-temperature Formation Path (LTFP), the working mechanism and outcome are totally different from previous reports by using specially designed growth parameters. The formation of quaternary CZTS phase has mainly happened in a limited temperature range (260±10 °C) at which SnS₂ has not dramatically decomposed into volatile SnS while binary compounds in precursor could readily react with each other. The purpose of the following annealing at higher temperature is to increase the crystal size and remove secondary phase like SnS. The annealing temperature is usually set to be higher than 430 °C around which SnS secondary phase starts to vaporize rapidly to leave pure phase CZTS in the thin film. A record PCE of 8.58% for Se-free CZTS solar cell has been achieved, which is a big step forward from the previous record set by Katagiri *et al* also

using co-sputtering/sulfurization process¹³. Overall, the devices fabricated by the new method exhibited more than 20% improvement in average PCE (Figure S1). The characterization results suggested that the formation of CZTS crystallites at relatively low temperature gave rise to more homogenous element distribution, less secondary phase, higher hole concentration and benign defects. Although an annealing temperature of 510 °C is employed for a shorter annealing time in this paper, we believe a temperature not higher than 450 °C is good enough to remove the secondary phase like SnS and get pure phase CZTS with comparable device performance if annealing time is further optimized in the future.

2. Experimental Section

Fabrication of CZTS thin films in this study was performed by sputtering/sulfuration technique as described before¹⁴. The precursors were deposited on Mo-coated 10x10 cm² sized soda lime glass by co-sputtering SnS₂, ZnS and Cu targets. Our precursors were different from that of stacking layers in the form of Cu/SnS₂/ZnS reported by Katagiri's group previously¹³. By using co-sputtering technique, the various elements in our precursors were mixed more homogeneously at nano-scale, which would be beneficial for a faster solid reaction in the annealing process. To fabricate CZTS thin films, these precursors were sulfurized in an atmosphere of N₂+H₂S (5%) vapor with pressure maintained at 300 Torr.

To make devices, a CdS buffer layer of 60 nm thickness was firstly deposited on the CZTS thin film by chemical bath deposition (CBD). A 300 nm thick i-ZnO/ZnO:Al layer prepared by sputtering was then used as the transparent conducting layer. Finally, Ni/Al metal grids were deposited by e-beam evaporation through an aperture mask to form the current collector.

The photo of the finished sample can be found in the supplementary Figure S4. The device performance of the solar cells with a total area around 0.5 cm^2 were measured using simulated AM 1.5 Global spectrum. The illumination intensity of 100 mW/cm^2 was calibrated using a certified silicon solar cell.

Grazing incidence X-ray diffraction measurements were carried out at BL14B1 of Shanghai Synchrotron Radiation Facility, Shanghai and BL23A1 of National Synchrotron Radiation Research Center, Hsinchu. The energy of the X-ray source was set to 10 keV (wavelength of 1.24 \AA) and the incident angle was 3.5° . Raman measurement was carried out using Horiba iHR550 UV-NIR spectrometer. The wavelength of the excitation light is 632.8nm. The cross-sectional morphology and EDS line scan of the thin films were characterized using scanning electron microscope (SEM, A Nova NanoSEM 450) operated at 5kV.

The admittance spectroscopy (AS) was measured using a Tonghui TH2400 LCR Meter. Drive-level capacitance profiling (DLCP) with varying frequencies was used to deduce the free carrier densities in the two devices. Temperature dependent measurements were carried out using a close-cycled cryostat (Advance Research Systems (ARS)) with Lakeshore temperature controller. The temperature was monitored by a calibrated Silicon diode sensor embedded close to the surface of the copper cold finger. In our experiment, the capacitance-frequency (CF) scans were measured in dark from 200 Hz to 2 MHz in the temperature range from 10 K to 300 K and an AC voltage of 50 mV was used with DC bias kept at zero. Before each measurement, the temperature of the sample was maintained for 20 minutes or longer to reach thermal equilibrium.

3. Results and Discussion

3.1 Device performances

Compared with the slow-ramping process widely employed in growing CZTS thin films by sulfurizing precursors prepared by sputtering³⁹ or electro-deposition¹⁶ (Figure 1a, P1), our Low-temperature Formation Process (Figure 1a, P2) replaces the ramping with a low temperature stage (260 °C). Both processes have a high temperature stage (510 °C) for the large CZTS grain growth. The samples were first kept at 260 °C for 75 min before going through a final fast annealing at 510 °C for 15 min. Previous reports have shown that the compositions of CZTS devices with PCE higher than 5% mostly fall into regions around $\text{Cu}/(\text{Zn}+\text{Sn}) \sim 0.8$ and $\text{Zn}/\text{Sn} \sim 1.2$ ^{1, 6, 40-44}. In this paper, the final CZTS absorbers were designed to have compositions of $\text{Cu}/(\text{Zn}+\text{Sn}) \sim 0.73$ and $\text{Zn}/\text{Sn} \sim 1.35$. The slightly larger than usual amount of Zinc content was to empirically improve the open circuit voltage of the device. Figure 1b presents the J-V characteristics under standard AM1.5 illumination of CZTS devices S1 and S2 with absorbers prepared through P1 and P2, respectively. Note here device S2 was capped by an anti-reflection (AR) coating of MgF_2 layer while device S1 was not. As a control, device S1 of a PCE of 6.41% represents the champion cell out of hundreds of devices we fabricated through the annealing profile P1. An anti-reflection layer usually lead to an additional 5% PCE improvement which makes it comparable to Katagiri's 6.77% champion cell fabricated through similar procedure¹³. Device S2 showed a PCE of 8.58% which was the best performing cell out of tens of devices made using the Low-temperature Formation Process P2. Following this strategy, devices with PCE above 8% could be routinely fabricated (Figure S1). These results clearly demonstrated that the Low-temperature

Formation Process was superior to the slow ramping profile in fabricating highly efficiency CZTS solar cells. It also suggested that the sputtering/sulfuration method could fabricate CZTS solar cells as good as or even better than co-evaporation/sulfuration method, which is a good news to future commercialization due to the advantage and maturity of the sputtering technology in scaling up the devices.

The detailed device parameters based on the standard Sites' model ⁴⁵ including open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}), fill factor (FF), series resistance (R_s), shunt resistance (R_{SH}), ideality factor (A), and reverse saturation current density (J_0) were listed in Table I. By comparing the characteristics of the two devices, we could easily find that the increased efficiency mainly came from the improved FF and J_{sc} . The dramatic decrease of the series resistance from $3.85 \Omega\text{cm}^2$ for S1 to $1.2 \Omega\text{cm}^2$ for S2 could well explain the gain in FF . The much smaller reverse saturation current density J_0 and ideality factor A in device S2 strongly indicated that it suffered less defects related recombination in the absorber than that in device S1.

The external quantum efficiency (EQE) curves of the two devices were shown in Figure 1c. For device S2, the EQE approaches 90% in the visible range but slowly decayed in long wavelength range. The loss at long wavelengths in CZTS high efficiency devices was believed to originate from the short carrier diffusion length and/or insufficient charge depletion region in the absorber ⁶. There still exists room for further pushing the PCE by spending more efforts to reduce the loss at long wavelengths. Device S1 resembled the EQE response of device S2 except with an overall lower efficiency in the entire spectral region.

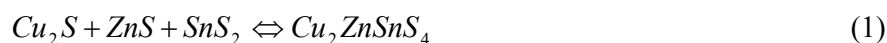
3.2 Absorber characterizations

Grazing incidence X-ray diffraction (GIXRD) measurements^{46, 47} for samples undergoing different stages along the annealing pathway (spots on P2 in Figure 1) were carried out in order to understand the CZTS crystallites formation process. The precursors of the samples were repeated within 5% error of their compositions and went through identical thermal process with different terminating points as indicated on P2 in Figure 1 to represent the absorber conformations at different stages. Intensity integrations of two-dimensional GIXRD patterns of these samples were plotted versus scattering wavevector q in Figure 2a. The diffraction peak located at $q \sim 2.8 \text{ \AA}^{-1}$ corresponds to the Molybdenum (110) reflection. The CZTS diffraction peaks with the most intense (112) peak located at $q \sim 1.97 \text{ \AA}^{-1}$ can be clearly identified as early as stage 1a, confirming the formation of CZTS started at the low-temperature stage. In Figure 2a, diffraction peaks corresponding to SnS rather than SnS₂ were also observed as early as stage 1a, indicating SnS₂ has either decomposed to SnS or reacted to CZTS without forming large enough crystallite phases to be detected by GIXRD.

To further understand the evolution of the CZTS phase, the corresponding (112) peak intensity were extracted and plotted versus the annealing stage in Figure 2b. The peak intensity shows a sharp increase at the beginning of stage 1 and gradually saturate by the end of stage 1, indicating the reaction of CZTS finished within stage 1. This trend is not unique amongst the other reflections (Figure S3), suggesting that the most intense CZTS (112) peak reflects mainly the CZTS instead of ZnS or Cu₂SnS₃ (CTS). It is also evident in the Raman spectrum (Figure 3b). For the SnS phase as shown in Figure 2c, its (111) peak intensity

exhibits an initial increase, followed by a plateau during stage 1 and a dramatic decrease during stage 2. The initial increase of SnS content is most likely due to the decomposition of SnS₂ and the final decrease could be attributed to the high temperature vaporization of SnS.

The above observations indicated our CZTS formation underwent a favorable pathway through this new method. Many studies suggested that there were mainly three possible reactions when annealing SnS₂ related precursors²⁶⁻³²:



The stable SnS composition indicates the formation of a balance between reaction (2) and (3). In other words, it is most likely that SnS₂ has reacted into CZTS phase through either (1) or (2)+(3), except for the initial decomposition during the low temperature stage. This reflects one important advantage of our Low-temperature Formation Process is that the low temperature annealing could significantly lower the decomposition rate of SnS₂ and thereby make route (1) more likely to happen. It also reduces the requirement of external S₂ (or H₂S) vapor to promote reaction (3), which will likely prevent the formation of unwanted thick MoS₂ at Mo electrode. This will consequently improve the element inhomogeneity issue due to the insufficient penetration of S₂ (or H₂S) gas into the precursor, as consistent with the SEM results (Figure 4).

To confirm our hypothesis, Raman spectra⁴⁸ was employed to investigate the phase change of SnS₂ under various temperatures. Figure 3a presents the Raman spectra of pure SnS₂

precursor annealed at different temperatures in a N_2+H_2S (5%) atmosphere for 60 minutes. The as-prepared thin film displayed the characteristic peak of SnS_2 phase at 315 cm^{-1} and the SnS related peaks at 163, 191 and 218 cm^{-1} with comparable intensity. This indicated that significant amount of SnS phase was mixed with SnS_2 in the sputtered film due to sulfur loss induced by the strong sputtering process. When the $Sn-S$ precursor was sulfurized at $240\text{ }^\circ\text{C}$, SnS_2 phase recovered and became the dominant phase with only a small amount of SnS . With the increasing of annealing temperature, the decomposition of SnS_2 into SnS was clearly observed by the drop of SnS_2 Raman peak at 315 cm^{-1} and the accompanied increase of SnS peaks at 163, 191 and 218 cm^{-1} . When the temperature was higher than $330\text{ }^\circ\text{C}$, no trace of SnS_2 was observable by the Raman measurement and only SnS was found to exist in the film. Together, the Raman results for the thermal behavior of SnS_2 confirm the necessity of low-temperature stage to suppress the drastic decomposition of SnS_2 . The Raman spectra of $Cu-ZnS-SnS_2$ precursors annealed at $280\text{ }^\circ\text{C}$, $260\text{ }^\circ\text{C}$ and $240\text{ }^\circ\text{C}$ were plotted in Figure 3b. The film annealed at $280\text{ }^\circ\text{C}$ contains substantial amount of SnS with CZTS phase, whereas the SnS signal is much weaker when the film is annealed at $240\text{ }^\circ\text{C}$ and $260\text{ }^\circ\text{C}$. The spectra of $260\text{ }^\circ\text{C}$ did not show much difference from that of $240\text{ }^\circ\text{C}$ except stronger CZTS characteristic peaks. This shows that at low temperature, SnS_2 react readily to form CZTS without decomposing into SnS . Although the main peak at 338 cm^{-1} may also be attributed to CTS phases (336 cm^{-1}), the clear existence of the other CZTS characteristic peaks at 260 cm^{-1} , 288 cm^{-1} , 366 cm^{-1} and 376 cm^{-1} suggests that the signal comes from the CZTS phases. However, some weak peaks around 305 cm^{-1} and 318 cm^{-1} can also be observed. These are contributed to the ternary compounds, such as Cu_2SnS_3 and Cu_3SnS_4 , which are hard to be completely removed under low temperature.

Figure 4(a) and (b) showed the cross sectional SEM images of the as-cleaved absorbers of device S1 and S2, respectively. The CZTS thin films in the two devices were of about 1000 nm thick. For device S1 (Figure 4(a)), it was clear that the absorber consisted of two regions with a large-grain top layer and a small-grain bottom layer. The small grain layer was about 1/3 of the film thickness. For device S2 (Figure 4(b)), the two-layer feature was less prominent, though smaller grains could still be found in the bottom region. In addition to the difference in grain structure revealed by SEM, Energy-dispersive X-ray spectroscopic (EDS) line scans in Figure 4(c) and (d) demonstrated more dramatic changes in the compositional distribution of the elements across the film thickness. For device S1, the bottom layer adjacent to the Mo back electrode was found to be dominated by Zn elements with a sharp decrease of Cu and Sn density. For device S2, the absorber showed a much homogeneous distribution of the elements except a slightly higher Cu concentration near the top surface. No sign of strong Zn segregation in the bottom layer of the absorber was observed. Small grains in the absorber were generally believed to be deleterious to device performance due to the increased recombination at the grain boundary and/or decreased carrier mobility. Excess ZnS secondary phase aggregated near the CZTS/Mo interface was identified to increase the serial resistance of the solar cells. The observed thick Zn-rich bottom layer in device S1 can well explain its larger serial resistance and thus poorer FF as compared to device S2.

3.3 Defects characterizations

To investigate the possible origin for the enhanced quantum efficiency and J_{sc} in the device made by the Low-temperature Formation Process, capacitance-based admittance spectroscopy

was employed to study the differences in defect physics of the devices fabricated via slow-ramping and Low-temperature Formation Process⁴⁹. By measuring the junction capacitance as a function of frequency at different temperatures, the energy level of defects within the band gap could be extracted. Using the model proposed by the work of Kimerling⁵⁰, the capacitance at high frequency mainly represented the response of free carriers, while the capacitance at low frequency represented the response of the sum of free carriers and deep traps where the traps were not freeze-out. The step transitions in the CF scans could be transformed to a peak feature in the differential capacitance curves as displayed in Figure 5 (a) and (b), from which the inflection frequencies could be easily identified. Plotting the inflection frequency versus temperature in an Arrhenius form allowed the extraction of activation energy E_a which was approximately the average value of the energy difference between defect level and the valance band edge for p-type absorbers. The E_a were determined to be 94 meV and 52 meV for device S1 and S2, respectively. A larger value of E_a was generally an indicator of a slower hole emission rate and thus it was more likely that defects with larger activation energies tended to act as more effective recombination centers⁵¹. Since the theoretically calculated acceptor level is around 20 meV above VBM for Cu vacancy and around 120-150 meV above VBM for Cu_{Zn} antisite, Assuming the activation energy of S1 and S2 are related to the ionization of both defects, device S2 should have more Cu vacancy than device S1, which is known to be benign to the device performance⁵². Figure 5(c) and (d) showed the defect density spectra resulting from the CF scans. The defect distributions derived from the CF curves measured at various temperatures collapsed together, indicating a correct scaling of the energy axis⁵³. The integrated defect (hole trap) density in the absorber of device S2 was $6.7 \times 10^{15} \text{ cm}^{-3}$, lower than the defect density of $1.07 \times 10^{16} \text{ cm}^{-3}$ in the

absorber of device S1. The hole concentration derived from drive-level capacitance profiling (DLCP) measurement, on the other hand, was $2 \times 10^{16} \text{cm}^{-3}$ for S2, higher than that of $1 \times 10^{16} \text{cm}^{-3}$ for S1. The observed much shallower trapping energy, smaller defect density and higher hole concentration for device S2 can well explain its improved device performance, in particular the higher current collection efficiency in terms of its EQE and J_{sc} , confirming our Low-temperature Formation Process is promising in producing high-efficiency CZTS solar cells.

4. Conclusion

In summary, we have developed a novel Low-temperature Formation Process for co-sputtered SnS₂-ZnS-Cu precursor which results in a record CZTS solar cell with 8.58% PCE. Compared with devices fabricated by the conventional slow ramping thermal annealing strategy, CZTS absorbers made by the Low-temperature Formation Process result in more homogeneous elemental distribution across the thickness direction without noticeable ZnS segregation near the CZTS/Mo interface, and thereby smaller serial resistance and larger fill factor. GIXRD and Raman characterization results suggest that the introduction of the low-temperature stage suppresses the drastic decomposition of SnS₂ and effectively promotes its reaction into CZTS phase during the first stage. Furthermore, the admittance spectroscopy results indicates shallower trapping energy, smaller defect density and higher hole concentration are resulted from the Low-temperature Formation Process, which explains the improved quantum efficiency and short circuit current of the devices. Our findings have clearly revealed that sputtering/sulfuration approach with appropriate annealing protocol not only is an attractive

and simple technique but also has the potential to fabricate more efficient CZTS solar cells. As indicated in figure S2, the grain size of thin films annealed at 430 °C is close to that thermally treated at 510 °C. We strongly believe that annealing temperature lower than 450 °C at the second stage can hopefully make CZTS devices with comparable performance if both annealing time and precursor compositions are further optimized in the future.

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Figure Captions:

Figure 1. (a) Temperature profiles for a Low-temperature Formation Process (P2) and a slow ramping annealing process (P1). (b) J–V measurements and (c) the external quantum efficiency (EQE) curves of the CZTS devices S1 and S2 under standard AM1.5 illumination.

Figure 2. (a) GIXRD patterns for samples undergoing different stages along the Low-temperature Formation Process as denoted along P2 in Figure 1a. The reference peaks displayed are CZTS (PDF#26-0575), SnS (PDF#39-0354) and Mo (PDF#42-1120). (b) The intensity of CZTS (112) diffraction peak at different stages. (c) The intensity of Sn (111) diffraction peak at different stages.

Figure 3. Raman spectra of (a) SnS₂ precursors and (b) SnS₂-ZnS-Cu precursors both annealed under H₂S+N₂ atmosphere at various temperatures as labeled.

Figure 4. Cross sectional SEM images of the cleaved absorbers for (a) S1 and (b) S2. The element distribution for S1 and S2 are shown by their EDS line scans across the film thickness in (c) and (d), respectively.

Figure 5. The measured admittance spectra of (a) S1 and (b) S2. The deduced density of states for the carrier traps in the absorbers of S1 and S2 are shown in (c) and (d), respectively.

Tables:

Table I. Device characteristics of the two CZTS solar cells. The diode parameters, series resistance under light (R_S), shunt resistance under light (R_{SH}), ideality factor (A), and reverse saturation current density (J_0) were determined using the Sites' method.

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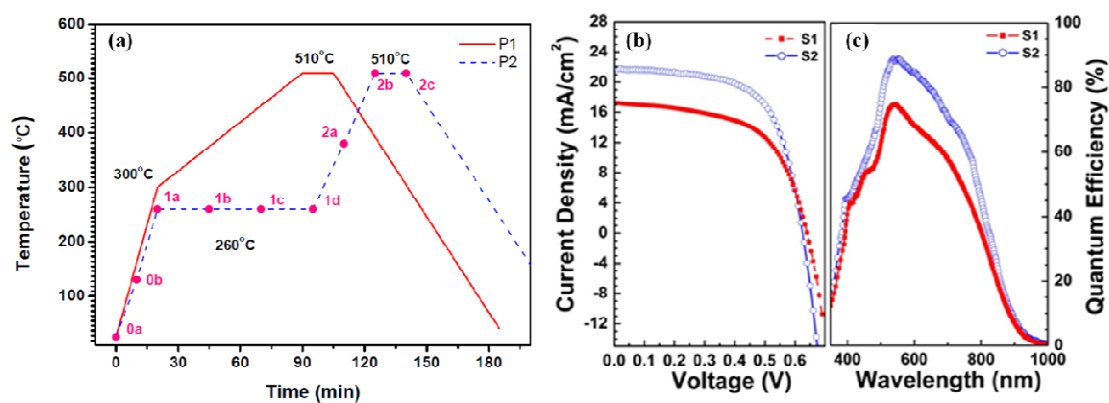


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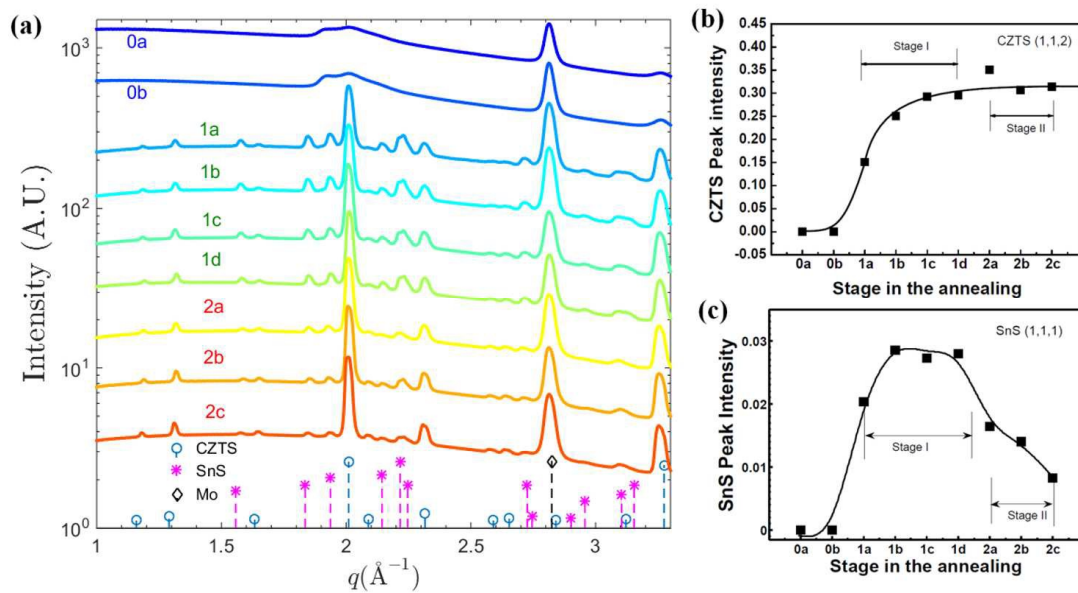


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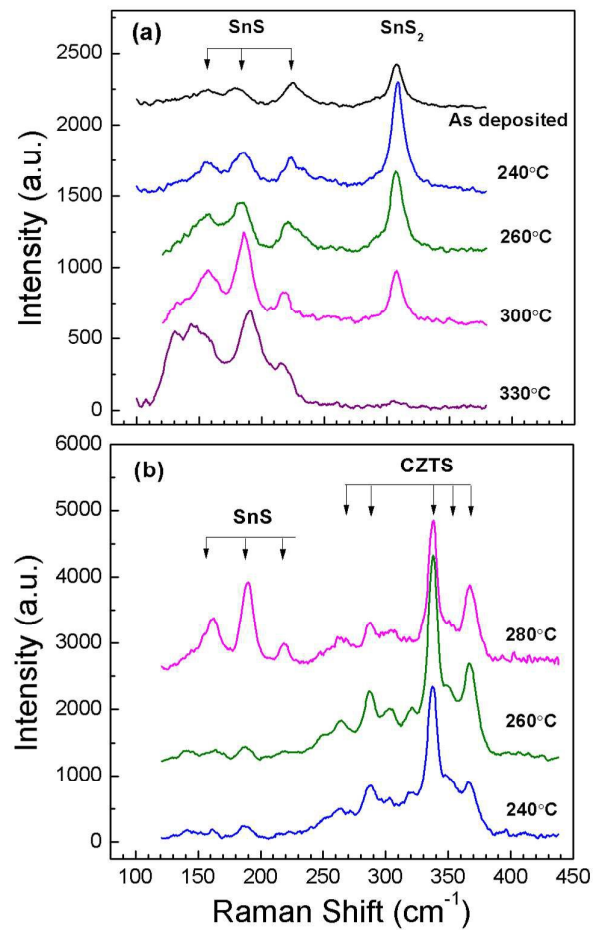


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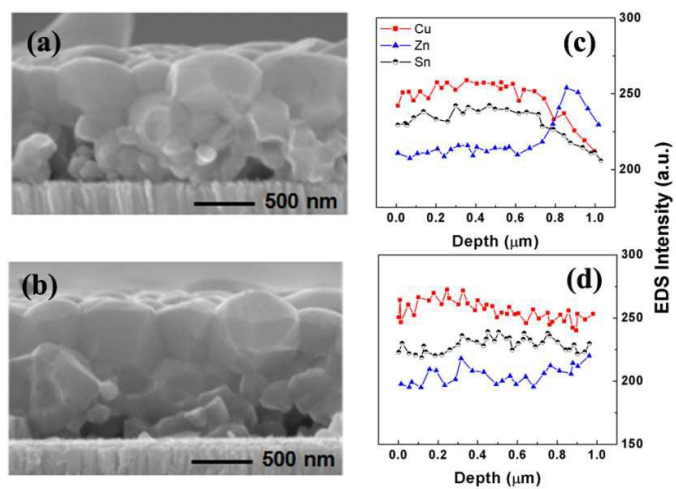


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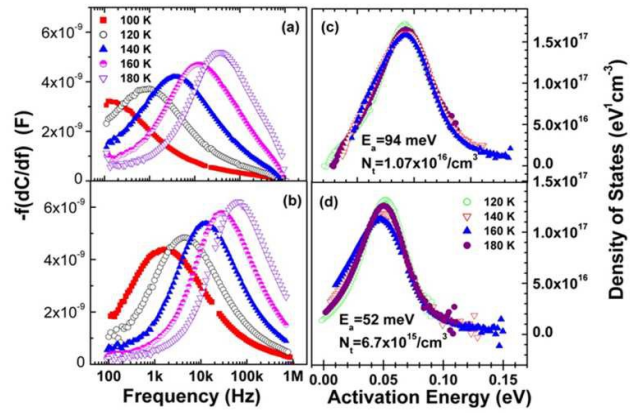


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Cell	Efficiency [%]	FF [%]	V_{oc} [mV]	J_{sc} [mAcm^{-2}]	R_s [Ωcm^2]	R_{SH} [Ωcm^2]	A	J_0 [Acm^{-2}]
S1	6.41	57.7	642	17.3	3.85	947	1.9	$3.1\text{e-}6$
S2	8.58	65.1	625	21.1	1.2	1183	1.7	$6.7\text{e-}7$