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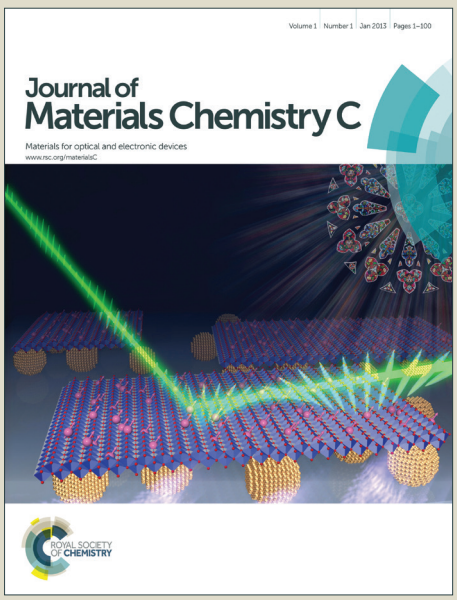

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ARTICLE TYPE

CdSe/ZnS core-shell quantum dots charge trapping layer for flexible photonic memory

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Light-responsive memory in which the writing, reading and erasing processes are sensitive to light signal has its own niche for the civilian and military application. However, control of memory property with ultraviolet (UV) is difficult since the common charge trapping layer of flash memory is insensitive to UV light signal. Here, we reported a novel design of UV-manipulated photonic nonvolatile memory based on spin-coated close-packed CdSe/ZnS quantum dots (QDs) monolayer. Our devices display remarkable UV-induced detrapping behavior and UV-controlled persistent threshold voltage (V_{th}) shifts of programmed or erased states. The electrically programmed flash memory has even been erased by a low intense UV light without additional external electric field within 1 s which is superior to the traditional silicon-based erasable programmable read only memory EPROM. With an advance in unique UV-detrapping effect of this novel structure, the UV-tunable complementary inverters constructed from p-channel and n-channel flash memory have further been demonstrated. The UV tunable charge trapping/detrapping facilitates the creation of new class of multifunctional optoelectronic memory devices.

Introduction

Photo-responsive nonvolatile memories are emerging as new class of optoelectronic design because of their potential advantages over conventional memory devices, for instance, they can display remarkable dual optoelectronic functionality including sensitive photo-detection and light-tunable persistent channel conductivity.[1] On the other hand, developments on multilevel data storage with 2^n threshold voltage (V_{th}) levels in single cell are driven by market requirement for low cost.[1-3] In fact, V_{th} of the photonic memory devices can be tuned via a change in channel conductance by storing photo-induced charge carriers in floating gate. Early research in photo-responsive nonvolatile memories were mainly focus on visible light manipulation.[2, 3] Parallel to perfecting the visible light responsive memory devices, there lies another highly promising axis for improving ultraviolet (UV)-sensible electronics since they has great application in both civilian and military areas such as environmental monitoring, large area display, optical communication, solar astronomy and missile plume detection.[4-8] However, control of memory property with UV is challenging since the commonly used charge storage layer of nonvolatile memory is insensitive to UV signal and most of molecular semiconductors are always operated in the visible region due to the typical size of their optical energy band gap.[9-11] For example, the traditional silicon based erasable programmable read only memory (EPROM) could only be erased by exposing it to strong UV light source such as mercury-vapour light for several minutes.[12] In order to make the nonvolatile memory more sensitive to the low intense UV light, a suitable charge trapping layer should fulfil the following requirements: (i) Strong UV absorption to allow an exceptional photo-response with large quantum efficiency and excitons generation. (ii) The emission peak cantered at visible region which overlaps the absorption peak of organic semiconductor to induce more photo-generated excitons in channel region. (iii) Well matched energy levels with organic semiconductor to achieve efficient programming/erasing operations. (iv) Solution-processed fabrication method for printed electronics application. Core-shell type quantum dots (QDs) have been subject of great scientific and technological interests owing to their tunable electronic and optical properties.[13-17] Overcoating nanocrystallites with higher band gap inorganic materials have been shown to improve the photoluminescence quantum yields by passivating surface nonradiative recombination sites.[18] CdSe/ZnS core-shell QDs generated a composite material that is strong absorber of UV light and an efficient emitter of saturated colour across the visible spectrum.[19, 20] Meanwhile, either electrons or holes can be confined in the cores of these type-I QDs due to the band offsets in which the conduction band of the shell is of higher energy than that of the core and the valence band of the shell is of lower energy than that of the core.[21-26]

In this manuscript, we present a novel design of UV-controlled photonic memories based on spin-coated close-packed CdSe/ZnS QDs monolayer. The CdSe/ZnS QDs are integrated between polyvinylalcohol (PVA)-aluminum oxide (Al_2O_3) hybrid blocking dielectric and Al_2O_3 tunneling dielectric layers. The pentacene and copper hexadecafluorophthalocyanine ($F_{16}CuPc$) are employed as p-type or n-type semiconductors, respectively. Compared with the previous reported work with different structure,[27-29] this architecture combines the UV light absorbing, visible light emitting and charge trapping capabilities of CdSe/ZnS monolayer along with visible light absorbing

capability of the organic semiconductor. The memory devices display UV-controlled multilevel data storage with persistent V_{th} shifts that is originated from UV-induced detrapping effect. The electrically programmed nonvolatile memories are erased by low intense UV light without external electric field within 1 s which is superior to the traditional silicon-based EPROM.[12] With continued advance in this novel structure, the UV-tuned complementary inverters have been further constructed from p-channel and n-channel flash memory. Collectively, the modulation by UV light allows new class of optoelectronic design that not only photo-responsive but also for the creation of multilevel data storage devices.

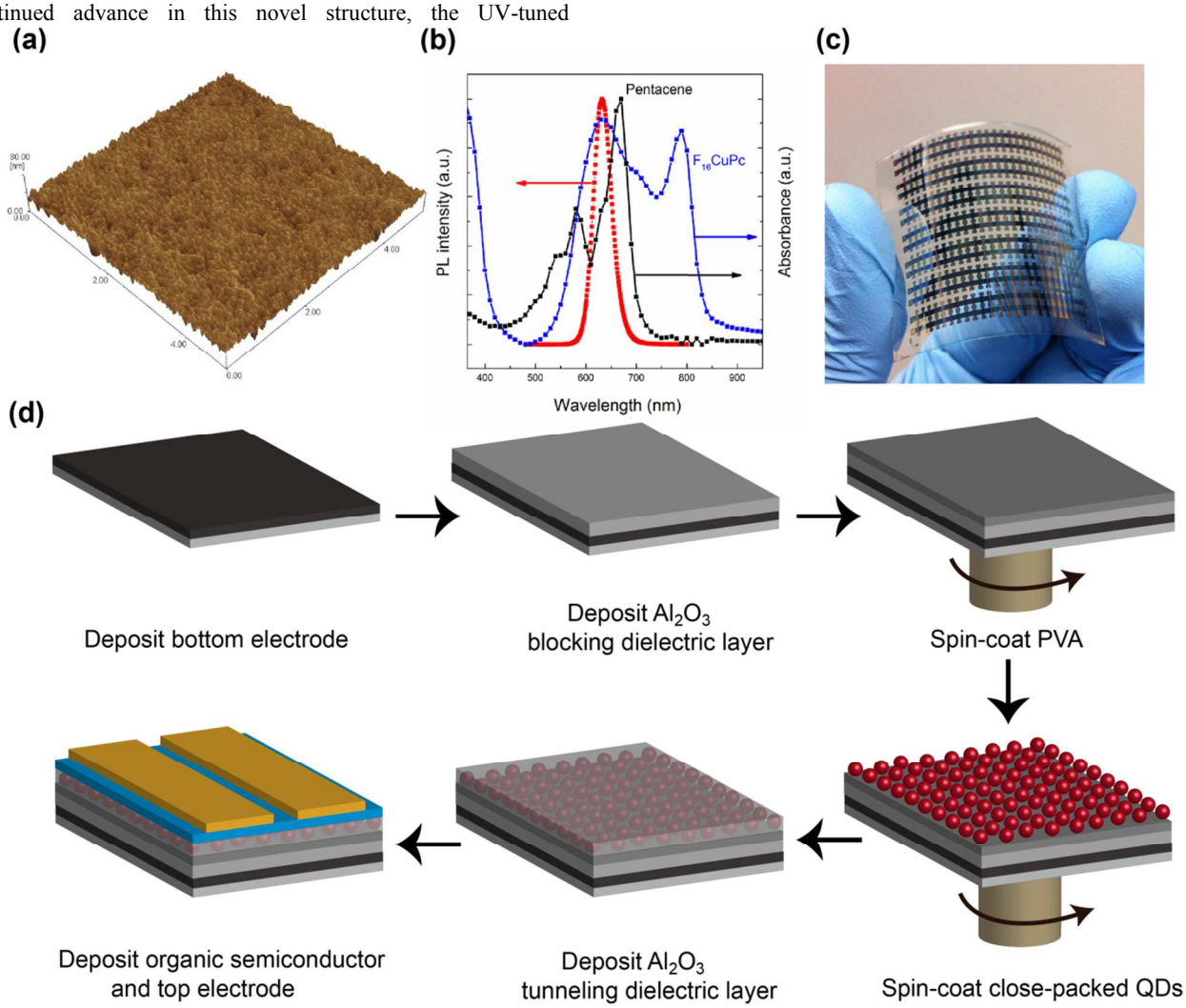

Fig.1 (a) Tapping-mode AFM image of the QDs monolayer on PVA coated Al_2O_3 in 5 μm × 5 μm area. (b) Normalized absorption spectra of as-deposited pentacene/F_{16}CuPc film and PL spectrum of solid-state CdSe/ZnS QDs monolayer. (c) Optical image of flexible photonic memory device. (d) Schematic diagram depicting the basic fabrication process of photonic memory device.

Experimental

Device fabrication

CdSe/ZnS QDs were purchased from Wuhan jiayuan quantum dots Co., Ltd. Memory devices were fabricated on 200 μm PET film with 25 nm thermal evaporated Ag as gate electrode. 15 nm Al_2O_3 layer were deposited using a Savannah 100 ALD system at a substrate temperature of 80 ℃. PVA solution of 0.5 w% dissolved in DI water with molecular weight 10,000 was filtered and spin-coated onto the Al_2O_3 layer to form a 10-nm-thick layer. The CdSe/ZnS QDs dissolved in the cyclohexane were spin coated on the top of PVA layer. Another 5 nm Al_2O_3 layer were deposited using a Savannah 100 ALD system at a substrate temperature of 80 ℃ to act as tunneling dielectric. A 40 nm thick pentacene and 30 nm thick F16CuPc were deposited as p-type and n-type semiconductor layer at a rate of 0.1 Å s^{-1} under a base pressure of 2 × 10^6 Torr. 30 nm thick gold electrodes were thermally evaporated through a shadow mask with a channel length (L) of 50 μm and width (W) of 1000 μm. For complementary inverters, the p-channel width and n-channel width were 500 μm and 2000 μm, respectively.

Characterization

The size distribution of the CdSe/ZnS nanocrystals was verified by transmission electron microscope (Jeol STEM/TEM JEM-2100F). The thicknesses of the deposited layers were measured using the ellipsometer. The morphologies of close-packed CdSe/ZnS monolayer were investigated by atomic force microscope (AFM, Veeco Multimode V & SPM-9500J3). The UV-visible spectra were obtained using PerkinElmer Lambda 750 UV-visible near infrared spectrophotometer with integrating sphere. The steady-state photoluminescence (PL) spectrum was recorded in transmission mode and the fluorescence emission signal was recorded using a Horiba FluoroMax-3 spectrofluorimeter by using continuous wave laser as excitation source. The electrical characteristics of the transistors were measured using a Keithley 2612 source meter and Agilent 4155C semiconductor analyzer at room temperature in ambient condition.

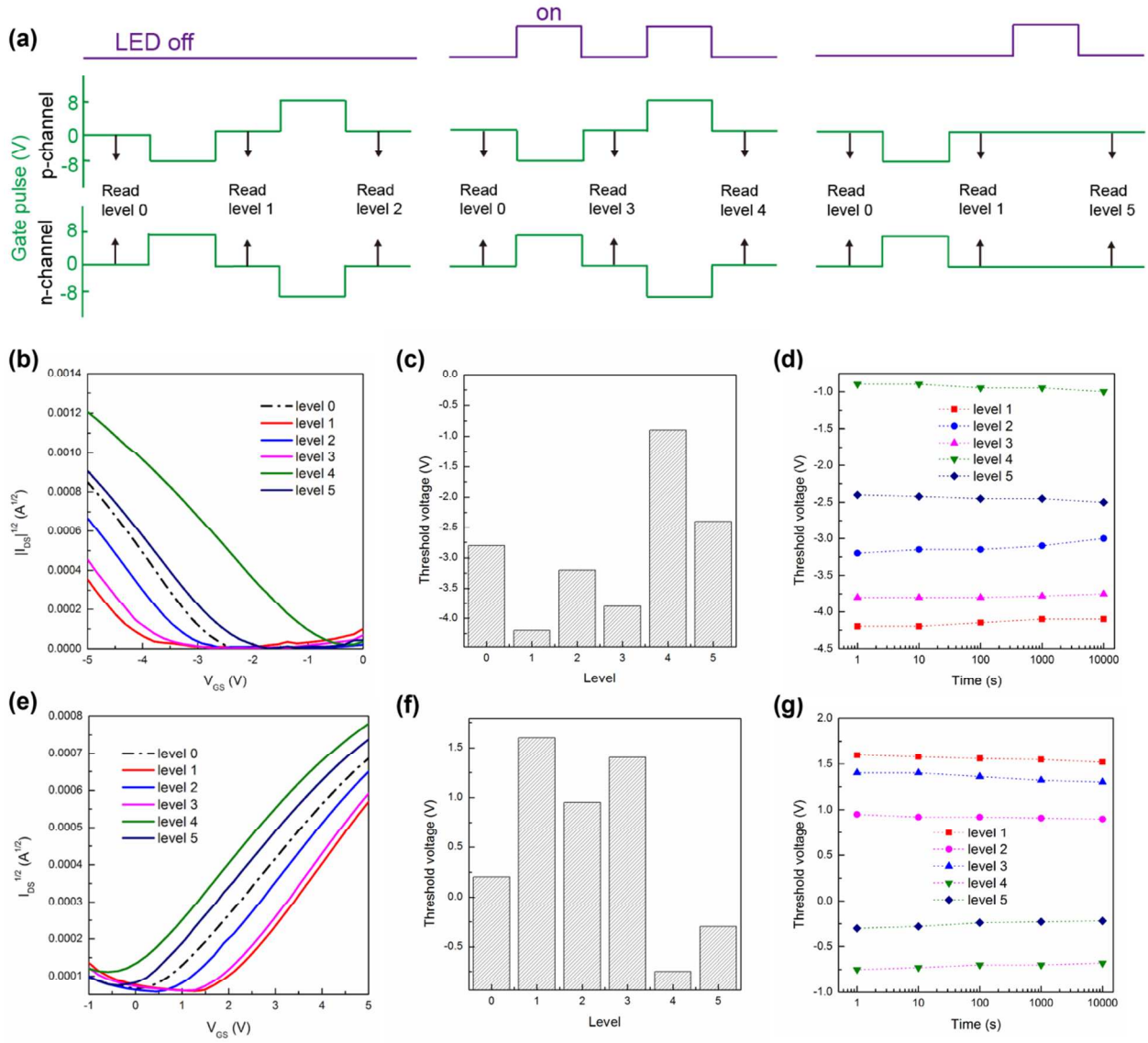

Fig.2 (a) Test pulse sequence for measurements. Memory characteristics of (b) p-channel and (e) n-channel photonic memories. Multilevel V_{th} of (c) p-channel and (f) n-channel photonic memories. Data retention capabilities of (d) p-channel and (g) n-channel photonic memories.

Results and discussion

High-resolution transmission electron microscopy (HRTEM) image of CdSe/ZnS nanocrystals (3 monolayers of ZnS) as depicted in supporting information (Fig. S1) shows nearly spherical crystalline particles. We used PVA whose dielectric constant is ~ 7, to form secondary blocking dielectric layer on the top of atomic layer deposited (ALD) Al_2O_3. A dense layer of QDs can be formed on the top surface of PVA layer by interchain interaction associated with the van der Waals force between the polymer chain and organic alkyl chain adhered to the QDs surface.[14, 16, 30] The hybrid blocking dielectric layer allows low voltage operation with less leakage current and uniform close-packed monolayer of QDs.[31, 32] Atomic force microscopy (AFM)

image in **Fig. 1**a shows result of spinning at the optimal QDs concentration and confirm that the high quality monolayer sheet of QDs formed during the spinning process. The poorly ordered QDs submonolayer on bare Al_2O_3 layer compared with single QDs monolayer on PVA-Al_2O_3 bilayer in large area are presented in Fig. S2. The UV-visible absorption spectrum of CdSe/ZnS core-shell QDs monolayer is shown in Figure S4. CdSe/ZnS core-shell QDs show an absorption coefficient of 3.57×10^5 and quantum efficiency of 55 %. The absorption spectra of as-deposited pentacene and F_{16}CuPc and photoluminescence (PL) spectrum of CdSe/ZnS core-shell QDs monolayer are shown in Fig. 1b. The PL peak of the QDs at 621 nm overlaps the optical absorption spectra of the pentacene and F_{16}CuPc with relatively broad peaks at 550 to 660 nm and 600 to 800 nm, respectively. Therefore, the red light emitted from the CdSe/ZnS can be reabsorbed by the semiconductor layer. We also found that pentacene and F16CuPc show some absorption in UV region. The memory device has both visible light absorption from the emission of CdSe/ZnS quantum dots monolayer and direct absorption of UV source.

The photograph of the fabricated photonic memory device is displayed in Fig. 1c. Fig. 1d illustrates the device fabrication procedure based on the close-packed QDs. A 25 nm silver (Ag) gate electrode was deposited on the PET substrate by thermal evaporation. A 15 nm aluminum oxide Al_2O_3 and 10 nm PVA were successively deposited as hybrid blocking dielectric layer by ALD and spin-coating, respectively. The close-packed QDs monolayer was then placed over the uniform PVA layer by spin-coating. After the construction of QDs charge trapping layer, another 5 nm Al_2O_3 was atomic layer deposited as tunneling dielectric layer. The pentacene and copper hexadecafluorophthalocyanine (F_{16}CuPc) were thermal evaporated as p-type and n-type semiconductors, respectively. Finally, a layer of 30 nm Au was thermal evaporated as source/drain electrodes.

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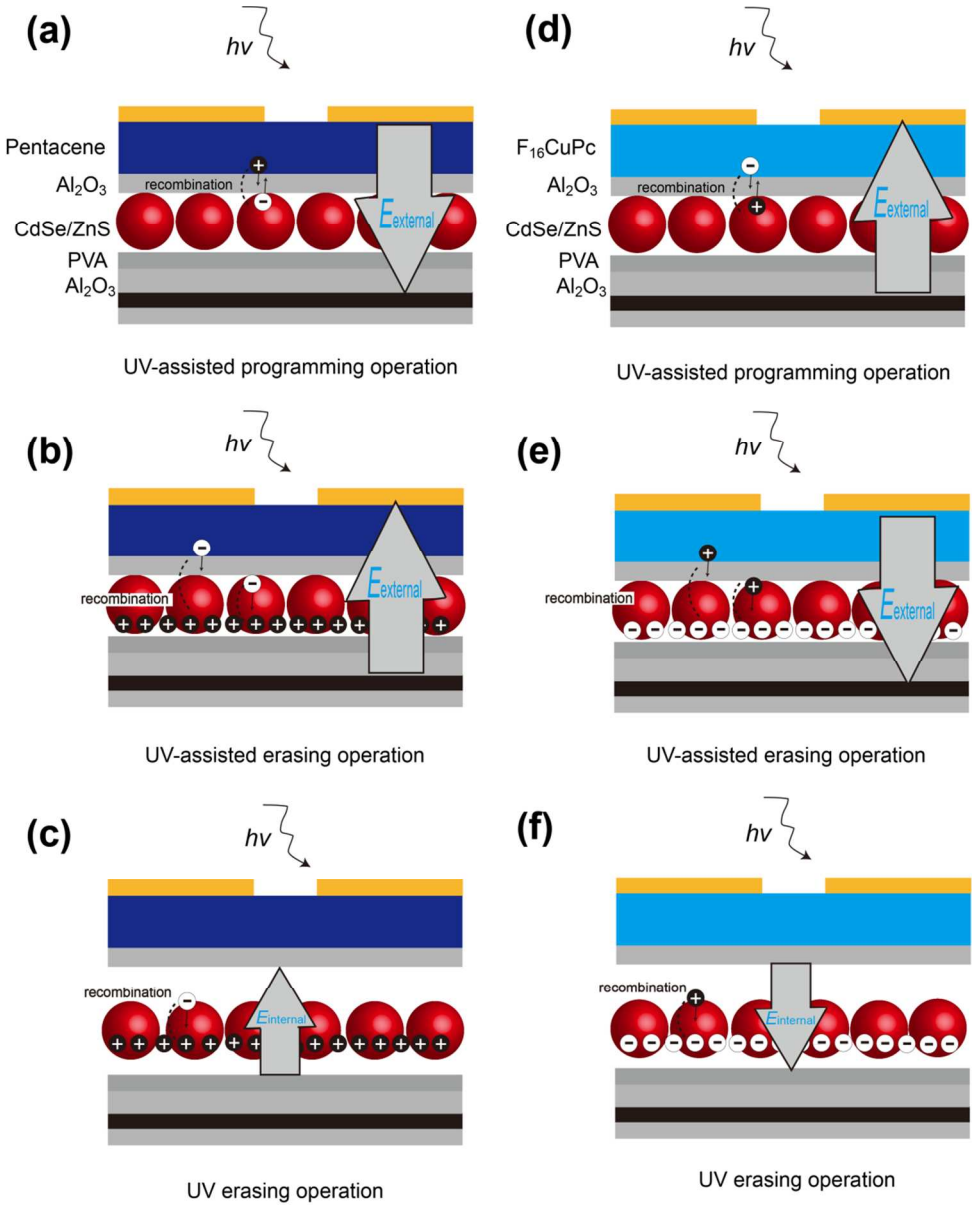

Fig.3 Operational principals of p-channel flash memory operated at (a) UV-assisted programming mode; (b) UV-assisted erasing mode; (c) UV erasing mode. Operational principals of n-channel flash memory operated at (d) UV-assisted programming mode; (e) UV-assisted erasing mode; (f) UV erasing mode.

The test pulse sequence for the measurements includes programming/erasing operation without UV illumination (part 1), UV-assisted programming/erasing operation (part 2) and UV erasing operation (part 3) are illustrated in **Fig. 2**a. The programming/erasing operations were - 8 V/+ 8 V for 1 s with or without UV assistance (light-emitting diode with the wavelength of ~ 365 nm and intensity of ~10 mW cm^{-2}) and the transfer curves were swept from 0 to -5 V in dark condition. The charge memory characteristics of p-channel photonic memory are shown in Fig. 2b. The control measurements without any nanocrystals in the gate stack have been carried out.[33] Structure of control device is Ag/10 nm Al_2O_3+PVA/5 nm Al_2O_3/pentacene or F16CuPc/Au source-drain. Negligible memory window implies that majority of trapping/detrapping does not occur at the organic semiconductor/gate dielectric interface (Figure S5). During the programming operation the stored charge carriers transferred from pentacene to the CdSe/ZnS monolayer screen the gate and modulate the channel conduction. In order to release the stored

charges, the gate should be reversed biased in erasing operation.[34-38] After the application of negative bias at the gate electrode, the transfer curve (level 1) is shifted in negative voltage direction in comparison with the initial state (level 0), suggesting that CdSe/ZnS monolayer act as trapping element of holes.[34, 39, 40] V_{th} is determined by extrapolating a plot of saturated source-drain current (I_{DS}, sat)$^{1/2}$ vs. source-gate voltage (V_{GS}) to source-drain current (I_{DS}) equal to 0. The transfer curves are shifted in positive direction where the V_{th} (level 1) of -4.2 V and V_{th} (level 2) of -3.2 V are remarkably changed to V_{th} (level 3) of -3.8 V and V_{th} (level 4) of -0.9 V when programming/erasing operations were carried out under UV illumination. Note that there is pronounced UV-assisted detrapping effect in the presence of UV light and the V_{th} (level 4) is further shifted in the positive direction beyond initial state (level 0). We obtained two bits per one photonic memory cell by programming/erasing the cell with or without the UV assistance for realizing the memory states of '00', '01', '10' and '11'. The V_{th} of initial state (level 0), programmed/erased state (level 1/level 2), UV-assisted programmed/erased state (level 3/level 4) and UV-erased state (level 5) are summarized in Fig. 2c. Fig. 2d shows the data retention characteristics for p-channel photonic nonvolatile memory, where the V_{th} of different states was measured at gate voltage (V_{GS}) = -5 V and source-drain voltage (V_{DS}) = -5 V with a time interval of 10^n s after application of V_{GS} = -8 V and +8 V for 1 s, respectively. The stored data is steadily sustained to the point that the estimated retention time of the p-channel photonic memory is 10^4 s, implying perfect non-volatile charge retention.

For photonic memory based on $F_{16}CuPc$ channel, the programming/erasing voltages were + 8 V/- 8 V for 1 s with or without UV illumination and then the transfer curves were swept from -1 to 5 V in the absence of light. The memory properties, multilevel V_{th} and data retention characteristics are summarized in Fig. 2e to 2g. The transfer curve of level 1 is shifted in the positive direction in comparison with the level 0 after the application of positive gate bias, due to trapping of electrons in n-channel photonic memory devices during the programming operation. Similar UV-induced detrapping effect was also observed in n-channel photonic memory.

The operation mechanisms of p-channel and n-channel photonic nonvolatile memory can be understood from **Fig. 3**. The excitons generated at the CdSe/ZnS monolayer and pentacene play an important role in the UV-induced detrapping effect. For pentacene based photonic memory, the external gate electric field ($E_{external}$) point towards the CdSe/ZnS QDs monolayer from pentacene during the UV-assisted programming operation. Once the electron-hole pairs are generated in CdSe/ZnS QDs and pentacene under UV illumination, the photo-electrons are swept towards pentacene under external gate bias. During the dynamic trapping process, the effective number of stored charge carriers decrease since the downward moving holes are partially compensated with the upward moving photo-induced electrons. The less stored holes in the CdSe/ZnS QDs monolayer deliver smaller built-in potential across the channel and induce a positively shifted transfer curve of level 3. The scenario is similar during the erasing process under UV illumination. Here the gate voltage changes its sign varying the direction of $E_{external}$ across the CdSe/ZnS QDs monolayer pointing towards the pentacene layer. The trapped holes in the CdSe/ZnS monolayer are completely detrapped by combining with counter charges (photo-generated electrons). Thereafter, the transfer curve of level 4 is further shifted in the positive direction beyond the level 0 due to the recharging of excess counter charges (photo-induced electrons) in the CdSe/ZnS QDs monolayer.

The electrical characteristics of photonic nonvolatile memories were investigated in more detail by applying the UV pulse without gate bias on the devices at level 1, and are illustrated in Fig. 2a (part 3). It should be noted that the pre-programmed state (level 0) can be recovered by a UV light pulses (level 5) while applying a reversible gate pulses does not remove the stored charge carriers completely (level 2). It indicates that the erasing efficiency of UV is higher than that of a voltage pulse. For the p-channel nonvolatile memory, there might be two ways for the charge carriers transfer between CdSe/ZnS monolayer and pentacene during the erasing process: (i) the negative electrons are injected into the charge trapping layer and eventually recombine with the stored holes in the valence band of CdSe/ZnS; (ii) the stored holes in the charge trapping layer release back to the channel.[2] For the electrical erasing operation, the applied electrical field in the tunneling dielectric layer can be calculated by the following equation.[41, 42]

$$E_{total} = \frac{V_{GS}}{d_1 + d_2\,(\varepsilon_1/\varepsilon_2) + d_3(\varepsilon_1/\varepsilon_3)} + \frac{Q}{\varepsilon_1 + \varepsilon_2\,(d_1/d_2) + \varepsilon_3(d_1/d_3)} \times \frac{1}{\varepsilon_0}$$

Where ε_0 is the permittivity of vacuum, ε_i are the dielectric constant, d_i is the thickness of the dielectric layers and Q is the stored charge carriers in the CdSe/ZnS QDs which can be calculated by the equation.[43-45]

$$Q = C_{total} \times \Delta V_{th}$$

Where C_{total} is the dielectric capacitance of total dielectrics and ΔV_{th} is the memory window. For UV erasing operation, it is worth noting that trapped charge carriers in CdSe/ZnS monolayer play the critical role for the internal electric field formation which can be estimated from the following equation:

$$\mathrm{E}_{internal} = \frac{Q}{\varepsilon_1 + \varepsilon_2\,(d_1/d_2) + \varepsilon_3(d_1/d_3)} \times \frac{1}{\varepsilon_0}$$

The applied electrical field is estimated to be about 2.85 MV/cm in electrical erasing process, which is much higher than the internal electric field ($E_{internal}$) of 0.25 MV/cm in UV erasing process. It implies that the first way, as mentioned above, might be dominated in the UV erasing process since the charge carriers release rate of 2nd path is proportional to the electrical field. During the UV erasing operation, the photoinduced electron-hole pairs are generated in CdSe/ZnS charge trapping layer and can be separated by the internal electrical field. The photogenerated electrons/holes recombine with the trapped holes/electrons to eliminate the screening effect (voltage drop) of the gate voltage during reading process so that a higher UV erasing efficiency was obtained (Fig. 3c and 3f). Now it is clear that the photonic

nonvolatile memories based on the CdSe/ZnS monolayer could be programmed or erased by voltage or UV assisted voltage pulse. Multilevel data storage with well separated data sensing margins and long retention time has been realized in the photonic memories under UV modulation. The electrically programmed photonic memories could be erased by UV light without external gate bias application within 1 s.

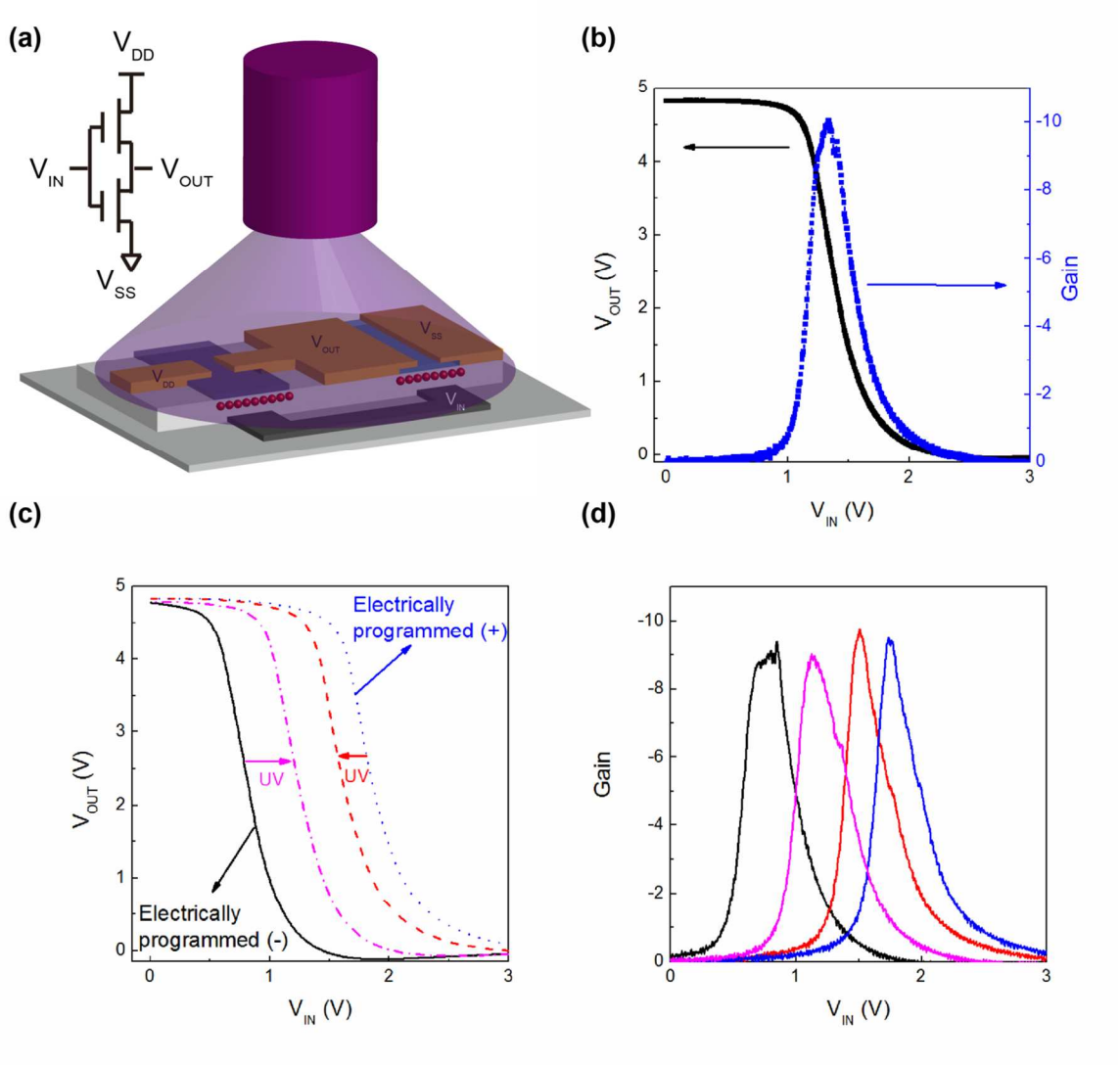

Fig.4 (a) Schematic cross-section and circuit diagram of the complimentary inverters under UV-illumination. (b) Transfer characteristics of a complementary inverter measured prior to any program voltages. (c) Transfer characteristics of the inverters measured at different conditions. (d) Signal gain of the inverters.

To demonstrate the applicability of these high performance flexible photonic nonvolatile memories as building blocks in integrated circuits, we constructed complementary inverters and studied their basic parameters for analogue and digital circuit applications. Based on p-channel pentacene and n-channel F_{16}CuPc, we fabricated the organic complementary circuits with patterned gates on flexible PET substrates. **Fig. 4**a shows the three-dimensional view of the complimentary inverter and the circuit diagram. During the patterning procedure, the gates of the p-channel and n-channel transistors are connected to form the input, while the drains of the two transistors are connected to form the output. The source of the p-channel acts as the power supply and the source of the n-channel acts as the ground. The p-channel width and n-channel width are 500 μm and 2000 μm, respectively while the channel lengths are 50 μm for both transistors. The voltage transfer characteristics (VTC) of the inverters are shown in Fig. 4b and 4c. After applying a input voltage (V_{IN}) pulse of +8 V for 1 s, the switching voltage (V_s) is shifted in positive direction from 1.5 to 1.91 V, confirming that the n-channel transistor is hard to be turned on since the electrons are injected and trapped in the CdSe/ZnS QDs.[46] After the application of a gate pulse of -8 V for 1 s, the V_s is shifted from 1.5 to 0.99 V due to the holes trapping. The complimentary inverters at electrons trapped state and holes trapped state were then illuminated under UV light for 1 s. The V_s of electron-trapped state and hole-trapped state are systematically shifted back to 1.7 V and 1.37 V, respectively. The relationship between the V_s shifts and UV light provide a similar insight into the

aforementioned UV detrapping effect. The small-signal gain is almost constant for electron-trapped state, hole-trapped state and UV-erased state in comparison with the initial state (Fig. 4d).

Conclusions

In summary, we developed a novel UV-modulated photonic nonvolatile memory based on the solution-processed close-packed CdSe/ZnS QDs monolayer and demonstrated its applications on flexible substrate and logic circuit. The memory characteristics of the devices are systematically tuned through varying the combinations of applied gate pulses and light pulses. UV manipulation is a feasible way to achieve multilevel V_{th} in single memory cell, which is the precondition of realizing multibit storage. The electrically programmed photonic memory can be completely erased by low power UV pulse without external gate voltage within a short time that shows the superiority of our photonic memory over traditional silicon-based EPROM. These effects can be explained by UV-induced detrapping in CdSe/ZnS QDs-organic semiconductor architecture, and may lead to a new class of flexible optoelectronic memory devices that are naturally scalable for large-area applications at room temperature.

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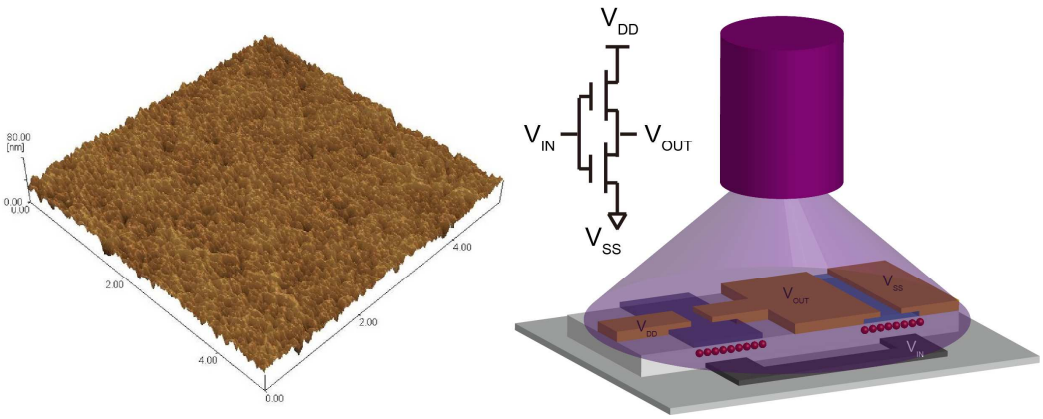

A novel design of UV-manipulated photonic nonvolatile memory based on spin-coated close-packed CdSe/ZnS quantum dots is reported.