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ARTICLE TYPE

Graphene oxide as an effective interfacial layer for enhanced graphene/silicon solar cell performance

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We show that interface tailoring is an effective approach towards high performance G/Si schottky-barrier solar cells. Inserting a thin graphene oxide (GO) interfacial layer can improve the efficiency of graphene/silicon solar cells by > 100%. The role of GO interfacial layer is systematically investigated by varying GO film annealing temperature and thickness. It is found that GO cannot be treated as the traditional thinking, i.e., an insulator. In other words, G/GO/Si solar cell is not suitable to be treated as a “MIS” cell. On the contrary, it should be regarded as a p-doped thin layer. The effects of GO film thickness on device response are also studied and there exists an optimal thickness for device performance. A record 12.3 % (device size: 3×3 mm²) power conversion efficiency is achieved by further performance optimization (chemical doping graphene and antireflection coating).

Introduction

Graphene, a two-dimension sheet of sp² hybrid carbon, is highly attractive for numerous applications such as high-performance nanoelectronics, optoelectronics, and energy storage.¹⁻³ Recently, in view of its fascinating physical properties,^{4,6} the integration of graphene into photovoltaic devices has been extensively explored.⁷⁻¹¹ Among these photovoltaic devices, graphene/silicon (G/Si) schottky-barrier solar cells are extremely appealing due to their simple device structure, low cost and potential for high efficiency.⁷ For schottky-barrier solar cells, the schottky barrier height (SBH) is a critical factor determining the device performance. Specifically, larger SBH is desirable for more efficient charge separation. Chemical doping graphene is the most commonly used method to increase SBH since it is determined by the difference between the work function (WF) of graphene and the electron affinity (χ) of Si (i.e., SBH = WF_G - χ).¹⁰

In parallel, the other significant research challenge originated from device structure aspect is to create interfaces that are tailored at the nanoscale to optimize transport of energy. It has been demonstrated that the interfaces play an important part in pursuing high power conversion efficiency (PCE). For example, in organic photovoltaic devices (OPVs), there is usually a hole/electron transport layer between the active layer and anode/cathode.^{12, 13} As another example, it is found that a thin SiO_x layer is beneficial for Si-based schottky-barrier solar cells, the introduction of a thin insulator changes the device structure from MS (Metal-Semiconductor) to MIS (Metal-Insulator-Semiconductor).¹⁴ However, there is little report on the interfaces in G/Si solar cells.

Herein, we show that interface tailoring is an important strategy in G/Si schottky-barrier solar cells. Owing to its tunable

electronic structure, GO and its derivatives have been used as a new class of efficient hole- and electron-extraction materials in polymer solar cells.¹⁵ The insertion of Graphene oxide (GO) films, which can be regarded as a graphene sheet functionalized with oxygen groups, leads to dramatic improvement of PCE by > 100 %. A 12.3 % PCE can be obtained with further modifications (chemical doping graphene and TiO₂ antireflection coating). More importantly, GO should be treated as a p-doped material rather than an insulator in G/GO/Si solar cells. This result thus serves as a model example toward high performance (G/Si) schottky-barrier solar cells.

Experimental Section

Synthesis of multilayer graphene (MLG). As reported previously,¹⁶ MLG is grown on copper foil (25 μ m thick, Alfa Aesar) using LPCVD method. Briefly, the system is first heated to 1000 °C for 10 min with a H₂ flow of 300 sccm to clean the surface of copper, then 10 sccm CH₄ is introduced for 20 min.

GO film preparation. GO is synthesized using modified Hummer's method.¹⁷ The concentration of GO used is ~1 mg/mL in a mixed solution (water: ethanol = 1:1). The solution is spun coating onto Si substrates at certain speed for 60 s, then GO films are either dried on a hot plate at 80 °C for 30 min or annealed at different temperature (200, 300, 400, 500 °C) under Ar atmosphere for a fixed 30 min.

Synthesis of TiO₂. For the synthesis of TiO₂,¹⁸ Ti(OBu)₄ is added to a mixture of solution of water and ethanol (water: ethanol = 1:60 molar ratio), then a small amount of HCl (37 wt%) is dropped to promote hydrolysis and stirred for 2 h before use.

Fabrication of Solar Cell Devices. n-type Si (with a square window of 3 mm × 3 mm surrounded by 300 nm thick SiO₂) is used as substrates. SiO₂ is used to define the active area of solar

cells. In addition, SiO₂ is used to make sure that the Ag paste (the front electrode) is separated from the underlying Si (connecting the rear electrode), and therefore the solar cells can work properly. GO is spun coating onto Si substrates at certain speed and then annealed at different temperature. The transfer of graphene onto GO/Si substrate is realized by the well-known wet transfer method.¹⁹ Briefly, the copper substrates are dissolved using FeCl₃ (~0.7 M), then the MLG film is washed several times using deionized water, finally the MLG film is picked up using the GO/Si substrates. Ga-In liquid (99.999 %) and Ag paste are applied as the rear electrode and the front electrode, respectively. HNO₃ doping is done by using concentrated HNO₃ (65 wt%) vapor for 1 min. TiO₂ solution is spun coating onto graphene film at 2000~6000 rpm for 1 min.

Characterizations. The solar cells are tested under Air Mass 1.5 illumination (100 mW/cm², the light density is calibrated using a standard solar reference cell, SRC-1000-TC-QZ, VLSI Standards S/N: 10510-0305). The current-voltage data are recorded with a Keithley 2400 SourceMeter. IPCE is obtained using QTEST STATION 500AD in the range 300 nm~1100 nm. AFM measurements are performed on Agilent Technologies 5500 Scanning Probe Microscope, and the thicknesses and surface roughness (R_q) are obtained using Picoview version 1.8. GO samples are prepared by dropping GO solution on Cu grid, then observed using JEOL-2010 transmission electron microscope (TEM). Raman Spectra are performed using Renishaw inVia-Reflex with 532 nm wavelength incident laser light. Scanning Electronic Microscope is acquired with JSM-7001F, and EDX spectrum is obtained using Oxford INCA X-MAX. UPS measurements are performed with an unfiltered HeI (21.22 eV) gas discharge lamp to determine the work function of graphene on different substrates. XPS measurements are made with a monochromatic Al K_α source (1486.6 eV) to detect the C-1S signal. Electrochemical Impedance Spectroscopy is measured using CHI 760E, Shanghai Chenhua Instrument Co., Ltd., the measurements are carried out under illumination (AM 1.5G condition) by applying a bias that is equal to V_{oc}.

Results and discussion

Fig. 1a depicts the schematic illustration of our device. It consists of three layers, namely G/GO/Si. In present work, MLG is employed because it has been demonstrated theoretically and experimentally that the performance of MLG/Si devices is superior over that of their single-layer graphene (SLG) counterparts.^{20, 21} MLG is synthesized by LPCVD as reported elsewhere.¹⁶ The multilayer structure is verified by Raman Spectrum (Fig. 1b, I_G/I_{2D} > 2) and Transmittance Spectrum (the inset of Fig. 1b, 84 % at 550 nm, corresponding to 6~7 layers). Pristine MLG/Si solar cells having stable PCE of ~2.3 % are used as the reference devices. A typical solar cell has J_{sc} = 23.7 mA/cm², V_{oc} = 0.35 V, FF = 0.26 and PCE = 2.13 % (Fig. 2, the red curve and Table 1). After GO is introduced at the interface, the PCE is dramatically decreased from 2.13 % to < 0.2 % (black curve). It means that unannealed GO interlayer has deleterious effect on device performance. However, if the GO film is annealed at 200 °C before transferring graphene (If not otherwise stated, GO(X) represents the GO films annealed at different temperature), the PCE is noted to be improved substantially by

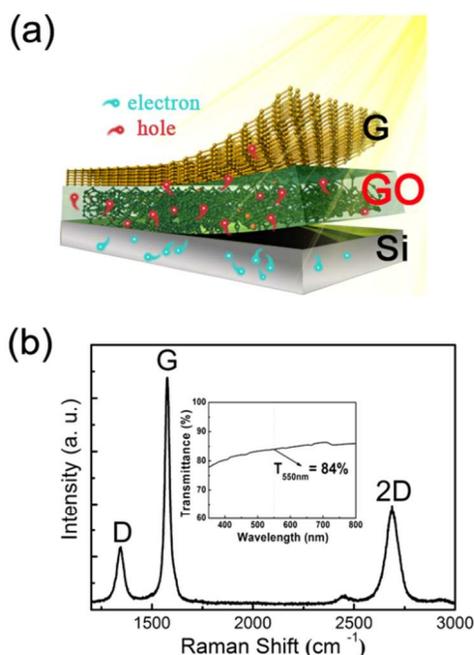


Fig. 1 (a) A schematic illustration of device structure. The device consists of three layers, namely G/GO/Si. (b) Raman spectrum of multilayer graphene used in this work. The inset shows a transmittance spectrum of graphene, T_{550nm}=84%, which corresponds to 6~7 layers.

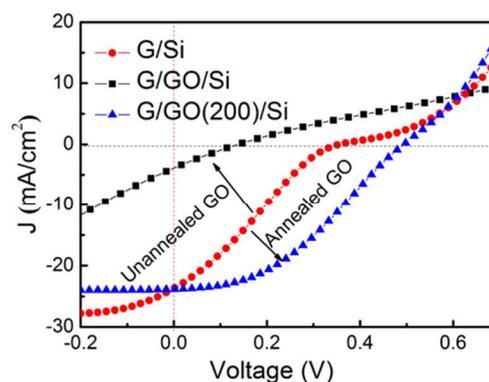


Fig. 2 The effects of GO interfacial layers on device performance. The insertion of as-deposited GO interlayers leads to an extremely low PCE (black curve). However, annealing the as-deposited GO at 200 °C (blue curve) improves the PCE by >100% compared with the reference device (red curve).

Table 1. Photovoltaic parameters of solar cells in Fig. 2.

Entry	J _{sc} (mA/cm ²)	V _{oc} (V)	FF	PCE (%)	R _{s1} /R _{s2} (Ω/cm ²)	n	SBH (eV)
Ref. (Red)	23.7	0.35	0.26	2.13	4.3/4.35	3.35	0.65
GO (Black) ^b	3.33	0.12	0.31	0.12			
GO (Blue) ^c	26.4	0.48	0.41	5.2	4.37/4.45	2.08	0.79

Footnotes: a. the units of R_{s1} and R_{s2} are Ω/cm²; b. unannealed GO interlayer; c. GO interlayer annealed at 200 °C under Ar atmosphere for 30 min.

42-fold from 0.12 % to 5.2 % (blue curve). Compared with the reference device, the PCE shows an increase of >100 %, as a result of the increase in J_{sc}, V_{oc} and FF from 23.7 to 26.4 mA/cm², 0.35 to 0.48 V and 0.26 to 0.41, respectively.

Obviously, the main improvements are from FF (an increase of 54 %) and V_{oc} (an increase of 37 %). If GO can be treated as an insulator, $J_{sc}(G/GO/Si)$ should be smaller than $J_{sc}(G/Si)$ since carriers are transported GO interfacial layer by tunneling. However, J_{sc} shows some increase after the insertion of GO film, and as shown later, there exists a clear trend of increasing J_{sc} with increasing GO film annealing temperature. We come to a conclusion that GO can no longer be treated as an insulator in G/GO/Si devices. Therefore, in G/GO/Si solar cells, the holes are injected and transported in GO interfacial layers *via* the sp^2 sites, and the content of sp^2 sites has critical impacts on the device performance.²² We first examine the Raman spectra of the GO films. As shown in Fig. S1, The I_D/I_G show little change upon annealing, which may be due to the fact that annealing does not lead to an expansion of the sp^2 cluster.²² X-ray photoelectron spectroscopy (XPS) is then employed to determine the content of sp^2 sites of GO interlayers before and after annealing because the

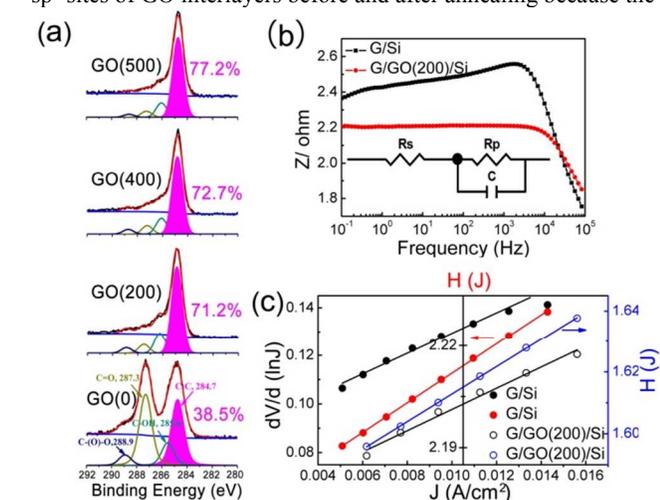


Fig. 3 (a) The C 1s XPS spectra of GO interfacial layers annealed at temperature (0, 200, 400, and 500 °C). The content of sp^2 sites is indicated by the pink area. Clearly, there is a trend of increasing sp^2 sites content with increasing annealing temperature. (b) The charge-transfer resistance (Z_t) of G/Si and G/GO(200)/Si devices. The inset shows an equivalent circuit of the devices. (c) Calculations of SBH from the J vs $H(J)$ plots. The J vs $dV/d(\ln J)$ plots are also given.

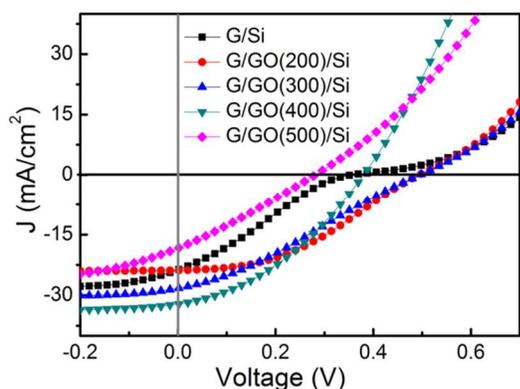


Fig. 4 The change of PCE with GO film annealing temperature. G/GO(X)/Si (X=200,300 and 400 °C) devices show improvements in PCE, whereas further increasing annealing temperature (500 °C) causes degradation in PCE.

Table 2. Photovoltaic parameters of solar cells in Fig. 4.

Ann. Temp. (°C)	J_{sc} (mA/cm ²)	V_{oc} (V)	FF	PCE (%)	R_{si}/R_c (Ω /cm ²)	n	SBH (eV)
200	26.4	0.48	0.41	5.2	4.37/4.45	2.08	0.79
300	28.2	0.48	0.30	4.2	4.53/4.64	2.46	0.74
400	32.2	0.39	0.39	4.6	1.51/1.56	3	0.6
500	20.3	0.28	0.28	1.6	2.56/2.6	4.43	0.55

absence of sp^3 C-C bonding (bonding energy in range 285.5~286.5 eV)²³ allows us to detect the sp^2 C-C bonding. As shown in Fig. 3a, The C 1s XPS signal consists of four different chemical shifted components which can be deconvoluted into: C-C (284.7 eV), C=O (287.3 eV), C-(O)-O (289 eV) and C-OH (285.5 eV).²⁴ The sp^2 C-C bonding fraction (the pink area) is 38.5 % in as-deposited GO interlayer. At sp^2 C-C bonding fraction < 60 %, the conduction in GO is *via* the tunneling between the sp^2 sites and therefore leading to poor carrier transport.²² So it is suggested that the very low density of sp^2 sites is responsible for the low PCE after the insertion of unannealed GO film. After annealing, the content of sp^2 sites is increased dramatically from 38.5 % to 71.2 %. This is believed to be the main reason for the significant improvements in PCE, because percolation among the sp^2 sites dominates at sp^2 fraction > 60%.²² In addition, the GO film thickness becomes thinner upon heating (from 6.7 nm to 5.6 nm, Fig. S4a and 4b), which is also beneficial for better carrier transport. As a consequence, the carrier injection and transport in GO films are greatly enhanced after annealing.

The charge-transfer resistance (Z_t) of G/Si solar cells has remarkable influence on FF because Z_t is related to series resistance (R_s), a resistance that is associated with schottky barrier (R_1), the front (R_2) and back (R_3) electrodes contact resistance.²⁵ For simplicity, R_1 , R_2 and R_3 can be substituted by a

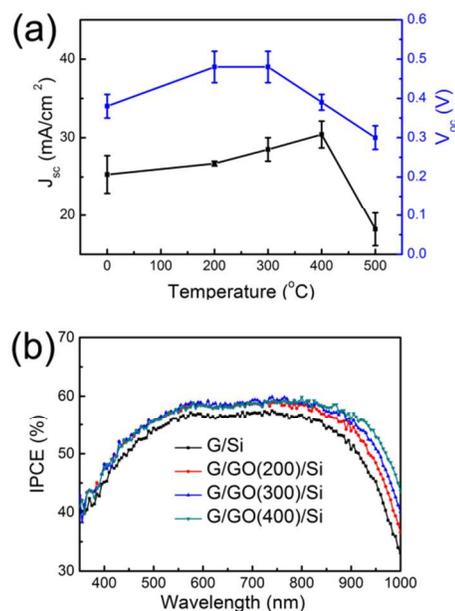


Fig. 5 (a) The statistical results (based on three parallel devices) of J_{sc} and V_{oc} . (b) The IPCE curves of devices with different GO film annealing temperature.

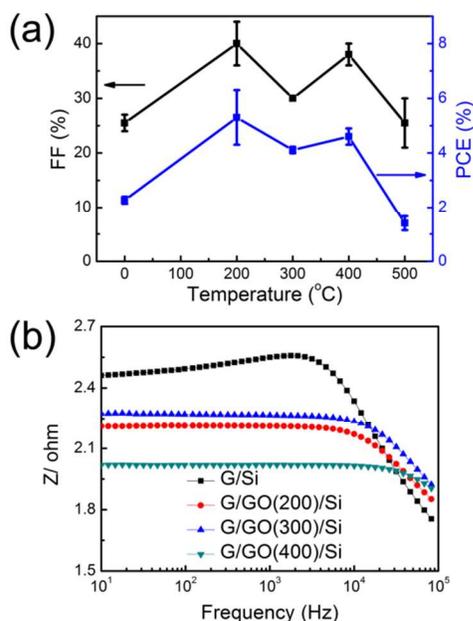


Fig. 6 (a) The statistical results (based on three parallel devices) of FF and PCE. PCE has the same changing trend with FF, indicating that the relatively low FF is the main reason for the relatively low PCE_{GO(300)}. (b) The charge-transfer resistance (Z_f) of G/GO(X)/Si devices ($X=0,200,300$ and 400 °C). Clearly G/GO(300)/Si device (the blue curve) has higher Z_f than G/GO(200,400)/Si devices.

single parallel resistance, R_p . The general equivalent circuit of the solar cells is given in the inset of Fig. 3b.²⁶ Electrochemical Impedance Spectroscopy (EIS) is then employed to determine Z_f . As shown in Fig. 3b, Z_f is 234.4 Ω for G/Si and 162.2 Ω for G/GO(200)/Si, respectively. The 31 % decrease in Z_f is thought to be the main reason for the remarkable improvement in FF. The decrease in Z_f may be due to the change in device capacitance and needs further study. In order to analyze the variations in V_{oc} , SBH is extracted from J vs $H(J)$ plot. The series resistance (R_s) is also calculated from both the J vs $dV/d(\ln J)$ (denote as R_{s1}) and J vs $H(J)$ plots (denote as R_{s2}) to see the consistency of this approach.²⁷ The results are given in Fig. 3c and all parameters are summarized in Table 1. As seen, R_{s1} and R_{s2} show good agreement with each other within 5 %. The calculated $SBH_{G/Si}$ is 0.65 eV, which is in good agreement with the difference between WF_G and χ (the WF_G on Si is 4.72 eV as measured from Ultraviolet Photoelectron Spectroscopy (UPS) in Fig. S2, and χ is 4.05 eV). The SBH increases by 0.14 eV from 0.65 eV to 0.79 eV after the introduction of GO(200) film, which is consistent with the 0.13 V increase in V_{oc} .

As discussed above, on one hand, simply annealing GO film at 200 °C improves the PCE significantly; on the other hand, the role of GO need further to be studied. This drives us to vary the GO film annealing temperature (300, 400, 500 °C) to look into its role in G/GO/Si solar cells. Fig. 4 shows the change of PCE with annealing temperature, and the device parameters are summarized in Table 2. As shown, G/GO(X)/Si ($X=200, 300, 400$ °C) devices show improvements compared with the reference devices. In order to have reliable results, each set of devices are fabricated with three parallel cells and the statistical results of J_{sc} and V_{oc} are plotted in Fig. 5a. As seen, J_{sc} increases with increasing annealing

temperature, whereas V_{oc} peaks at 200 °C. The variations in J_{sc} can be explained as follows. Under the same illumination conditions (AM 1.5G) and using the same graphene, J_{sc} can be expressed as $J_{sc} = f(\beta, SBH)$, where β is the quantum efficiency.²⁸ After the insertion of GO film, the hole injection and transport in GO film also have important impacts on J_{sc} , and J_{sc} should be therefore written as: $J_{sc} = f(\beta, SBH, \theta)$, where θ represents the hole injection and transport in GO film. Since the GO film absorbs little light (Fig. S3) and SBH is in the $e^{-\alpha W}$ form,²⁸ β and θ dominate J_{sc} . β can be estimated from incident photon-to-electron conversion efficiency (IPCE) spectra. As shown in Fig. 5b, $IPCE_{GO(400)} > IPCE_{GO(300)} > IPCE_{GO(200)}$, which means that higher annealing temperature leads to larger β . Moreover, all the IPCE are larger than the reference IPCE (black curve), indicating that the incorporation of GO films can suppress interface recombination, which may be due to the negative interface charge nature (or oxide charge) of GO.²⁹ θ also increases with increasing annealing temperature because the content of sp^2 sites, which has significant impacts on θ , goes higher at higher annealing temperature (Fig. 3a). As a result, J_{sc} increases with increasing annealing temperature. The change in V_{oc} is explained by exploring the change in SBH. SBH are again calculated from J vs $H(J)$ plots (see Fig. S7 and Table 2) and there is a clear trend of reducing SBH with increasing annealing temperature. In fact, GO can be regarded as a p-doped material because the Fermi level is very close to the valence band, both supported by theoretical calculations and experiments.^{30, 31} The existence of an opposite doped thin layer on silicon gives rise to the following increase in SBH:³²

$$\Delta SBH = q\delta p^2 / 2\epsilon_s \quad (1)$$

where q is the electronic charge, ϵ_s is the permittivity of Si, δ and p are respectively the thickness and the doping level of the interfacial layer. Upon heating, oxygen atoms are removed from GO, and gradually GO is converted to graphene.²⁴ From this point of view, the p-doping level of GO decreases as annealing temperature increases. Hence SBH shows a down trending at higher annealing temperature using equation (1) due to the smaller δ and p , which is in good agreement with the results obtained from J vs $H(J)$ plots. It should be pointed out that WF_G on GO(400) is 4.62 eV (21.22 - 16.6 = 4.62 eV, the green curve in Fig. S2), therefore $SBH_{G/Si}$ changes to 0.67-0.1 = 0.57 eV, and the increased SBH due to the incorporation of GO(400) film is 0.03 eV. The p-doping level of GO(X) ($X=200, 300,$ and 400) films are respectively 1.06, 0.93 and $0.58 \times 10^{13}/\text{cm}^2$ as calculated from equation (1), consisting with the fact that the sp^2 C-C bonding fraction increases upon annealing at 200 ~ 400 °C (Fig. 3a). Though $SBH_{GO(200)}$ (0.79 eV) > $SBH_{GO(300)}$ (0.74 eV), $V_{oc,GO(200)} \approx V_{oc,GO(300)}$. It is thought that the interface recombination is responsible for this phenomenon for higher recombination reduces V_{oc} ($IPCE_{GO(300)} > IPCE_{GO(200)}$, suggesting that G/GO(200)/Si device has higher recombination).³³

Fig. 6a gives the statistical results of FF and PCE. PCE shows the same trend as FF. Comparing the device parameters, the relatively lower PCE of G/GO(300)/Si is mainly due to its lower FF. The variations in FF are again explained by Z_f . As revealed by EIS in Fig. 6b, the relatively larger $Z_{f,GO(300)}$ with respect to $Z_{f,GO(200,400)}$ is responsible for the lower FF.

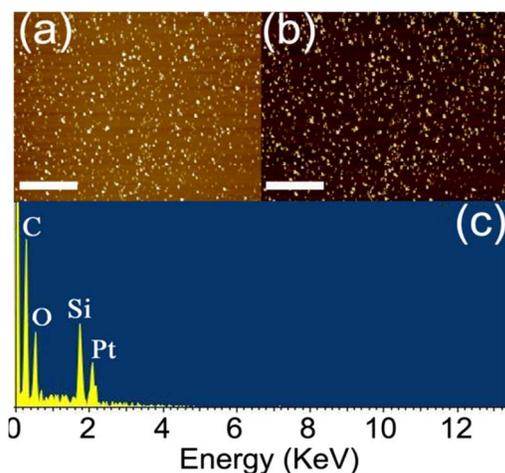


Fig. 7 (a) The AFM topology image of GO(500) film on Si substrate, the scale bar is 1 μm . (b) The corresponding phase image. (c) The EDX of the white dots in Fig. 7a, the Pt signal is from the sputtered Pt.

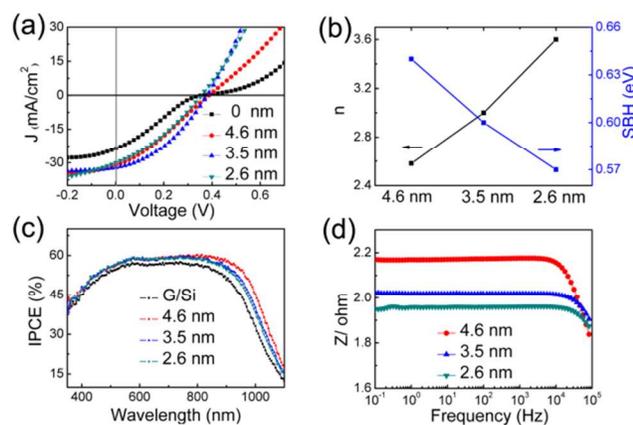


Fig. 8. (a) The change of PCE with δ . (b) The change of SBH and n with δ . (c) IPCE curves of G/GO(400)/Si solar cells with different δ . (d) Z_f measurements of G/GO(400)/Si solar cells with different δ .

It is found that further increasing annealing temperature (500 $^{\circ}\text{C}$) causes degradation in PCE. The surface becomes very rough ($R_q = 3.7$ nm, Table S1) after annealing at 500 $^{\circ}\text{C}$, which may be the main reason for the bad junction ($n=4.45$) and low SBH (0.55 eV). AFM topology image (Fig. 7a) suggests that the rough surface is caused by the white dots, which are identified as new substance by phase image (Fig. 7b). Two elements, Si and O, are detected by EDX as shown in Fig. 7c, suggesting that the white dots may come from the reactions of Si/SiO₂ with residual water/ oxygen at high temperature.³⁴ (see SI for details, Figure S11)

The effects of GO film thicknesses (δ) on device response is also investigated and there clearly exists an optimal thickness for device performance. GO(400) films with different δ are employed (δ is determined by AFM, see Fig. S5). Fig. 8a shows the change of PCE with δ . Clearly the best PCE is obtained with $\delta = 3.5$ nm. The statistical graphs of photovoltaic parameters are given in Fig. S8, G/GO _{$\delta=3.5$ nm}/Si devices have the best J_{sc} , V_{oc} , and FF, leading to the highest PCE. Fig. 8b gives the plots of n and SBH vs δ (the J vs $dV/d\ln J$ and J vs $H(J)$ plots are given in Fig. S9). SBH decreases (again the calculated result is consistent with the result obtained from equation (1), further showing that treating GO as a

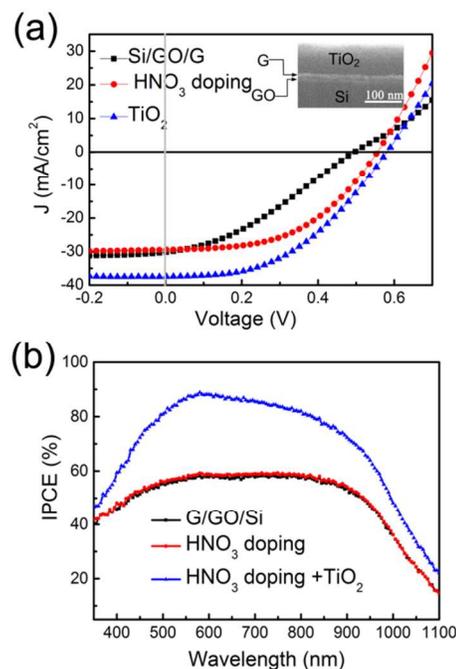


Fig. 9 (a) The PCE of a G/GO/Si solar cell after different treatment steps: pristine state (G/GO/Si, black curve), after HNO₃ doping (red curve) and after TiO₂ coating (blue curve). Inset shows a SEM cross-section image of the device. (b) The corresponding IPCE curves of the solar cell after different treatment steps.

p-doped layer is valid) while n increases with reducing δ . In addition, IPCE increases with increasing δ (Fig. 8c). It seems that larger δ is better for device performance. However, $Z_f/\delta=4.6\text{nm} > Z_f/\delta=3.6\text{nm} > Z_f/\delta=2.6\text{nm}$ (Fig. 8d), indicating that Z_f increases rapidly with increasing δ . As a result, there exist an optimal thickness for device performance.

The simple fabrication process and low cost make G/Si solar cell a competitive candidate for next-generation commercial solar cell. A major problem that hinders its commercialization is the low PCE (typically $< 10\%$). We show that the PCE can reach 12.3 % by further treating the G/GO/Si solar cells with chemical doping and antireflection coating. Here chemical doping is done by exposing the device to HNO₃ vapor and TiO₂ coating is employed as the antireflection coating.¹¹ The final structure of solar cells is Si/GO/G/TiO₂, as confirmed by the SEM cross-section image (inset of Fig. 9a) and the back-scattered electron image (Fig. S10). A typical Si/GO/G solar cell with PCE of 5 % is used (Fig. 9a, black curve), with $V_{oc} = 0.48$ V, $J_{sc} = 30.1$ mA/cm² and FF = 0.35. By doping graphene with HNO₃ (red curve), the PCE is increased to 8.2 %, with $V_{oc} = 0.55$ V, $J_{sc} = 29.4$ mA/cm² and FF = 0.5. After coating with an antireflection TiO₂ layer, the PCE is further improved to 12.3 %, with $V_{oc} = 0.57$ V, $J_{sc} = 37.4$ mA/cm² and FF = 0.57 (blue curve). HNO₃ doping mainly increases V_{oc} and FF, while TiO₂ coating mainly enhances J_{sc} . IPCE (Fig. 9b) also confirms this conclusion: after HNO₃ doping, there is little change in IPCE; while the IPCE is greatly enhanced after TiO₂ coating.

Conclusions

In conclusion, we demonstrate that interface tailoring can serve as

an effective approach towards high performance G/Si schottky-barrier solar cells. By inserting a GO film through a simple spin-coating process, the PCE can be increased by > 100 % compared with the reference devices. The critical role of GO in G/Si solar cells is systematically studied by varying the GO film annealing temperature and thickness. Unlike traditional thinking, i.e., GO acts as an insulator, it is found that GO can be treated as a p-doped material. This simple method offers us another choice to obtain high efficiency G/Si solar cells, which potentially opens up new opportunities for the next-generation high-efficiency and low-cost solar cells.

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Notes and references

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† Electronic Supplementary Information (ESI) available: [Fig. S1 to S14, Table S1 and S2]. See DOI: 10.1039/b000000x/

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