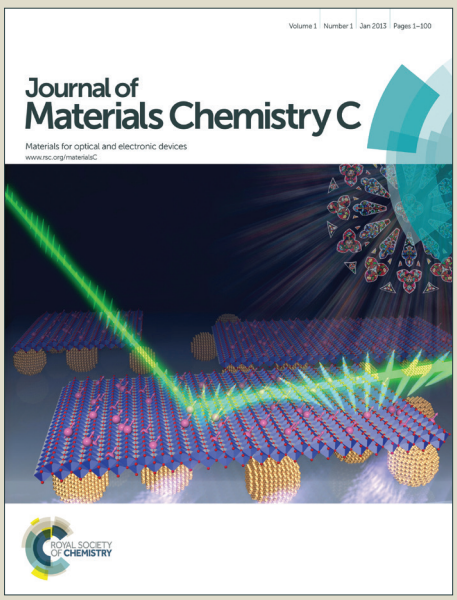
Journal of Materials Chemistry C

Accepted Manuscript



ROYAL SOCIETY OF CHEMISTRY

www.rsc.org/materialsC

Cite this: DOI: 10.1039/c0xx00000x

www.rsc.org/xxxxxx

ARTICLE TYPE

Selective n-Type Doping in Graphene via the Aluminium Nanoparticle Decoration Approach

Xiaoling Shi, ‡[a] Guofa Dong, ‡[ab] Ming Fang, ‡[ab] Fengyun Wang,[c] Hao Lin,[ab] Wen-Chun Yen,[d] Kwok Sum Chan, [ab] Yu-Lun Chueh [d] and Johnny C. Ho[ab]*

Received (in XXX, XXX) Xth XXXXXXXXX 20XX, Accepted Xth XXXXXXXXX 20XX
DOI: 10.1039/b000000x

Selective and reliable n-type doping as well as tuning the Dirac point of graphene are important for the realization of high-performance complementary circuits. In this work, we present a simple but effective technique to left shift the Dirac point of graphene transistors to induce n-type doping via the thermal decoration of Al nanoparticles. The decorated discrete nanoparticles are uniformly distributed on top of the graphene channel surface with the consistent size and shape. Detailed electrical measurements reveal that the decoration can efficiently shift the Dirac point of graphene towards negative gate voltages along with the improved on/off current ratio and excellent air-stability. All these further indicate the technological potency of this doping technique for the fabrication of future CMOS graphene electronics.

Introduction

Due to the unique chemical, electrical, optical and thermomechanical properties, graphene has aroused a widespread interest in recent years.[1-10] However, many practical technological applications of graphene are inherently handicapped by its semi-metal nature. For example, selective doping as well as tuning the Dirac point of graphene are the key areas drawing the tremendous attention, since the reliable control in carrier concentration is necessary to construct integrated graphene devices with complicated architectures such as diodes, transistors and logic gates.[11-17] Even though both p- and n-type doping are equally important for the development of high-performance graphene-based electronic devices, the realization of n-type semiconducting graphene is imperative for the complementary circuit since the p-type graphene channel can be readily prepared by chemical vapour deposition (CVD) growth due to the unintentional p-type doping induced by the oxygen and moisture or solution based transfer processes.[18-25] In this regard, various methods have been proposed to fabricate n-type graphene transistors employing the surface dopants of nitrogen or phosphorus atoms[26-31] or metallic thin films.[32-34] Doping with the incorporation of nitrogen and phosphorus dopants into the carbon lattice can lead to the n-type transport characteristics in graphene;[22,35] but at the same time, all these dopants can introduce defects into the lattice which may deteriorate the resulting carrier mobility.[23-24] While in the thin film cases, Kim at al. have recently reported the n-type doping in graphene utilizing the deposition of photo-patterned gold nanoparticles.[36] In any case, these fabricated n-type graphene devices have very limited air stability, being sensitive to the influence of ambient environment; therefore, it is still remained a challenge to achieve the air-stable n-type semiconducting properties of graphene. In this report, we present a simple but effective technique to left shift the Dirac point of graphene transistors inducing n-type doping via the thermal decoration of Al nanoparticles and Al_2O_3 passivation layer. The morphologies of these Al nanoparticles are carefully characterized with atomic force microscopy (AFM). Combined with the detailed electrical measurements, it is revealed that the Al-decorated graphene devices exhibit impressive on/off current ratio and the corresponding electrical properties are highly dependent on the dimension of deposited Al nanoparticles.

Experimental Section

Growth and transfer of monolayer graphene:
Here, we successfully grew monolayer graphene using low pressure CVD on copper foils and optimized the graphene transfer onto the Si/SiO_2 substrates. In brief, copper foils were first annealed at 1000 ^oC for 30 to 45 minutes in the H_2/Ar environment at a process pressure of 300 mTorr and then methane was introduced through the feeding of $CH_4/Ar/H_2$ mixture at a higher process pressure of 500 mTorr for 30 minutes. Next, the entire system was cooled down to room temperature where graphene percolated on the surface of the copper foils. The foils were covered by Poly(methyl methacrylate) (PMMA) to protect the top surface while O_2 plasma treatment was performed on the backside to remove any graphene growth. Later, the copper foils were etched in the commercial copper etchant for 30 minutes, transferred to 10 % HCl/DiH_2O solution and then rinsed with DiH_2O for multiple times. Finally, the graphene layer was transferred onto the Si/SiO_2 substrates with 50 nm thick thermal grown oxide as the gate-dielectric and annealed at 500 ^oC for 2 hours in the ambient of H_2/Ar (150 SCCM and 400 SCCM, respectively) to remove the PMMA.

Fabrication of graphene field-effect transistors:
The back-gated graphene field-effect transistors (FETs) studied in

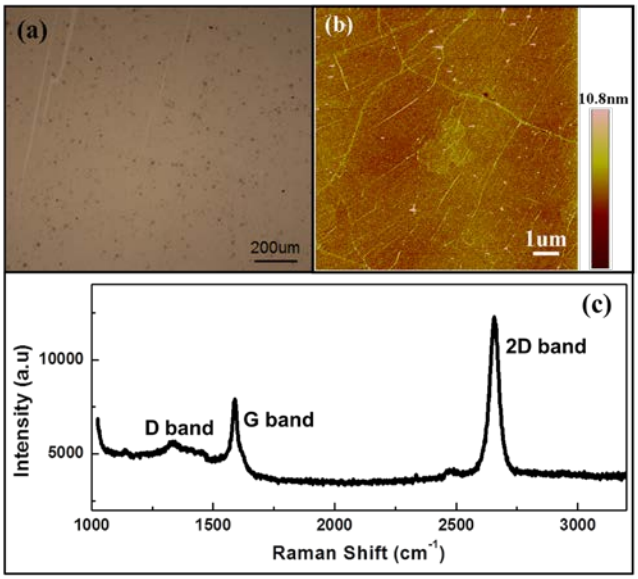


Figure 1. Characterization of the synthesized and transferred graphene layer. (a) Optical microscope image, (b) AFM topography image and (c) Raman spectrum (514 nm wavelength excitation).

this work were fabricated as follows. The source/drain electrode region was first patterned by photolithography. The Cr (5 nm) and Au (90 nm) metal layers were deposited onto the photoresist pattern by electron beam evaporation, followed by a lift-off process. After the metal patterning, the graphene channels [Device Type A: channel width (W) = 3 μm, channel length (L) = 10 μm and Device Type B: W = 5 μm, L = 10 μm] were defined utilizing photolithography and subsequent reactive ion etching (RIE) in an oxygen ambient. The RIE was performed for 30 s at 100W at room temperature with 5 mTorr of O_2. Afterwards, Al nanoparticles were decorated onto the graphene channels with different nominal thicknesses employing thermal evaporation. Notably, the 30 nm thick Al_2O_3 protective layer was deposited as well to prevent Al nanoparticles from further oxidation.[37] Schematic of the Al decorated graphene FET device structure is illustrated in Supporting Figure S1(a) while the corresponding top-down SEM image is depicted in Figure S1(b).

Results and discussion

As shown in the microscope image in Figure 1a, we have successfully synthesized and transferred the large-scale monolayer layer graphene onto the Si/SiO_2 substrates. The AFM image (Figure 1b) indicates the corresponding grain structure and wrinkles of the transferred graphene. From the AFM analysis, the thickness of this monolayer graphene is about 1 nm. Notably, the Raman mapping of this graphene in Figure 1c gives the very weak intensity of D band at ~1350 cm^{-1}, which suggests the minimal defect concentration here. Also, the 2D band is very sharp and symmetric at ~2660 cm^{-1} with the full-width-at-half-maximum (FWHM) of ~39 cm^{-1} as well as the intensity ratio of G/2D is less than 1. All these confirm the excellent crystal quality of as-synthesized graphene layer utilized in this work.[38]

In order to investigate the effect of Al nanoparticle decoration on the fabricated graphene FETs, various thickness of Al film were

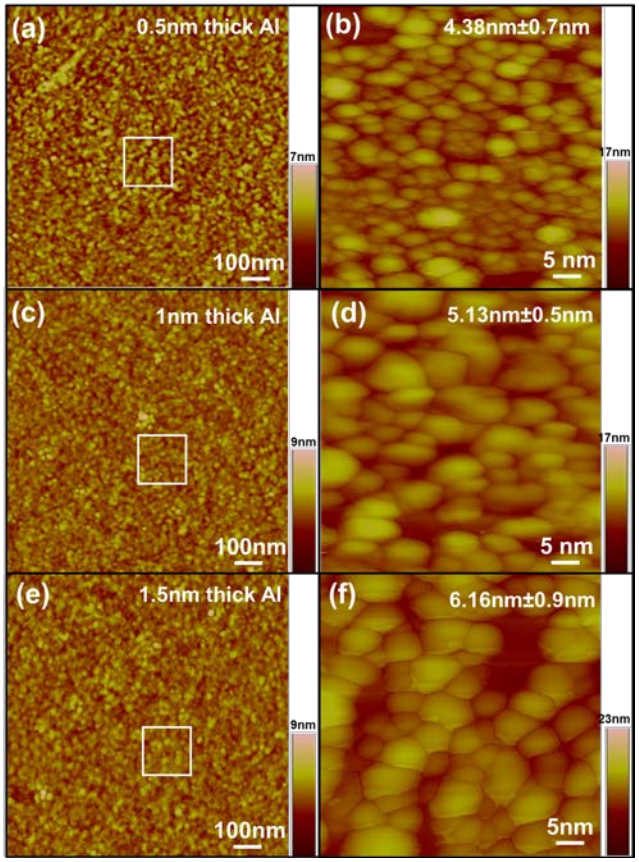


Figure 2. AFM topography images of graphene layer with different Al decoration thicknesses. (a) and (b) 0.5 nm, (c) and (d) 1.0 nm, (e) and (f) 1.5 nm. White colored square boxes designate the zoom-in characterization region. Statistics of the decorated nanoparticle size are given in the top right corner.

deposited on the graphene layer. As presented in the AFM images in Figure 2, the topography of three different decoration thicknesses are revealed, which corresponds to the nominal Al deposition thickness of 0.5, 1.0 and 1.5 nm, respectively. Based on the statistic of more than 50 individual particles from AFM images, the average size of Al nanoparticles is determined to be 4.38 nm ± 0.7 nm, 5.13 nm ± 0.5 nm and 6.16 nm ± 0.9 nm, accordingly (Supporting Information Figure S2). This relatively narrow particle size distribution is remarkably good considering the simplicity of this simple thermal evaporation technique as compared to the variation of commercially available colloidal metal nanoclusters. Importantly, this reasonably well particle size control can give us the capability to modulate the decorated cluster dimension in the subsequent studies.

At the same time, two kinds of FET devices (device type A with a channel width of 3 μm and device type B with a channel width of 5 μm) were prepared for electrical transport measurements before and after the nanoparticle decoration in order to evaluate the decoration effect on different device geometries. During the FET measurement, 1.0 V bias was applied between the source and drain while a variable gate bias, V_{GS}, ranging from -20 to +40 V, was applied to the highly doped Si, which served as a back-gate. Sequentially, the source-drain current (I_{DS}) was monitored as

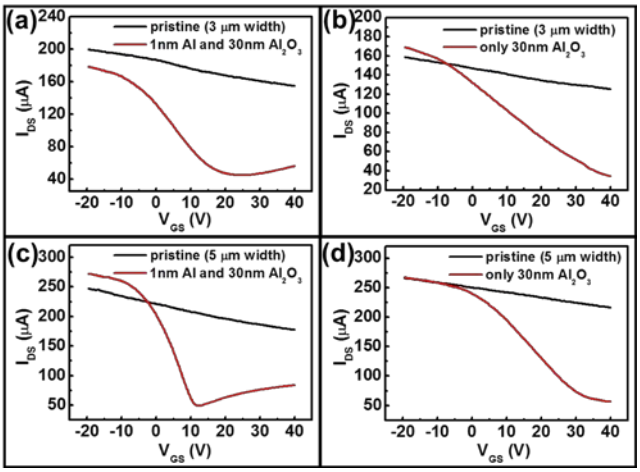


Figure 3. Transfer characteristics of Al nanoparticle decorated graphene FETs. (a) and (c) decoration thickness of 1.0 nm capped with 30 nm Al_2O_3 for the device type A (3 μm channel width) and device type B (5 μm channel width), respectively, (b) and (d) no decoration capped with only 30 nm Al_2O_3 for device type A and B, respectively.

a function of V_{GS} to assess the corresponding transfer characteristics of graphene FETs. As depicted in Figure 3, the graphene devices exhibit p-type behaviour due to the unintentional doping from defects and pre-existing adsorbates, such as the oxygen and water in air.[18-25] In this case, the black curves give the I_{DS}-V_{GS} relationship of pristine graphene before the decoration. One can see that the I_{DS} increases slowly with decreasing V_{GS} and the on/off ratio is about 1.3. The gate dependence of maximum resistance defines the position of the Dirac point, which does not show up within the measured range. However, after the 1 nm Al decoration, the pure p-type characteristic is transformed into the ambipolar behaviour with significant n-type conduction, indicating a successful n-type doping in these devices (Figure 3a and c). Also, the Dirac point is then shifted to ~20 V and ~10 V for device type A and B, corresponding to the hole concentration of 1.78×10^{12} cm^{-2} and 0.87×10^{12} cm^{-2}, respectively (Supporting Information), and the on/off current ratio is enhanced to ~4 to 6 times without any significant change in the on-current, as compared to those before the decoration. It is noted that the n-type doping phenomenon is more pronounced for the wider device channel (Supporting Information Figure S3 and S4), which is expected owing to the suppressed edge effect as compared to the narrower ones since the oxygen plasma defined edges could behave as p-type dopants. In future, edge passivation may be further needed to improve the n-doping effect, especially for narrow channel graphene FETs. More importantly, the decorated devices show consistent electrical results even after ten days of exposure in the ambient, indicating the long-term air-stability with this simple doping technique.

To shed light to verify the doping effect coming from the Al decoration, not the protective Al_2O_3 layer, other devices with the same dimension are also deposited with only a pure 30 nm thick Al_2O_3 layer as the control. As illustrated in Figure 3b and d, the Al_2O_3 layer cannot move the Dirac point; instead it does improve the on/off current ratio to ~4 to 6 times due to the passivating

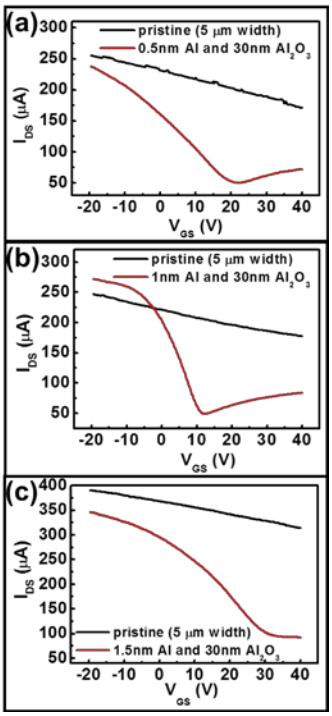


Figure 4. Transfer characteristics of Al nanoparticle decorated graphene FETs with different decoration thicknesses. (a) 0.5 nm, (b) 1.0 nm and (c) 1.5 nm.

effect in minimizing the exposure to ambient, which helps to eliminate the hydroxyl, oxygen and water related molecules adsorbed onto the graphene channel.[37,39] Another set of control samples are as well performed on the same device structure without the active graphene channel layer, and as expected no current can be measured (Supporting Information Figure S5), which indicates our nanoparticles are still disconnected at the decoration thickness of 1 nm. All these can experimentally confirm the role of Al nanoclusters in the n-type doping and left-shifting of the Dirac point of graphene.

It should also be noted that the doping effect of Al nanoparticle decoration on graphene FETs is observed to depend highly on the particles size. As shown in Figure 4, when the nominal decoration thickness is increased from 0.5 to 1.5 nm, the Dirac point is first shifted towards the negative voltages from +20 to +10 V and then moved back to +30 V. The maximum left-shifting of the Dirac point is corresponded to the decoration thickness of 1 nm, which suggests that as the nanoparticle size is too small (i.e. 0.5 nm thickness), the isolated nanoparticles have insignificant contact area with the graphene channel to achieve the maximum doping effect; whereas for the too large particle size (i.e. 1.0 nm thickness), the nanoparticles start to coalescence towards a continuous thin in reducing the electronic doping level of graphene such that the Dirac point is moved back to the positive gate voltages. We notice that in a previous numerical study,[40] the Fermi level shift of graphene illustrates a strong dependence on the graphene-metal surface separations, as the different distance means different intensities of interactions between the two bodies. In this case, when the Al gets thicker and become a quasi-film, the equilibrium separations between graphene and Al gets

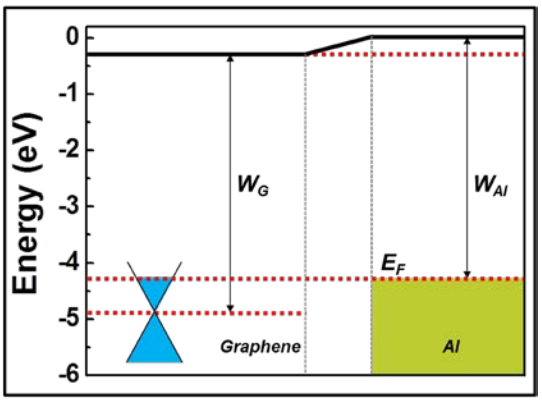


Figure 5. Schematic illustration of the relationship between Fermi energy and work function along the graphene/nanoparticle contact interface.

larger because of the surface wrinkling/fluctuation of the graphene; as a result, the doping effect of Al gets weaker this way. Further increase of the Al particle size would form a continuous conducting mesh turning the graphene into metallic.

To intuitively understand the physical mechanism of this Al nanoparticle decoration, Figure 5 shows the effective potential along the graphene/nanoparticle contact interface. It is all known that the work function of Al nanoparticles (W_{Al} = 4.28 eV) is lower than that of the pristine graphene (W_G = 4.6 eV). When the nanoparticles are deposited onto the graphene surface, due to the large negative work function difference (W_{Al}-W_G), there would be an upshift resulted for the graphene Fermi energy. Specifically, the left valley represents the potential of graphene while the right valley represents the potential of Al. Driving from the potential difference, electrons would be donated from the Al particles and be injected into the graphene creating a built-in electric field in the same direction. This way, the transferred electrons will raise the Fermi level and achieve n-type doping in the graphene here.

Apart from Al, the doping effect of other metal nanoparticle decoration such as Sn has also been investigated. It is found that the Sn decoration could also shift the Dirac point of same graphene FETs to +20 V, which was not as efficient as compared to the n-type doping case of Al (Supporting Information Figure S6). It is due to the fact that Sn has a work function of 4.42, which is larger than the one of Al, then the induced Fermi energy up-shift of graphene would not be as large to result the same amount of energy transfer for the n-type doping. More studies on the further control in this doping technique on graphene are currently in the process.

Conclusions

In conclusion, a simple n-type doping technique to left shift the Dirac point of graphene transistors via the thermal decoration of Al nanoparticles is presented. The morphologies of these Al nanoparticles on graphene are carefully characterized, suggesting that the particles are distributed with relatively uniform size and shape. Combined with the detailed electrical measurements, the decorated graphene devices exhibit an obvious left-shifting of the Dirac point inducing the efficient n-type doping along with the impressive on/off current ratio and excellent air-stability. All these indicate the technological potency of this decoration technique for the reliable n-type doping for future fabrication of graphene devices.

Acknowledgements

This research was supported by the City University of Hong Kong (Project no. 9610180), the National Natural Science Foundation of China (grant number 51202205), the Science Technology and Innovation Committee of Shenzhen Municipality (Grant JCYJ20120618140624228) and the Ministry of Science and Technology of the Republic of China through Grant. 101-2112-M-007-015-MY3.

Notes and references

[a] *Department of Physics and Materials Science, City University of Hong Kong, 83 Tat Chee Avenue, Kowloon Tong, Kowloon, Hong Kong, People's Republic of China. E-mail: johnnyho@cityu.edu.hk*
[b] *Shenzhen Research Institute, City University of Hong Kong, Shenzhen, People's Republic of China*
[c] *Cultivation Base for State Key Laboratory, Qingdao University, No. 308 Ningxia Road, Qingdao, People's Republic of China*
[d] *Department of Materials Science and Engineering, National Tsing Hua University, No. 101 Sec. 2 Kuang-Fu Road, Hsinchu, 30013, Taiwan*

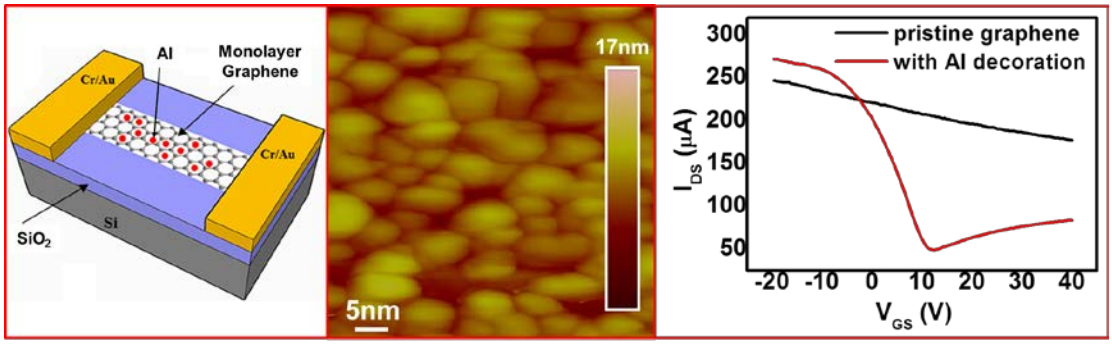
† Electronic Supplementary Information (ESI) available: Schematic and SEM image of the Al decorated graphene FET; electrical measurement on the control device without the active graphene channel layer; electrical measurement of the typical Sn decorated graphene FET. See DOI: 10.1039/b000000x/

‡ These authors contributed equally to this work.

1 K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, A. A. Firsov, *Science*, 2004, **306**, 666.
2 Y. B. Zhang, Y. W. Tan, H. L. Stormer, P. Kim, *Nature*, 2005, **438**, 201.
3 K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, M. I. Katsnelson, I. V. Grigorieva, S. V. Dubonos, A. A. Firsov, *Nature*, 2005, **438**, 197.
4 J. S. Bunch, A. M. van der Zande, S. S. Verbridge, I. W. Frank, D. M. Tanenbaum, J. M. Parpia, H. G. Craighead, P. L. McEuen, *Science*, 2007, **315**, 490.
5 J. R. Williams, L. DiCarlo, C. M. Marcus, *Science*, 2007, **317**, 638.
6 S. Watcharotone, D. A. Dikin, S. Stankovich, R. Piner, I. Jung, G. H. B. Dommett, G. Evmenenko, S. E. Wu, S. F. Chen, C. P. Liu, S. T. Nguyen, R. S. Ruoff, *Nano Lett.*, 2007, **7**, 1888.
7 X. Du, I. Skachko, A. Barker, E. Y. Andrei, *Nat. Nanotechnol.*, 2008, **3**, 491.
8 M. D. Stoller, S. Park, Y. Zhu, J. An, R. S. Ruoff, *Nano Lett.*, 2008, **8**, 3498.
9 I. -W. P. Chen, S. -H. S. Jhoua, Y. -W. Chen, *J. Mater. Chem. C.*, 2013, **1**, 5970.
10 C. M. Lee, K. S. Chan, J. C. Ho, *Journal of the Physical Society of Japan*, 2014, **83**, 034007.
11 T. Ohta, A. Bostwick, T. Seyller, K. Horn, E. Rotenberg, *Science*, 2006, **313**, 951.
12 B. Huard, J. A. Sulpizio, N. Stander, K. Todd, B. Yang, D. Goldhaber-Gordon, *Phys. Rev. Lett.*, 2007, **98**, 236803.
13 B. Oezyilmaz, P. Jarillo-Herrero, D. Efetov, D. Abanin, L. S. Levitov, P. Kim, *Phys. Rev. Lett.*, 2007, **99**, 166804.
14 T. Lohmann, K. V. Klitzing, J. H. Smet, *Nano Lett.*, 2009, **9**, 1973.
15 U. Bangert, A. Bleloch, M. H. Gass, A. Seepujak, J. van den Berg, *Phys. Rev. B*, 2010, **81**, 245423.
16 F. M. Koehler, A. Jacobsen, K. Ensslin, C. Stampfer, W. J. Stark, *Small*, 2010, **6**, 1125.
17 K. C. Kwon, B. J. Kim, J. -L. Lee, S. Y. Kim, *J. Mater. Chem. C.*, 2013, **1**, 2463.
18 T. B. Martins, R. H. Miwa, A. J. R. Silva, A. Fazzio, *Phys. Rev. Lett.*, 2007, **98**, 196803.

19 F. Schedin, A. K. Geim, S. V. Morozov, E. W. Hill, P. Blake, M. I. Katsnelson, K. S. Novoselov, *Nat. Mater*., 2007, **6**, 652.
20 T. O. Wehling, K. S. Novoselov, S. V. Morozov, E. E. Vdovin, M. I. Katsnelson, A. K. Geim, A. I. Lichtenstein, *Nano Lett*., 2008, **8**, 173.
21 X. Wang, X. Li, L. Zhang, Y. Yoon, P. K. Weber, H. Wang, J. Guo, H. Dai, *Science*, 2009, **324**, 768.
22 B. Guo, Q. Liu, E. Chen, H. Zhu, L. Fang, J. R. Gong, *Nano Lett*., 2010, **10**, 4975.
23 D. Wei, Y. Liu, Y. Wang, H. Zhang, L. Huang, G. Yu, *Nano Lett*., 2009, **9**, 1752.
24 Y. C. Lin, C. Y. Lin, P. W. Chiu, *Appl. Phys. Lett*., 2010, **96**, 133110.
25 N. Li, Z. Wang, K. Zhao, Z. Shi, Z. Gu, S. Xu, *Carbon*, 2010, **48**, 255.
26 X. Wang, X. Li, L. Zhang, Y. Yoon, W. Weber, H. Wang, J. Guo, H. Dai, *Science*, 2009, **324**, 768.
27 X. Li, H. Wang, J. Robinson, H. Sanchez, G. Diankov, H. Dai, *J. Am. Chem. Soc*., 2009, **131**, 15939.
28 X. Dong , D. Fu , W. Fang , Y. Shi , P. Chen , L. Li , *Small*, 2009, **5**, 1422.
29 D. B. Farmer, R. Golizadeh-Mojarad, V. Perebeinos, Y. Lin, G. Tulevski, J. Tsang, P. Avouris, *Nano Lett*., 2009, **9**, 388.
30 Z. Jin, J. Yao, C. Kittrell, J. M. Tour, *ACS Nano*, 2011, **5**, 4112 .
31 P. Wei, N. Liu, H. R. Lee, E. Adijanto, L. Ci, B. D. Naab, J. Q. Zhong, J. Park, W. Chen, Y. Cui, Z. Bao, *Nano Lett*., 2013, **13**, 1890.
32 J. H. Chen, C. Jang, S. Adam, M. S. Fuhrer, E. D. Williams, M. Ishigami, *Nat. Phys*., 2008, **4**, 377.
33 K. Pi, K. M. McCreary, W. Bao, W. Han, Y. F. Chiang, Y. Li, S. W. Tsai, C. N. Lau, R. K. Kawakami, *Phys. Rev. B*, 2009, **80**, 075406.
34 K. M. McCreary, K. Pi, R. K. Kawakami, *Appl. Phys. Lett*., 2011, **98**, 192101.
35 D. Usachov, O. Vilkov, A. Grüneis, D. Haberer, A. Fedorov, V. K. Adamchuk, A. B. Preobrajenski, P. Dudin, A. Barinov, M. Oehzelt, *Nano Lett.*, 2011, **11**, 5401.
36 S Huh, J. Park, K. Kim, B. H. Hong, S. B. Kim, *ACS Nano*, 2011, **5**, 3639.
37 N. Han, F. Wang, J. J. Hou, S. P. Yip, H. Lin, F. Xiu, M. Fang, Z. Yang, X. Shi, G. Dong, T. F. Hung, J. C. Ho, *Advanced Materials*, 2013, **25**, 4445.
38 A. C. Ferrari, J. C. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K. S. Novoselov, S. Roth, A. K. Geim, *Phys. Rev. Lett*,. 2006, **97**, 187401.
39 C. G. Kang, Y. G. Lee , S. K. Lee, E. Park, C. Cho, S. K. Lim, H. J. Hwang, B. H. Lee, *Carbon*, 2013, **53**, 182.
40 G. Giovannetti, P. Khomyakov, G. Brocks, V. Karpan, J. van den Brink, and P. Kelly, *Phys. Rev. Lett.*, 2008, **101**, 026803.

TOC



A simple and effective technique is presented to left shift the Dirac point of graphene transistors to induce n-type doping via the thermal decoration of Al nanoparticles. The versatility of this approach is illustrated by the fabrication of air-stable n-type doping in graphene devices with the improved on/off current ratio, which further indicate the technological potency of this doping technique for the construction of future CMOS graphene electronics.