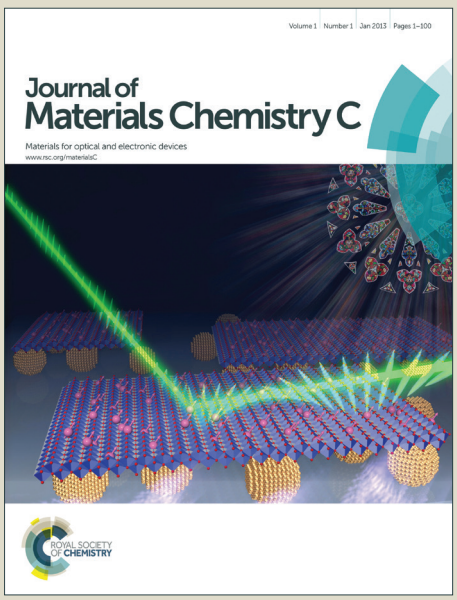
Journal of Materials Chemistry C

Accepted Manuscript



ROYAL SOCIETY OF CHEMISTRY

www.rsc.org/materialsC

Journal Name

RSCPublishing

ARTICLE

Fabrication of locally thinned down silicon nanowires

Cite this: DOI: 10.1039/x0xx00000x

Phu Duy Tran[a], Bernhard Wolfrum[b], Regina Stockmann[b], Andreas Offenhausser[b] and Benjamin Thierry[a*]

Received 00th January 2012,
Accepted 00th January 2012

DOI: 10.1039/x0xx00000x

www.rsc.org/

We report a new and controlled top-down fabrication process to prepare locally thinned down silicon nanowire field-effect devices at wafer-scale. In this process, a low temperature size reduction method based on optimized tetramethylammonium hydroxide wet-etching has been developed on silicon (100) to yield slow (~ 0.5 nm s^{-1}) and controllable etching speed as well as ultra-smooth silicon surface morphology (rms ~ 0.15 nm). Combined with electron beam lithography, arrays of monocrystalline silicon nanowires with locally confined thicknesses down to sub-20 nm, lateral dimensions of 150 nm, and lengths of 10 µm were reliably prepared and used. This novel fabrication process provides an alternative route for the fast and reliable preparation of ultrathin silicon nanostructures that can be easily integrated in nanodevices.

1. Introduction

Owing to quantum confinement effects, silicon nanowires (SiNWs) with sub-30 nm in thickness are one of the most promising nanotechnology constructs and their exciting potentials has already been demonstrated in a range of devices with extraordinary electrical performances (e.g. high carrier mobility, high drive current, near ideal sub-threshold slop and high current on/off ratio)[1-4]. SiNWs are actively being integrated in hybrid nano scale devices for towards applications in bio-sensing,[5] and photovoltaics[6-8] for instance. However, the technological fabrication, implementation and efficient integration within functional devices of such thinned down SiNWs remain challenging for both synthetic bottom-up[9, 10] and top-down fabrication approaches[1, 3, 4, 11]. Unlike synthetic routes, top-down fabrication can produce highly ordered SiNWs with superior integration efficiency into functional device. It is also compatible with standard packaging techniques (e.g. lithography, microscopic contact formation and packaging). When it comes to sub-30 nm SiNWs however, current top-down fabrication techniques are limited. The latter techniques relies on either the use of conformal top silicon layer silicon-on-insulator (SOI) wafer for patterning structures[1, 3, 11, 12] or high temperature oxidation trimming of the patterned silicon structures[4, 13]. Although preparation of wafer-scale thinned down nanowire structures using these methods is straightforward, impurity doping and efficient metal interconnect formation are still in difficulty due to the thickness confinement of the silicon device structures. The local oxidation on silicon (LOCOS) approach has been advanced recently to improve the fabrication of SiNWs with sub-30 nm thicknesses[14, 15]. However, the inherent limitations of LOCOS are on its long fabrication process with multiple steps (e.g. silicon nitride deposition, patterning, oxidation), bird's beak formation and stress induced silicon defect. These limitations make LOCOS less compatible with large-scale fabrication of thinned down silicon nanowires. Thin SiNWs could also be fabricated using photo-electrochemical size-reduction etching[16]. This technique is less complicated than LOCOS but it is difficult to effectively control the dimensions and the surface roughness of the resulting nanowires.

In this work, we present an improved and straightforward wafer-scale fabrication process of thinned down SiNWs with local thicknesses down to sub-20 nm. The key feature of the proposed approach is the use of a simple and low-temperature size reduction method to precisely thin down silicon nanowires. The latter is achieved through an optimized tetramethylammonium hydroxide (TMAH) wet-etching step combined with conformal masking. The TMAH wet-etching has been optimized by adjusting the etching temperature and using isopropanol as an additive, resulting in a very low (~ 0.5 nm s^{-1}) and controllable etching rate at near room temperature (35°C). Importantly, the optimized process creates atomic smooth silicon etched surface (rms ~ 0.15 nm) required to achieve high quality field-effect devices. Taking advantage of this optimized etching method, SiNW (width 150 nm, length 10 µm) arrays prepared at the wafer-scale could be locally thinned-down with high precision using a simple photomasking step without impacting on the dimensions of the other structures. This novel approach therefore mitigates on the issues of impurity doping and device integration typically associated with ultrathin silicon nanostructures. Electrical and electrochemical characterizations on the prepared locally thinned down SiNWs devices are also presented in this work.

2. Experimental

2.1 Optimized TMAH wet etching with isopropyl alcohol additive

The first aim of our fabrication process was to develop a very slow and therefore well-controlled TMAH wet-etching process yielding high surface smoothness for the (100) silicon. Although, the optimization of TMAH etching on silicon (100) has been reported elsewhere[17-19], the optimization of TMAH wet-etching at near room

temperature for locally confining silicon nanowire structures is still unreported. To conduct this study, (100) SOI substrate was first diced in small samples (3cm x 3cm) and subsequently cleaned using Piranha solution (2:1 v/v 30% H_2O_2:H_2SO_4). The cleaned silicon samples were then immersed in 1% HF solution in 30 seconds to remove native SiO_2 before conducting the time controlled TMAH wet etching. To maximize the surface smoothness, the etching solutions were prepared by mixing TMAH $(CH_3)_4NOH$ (25wt%; Riedel-de-Haen) with pure isopropyl alcohol (IPA). 10 vol % IPA and 90 vol% TMAH was determined as an optimum etching solution and the etching was conducted at temperatures of 35 ^oC, 45 ^oC, 55 ^oC and 65 ^oC in a wet-etching bath equipped with a heating system and gentle agitation. Etching rates were calculated using thickness profiles obtained from spectroscopic ellipsometry measurements (Sentech SE800) and the roughness of the etched samples were determined by atomic force microscopy (AFM) (Zeiss-Axiotech/SIS).

2.2 Fabrication of locally thinned down silicon nanowire devices

The fabrication process of locally thinned down SiNWs is briefly illustrated in Fig. 1. In this process, Unibond SOI wafers (SOITEC; p-doped to $1x10^{15}$ cm^{-3}) with 145 nm of buried oxide and a 70 nm top silicon layer were used. The process was initialized with an optimized dry oxidation step at 1000^oC to form a silicon dioxide (SiO_2) layer of approximately 45 – 50 nm as a mask for the TMAH wet-etching step. Subsequently, a bilayer of PMMA photoresist (150 nm of PMMA 200K/ 220 nm of PMMA 600K) was deposited on the wafer and structured by means of electron beam writing (Leica EBPG 5000+, 50kV, dose: 250μC cm^{-2}) followed by a resist development (Fig. 1a). The nanowire patterns were carefully aligned along the <110> wafer direction in order to enable the fabrication of reliable nanowire arrays at the whole wafer scale during the wet-etching step. A 40 nm of aluminum pattern was then formed on the structured wafer via e-beam deposition followed by a lift-off step in acetone. The aluminum pattern was used as a metallic mask for protecting the SiO_2 structure beneath during subsequent reactive ion etching (CHF_3, 20 sccm gas flow and 0.02 mbar of chamber pressure). The dry etching was time-controlled to stop right on top of the silicon to minimize the damage to the nanowire. Next, the entire aluminum mask was removed by using an aluminum etchant AZ MIF 326 followed by a standard RCA cleaning step to remove remaining metallic ions on the wafer. The wafers were then processed through the first wet-etching step (TMAH 25wt%; etching temperature at 80^oC, agitation) in 2 minutes and immediately immersed in de-ionized water to stop the etching. Silicon nanowire arrays were revealed on the wafer by removing the SiO_2 mask in 1% HF solution for 12 minutes (Fig. 1b). After fabricating the SiNWs arrays, a 15 nm of dry-oxidized SiO_2 (820 ^oC; 150 minutes) was formed on the patterned wafers. Standard photolithography was then employed to open a window in the middle section of the nanowire arrays, which was used to remove exposed SiO_2 layer using HF 1% etching (Fig. 1c). In the next step, the wafers were step-etched using the optimized TMAH wet-etching process for 40 seconds and 50 seconds (25wt% TMAH with 10vol% IPA, 35 ^oC, agitation) aiming to thin down the SiNWs by 20 nm and 25 nm respectively. The remaining SiO_2 mask was then removed by HF 1% solution (Fig. 1d). Two SiNW arrays were randomly chosen for both etching time, sectioned using focused ion beam and observed using SEM to determine the thicknesses of the resulting silicon nanostructures.

Towards their integration into functional devices, the fabricated nanowires were subjected to a selective ion implantation (B, $1x10^{15}$ ion cm^{-2}) at the contact regions followed by a thermal activation step at 900^oC for 30 minutes to activate the dopant. Afterward, electrical feed lines for the nanowire arrays were created by lift-off 300 nm of aluminum followed by a short thermal annealing (400^oC, N_2/H_2 gas - 20:1 sccm). A thick hard-baked AZ 1518 photoresist (~1.5 μm) was employed as a passivation layer for the protection of the contact regions during the wet-characterization step later on. Finally, the wafer was diced in small silicon chips with a typical size of 18 x 8 mm and then was packaged in ceramic chip holder. Each diced chip contains 4 independent ultra-thin silicon nanowire arrays, which are connected separately to the aluminum contact lines.

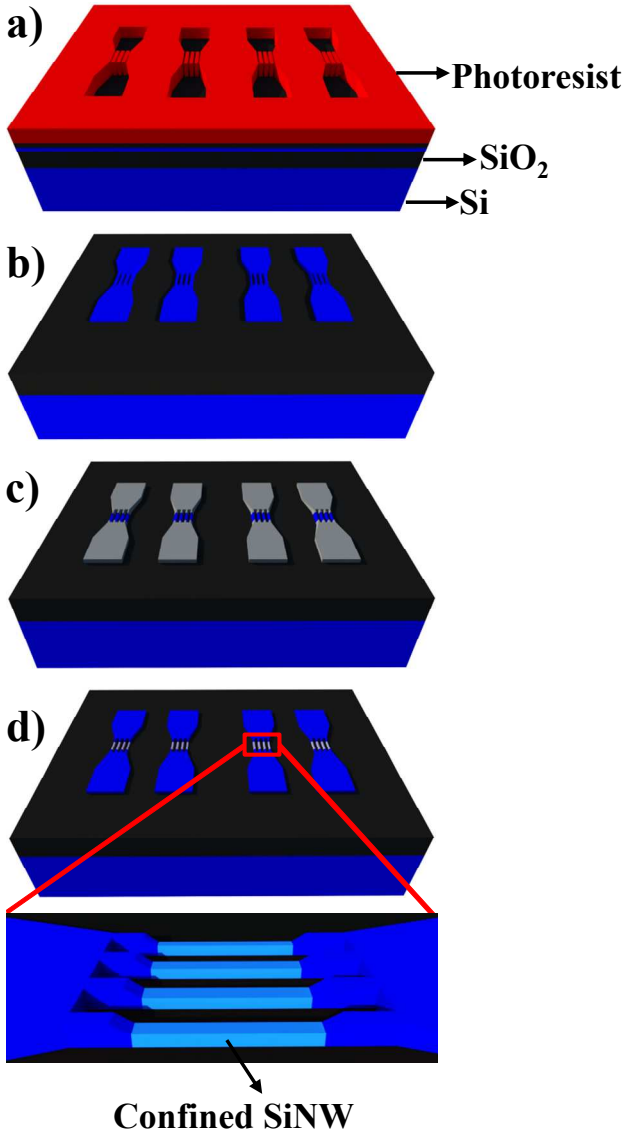


Fig. 1 Fabrication process of locally thinned down silicon nanowires. (a) and (b) fabrication of silicon nanowire by e-beam patterning and wet-etching. (c) and (d) locally thinning down silicon nanowires by conformal masking and optimized TMAH wet-etching.

3. Results and Discussion

3.1. Optimization of TMAH wet-etching

The surface roughness of nanowire has a significant impact on their electronic transport properties[20-22]. It has been reported that low surface roughness is an important criteria to obtain optimal

performances for nanowire field-effect devices[22]. To this end, the first aim of this work was to develop a very slow and therefore well-controlled silicon etching process yielding high surface smoothness for the fabrication of high quality thinned silicon nanowires. In micro-nanofabrication, isopropyl alcohol has been known as an inhibitor to slow down the TMAH etching processes and significantly improve the surface smoothness of the etched silicon due to the inhibition phenomena of IPA molecules onto silicon surface[17, 18]. Using 10% IPA additive, our ellipsometric measurements revealed that the etching rates decrease by a factor of two as the etching temperature is reduced by 10 °C (Fig. 2). The maximum etching rate obtained in our study is 3.2 nm s^{-1} (~192 nm min^{-1}) at 65 °C while the minimum one is ~ 0.5 nm s^{-1} (~ 30 nm min^{-1}) at 35 °C, which is among the slowest etching rates based on TMAH on (100) silicon reported. When the etching temperature was further reduced (e.g. 25°C or lower), no detectable etching of the silicon occurred.

Next we studied the effect on the surface morphology of the temperature at which the etching is performed. Atomic force microscopy showed that IPA/TMAH etched samples possessed atomically smooth surfaces with rms roughness in the 0.15 nm range which is comparable to that of pristine silicon samples as well as that of a thinned-down sample using the standard combination of dry-oxidation and HF 1% etching (Fig. 3). From these studies and in view of our requirements for the local thinning down of SiNW arrays at the wafer-scale, the optimum wet-etching process has been identified to be 35 °C and 25wt% TMAH with 10vol% IPA additive.

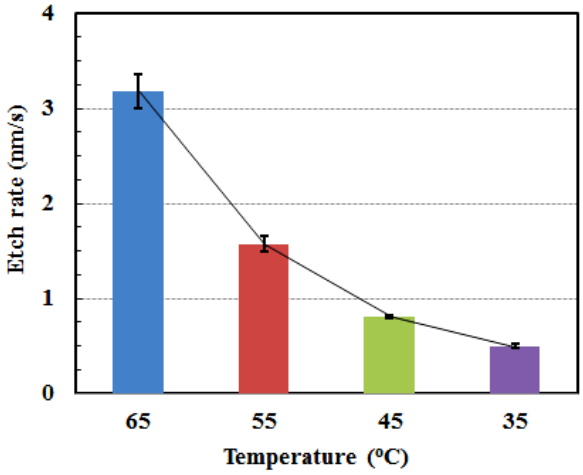


Fig. 2 Etching rates at different temperatures of (100) silicon in TMAH with 10% isopropyl alcohol additive.

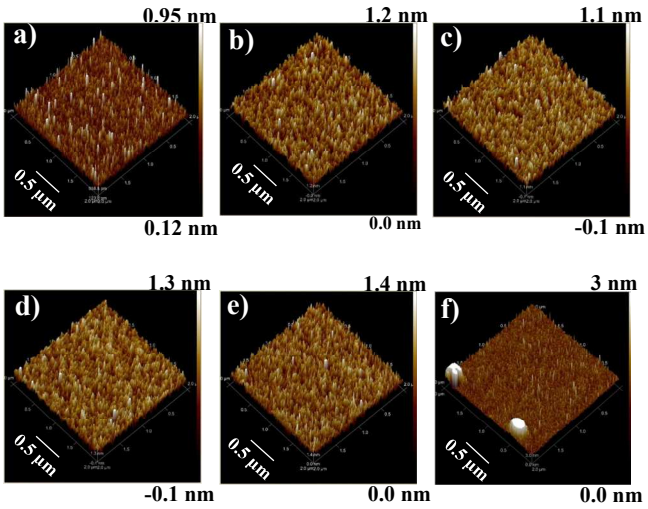


Fig. 3 AFM surface topography of silicon samples. (a) Pristine silicon. (b), (c), (d) and (e) Silicon samples etched with TMAH with IPA additive at 35 °C – 45 °C – 55 °C and 65 °C, respectively.(f) Silicon sample thinned by dry-oxidation and HF 1% etching.

3.2. Locally thinned down silicon nanowire fabrication

In the proposed fabrication process, maintaining the thickness homogeneity of the silicon device layer is critical towards enabling the reliable fabrication of the locally thinned down SiNWs at the whole-wafer scale. After the first dry-oxidation step, spectroscopic ellipsometry thickness mapping confirmed the thickness homogeneity of the dry-oxidized SiO_2 layer across the wafer, ranging from 42 – 46 nm (Fig. 4).

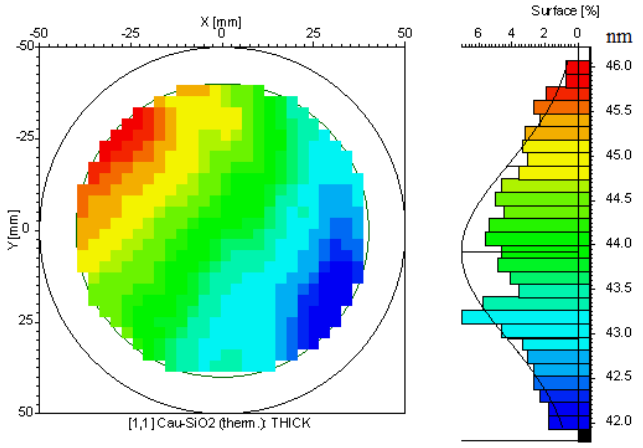


Fig. 4. Ellipsometric thickness mapping of the silicon dioxide after dry-oxydation on a wafer.

Scanning electron microscope images of fabricated SiNW arrays before performing the locally thinning down step are exhibited in Fig. 5. It can be seen that the prepared SiNW arrays contain up to 8 nanowires connected to the two source-drain (S-D) contact regions, which were designed to facilitate an efficient contact between SiNWs and the electrical metal feed lines in later steps (Fig. 5a). As seen in Fig. 5b and 5c, structural characterization confirmed that the

fabricated SiNWs were highly ordered, straight, smooth with a typical trapezoidal configuration resulting from the TMAH wet etching. The thickness of the nanowires is controlled during the first dry-oxidation step and fixed at 40 nm. In a typical design, length of up to 10 µm and width of 150 nm were used. In our design, the width of the SiNWs was selected to achieve a reasonably large surface area to increase available binding sites for detecting a limited amount of analyte molecules in bio-sensing applications. On the other hand, the thicknesses of the nanowires were confined in the next step towards the fabrication of high performance field-effect devices.

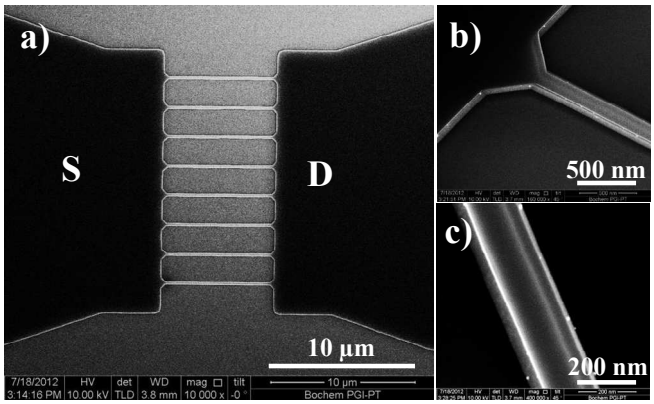


Fig. 5 (a) SEM images of the fabricated SiNWs arrays connected to contact regions before the local thinning down step. (b) and (c) Magnification of a single SiNW in the side and middle section, respectively.

After fabricating the SiNW arrays, the wafer was locally thinned down using the optimized TMAH wet-etching process. A key aspect of the proposed size-reduction approach is that by combining the optimized TMAH wet-etching process and SiO_2 masking on the silicon contact regions, only the middle sections of the SiNW arrays are thinned down. In the unprotected regions corresponding to the middle sections of the SiNWs, etching occurs for both the (100) and (111) planes but at different rates depending on the crystallographic orientation of the silicon. TMAH etching rate on (111) silicon plane is indeed lower than that of (100) plane by at least one order of magnitude [17, 23]. At 35 °C, the etching rate of the optimized TMAH solution on (100) silicon plane is ~ 0.5 nm s^{-1} and extremely slow on the (111) silicon plane of the nanowire sidewall. As shown in Fig. 6a, a clear "staircase" structure with negligible reduction in width is obtained after the optimized TMAH etching and removal of the SiO_2 mask with a standard HF 1% solution. The fabricated staircase structure confirmed that the unprotected silicon regions were efficiently thinned down while the rest of the nanostructures retained their original thicknesses due to the protection of SiO_2 mask. Cross-sectional SEM images taken from SiNW arrays processed by focussed ion beam further confirmed the effective thinning down of the SiNWs. Although further studies are warranted to fully ascertain the homogeneity of the process at the wafer-scale, the thickness of the SiNWs could be controlled by the etching time. For instance, etching times of 40 and 50 sec resulted respectively in SiNWs with thicknesses of 20 nm and 15 nm, in agreement with the prediction from the calibration study (Fig. 6b and 6c). In comparison with similar SiNW structures fabricated by other size reduction techniques [4, 13, 15, 16], the proposed local thinning process is very straight-forward, easy to implement and does not require high temperature oxidation or additional deposition techniques. Currently, we were able to fabricate up to 144 locally thinned down SiNWs from a single octagon SOI wafer (diameter c.a. 100 mm) and package them in a total of 36 ready-to-test chips units (inset plot Fig. 7). In the proposed fabrication process, it is critical to use high quality SOI wafers with very low thickness variations of the Si layer. The possibility to fabricate the ultrathin SiNW arrays on a large scale relies indeed not only on the very low and highly controllable etching rates afforded by the optimized process but also on the use of SOI wafers with high thicknesses homogeneity (e.g thickness variation less than 5 % of the total thickness of Si layer). It is expected that this process could be used to produce ultra-thin SiNWs with thickness down to 10 nm or less by simply adjusting the TMAH etching time, although such ultralow thicknesses might require limitation over the patterning scale to ensure the required homogeneity of the silicon layer (e.g. 2-3 inch wafers or less). In addition, by replacing ion-beam lithography used in the first step by conventional lithography, this novel fabrication process appears a promising way to fabricate structures using only conventional micro-fabrication techniques.

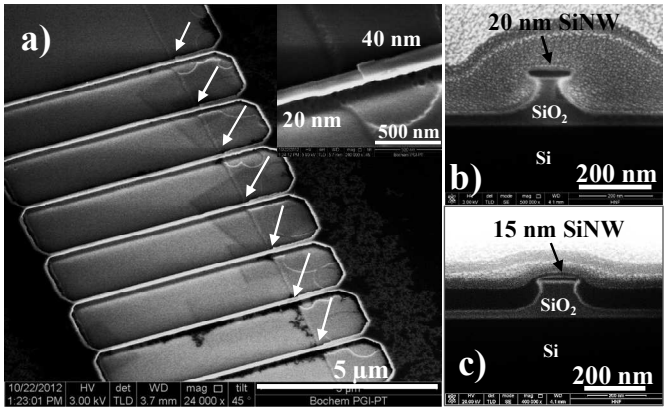


Fig. 6 (a) SEM images of locally thinned down SiNW arrays after the locally wet-etching. The white arrows show the staircase structures at etched SiNW arrays. Inset is the magnification of a staircase structure. (b) and (c) SEM-Focused ion beam cross-section images of the thinned down of SiNW with thicknesses of 20 nm and 15 nm respectively.

3.3. Electrical characterizations of locally thinned down silicon nanowires

Current-voltage (*I-V*) characterization of the locally thinned down 20 nm SiNW devices with 8-10 nm of SiO_2 isolation was performed in liquid (Phosphate Buffer Saline – PBS 1X, pH 7.4) at room temperature using a custom-built 16-channels low-noise amplifier system modified from[24]. The measurement was carried out with a liquid front gate based on a reference electrode (Ag/AgCl micro-bead) immersed in PBS (inset plot Fig. 8).

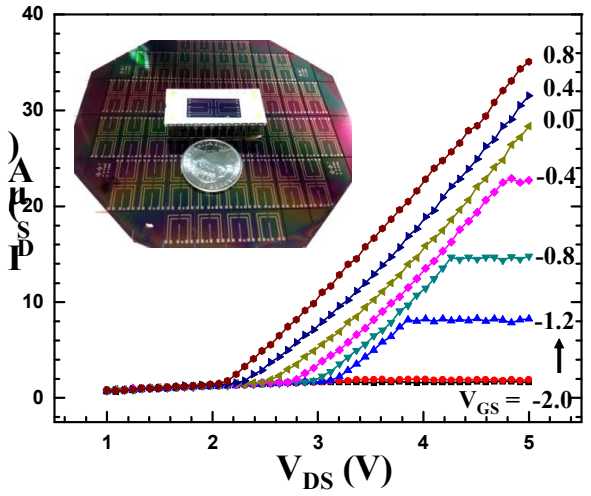


Fig. 7 I_{DS}-V_{DS} output characteristic of SiNWs array measured in PBS. The inset is a photographic picture of SiNWs on-a-chip unit on top of wafer-scale packaged locally thinned down SiNWs devices.

As shown in Fig. 7, when the liquid gate voltage (V_{GS}) is increased from -2.0 to 0.8 V with voltage step of 0.4 V, increase of the output current I_{DS} values was observed with clear linear and saturation regions - similar to conventional *n*-channel metal–oxide–semiconductor field-effect transistor (MOSFET) in depletion mode. Under the negligible gate leakage current in the ~ pA range (data not shown), we hypothesize that the observed n-channel depletion mode behaviour of the 20 nm thin SiNWs nanowires is the result of surface effect for the lowly doped nanowires. It has indeed been shown that the SiO_2 surface states have a significant influence on the charge carrier density and hence on the nanowire conductivity in comparison with bulk silicon due to dopant segregation and deactivations at the Si/SiO_2 interface[25-27]. As the diameters of the SiNWs are scaled-down, the influence of the surface state can be expected to increase significantly and the free carriers can be completely depleted on the carrier traps at the Si/SiO_2 interface in case of lightly-doped SiNWs [28]. As observed in our measurements, a high drain-source current has been observed at V_{GS} = 0 in comparison to applied negative gate voltages. This phenomenon indicates that the negative charged SiO_2 surface in PBS solution has a strong influence, driving a majority of the dominant carriers (holes) to the nanowire surface. As soon as negative gate voltage is applied on the nanowires, hole carriers could be completely trapped in the fix-charge traps at the interface of Si/SiO_2. In fact, holes carriers in the 20 nm thin SiNWs with background doping at 10^{15} cm^{-3} can be completely depleted by surface charge density at ~ 10^{11} cm^{-2} [14, 28]. Under high electrical field (V_{DS} = 5V), electrons from the metal source/drain electrodes in this case could tunnel to the ultrathin nanowire, resulting in an n-type FET with depletion behavior as observed here. While further study is required to confirm the cause of this experimental observation, our results indicate that it is critical to carefully control the doping concentration of silicon nanowires when their dimensions are constrained. Electrochemical measurement of the fabricated locally thinned down SiNW devices showed a good response to changes in pH solution (Titrisol buffer; pH 2.0 - 10.0). For increasing pH value, the V_{GS} curve shift to more positive gate value with sensitivity at ~ 18.8 mV/pH unit. These results confirmed the successful operation of the locally thinned down SiNW FET devices.

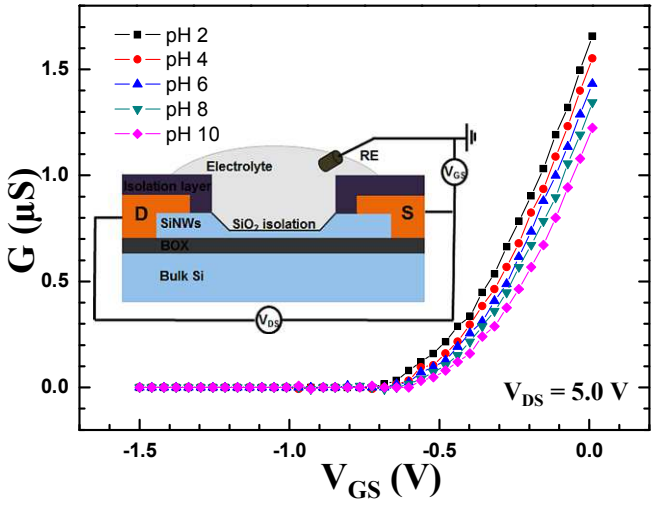


Fig. 8 Conductance (G) response of locally thinned down SiNWs-FET sensor in different pH buffer solutions. Front gate -source voltages (V_{GS}) were applied via electrochemical Ag/AgCl electrode immersed in the solutions (inset plot).

Conclusions

A novel and robust top-down fabrication process is reported for the wafer-scale fabrication of silicon nanowire arrays with locally confined thickness at sub-20 nm. An optimized TMAH wet etching with controllable low-etching rate and ultra-smooth silicon surface morphology has been optimized to precisely confine the nanowire feature sizes. Using this process, locally thinned down SiNWs have been fabricated and packaged in a chip unit. Current-voltage characterizations in liquid demonstrated depletion-mode field-effect silicon nanowire devices with a good response to pH changes. Considering the excellent performance of such nanostructures in FET-based bioelectronics, this novel fabrication process is expected to foster their translational application in a range of applications.

Acknowledgments

This work is supported by the NH&MRC project grant 631939 as well as by a grant from the joint initiative of the Australian Technology Network of Universities (ATN) and the German Academic Exchange Service (DAAD). The authors also would like to thank Dr. Dirk Mayer and technicians in the Forschungszentrum Jülich, ANFF-SA node for their help and support.

Notes and references

[a] Ian Wark Research Institute, University of South Australia, Mawson Lakes Campus, Mawson Lakes, South Australia 5095, Australia.
[b] Peter Grünberg Institute, Forschungszentrum Juelich GmbH, Juelich, Germany.
Email: benjamin.thierry@unisa.edu.au

1. K. Trivedi, H. Yuk, H. C. Floresca, M. J. Kim and W. Hu, *Nano Letters*, 2011, **11**, 1412-1417.
2. Y. Cui, Z. Zhong, D. Wang, W. U. Wang and C. M. Lieber, *Nano Letters*, 2003, **3**, 149-152.
3. J. Martinez, R. V. Martínez and R. Garcia, *Nano Letters*, 2008, **8**, 3636-3639.
4. N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo, N. Balasubramanian and D. L. Kwong, *Electron Device Letters, IEEE*, 2006, **27**, 383-386.
5. K.-I. Chen, B.-R. Li and Y.-T. Chen, *Nano Today*, 2011, **6**, 131-154.
6. E. Garnett and P. Yang, *Nano Letters*, 2010, **10**, 1082-1087.
7. E. C. Garnett and P. Yang, *Journal of the American Chemical Society*, 2008, **130**, 9224-9225.
8. M. M. Adachi, M. P. Anantram and K. S. Karim, *Sci. Rep.*, 2013, **3**.
9. J. V. Wittemann, W. Munchgesang, S. Senz and V. Schmidt, *Journal of Applied Physics*, 2010, **107**, 096105-096103.
10. S. Sharma, T. I. Kamins and R. S. Williams, *Applied Physics A*, 2005, **80**, 1225-1229.
11. H. D. Tong, S. Chen, W. G. van der Wiel, E. T. Carlen and A. van den Berg, *Nano Letters*, 2009, **9**, 1015-1022.
12. R. Sozaraj, B. Dipu, C. F. Colm, L. Tarek, T. S. Matthew, D. H. Justin and A. M. Michael, *Nanotechnology*, 2013, **24**, 065503.
13. K.-N. Lee, S.-W. Jung, K.-S. Shin, W.-H. Kim, M.-H. Lee and W.-K. Seong, *Small*, 2008, **4**, 642-648.
14. N. Rochdi, D. Tonneau, F. Jandard, H. Dallaporta, V. Safarov and J. Gautier, *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, 2008, **26**, 159-163.
15. S. Chen, J. G. Bomer, W. G. van der Wiel, E. T. Carlen and A. van den Berg, *ACS Nano*, 2009, **3**, 3485-3492.
16. R. Juhasz, N. Elfström and J. Linnros, *Nano Letters*, 2004, **5**, 275-280.
17. K. B. Sundaram, A. Vijayakumar and G. Subramanian, *Microelectronic Engineering*, 2005, **77**, 230-241.
18. I. Zubel and M. Kramkowska, *Sensors and Actuators, A: Physical*, 2001, **93**, 138-147.
19. I. Zubel, M. Kramkowska and K. Rola, *Sensors and Actuators A: Physical*, 2012, **178**, 126-135.
20. S. Poli, M. G. Pala, T. Poiroux, S. Deleonibus and G. Baccarani, *Electron Devices, IEEE Transactions on*, 2008, **55**, 2968-2976.
21. M. Lenzi, A. Gnudi, S. Reggiani, E. Gnani, M. Rudan and G. Baccarani, *J Comput Electron*, 2008, **7**, 355-358.
22. F. Wang, S. Yip, N. Han, K. Fok, H. Lin, J. J. Hou, G. Dong, T. Hung, K. Chan and J. C. Ho, *Nanotechnology*, 2013, **24**, 375202.
23. E. Steinsland, T. Finstad and A. Hanneborg, *Sensors and Actuators A: Physical*, 2000, **86**, 73-80.
24. J. F. Eschermann, R. Stockmann, M. Hueske, X. T. Vu, S. Ingebrandt and A. Offenhausser, *Applied Physics Letters*, 2009, **95**, 083703-083703.
25. V. Schmidt, S. Senz and U. Gösele, *Applied Physics A*, 2007, **86**, 187-191.
26. M. T. Bjork, H. Schmid, J. Knoch, H. Riel and W. Riess, *Nat Nano*, 2009, **4**, 103-107.
27. S. Ingole, P. Manandhar, S. B. Chikkannanavar, E. A. Akhadov and S. T. Picraux, *Electron Devices, IEEE Transactions on*, 2008, **55**, 2931-2938.
28. K.-i. Seo, S. Sharma, A. A. Yasseri, D. R. Stewart and T. I. Kamins, *Electrochemical and Solid-State Letters*, 2006, **9**, G69-G72.