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Electrical characteristics of gallium-indium-zinc oxide thin-film transistor nonvolatile memory with Sm_2O_3 and $SmTiO_3$ charge trapping layers

Jim-Long Her,[a] Fa-Hsyang Chen,[b] Ching-Hung Chen,[b] and Tung-Ming Pan,*[b]

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In this study, we report the structural and electrical characteristics of high-κ Sm_2O_3 and $SmTiO_3$ charge trapping layers on indium-gallium-zinc oxide (IGZO) thin-film transistor (TFT) for nonvolatile memory device applications. The IGZO TFT nonvolatile memory featuring a $SmTiO_3$ charge trapping layer exhibited better characteristics, including a larger memory window (2.7 V), long charger retention time (10^5 s with charge loss <15%) and better endurance performance for program/erase cycles (10^4), compared with Sm_2O_3 charge trapping layer. These results can be attributed to the $SmTiO_3$ film possessing a high dielectric constant and deep trapping level. The high-κ $SmTiO_3$ is an excellent candidate for use as the trapping layer in IGZO TFT nonvolatile memories.

Introduction

Amorphous indium-gallium-zinc oxide (IGZO) is widely investigated as a channel material in thin-film transistors (TFTs) for flat, flexible and transparent display applications due to its high field mobility, wide band gap, good uniformity, high transparency, and low processing temperature.[1-2] To develop the next-generation system-on-panel (SOP) applications, IGZO TFT nonvolatile memories have been studied as a TFT switch and memory element.[3-7] Various IGZO TFT memories with different charge storage media such as, metal nanocrystals (Pt, Au)[4-5] and dielectrics (SiO_x, Si_3N_4, Al_2O_3),[6-7] are explored. However, the high operating voltages, retention loss and cycling decay are the challenges. To obtain high erasing efficiency, a large number of holes must be generated in the IGZO channel during an erasing operation. Several methods, such as light irradiation[8] and light-assisted negative-gate-bias erasing,[9] have been proposed to improve the erasing efficiency of IGZO TFT memory. However, the addition of instrument of an ultraviolet light is required during the erasure process. In order to address this issue, high-κ dielectric materials have been studied as a charge trapping layer for silicon-oxide-high-κ-oxide-silicon-type memories without decreasing the thickness of tunneling oxide.[10-11] Previously, it has been proved that the Ti-doped HfO_2 (HfTiO) high-κ dielectric has better material and electrical properties than the un-doped HfO_2 film, such as the thinner interfacial layer, higher κ value and lower leakage current.[12-13]

Recently, rare-earth (RE) oxide films are considered to be suitable materials for further scaling of nonvolatile memory devices because of their promising thermal stability and better electrical properties.[14-15] Among RE oxide materials, thin Sm_2O_3 film is one of the most potential candidates as a charge trapping layer for nonvolatile memory applications due to its high dielectric constant of 15, wide energy bandgap of 4.33 eV and high breakdown electric field of 7 MV/cm.[15-17] However, the formation of hydroxide film is found at the surface of RE oxide due to high hygroscopicity.[18] To avoid this problem, the high stability properties of RE oxide film can be realized by the addition of Ti atoms into the RE film.[19] In our previous research results showed that the incorporation of Ti into RE oxide films exhibited excellent electrical characteristics including a high dielectric constant, a low leakage current and a large breakdown voltage.[20] In this paper, we compared the high-κ Sm_2O_3 and $SmTiO_3$ films as a charge trapping layer in metal-oxide-high-κ-oxide-IGZO (MOHOI) nonvolatile memory based on TFT device. The film structure and composition of high-κ Sm_2O_3 and $SmTiO_3$

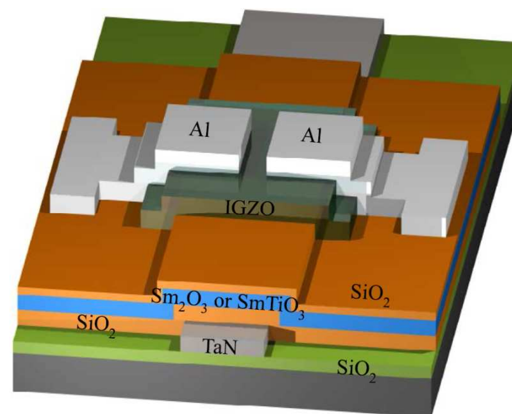

Fig. 1 Schematic structure of the IGZO TFT nonvolatile memory with a high-κ Sm_2O_3 or $SmTiO_3$ charge trapping layer.

[a]Division of Natural Science, Center for General Education, Chang Gung University, Taoyuan 333, Taiwan.
[b]Department of Electronics Engineering, Chang Gung University, Taoyuan 333, Taiwan.
*Corresponding author: Dr. Tung-Ming Pan ;Fax: +886-3-2118507
Tel: +886-3-2118800 Ext. 3349;E-mail: tmpan@mail.cgu.edu.tw

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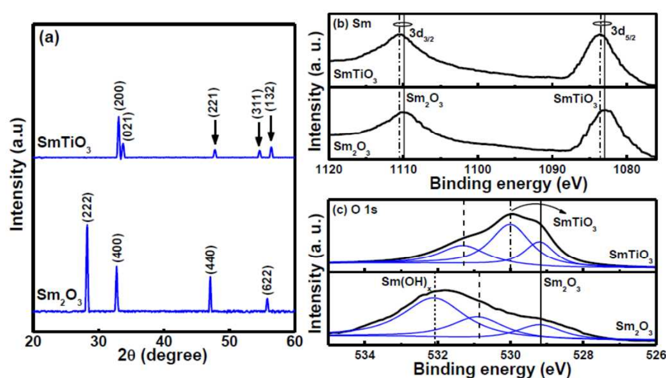


Fig. 2 (a) XRD pattern of the Sm_2O_3 and $SmTiO_3$ dielectric films. XPS spectra of (b) Sm 3d and (c) O 1s for Sm_2O_3 and $SmTiO_3$ dielectric films.

films were analyzed by X-ray diffraction (XRD) and X-ray photoelectron spectroscopy (XPS), respectively. The electrical characteristics of high-κ Sm_2O_3 and $SmTiO_3$ MOHOI-type TFT nonvolatile memories are also investigated.

Experimental

Inverted staggered IGZO TFT nonvolatile memory devices with high-κ Sm_2O_3 and $SmTiO_3$ charge trapping layers were processed on SiO_2/Si substrate as shown in Fig. 1. A TaN (40 nm) was deposited as a bottom gate electrode by reactive sputtering at room temperature. A SiO_2 (50 nm) blocking layer was deposited on the bottom gate electrode, followed by 40 nm Sm_2O_3 and $SmTiO_3$ charge trapping layers and a 8 nm SiO_2 tunneling layer. The blocking layer and tunneling layer were deposited through rf sputtering using a SiO_2 target. Next, the Sm_2O_3 charge trapping layer was deposited by rf sputtering using a Sm target in Ar/O_2 ambient, whereas the $SmTiO_3$ charge trapping layer was deposited through rf cosputtering using both Sm and Ti targets. All samples were annealed at 400 °C in O_2 ambient for 10 min. Then, a 20 nm channel layer was deposited by means of rf sputtering using an IGZO target (In_2O_3:Ga_2O_3:ZnO= 1:1:1 in mol ratio) at room temperature. The post-deposition annealing was performed in N_2 ambient for 1 hr at 200 °C. Finally, the patterned Al layer (~50 nm) as the source and the drain electrodes was deposited using the thermal evaporation technique, followed by a typical lift-off process. The channel width and length of the fabricated TFTs were 100 μm and 10 μm, respectively.

The crystalline structure and the chemical composition of the dielectric films were investigated using XRD and XPS analyses, respectively. XRD analysis was performed using a Bruker-AXS D5005 diffractometer with a Cu K_α (λ = 1.542 Å) radiation. The chemical bonding of the dielectric was determined using a monochromatic Al K_α (1486.7 eV) source. The transfer characteristics (drain current-gate voltage, I_{DS}-V_{GS}) of the high-κ Sm_2O_3 and $SmTiO_3$ IGZO TFT nonvolatile memories were measured by an Agilent 4156C semiconductor parameter analyzer. The threshold voltage (V_{TH}) of TFT nonvolatile memories was defined as the V_{GS} at which the I_{DS} reaches 0.1 nA for a drain voltage of 1 V.

Results and Discussion

Fig. 2(a) displays the XRD pattern of the Sm_2O_3 and $SmTiO_3$ thin films after 400 °C annealing in O_2 ambient. Three strong (222), (400) and (440) peaks and one weak (622) peak were found in the Sm_2O_3 film. In contrast, for the $SmTiO_3$ sample, a large (200) reflection peak and four small (021), (221), (311), and (132) reflection peaks are observed in the 2θ diagram. These dielectric films are belong to polycrystalline structures. Figs. 2 (b) and (c) show the Sm 3d and O 1s XPS spectra of the Sm_2O_3 and $SmTiO_3$ films, respectively. Fig. 2 (b) depicts that the binding energy of Sm $3d_{5/2}$ and $3d_{3/2}$ double peaks is located at 1083.1 eV and 1110.1 eV, respectively, for the Sm_2O_3 film.[21] The Sm 3d double peaks (Sm $3d_{5/2}$ at 1083.6 eV and Sm $3d_{3/2}$ at 1110.6 eV) for the $SmTiO_3$ film shift to higher binding energy by 0.5 eV relative to those for the Sm_2O_3. This shift can be related to the reaction of TiO_x with the Sm atom to form a $SmTiO_3$ structure. The O 1s spectra of the Sm_2O_3 and $SmTiO_3$ films are shown in Fig. 2(c) with their appropriate peak curve-

Fig. 3 Transfer characteristics of the MOHOI-type TFT nonvolatile memories with Sm_2O_3 and $SmTiO_3$ charge trapping layers.

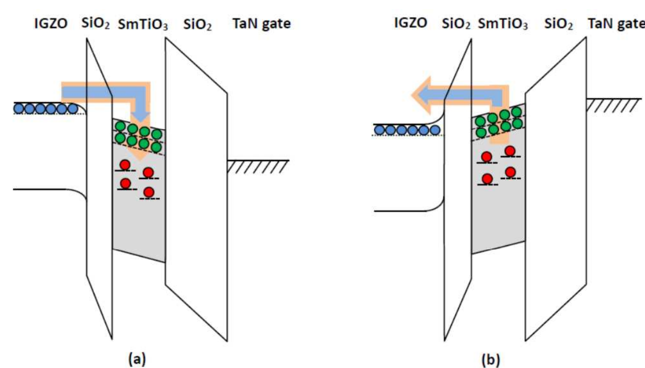
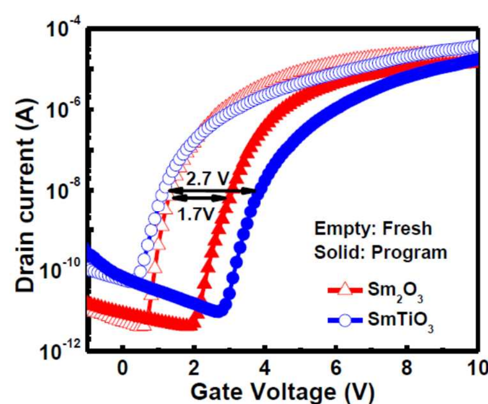


Fig. 4 Schematic illustration of band diagram of the $SmTiO_3$ IGZO TFT nonvolatile memory when the (a) positive and (b) negative bias applied to the gate electrode. The channel electrons is indicated as blue circles, whereas inherent electrons of $SmTiO_3$ located in shallow level states and deep level states are green circles and red circles, respectively. The probability of charge trap or detrap is described as size of arrow.



fitting lines. The O 1s signal of Sm_2O_3 film comprised three peaks: one peak for Sm–O boding at 529.2 eV,[21] one for oxygen vacancy at 530.9 eV[22] and one for Sm–OH bonding at 532.1 eV.[23] The intensity of the O 1s peak corresponding to $Sm(OH)_x$ was larger than that of Sm_2O_3. This result can be attributed to the oxygen vacancies in the Sm_2O_3 film leading to the moisture absorption property exposed to the air.[18] Furthermore, the $SmTiO_3$ film also comprised three peaks at

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529.2, 530 and 531.3 eV, which we can assign to Sm–O binding, Sm–O–Ti binding[24] and oxygen vacancy[25], respectively. The O 1s peak corresponding to $SmTiO_3$ exhibits a larger intensity peak compared with Sm_2O_3. This result indicates that the reaction of TiO_x with Sm atom form a $SmTiO_3$ structure reducing the formation of a Sm_2O_3 film.

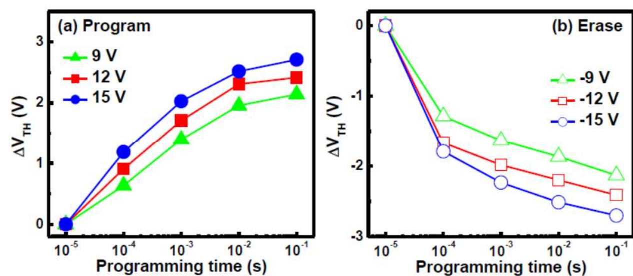

Fig. 5 Threshold voltage shift of the $SmTiO_3$ MOHOI-type TFT nonvolatile memory as a function of the (a) programming time (b) erasing time.

Fig. 3 shows the transfer (I_{DS}-V_{GS}) characteristics of the MOHOI-type TFT nonvolatile memories with Sm_2O_3 and $SmTiO_3$ charge trapping layers after programming voltage at 15 V for 100 ms. The κ value of Sm_2O_3 and $SmTiO_3$ dielectric films was determined to be 8.6 and 11, respectively, from capacitance-voltage curve. The IGZO TFT nonvolatile memory with a $SmTiO_3$ charge trapping layer has a larger memory window (2.7 V) than that with Sm_2O_3 charge trapping layer (1.7 V). The IGZO is a natural n-type semiconductor that generally only supplies electrons for charge transport in the channel. During electrical programming, electrons from the a-IGZO channel can be easily trapped in the $SmTiO_3$ by Fowler-Nordheim (F–N) tunneling. The high dielectric constant of $SmTiO_3$ film increased the effective electric field across the tunneling oxide, thus enhancing more electrons trapped in the $SmTiO_3$ film. The effective electric field across the SiO_2 tunneling layer in Sm_2O_3 and $SmTiO_3$ IGZO TFT memories was estimated to be 1.97 and 2.08 MV/cm, respectively.

Figs. 4(a) and (b) illustrate the band diagram of the $SmTiO_3$ IGZO TFT memory device after the programming and erasing operation. When the positive voltage pulse was applied for the program state, as shown in Fig. 4(a), the electrons accumulated in the IGZO channel were transferred into the $SmTiO_3$ trap layer. Therefore, the V_{TH} is shifted to the positive direction. At this state, it can be expected that most electrons trapped in the $SmTiO_3$ trap layer were located in deep level states, because shallow levels of $SmTiO_3$ were mostly filled with inherent electrons.[26] The electrons should pass through the shallow level states to the deep level states. A large number of electrons located in the shallow level states of $SmTiO_3$ could act as some self-limiting elements due to their same polarity. Furthermore, for the case of erasing state shown in Fig. 4(b), the electrons accumulated in shallow levels can be firstly transported to the IGZO channel and the electrons trapped in deep levels are subsequently detrapped. Then, the required erase time for the erasing operation, which was involved with the trapping event into the deep levels of $SmTiO_3$, may be longer than that for the program state, which was related to the charge transfer from the shallow levels of $SmTiO_3$.

Fig. 5(a) illustrates the ΔV_{TH} values of the $SmTiO_3$ MOHOI-type TFT memory device as a function of the programming time under various gate voltage stresses, where drain and source are grounded. The ΔV_{TH} is defined as the change in threshold voltage between the virginal and programmed states. The F–N tunneling programming and erasing were used for

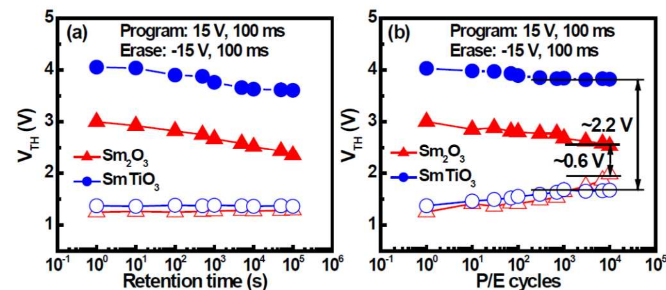

Fig. 6 (a) Charge retention and (b) endurance characteristics for the Sm_2O_3 and $SmTiO_3$ MOHOI-type TFT nonvolatile

high-κ $SmTiO_3$ IGZO TFT nonvolatile memory operations. We find that the ΔV_{TH} value increases with increasing the programming time. The amount of electrons, which are responsible for the shift of the V_{TH}, trapped in the $SmTiO_3$ layer during the programming process is a function of the programming time, and hence it increases with increasing the programming time. In addition, program voltage was increased, memory window was also increased. After the programming condition of V_{GS} =15 V at 100 ms, the $SmTiO_3$ IGZO TFT memory device exhibits a large memory window of 2.7 V. The energy bandgap of $SmTiO_3$ film could be decreased by the incorporation of Ti into the Sm_2O_3.[27] This bandgap narrowing gives rise to a large conduction band offset to the trapping layer that facilitates the trapping of the electrons. The $SmTiO_3$ layer was employed to store the high density of injected electrons from the IGZO active layer, causing a large threshold voltage shift. Fig. 5(b) displays the ΔV_{TH} value of the $SmTiO_3$ IGZO TFT memory device as a function of the erasing time under different gate voltage stresses (drain and source are grounded). The gate voltage-dependent erasing characteristics are investigated with a fixed erasing time of 100 ms. The ΔV_{TH} decreases from -2.1 to -2.7 V as the erasing voltage decreases from -9 to -15 V, respectively.

Fig. 6(a) shows the data retention characteristics of the Sm_2O_3 and $SmTiO_3$ MOHOI-type TFT memory devices measured at room temperature. In the programming state, the IGZO TFT memory device using a $SmTiO_3$ film has a lower charge loss (<15%) than that with a Sm_2O_3 film, measured at 10^5 s. The addition of Ti into the Sm_2O_3 created more deep trapping level in the $SmTiO_3$. The trapping electrons transferred readily from shallow level to adjacent deeper level by lateral hopping.[28] Therefore, the good data retention characteristic can be related to the most of trapped charges are trapped in the deep trap states of $SmTiO_3$ dielectric. In the erasing state, there is almost no change in the V_{TH} with time. Fig. 6(b) displays the endurance characteristics of the Sm_2O_3 and $SmTiO_3$ MOHOI-type TFT memory devices under programming condition: V_{GS}=15 V for 100 ms and erasing condition: V_{GS}=-15 V for 100 ms. The IGZO TFT memory device featuring a $SmTiO_3$ film exhibited better endurance characteristics compared with Sm_2O_3 film. A slight memory window narrowing occurred and individual threshold voltage shifts become visible in the program and erase states after 100 cycles. This behaviour may be attributed to a large number of storage charges causing the defects in the tunnel oxide during charge transportation process.[29] Another possible reason for narrowing of the memory window is that the IGZO film itself is sensitive to the atmosphere and becomes unstable under long time exposure to

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TABLE I. Comparison of electrical characteristics for IGZO TFT memory devices fabricated with SiO_2/IGZO/SiO_2, Al_2O_3/IGZO/Al_2O_3, HfLaO/HfON/HfLaO, $SiO_2/Sm_2O_3/SiO_2$, and $SiO_2/SmTiO_3/SiO_2$ stacked structures.

Gate stacks	Memory window (V)	P/E voltage (V) and time (ms)	Charge loss (10^5 s)	P/E cycles
SiO_2/IGZO/SiO_2	5.6	P: VG= 18 for 10 E: VG= -23 for 100	>15%	NA
Al_2O_3/IGZO/Al_2O_3	3.8	P: VG= 14 for 10 E: VG= -14 for 10	> 30%	10^3
HfLaO/HfON/HfLaO	1.2	P: VG= 8 for 1 E: VG= -8 for 0.1	> 60%	10^2
$SiO_2/Sm_2O_3/SiO_2$	1.7	P: VG= 15 for 100 E: VG= -15 for 100	> 20%	10^3
$SiO_2/SmTiO_3/SiO_2$	2.7	P: VG= 15 for 100 E: VG= -15 for 100	<15%	10^4

air or electrical field stressing.[30] The trapped charge in the trapping layer easily escapes because of the film variation or is neutralized by the charges in the gate dielectric and gate-dielectric/channel interface.[31] After 10^4 program/erase (P/E) cycles, the memory window of $SmTiO_3$ MOHOI-type TFT memory is still fixed around 2.2 V.

The important device parameters of MOHOI-type TFT memory devices are listed in table I, where the data from IGZO TFT memory devices using SiO_2/IGZO/SiO_2,[31] Al_2O_3/IGZO/Al_2O_3,[32] HfLaO/HfON/HfLaO,[33] $SiO_2/Sm_2O_3/SiO_2$, and $SiO_2/SmTiO_3/SiO_2$ stacked structures are listed for comparison. Although our $SiO_2/SmTiO_3/SiO_2$ TFT memory has a low memory window and a high P/E voltage, it exhibits good data retention and endurance.

Conclusions

In this paper, we compared the MOHOI-type TFT nonvolatile memory device with high-κ Sm_2O_3 and $SmTiO_3$ films as a charge trapping layer. The $SmTiO_3$ IGZO TFT nonvolatile memory exhibited a larger memory window (2.7 V), smaller charge loss (< 15% after 10^5 s) and better endurance performance (~2.2 V after 10^4 P/E cycles), compared with Sm_2O_3 IGZO TFT memory. These results are attributed to the $SmTiO_3$ structure with a high dielectric constant and the formation of deep trap states, resulting in the high probability for trapping the charge carrier. The high-κ $SmTiO_3$ MOHOI-type TFT nonvolatile memory device is considered as a promising candidate for SOP applications.

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