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Integration of Large Single-Grain Pb(Zr,Ti)O_3 into Low-Temperature Polycrystalline-Silicon Thin-Film Transistors for System-On-Glass Display

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The large single-grain Pb(Zr,Ti)O_3 (PZT) film was integrated into the low-temperature polycrystalline-silicon (poly-Si), crystallized by $NiSi_2$ seed-induced lateral crystallization (SILC), thin-film transistor fabricated on glass substrate. The SILC poly-Si showed a superior electrical performance to the other crystallization methods due to its high crystalline volume fraction (91.2%). PZT with perovskite phase was generally obtained by 800 ℃ which is not acceptable for using glass substrate, however, here we developed a low-temperature perovskite PZT using artificially controlled seeding process. First, we formed an artificially controlled nucleation seed with rapid thermal annealing at 650 ℃ in a 1 sec pulse, and grew the single seed by tube-furnace at 550 ℃ for 2 hrs. The device exhibited a large memory window (3.5 V) and a high reliable memory operation. Therefore, this approach could potentially be applied to the next generation non-volatile memory device as well as integrated system-on-glass displays.

1. Introduction

Polycrystalline-silicon (poly-Si) thin-film transistors (TFTs) have been widely used in active-matrix liquid crystal display (AMLCD) and active-matrix organic light-emitting diode (AMOLED) display due their high field-effect mobility, high current density, and the capacity to integrate functional circuits to realize the system-on-glass (SOG) technology[1-5]. However, the power consumption of SOG technology tend to be higher than that of the single crystalline-Si (c-Si) based silicon integrated-circuits (IC), because poly-Si TFTs are fabricated with larger design rules, higher threshold voltages, and lower field-effect mobility. Therefore, power reduction in SOG techniques is one of the major challenges to be realized. Embedding dynamic memory circuits into the mobile AMLCD pixel in order to reduce the power consumption was first proposed by H. Tokioka *et al.*[6] but the complicated process steps and reducing the emitting area issues still remains. Y. Haung *et al.*[7] suggest that integrating an amorphous-silicon (a-Si) non-volatile memory (NVM) in to the AMOLED pixel can reduce the power consumption during the static image on the screen and increase the light-emitting fill factor by eliminating the large storage capacitor. However, the a-Si TFT shows a slow switching speed, short charge retention time, and poor fatigue cycles. Among many types of non-volatile memory, ferroelectric memory field-effect transistors (FEMFETs) are highly attractive for the next generation memory due to its high switching speed, device scalability, high integration, and non-destructive read out[8-10]. B. H. Kim *et al.*[11] developed an active-matrix array using metal-oxide based semiconductor TFTs with poly(vinlyidene fluoride trifluoroethylene) [P(VDF-TrFE)] ferroelectrics. Although the metal-oxide based semiconductor TFTs showed a higher switching speed than that of a-Si based NVM, the low switching speed due to its low mobility, short retention and poor fatigue still shows a serious problem. Note that the field-effect mobility of metal-oxide based semiconductor has about 2 magnitude order lower than that of the poly-Si.

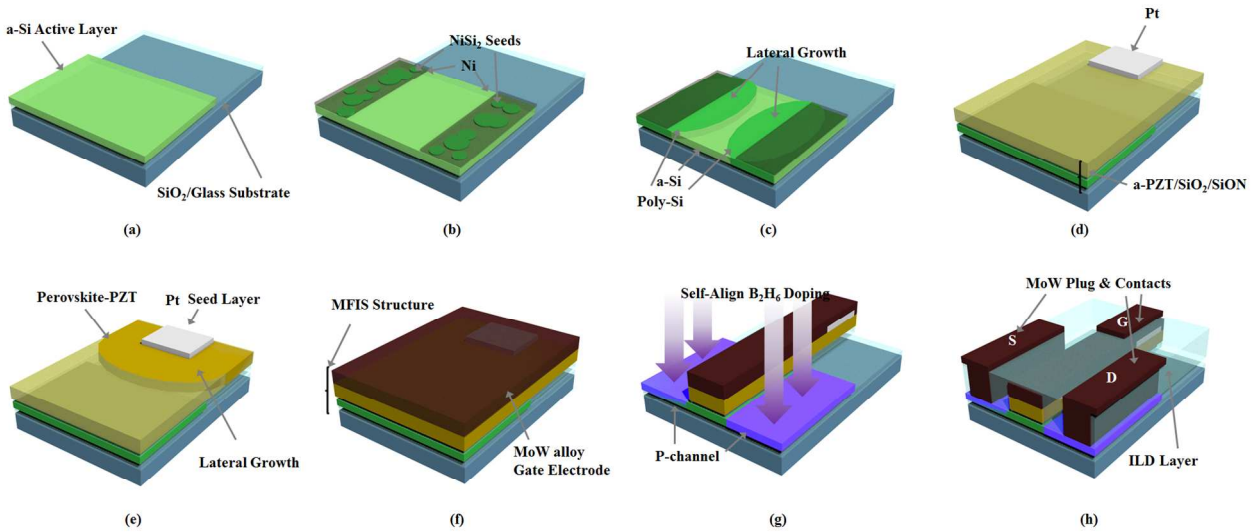

Fig.1. Configuration of 1T-FeRAM process flow on glass substrate. (a) depositing a-Si active layer on glass, (b) $NiSi_2$ seed formation, (c) $NiSi_2$ seed-induced lateral crystallization (SILC) process, (d) depositing Pt/a-PZT/SiO_2/SiON stacked layer, (e) nucleation and growth of perovskite PZT, (f) depositing MoW alloy gate electrode for MFIS structure, (g) self-aligned P^+ source and drain doping, and (h) Completing the 1T-FeRAM cell with SiO_2 passivation and MoW metal alloy contact.

A low-temperature process is required for depositing a poly-Si film and perovskite-dominated ferroelectric film on a glass substrate. For, the low-temperature poly-Si, there are three main methods, including solid-phase crystallization (SPC), excimer laser annealing (ELA), and metal-induced crystallization (MIC). S. Jung *et. al*[12] reported that applying ELA poly-Si to the NVM showed a good electrical properties, however the ELA poly-Si has disadvantages of high roughness which degrades the storage ability and reliability performance and limits the panel-size due to its beam size. Chen *et al.*[13] showed the fabrication of NVM poly-Si cells via SPC with planarization to control the roughness surface. However, SPC poly-Si cannot be easily applied to the industry, due to the long crystallization period (>24 hrs) and the high temperature of 600 ℃. T. N. Nguyen *et al.*[14] reported that the MIC poly-Si can overcome the disadvantages of the roughness of ELA, size limitation by the beam size of ELA, long crystallization period of SPC, and high-temperature process of SPC. However, electrical properties, such as leakage current, threshold voltage, and field effect mobility, of MIC poly-Si are known to be poor due to its highly contaminated by the Ni[15], Pd[16], Co[17], Al[18], etc sources which trigger the phase transformation. Recently, C. W. Byun *et al*[19] developed a novel poly-Si crystallized by $NiSi_2$ seed-induced lateral crystallization (SILC). The $NiSi_2$ SILC poly-Si, which minimizes the metal contamination, showed superior electrical properties to other crystallizations methods.

For the perovskite-dominated ferroelectric film, poly grain structure of metal-oxide films have been widely investigated, such as $BaTiO_3$[20], $(Ba,Sr)TiO_3$[21], $Pb(Zr,Ti)O_3$ (PZT)[22], $SrBi_2Ta_2O_9$[23], etc for the dynamic random access memory (DRAM) and ferroelectric random access memory (FeRAM). Materials with crystalline structure have advantages over amorphous materials including high storage density and good reliable performance. In case of poly grain storage capacitor, two the main concerns to be considered will be the non-uniformity characteristics throughout the device due to the grain boundaries within the dielectrics and the high temperature processing (>800 ℃) which is impossible to be integrated in glass substrate electronics. J. S. Lee *et al*[24] investigated the degradation of the poly grain PZT which is originating from the grain boundaries. However, they are for sure the main cause, there is not much we can do to remove or control the grain boundaries.

In this work, we fabricated 1T-FeRAM with a single-grained PZT embedded in the $NiSi_2$ SILC poly-Si TFT fabricated on glass substrate. A large single-grained PZT was obtained by forming an artificial nucleated seed with a platinum metal anneal by a pulse of rapid thermal annealing (RTA) system and the nucleated seed and the nucleated seed was grown at 550 ℃ which is 200~300 ℃ lower than pervious reported papers. The device was fabricated within the large single-grain PZT. The proposed device showed a high electrical performance, including a long charge retention time and excellent fatigue characteristics on glass.

2. Experimental

Fig.1 shows a schematic illustration of the 1T-FeRAM based on single grained PZT as a gate insulator and $NiSi_2$ SILC poly-Si as an active layer. The detailed fabrication process is as follows. First a 200-nm-thick SiO_2 buffer layer was deposited on a glass substrate and 100-nm-thick a-Si channel was deposited by plasma-enhanced chemical vapour deposition (PECVD) at 350 ℃ shown in fig.1(a). A 5-nm-thick $NiSi_2$ layer

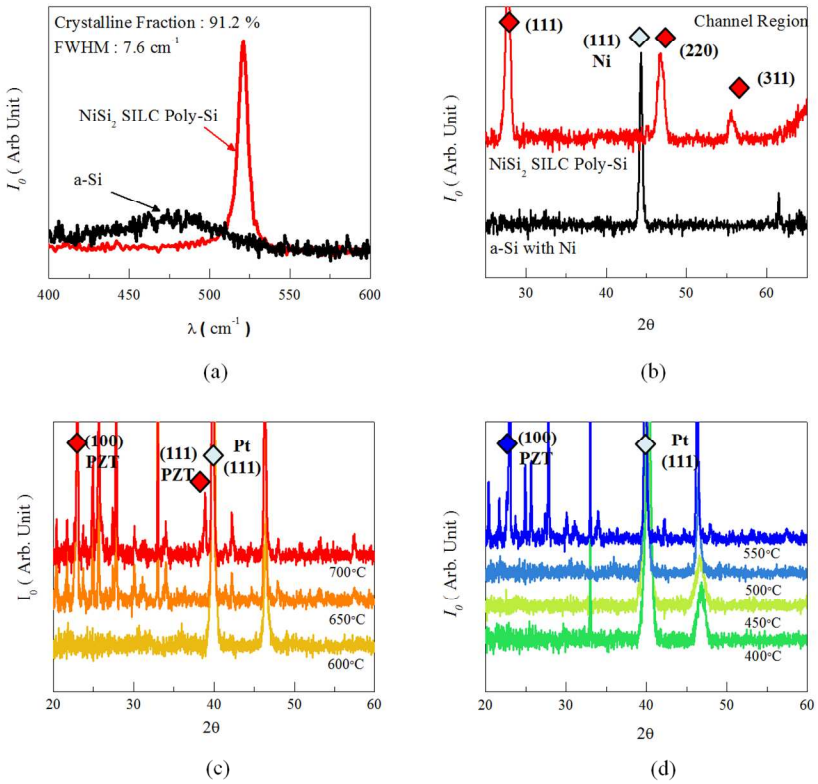

Fig. 2. (a) Raman spectra shift and (b) XRD patterns of a-Si and $NiSi_2$ SILC poly-Si film on glass substrate. XRD patterns of (c) PZT seed and (d) PZT grains depending on the various annealing temperature.

was formed on the 4 μm off-set from the active region by lift-off process and a direct-current (DC) magnetron sputtering system shown in fig.1(b). The details of $NiSi_2$ formation are reported, elsewhere[19,25]. The heat treatment was carried out hydrogen ambient at 550 ℃ for 2 hrs, so that the $NiSi_2$ triggered the lateral growth of poly-Si shown in fig.1(c). After the channel crystallization, 2-nm-thick SiON for PZT diffusion barrier was deposited by the plasma-assisted oxynitridation using N_2O gas in 100 Watts of radio-frequency plasma power at 350 ℃. Oxynitridation has advantages for smoothing the interface between the gate insulator and poly-Si channel and forming an ultra-thin layer. It is well known that PECVD methods cannot deposit an ultra-thin layer with a uniform thickness[26,27]. A 10-nm-thick SiO_2 layer as the second diffusion barrier was deposited by the PECVD at 350 ℃. A 100-nm-thick amorphous phase PZT layer was deposited by a radio-frequency (RF) magnetron sputtering system, using a single composite target of $PbZrO_{0.52}Ti_{0.48}O_3$ at 200 ℃ with a gas ratio of $Ar:O_2$=1:3. The 50-nm-thick platinum metal that formed an artificially controlled nucleated seed was deposited on the 10 μm off-set from the poly-Si channel shown in fig.(d). The perovskite-dominated PZT seeds were formed under the platinum metal after a 1 sec pulse of RTA at 650 in oxygen ambient. Afterward, the nucleated seed was grown by the tube-furnace at 550 ℃ for 2 hrs in oxygen ambient until the single grain reaches the poly-Si channel shown fig.1(e). ℃ After the single-grained PZT covers the poly-Si channel, a 200-nm-thick molybdenum-tungsten (MoW) alloy metal was deposited by DC sputtering system shown in fig (f). Although the platinum electrode is widely reported for the ferroelectric capacitor, it is not acceptable for high-density devices due to its poor adhesion and accumulation of oxygen vacancies during large number of bipolar cycles[34]. After patterning the MoW/PZT/SiO_2/SiON structure, the B_2H_6 was doped at 17 keV by ion shower system in order to form source and drain region shown in fig.1(g). The finial heat treatment was carried out in hydrogen ambient at 550 ℃ for 2 hrs, to electrically activate the dopants, and passivate the channel grain boundaries. Finally, the 500-nm-thick SiO_2 as an inter-dielectric layer (ILD) was deposited and opened for MoW alloy metal contacts in gate, source and drain shown in fig.1(h). The whole process was fabricated in a 1000-class clean room, and the electrical properties were measured by an HP E5270B system.

3. Results and discussion

To observe the crystalline fraction of 100-nm-thick $NiSi_2$ SILC poly-Si on glass was confirmed by the Raman spectra shift measurement in fig 2(a). The spectrum of the sample before the crystallization shows an broad structure at 480 cm^{-1} with a full width

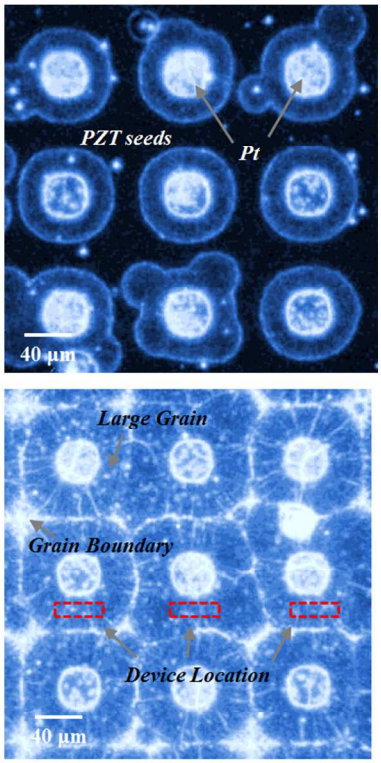

Fig. 4. SEM image of artificial nucleation and growth.

at half maximum (FWHM) of 68 cm^{-1}. This board structure is well known as a transverse optical (TO) phonon mode of the a-Si:H. After the $NiSi_2$ SILC crystallization, the longitudinal optical (LO) phonon mode of the SILC poly-Si at 520 cm^{-1} appears to replace the TO spectrum. This indicates that during the crystallization, the $NiSi_2$ seeds diffuse into the a-Si thin film acts as nucleation centres of crystal growth. The only peak point at 520 cm^{-1} with FHWM of 7.6 cm^{-1} shows that a-Si thin film has totally changed to the poly-Si thin film. The crystalline fraction is increased up to 91.2 % after the hydrogen annealing for 3 hours at 550 ℃. The shift of the visible spectrums LO-phonon peak from the position of 520 cm^{-1} was due to the stress and the defected grains by $NiSi_2$ related to the decreasing of the phonon peak coherence length which has been reported[28,29]. However, if the FWHM is smaller than 8 cm^{-1}, and if the broadening peak at 480 cm^{-1} is absent in the poly-Si, then the $NiSi_2$ defects could be disregarded. Thus, the very low metal contaminated $NiSi_2$ SILC poly-Si was obtained. The texture of the $NiSi_2$ SILC poly-Si was obtained from the XRD patterns. It can be seen that the main 3 texture of the poly-Si grains are (111), (220) and (311) at 28, 47, and 56°. Note that the a-Si phase does not reflect any preferred orientation. Thus, the a-Si with Ni film has been compared and the $NiSi_2$ seed peaks can be detected on the 45° while the $NiSi_2$ SILC poly-Si showed no peaks on the 45°.

Fig. 2(c) and 3(d shows XRD patterns of the PZT films deposited on the PZT/Pt/SiON/SiO_2/Si substrate at various annealing temperatures. XRD patterns shows that the main phase of PZT was pyrochlore under 650 ℃. The perovskite phase began to appear at 650 ℃, still with mixed pyrochlore phase. After the nucleated seed

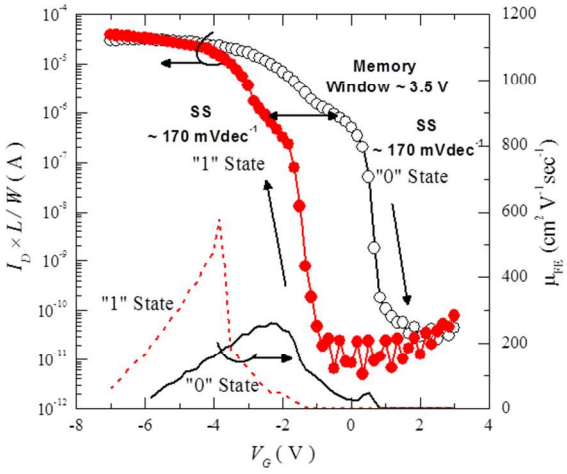

Fig. 5. Transfer and field-effect mobility characteristics of 1T-FeRAM at V_D = -0.1V

growth by the tube-furnace in various temperature, the phase of PZT films was dominated by perovskite at 550 ℃ and the texture of the perovskite-dominated PZT was (100) at 23°. Note that 40 and 47° peaks were (111)-oriented platinum layer and the poly-Si layer respectively. Compared to the results as seen in XRD patterns, the crystallization temperature was lowered more than 100℃ from the nucleated seed PZT. Thus, it enables to achieve a perovskite-dominated PZT film on a glass substrate. From above results, interval dots of Pt layers are deposited on the top of the amorphous phase of PZT and then the nucleation and lateral growth formed a large poly grains. Fig. 4 shows the scanning electron microscope (SEM) images of forming PZT nucleated seed and seed growing laterally, respectively. A 10 μm diameter of single grain was obtained and an array of devices can be fabricated within the large grains. The lateral growth was saturated of 10, 14, and 20 μm for 550, 585, and 600℃ heat treatment, respectively. Consistent results were that grain size was determined by annealing temperature, not by annealing time. J. S. Lee *et. al*[30] reported that the saturation of PZT grain growth was not observed by random nucleation and growth but observed in artificially controlled growth. The grain size was determined by the distribution of the nucleation sites and during grain growth, the other nuclei were grown and collide each other. The mechanism for this saturation of grain size is not clear yet.

The transfer and field-effect mobility (μ_{FE}) characteristics of 1T-FeRAM cell operating "0" and "1" states are shown in fig 5. According to the simplified theory of TFTs, a field-effect mobility can be extracted by the low drain voltage region (V_D = -0.1 V)

$$\mu_{FE} = \frac{\partial I_D}{\partial V_G}\frac{L}{W}\frac{1}{C_{ox}V_D}$$

where L is the channel length, W is the channel width, C_{ox} is the gate insulator capacitance, and V_D is the drain voltage. The obtained

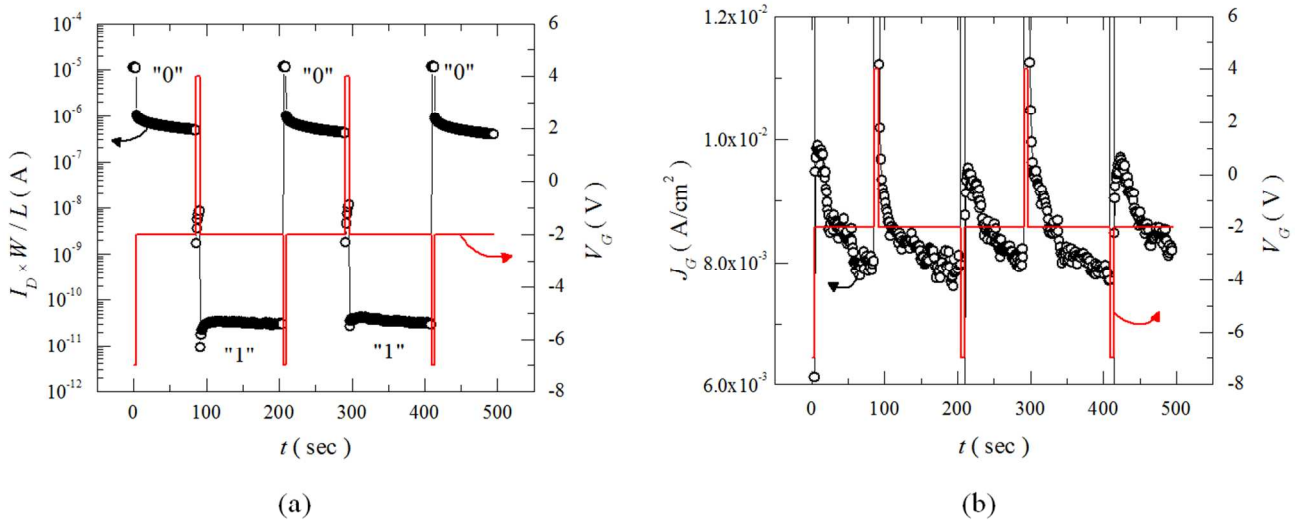

Fig. 6. (a) I_D versus time plot and (b) J_G versus time achieved from alternate -7 V for "1" state and 4 V for "0" state. The dynamic-retention measurement scheme was carried under the gate pulse width 3 msec at $V_S = V_D = 0$ V.

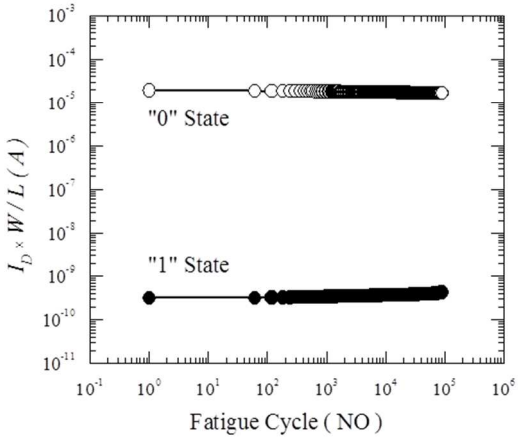

Fig. 7. Fatigue characteristics of bipolar state cycles.

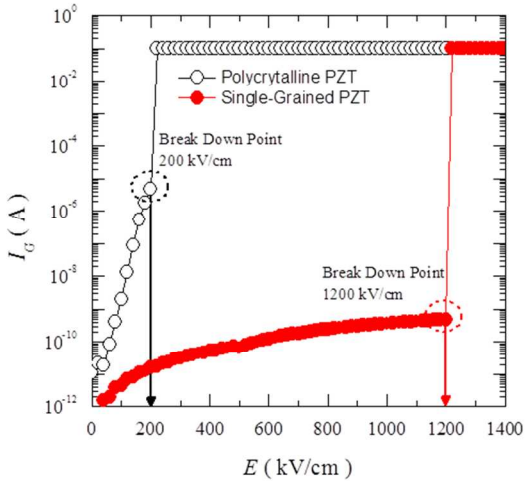

Fig. 8. Break down measurements on polycrystalline and single-grained PZT thin-films.

field-effect mobility of "0" and "1" state was 263 and 573 $cm^2V^{-1}s^{-1}$, which is the best value among those of the previously ferroelectric memory TFT based on low-temperature poly-Si and c-Si[31-35]. It is obvious that high field-effect mobility boosts the switching speed of the system. The device also demonstrated excellent electrical properties, such as high mobility, a high On/Off drain current ratio, $5x10^6$, and a steep subthreshold slope (SS), 170 $mVdec^{-1}$. From the results, strict electrical requirements for the SOG display are satisfied enough. To measure the memory characteristics of the device, the cells were programmed to "1" and erased to "0" state by applying the gate bias of -7 V and 3 V, respectively, for 1 msec where $V_S = V_D = 0$ V. It is important that lowering the gate bias and shortening the bias time drastically reduce the power consumption of the system. The memory window, defined by the difference of the threshold voltage between "0" and "1" state, was 3.5 V. Threshold voltage was defined at a normalized drain current ($I_d \times$ W/L) of 1 uA. In fig. 6, our device shows a good distinguishable on/off retention ratio of $3x10^6$ with a repetitive 1 msec pulse of -7 and 3V which are very low to operate. After the short pulse, the polarized dipole momentum is determined and the remnant polarization of the PZT controls the surface conductivity of a silicon substrate. Consequently, between "0" and "1" state electrical differences, such as subthreshold slope (SS), field-effect mobility, and threshold voltage, is affected by the remnant polarization of PZT. Reliable operation is very important in the memory device. It is well known that grain boundaries, which are randomly generated during the

phase transformation, are the serious degradation sources. To verify the reliable operation, the gate current density (J_G) was measured during the "0" and "1" state operation. The leakage level was $1x10^{-2}$ A/cm^2 at the short pulsing and $7x10^{-3}$ A/cm^2 during the remnant time. It was reported that the polycrystalline PZT thin films shows 0.1~1 A/cm^2 of J_G even at a short pulse[24,36]. The break down electric field was over 1200 kV/cm, however the polycrystalline PZT was reported to be about 200 kV/cm shown in fig. 8. We hypothesize that the small amount of drain current reduction in the initial few seconds is due to the hole charge trapping in the SiO_2/SiON diffusion barrier. It may look the PZT is losing the polarization however, a few seconds later "0" and "1" shows a very stable polarize dipole without any reduction of drain current. Fig.7 shows the test pulse sequence for fatigue measurements along with the long operation until 10^6 cycles. "1" state and "0" state operation were repeated with the continuous gate bias of -7 and 4 V for 1 msec and the reading voltage of -2 V was applied. Almost no degradation was observed for the drain currents with respect to the number of state cycles, and the memory device did not break down until more than 10^5 cycles. It has reported that the pinning of the domain walls, which inhibits polarization switching of domains, are originated from the grain boundaries of the ferroelectric material itself. In the grain boundaries, extended defects and not fully crystallized structures result in the electronic charge trapping and the oxygen vacancies shifts in the PZT[37-39]. The limitation of the ferroelectric fatigue was 10^3~10^4 cycles due to accumulation of oxygen vacancies near the electrode during the fatigue cycles. However, the number of fatigue cycles should be at least 10^5 comparing with the other non-volatile memories. The single-grained PZT were believed to be promising for the future SOG displays.

4. Conclusions

The integration of single-grained PZT films into the $NiSi_2$ SILC poly-Si TFT fabricated on glass were developed for the system-on-glass displays. The total structure of the device was MoW/PZT/SiO_2/SiON/poly-Si/SiO_2/glass. The $NiSi_2$ SILC poly-Si showed excellent field effect mobility, high On/Off drain current ratio, and steep subthreshold slope due to its high crystalline volume fraction (91.2%). We formed an artificially controlled seed from the 100-nm-thick Pt located 10μm distance from the poly-Si channel, by a short time of RTA at 650 ℃, and the seed was grown until the device was within the PZT grain, by tube-furnace at 550 ℃ for 2 hrs. This process method lowers the PZT crystallization temperature to 550 ℃, which makes it possible to use glass substrate. A large memory window (3.5 V) as well as reliable memory operation was obtained in a small voltage range, -7~3 V, and a short pulsing time of 1 mse. Operating "0" and "1" are clearly distinguished by the drain current controlled by the polarization of PZT. Moreover, it confirms that the device was very reliable after more than 10^5 repeated bipolar cycles. Therefore, these results could be potentially be integrated with the display application to realize the system-on-glass technique.

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References

1 John Y. W. Seto, *J. Appl. Phys.*, 1975, **46**, 5247
2 Gang Liu and Stephen J. Fonash, *Appl. Phys. Lett.*, 1993, **62**, 2554
3 J. Levinson, F. R. Shepherd, P. J. Scalon, W. D. Westwood, G. Este, and M. Rider, *J. Appl. Phys.*, 1982, **53**, 1193
4 C. T. Anglies, C. A. Dimitriadis, M. Miyasaka, F. V. Farmakis, G. Kamarinos, J. Brini and J. Stoemenos, *J. Appl. Phys.*, 1999, **86**, 4600
5 Z. Meng, M. Wang, and M. Wong, *IEEE Trans. Electron Devices*, 2000, **47**, 404
6 H. Tokioka, M. Agari, M. Inoue, T. Yamamoto, H. Murai, and H. Nagata, *J. SID*, 2002, **10**, 123
7 Y. Huang, B. Hekmatshoar, S. Wagner, and Jame C. Strum, *J. SID*, 2010, **18**,879
8 J. Vargheses, Roger W. Whatmore, and Justin D. Holmes, *J. Mater. Chem. C*, 2013, **1**, 2618
9 J. Hoffman, X. Pan, James W. Reiner, Fred, J. Walker, J. P. Han, Charles H. Ahn, and T. P. Ma, *Advanced Mat.*, 2010, **22**, 2957
10 J. Sung and X. Zheng, *IEEE Trans. Electron Devices*, 2011, **58**, 3559
11 B. H. Kim, C. W. Byun, S.-M. Yoon, S. H. Yang, S.-W. Jung, M. K. Ryu, S.-H. K. Park, C.-S. Hwang, K.-I. Cho, O.-S. Kwon, E.-S. Park, H. C. Oh, K.-H. Kim, and K. C. Park, *IEEE Electron Lett.*, 2011, **32**, 324
12 S. W. Jung, J. Kim, H. Son, K. Jang, J. Cho, K. Kimg, B. Choi, and J. Yi, *J. Phys. D: Appl. Phys.*, 2008, **41**, 172006
13 S.-C. Chen, T.-C. Chang, P.-T. Liu, Y.-C. Wu, P.-H. Yeh, C.-F. Weng, S. M. Sze, C.-Y. Chang, and C.-H. Lien, *Appl. Phys. Lett.*, 2007, **90**, 122111
14 T. N. Nguyen, S. W. Jung, V. D. Naguyen, and J. Yi, *J. Phys. D: Appl. Phys.*, 2010, **43**, 105406
15 S. W. Lee and S. K. Joo, *IEEE Electron Device Lett.*, 1996, **17**, 160
16 S. W. Lee, Y.-C. Jeon, and S. K. Joo, *Appl. Phys. Lett.*, 1995, **66**, 1671
17 A. E. Morgan, E. K. Broadbent, M. Delfino, B. Coulman, and D. K. Sadana, *J. Electrochem. Soc.*, 1987, **134**, 925
18 G. Radnoczi, A. Robertsson, H. T. G. Hentzell, S. F. Gong, M.-A. Hasan, *J. Appl. Phys.*, 1991, **69**, 6394
19 C. W. Byun, S. W. Son, Y. W. Lee, H. M. Kang, S. A. Park, W. C. Lim, T. Li, and S. K. Joo, *J. Electrochem. Soc.*, 2012, **159**, J115
20 L.-F. Zhung, B.-P. Zhang, L. Zhao, J.-F. Li, *J. Mater. Chem. C*, 2014, **2**, 4764
21 C. S. Hwang, S. O. Park, H.-J. Cho, C. S. Kang, H.-K. Kang, S. I. Lee, and M. Y. Lee, *Appl. Phys. Lett.*, 1995, **69**, 2819
22 S. B. Krupanidhi, N. Maffei, M. Sayer, K. and El-Assal, *J. Appl. Phys.*, 1983, **54**, 6601
23 K. Amanuma, T. Hase, and Y. Miyasaka, *Appl. Phys. Lett.*, 1995, **66**, 221
24 J.-S. Lee, and S.-K. Joo, *Solid-State Electronics*, 2002, **46**, 1651

25 C. W. Byun, S. W. Son, Y. W. Lee, S. J. Y, S. J. Lee, and S. K. Joo, *Electron. Mat. Lett.*, 2011, **7**, 298
26 K.-M. Chang, W.-C. Yang, C.-P, and C.-P. Tasi, *IEEE Trans. Electron Devices*, 2004, **51**, 63
27 C. M. M. Denisse, K. Z. Troost, J. B. Oude Elferink, F. H. P. M. Habraken, W. F. Van der Weg, and M. Hedriks, *J. Appl. Phys.*, 1986, **60**, 2536
28 J. Macia, E. Martin, A Perez-Rodriguez, J. Jimenez, J. R. Morante, B. Apar, and J. Margail, *J. Appl. Phys*., 1997, **82**, 3730
29 P.S. Lee, D. Mangelinck, K. L. Pey, Z. X. Shen, J. Ding, T. Osipowicz, and A. See, *Electrochem. Solid-State Lett.*, 2000, **3**, 153
30 J.-S. Lee and S.-K. Joo, *J. Appl. Phys.*, 2002, **92**, 2658
31. J.-H. Park, Y.-G. Yoon, and S.-K. Joo, *Integr. Ferroelectr*. 2002, **49**, 13
32. A. Chin, M. Yang, C. L. Sun, and S. Y. Chen, *IEEE Electron Device Lett.*, 2001, **22**, 336
33. G. G. Lee and B. E. Park, *J. Korean Phy. Soc.* 2010, **56**, 1484
34. J.-W. Yoon, S.-M. Yoon, and H. Ishiwara, *Curr. Appl. Phys*., 2011, **11**, S225
35. E. Tokumitsu, R.-I, Nakamura, and H. Ishiwara, *IEEE Electron Device Lett.*, 1997, **18**, 160
36 J.-S. Lee and S.-K. Joo, *Appl. Phys. Lett.*, 2002, **81**, 2602
37 W. L. Warren, D. Dimos, B. A. Tuttle, R. D. Nasby, and G. E. Pike, *Appl. Phys. Lett.*, 1994, **65**, 1018
38 S. B. Desu and I. K. Yoo, *Integr. Ferroelectr*. 1993, **3**, 365
39 J. F. Scott and M. Dawber, *Appl. Phys. Lett.*, 2000, **76**, 3801