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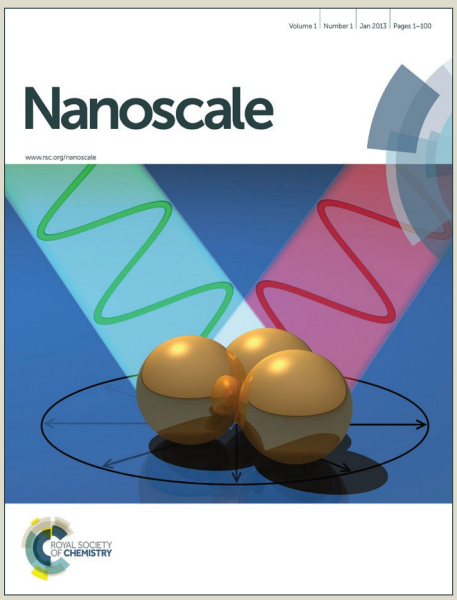

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Large-area Synthesis of Monolayer WSe_2 on SiO_2/Si Substrate and its Device Applications

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Abstract

Recently two-dimensional layered semiconductors with promising electronic and optical properties, have opened up a new way for applications in atomically thin electronics and optoelectronics. Here we report a large-area growth of monolayer WSe_2 directly on SiO_2/Si substrate by chemical vapor deposition (CVD) method under atmosphere pressure. A sub-cooling step was demonstrated as a key role to achieve this large-area growth. The monolayer configuration of the as-grown WSe_2 was proven by spherical-aberration-corrected high resolution scanning transmission electron microscopy (HRSTEM), atomic force microscopy (AFM), Raman spectroscopy and photoluminescence (PL) spectroscopy. P-type behavior of as-grown monolayer WSe_2 with mobility of ~ 0.2 $cm^2\ V^{-1}\ s^{-1}$ and carrier concentration of $1.11\times10^{18}\ cm^{-3}$ was confirmed by back-gated field effect transistor (FET) devices. This large-area growth directly on SiO_2/Si substrate provides a new way to meet the industrial manufacturing requirements.

Introduction

Monolayer transition metal dichalcogenides (TMDs), such as MoS_2, WS_2, $MoSe_2$, and WSe_2, have attracted considerable interest due to their promising electronic and optical[1-7] properties that are complementary to yet distinct from graphene[8] and boron nitride.[9,10] Flexible, nearly transparent characters with a direct band gap of 1.6 eV enable monolayer WSe_2 to fulfill the most basic requirement for electronic and optoelectronic devices.[11-13] Monolayer WSe_2 consists of three layer atoms, the selenium atoms in two hexagonal planes separated by a plane of tungsten atoms. In monolayer WSe_2, the pristine surface with free of dangling bonds dramatically decreases the surface roughness scattering, resulting in high carrier mobility and better channel charge modulation by gate voltage.[14]

Most of monolayer WSe_2 is commonly obtained from mechanical exfoliation.[11-18] However, the size of these transferred WSe_2 is too small with lack of uniformity which hinders them from being processed for devices. There are few reports on synthesis of large area monolayer WSe_2 compared to MoS_2.[19-24] Physical vapor deposition (PVD) method has been employed to synthesize the monolayer WSe_2 by using the sapphire substrate, but the size of the monolayer WSe_2 is too small as well.[25] Most recently, large-area synthesis of monolayer WSe_2 on sapphire substrate in a vacuum environment by CVD has been reported.[26] However, the expensive sapphire substrate increases the industrial manufacture cost and complicates the device fabrication process. In addition, the vacuum growth condition also increases the manufacture cost. Here we report a large area synthesis of

monolayer WSe_2 directly on SiO_2/Si substrate at atmosphere pressure by CVD method. The atomic analysis of the as-grown WSe_2 was conducted by spherical-aberration-corrected HRSTEM and AFM. Elemental composition and bonding were examined by X-ray photoelectron spectroscopy (XPS). Raman spectroscopy was utilized to identify the monolayer configuration of the as-grown WSe_2. A strong photoluminescence peak at a wavelength of 770 nm (1.61 eV) was observed at room temperature in the as-grown monolayer WSe_2. This as-grown monolayer WSe_2 was employed for fabrication of back-gated FET devices. Its photo-response was also investigated under a laser illumination with a wavelength of 514 nm.

Results and Discussions

The monolayer WSe_2 growth was conducted in a traditional tube furnace at atmosphere pressure [details in Methods]. The furnace temperature was heated to 925 ˚C followed by a sub-cooling step to a lower temperature and was kept for 15 minutes. This lower temperature was treated as the monolayer growth temperature. At 925 ˚C followed by this sub-cooling process, WO_3 first suffered a reduction reaction with H_2 without incorporation of selenium, forming a transition phase of $WO_{(3-x)}$. It was subsequently transported onto the growth substrate by carrier gas. Without this sub-cooling process, there is no growth observed on the substrate. The introduction of the sub-cooling process brings the system much less turbulence induced from vibration of the temperature. It helps the nucleation and growth. In the presence of the growth temperature, it triggered a reaction between $WO_{(3-x)}$ and selenium on the

substrate, leading to the formation of WSe_2 nuclei and growth. As we cooled the furnace to 835 ˚C, monolayer WSe_2 growth was obtained as shown in Figure 1a. However, a few WSe_2 nano-islands were observed on the top of as-grown monolayer WSe_2. It could be due to precursor lower diffusion velocity at lower temperature, resulting in precursor short diffusion length. After the formation of the monolayer WSe_2, the precursor remnants with short diffusion length could be easily trapped by as-grown monolayer WSe_2. As a result, continuous nucleation and growth happened on the surface of the as-grown monolayer WSe_2. To remove those nano-islands for high quality of monolayer growth, we intentionally cooled the furnace down to 850 ˚C instead of 835 ˚C, which causes a larger diffusion velocity in the precursor transport. Once achieving a longer diffusion length, less precursors could be trapped by the surface of as-grown monolayer WSe_2 shown in Figure 1b. As the growth temperature went to 875 ˚C, the precursor diffusion length became longer leading to much less nano-islands overlaying the surface of as-grown monolayer WSe_2 as shown in Figure 1c. However, too high growth temperature generally causes too long precursor diffusion length, which causes much less nucleation process occurred on the substrate. It explains why we are not able to achieve WSe_2 growth when the growth temperature went to 900 ˚C. The thickness of as-grown monolayer WSe_2 was characterized by AFM. The height profile in Figure 1d indicated the measured thickness was ~ 0.8 nm in consistence with reported value.[14,15,26]

Raman spectroscopy and PL are utilized for the identification of WSe_2 layer number and band gap size.[27,28] Two typical Raman active modes at 249 cm^{-1} and 260

cm^{-1} (Figure 2a) were observed in our as-grown monolayer WSe_2. E^1_{2g} (249 cm^{-1}) represents in-plane vibration and A_{1g} (260 cm^{-1}) is correlated with the vibration of selenium atoms along the out-of-plane direction. As for multilayered WSe_2, the Van der Waals force induced interactions between adjacent layers result in presence of a peak around 308 cm^{-1}.[16,26] In general, this special peak has been assigned to confirm the monolayer configuration for WSe_2 instead of peak spacing between E^1_{2g} and A_{1g}.[16,26,29] As shown in Figure 2b, there is no peak observed around 308 cm^{-1}, which indicates monolayer configuration in our as-grown WSe_2. PL in Figure 2c demonstrates a direct band gap of ~ 1.6 eV observed in our as-grown monolayer WSe_2 at room temperature, in agreement with the reported value of monolayer WSe_2.[26,30,31]

X-ray photoelectron spectroscopy (XPS) is an effective tool to examine the elemental composition and binding energy. The binding energy profile for W 4f was demonstrated in Figure 3a. The peaks at 32.6 and 34.8 eV (red line and green line) were assigned to the doublet W $4f_{7/2}$ and W $4f_{5/2}$ binding energies, respectively. The Se peaks at 54.9 and 55.7 eV (Figure 3b) were indexed to be Se $3d_{5/2}$ and Se $3d_{3/2}$ respectively. These results are in agreement with previous reported values.[26,32,33] We also observed a weak peak around 35 eV shown in Figure 3a, which could be due to the oxidation reaction during sample preparation.[26] The atom proportions of W 4f and Se 3d are 3.9% and 6.31% respectively. Comparing with the integral area covered by the peaks of W^{4+} and W^{6+}, we achieved the percentage of W^{4+} and W^{6+} atoms with the value of 82.2% and 17.8%, respectively. As a result, the atomic ratio of W:Se is

calculated to be 0.508, which is larger than the value of 0.5. Since the monolayer WSe_2 growth is from a selenization reaction of WO_{3-x}, the larger atomic ratio could be from the contribution of the reduced tungsten oxide of WO_{3-x}.[34,35] Spherical-aberration-corrected HRSTEM was applied to examine the atomic structure of the as-grown monolayer WSe_2. The WSe_2 were transferred to a TEM grid with the aid of the poly (methyl methacrylate) (PMMA) solution.[20,21] The TEM image of the transferred WSe_2 film was shown in Figure 3c. The selected area electron diffraction (SAED) pattern in the inset of Figure 3c presented one set of six-fold symmetry diffraction spots with a zone axis of [001]. The defect-free structure of the monolayer WSe_2 at the atomic level was demonstrated by HRSTEM image in Figure 3d. The brighter and dimmer dots in the honeycomb-like structure dependent on the atomic number represent the W and Se atoms, respectively. The lattice constants were measured to be a = b ~ 0.33 nm (Figure 3d) consistent with the reported WSe_2 materials.[26,36]

To evaluate the electronic property of the synthesized monolayer WSe_2, back-gated FET devices were fabricated by electron-beam lithography. The electrodes were 10 nm Ti / 50 nm Au on top of the as-grown monolayer WSe_2. An annealing process was applied to the fabricated devices at 110 ˚C for 1 h in vacuum to improve the contact between the electrodes and WSe_2.[14,37] The typical I_{ds}-V_{ds} plots of the FET device were shown in Figure 4a. It indicates that the drain current increases as an increase of negative gate, which suggests a typical p-type behavior in as-grown monolayer WSe_2-based FET device. The I_{ds}-V_{gs} plot was demonstrated in Figure 4b

by constantly applying a voltage of -2 V between source and drain. It also indicates a p-type behavior in our as-grown monolayer WSe_2. The field-effect mobility of charge carriers was calculated to be ~ 0.2 cm^2 V^{-1} s^{-1} by using an expression of $\mu = \left[{dI_{ds}}/{dV_g} \right] \times \left[{L}/{(WC_iV_{ds})} \right]$,[2,14] where L and W are the length and width of the device channel, respectively. C_i is the capacitance of the gating oxide (C_i=1.17×10^{-4} Fm^{-2} for 300 nm SiO_2), and V_g is the voltage applied as the back gate voltage. Our calculated carrier mobility is one order smaller than the reported value.[31] In our as-grown monolayer WSe_2, there are some grain boundaries observed on the surface as shown by AFM image in Figure 1d. This low field-effect mobility could be due to those grain boundaries in as-grown monolayer WSe_2. The grain boundaries cause the carriers experiencing more scattering events during the transport, which decreases the carrier mobility. From the expression of $n = {\sigma}/{\mu q}$,[38] the hole carrier concentration was calculated to be ~ 1.11×10^{18} cm^{-3}.

To investigate the device photo-response, the electrical property of the FET device was studied in dark and under different laser illumination intensities ranging from 11.7 μW to 23.3 nW (Figure 4c). The photocurrent I_{ph} (I_{ph} = $I_{illuminated}$ - I_{dark}) becomes larger with an increase of V_{ds}, resulting from the raise of the carrier drift velocity and the reduction of the carrier transit time.[5] The photocurrent was also enhanced with a dependence of the increased laser intensity. Figure 4d shows the power density dependence of the photocurrent extracted from Figure 4c. By fitting the plot with $I_{ph} \sim P^{\alpha}$, we obtained α with the value of 0.34, which is smaller than the reported value. The small value of α indicates that only part of absorbed photons are

transformed into photocurrent. The lost of photocurrent could be mainly due to boundary scattering during the photo-generated carrier transport in the as-grown monolayer WSe_2, which causes a short photo-carrier lifetime with a fast recombination of photo-generated carriers. In addition, the high contact resistance observed in our FET device also gives a rise to low photocurrent. The photo-gain (G) can be calculated by equation of $G=(I_{ph}/e)/(PS/hv)=hvR_\lambda/e$, where I_{ph} is the photocurrent, e is the electron charge, P is the incident laser intensity, S is the effective area, h is the Planck's constant, v is the light frequency, R_λ is the photo-responsivity.[39] We have a calculated photo-gain G of 0.04 and photo-responsivity R_λ of 20 mAW^{-1} at V_g = 0, and V_{ds} = 4V. The calculated value of photo-responsivity is much smaller than the reported phototransistors based on GaTe nanosheets or Si nanowires.[39,40] But our calculated value is comparable to the reported value of other monolayer 2D materials.[41] The boundary scattering and the large contact resistance could be mainly responsible for the low photo-responsivity in 2D materials.

Conclusions

In summary, we have successfully synthesized high quality of large area monolayer WSe_2 directly on SiO_2/Si substrate by CVD method at atmosphere pressure. A sub-cooling step was demonstrated as an important key to achieve large area monolayer WSe_2 growth, which should be also applicable to obtain large area growth of other monolayer TMD materials. Large area monolayer growth directly on SiO_2/Si substrate facilitates subsequent cost-effective device fabrication process. The

electronic and photo-response properties of the as-grown monolayer WSe_2 were confirmed by back-gated FET devices, exhibiting high potential for future optoelectronic applications.

Methods

Growth of monolayer WSe_2

The WO_3 powder (0.25 g) was placed in an alumina boat at the center of the furnace chamber. The SiO_2/Si substrate which is heavily doped silicon substrate coated with 300-nm-thick SiO_2 was faced down and placed on the top of the boat. The resistivity of the substrate was 1-3 Ω·cm. The SiO_2/Si substrate was placed at 4 cm away from the center of the furnace at downstream side. Another alumina boat containing selenium powder (0.03 g) was located at the upstream side of the chamber with 16.5 cm far from the center of the furnace. This location temperature is slightly higher than the melting point of selenium. During the growth process, the precursor vapor were transported to the SiO_2/Si substrate by a carrier gas of mixture of argon and hydrogen (5% hydrogen) with a flow rate of 50 sccm.

The furnace temperature was heated from room temperature to 925 ˚C at a rate of 30 ˚C/min. As long as temperature reaches 925 ˚C, a sub-cooling step was followed during the process. Furnace temperature was cooled from 925 ˚C down to a certain temperature (T) via several minutes (Δt) to gain the WSe_2 growth. After kept in this growth temperature (T) for 15 minutes, the furnace was cooled down to room temperature naturally. The monolayer WSe_2 growth under three different growth

temperature 835˚C, 850 ˚C and 875 ˚C with different cooling time of 30 min, 40 min and 50 min, respectively was demonstrated.

TEM sample preparation

We spin-coated a PMMA layer onto the top of monolayer WSe_2 on SiO_2/Si substrate at 3000 r.p.m. for 60s. Then the substrate was immersed in 5 M KOH solution. KOH solution etched the SiO_2 layer causing the PMMA/WSe_2 layer peeled off from the substrate. Subsequently, the PMMA/WSe_2 layer was transferred to deionized water to remove the KOH solution. Finally, the layer was scooped onto a TEM grid. The transferred sample was washed several times by acetone to remove the PMMA.

FET device fabrication

As-grown monolayer WSe_2 were coated with PMMA, then baked at 140 ℃ for 5 min. The electrode patterns were designed by using an electron-beam lithography system. After development in developer solution for 20s, electrode contact patterns were coated 10 nm Ti and 50 nm Au on top by e-beam evaporation process. The rate of deposition of titanium and gold was maintained at 0.02 and 0.05 nm/s, respectively. After the deposition, the devices were lift off, then baked for 1 h at 110 ℃ under vacuum environment to improve the contacts between the metal electrodes and the monolayer WSe_2.

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Figures

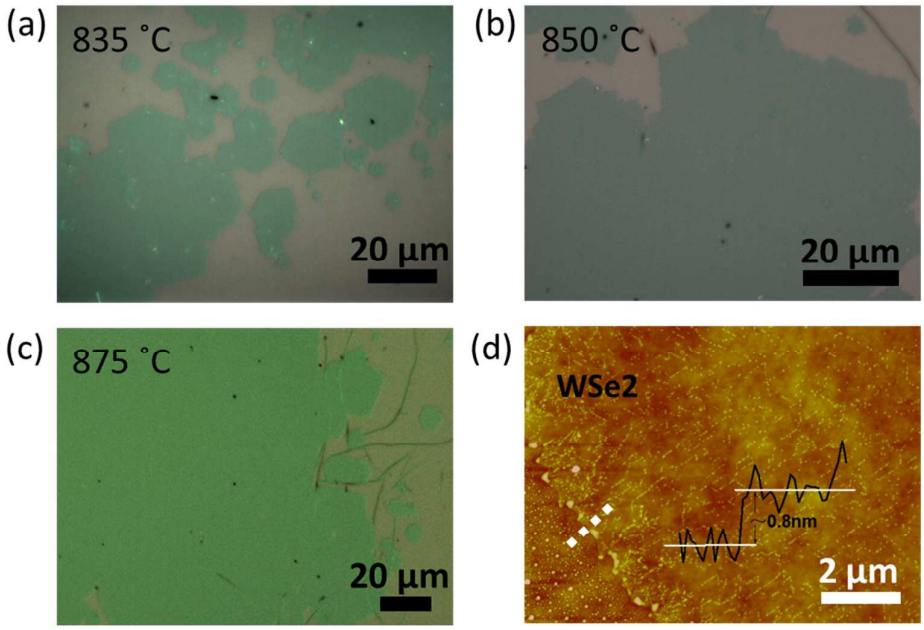

Figure 1. The morphology of monolayer WSe_2 grown directly on SiO_2/Si substrate at different growth temperature by CVD method. (a) 835˚C (b) 850˚C (c) 875˚C. (d) Height profile of monolayer WSe_2 characterized by AFM, showing a thickness of ~0.8 nm as measured along the white dotted line.

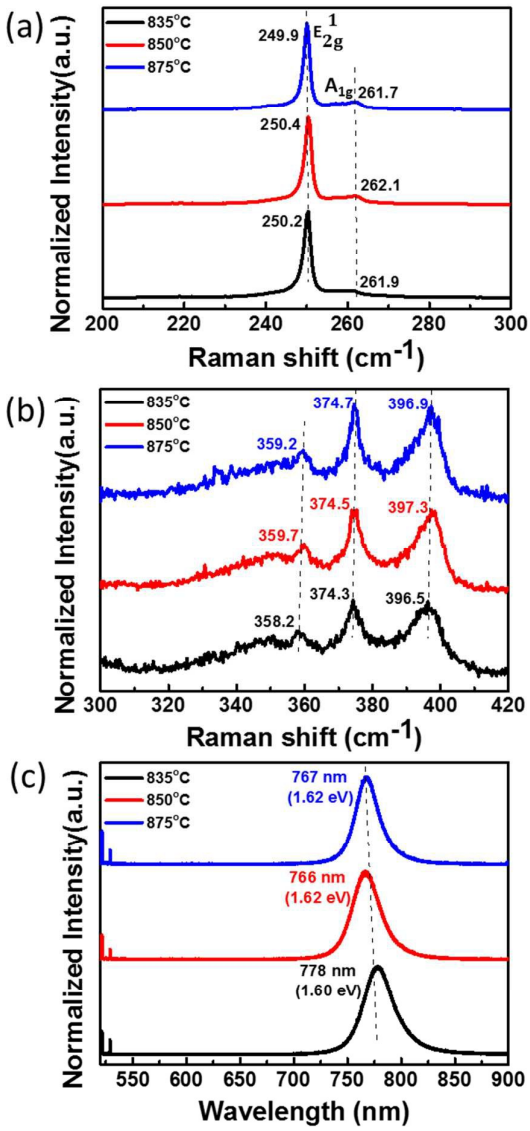

Figure 2. Raman and PL characterization of monolayer WSe_2 at different growth temperature. Raman spectra of the monolayer WSe_2 in a range of (a) 200-300 cm^{-1} and (b) 300-400cm^{-1}. (c) Photoluminescence spectra of the monolayer WSe_2 grown at different growth temperature (excitation wavelength: 514 nm).

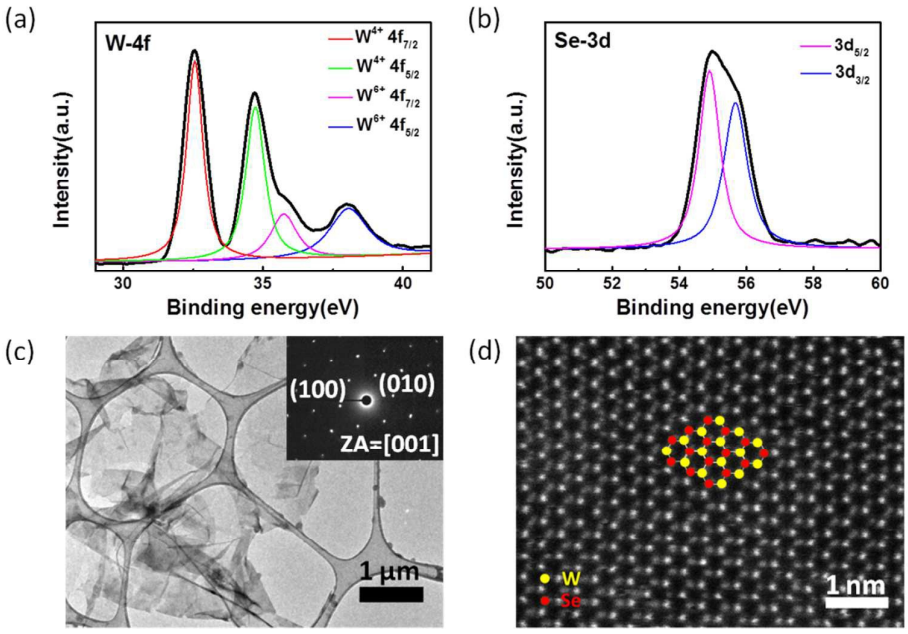

Figure 3. XPS and electron microscopy characterization of as-grown monolayer WSe_2. (a) XPS spectrum of W 4f and (b) XPS spectrum of Se 3d. (c) TEM image of monolayer WSe_2 transferred to a TEM grid. Inset: the SAED pattern demonstrating a single crystal of hexagonal structure (d) HRSTEM image of monolayer WSe_2 shows its defect-free atomic lattices. The inset cartoon spheres represent the W and Se atoms, respectively.

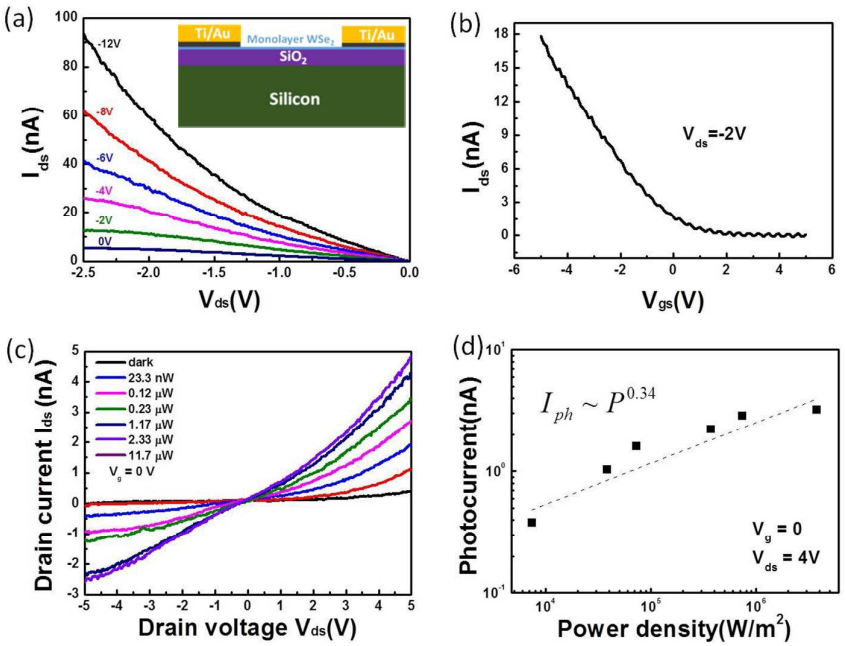

Figure 4. Electrical characterization of monolayer WSe_2 based back-gated FET device. (a) I_{ds}-V_{ds} plots of back-gated FET under different gate voltages. Inset: Schematic illustration of FET device. (b) I_{ds}-V_{gs} plot of monolayer WSe_2 based FET at V_{ds}= - 2 V. (c) Drain-source (I_{ds}-V_{ds}) behavior of the monolayer WSe_2 FET device in the dark and under different illumination intensities. (d) The power density dependence of the photocurrent at V_g=0 and V_{ds}=4V (ON state).