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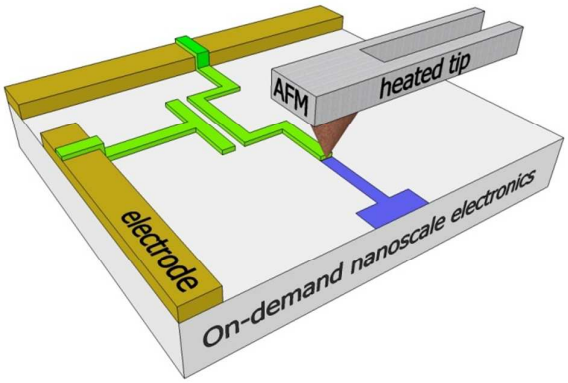
Graphical and Textual Abstract

A high-speed nanopatterning method is developed for the rapid prototyping of nanostructured active and passive components as well as fully functional organic electronic devices.



High-Speed Scanning Thermal Lithography for Nanostructuring of Electronic Devices

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Abstract

We report a detailed analysis on the use of simultaneous substrate heating in conjunction with scanning thermal lithography (SThL) to dramatically increase the patterning speed of conventional SThL systems. The investigation consists of finite element simulations as well as practical assessments of the speed at which different organic precursors are thermally converted to produce standalone electrically active and passive nanostructures. As a proof of concept the high-speed SThL method was used to pattern semiconducting pentacene nanoribbons which were subsequently incorporated into functioning transistors. Simultaneous substrate heating was found to allow patterning of functional devices at writing speeds >19 times higher than transistors produced at identical speeds but with the substrate maintained at room temperature. These fast written transistors exhibit ×100 higher hole mobility with high on/off current ratio and negligible operating hysteresis. The generality of the proposed high-speed SThL method was further demonstrated with the rapid patterning of conductive nanostructured metal electrodes with excellent spatial resolution employing an appropriate polymer precursor as the chemical resist. It is proposed that these advances further support the case for using SThL systems as rapid prototypers for low micron and nanoscale structures for both direct patterning of precursors and indirect patterning of metals and other materials using suitable chemical resist.

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Introduction

Scanning thermal lithography (SThL) used in conjunction with thermally convertible materials represent a powerful approach to create and define arbitrary patterns with nanoscale resolution directly onto different substrate materials including plastic.[1-4] A variant of scanning probe lithography, SThL uses specialised atomic force microscopy (AFM) probes that can be heated to several hundred degrees (℃) through the application of an electric current. Existing demonstrations have relied on the heat transferred from the SThL probe to a thermally convertible precursor material to initiate the chemical reaction. Important factors

involved include; the contact area between the heated probe and the precursor material, the probe temperature, the thermal properties of both substrate and precursor material i.e. density, heat capacity, thermal conductivity as well as the precursor film thicknesses. The need to transfer enough heat to the precursor to reach conversion temperature necessarily imposes a limit on the maximum scanning speed of the heated probe. This technological bottleneck has been partially overcome through the development of high-temperature SThL probes, use of *Wollaston* wire probes and by mounting arrays of heatable probes.[5-7] Although very promising, these approaches are highly complex and often costly to implement. Thus, simpler and inexpensive methods are required to fully exploit the potential of SThL in practical device applications. In spite of these current difficulties, the capabilities of the most up to date systems allow three dimensional patterning of resist materials with resolutions below 20 nm and with areal throughputs approaching those of current electron beam systems.[2] These benefits, coupled with relatively inexpensive unit costs and the ability to thermally pattern materials without the need for single pattern masks, may one day result in SThL being utilised as an alternative to established but costly methods such as photolithography and electron beam lithography.

Here we show how simultaneous sample heating during SThL can significantly increase the conversion speed of different precursor materials enabling fast patterning of electrically passive as well as active nanostructures and devices. The work has two main aspects: (i) finite element simulations to analyse the effects of simultaneous substrate heating and identifying basic trends in the maximum speed of precursor conversion that can be achieved for different substrate temperatures, (ii) practical investigations to assess the actual increase in speed that could be accomplished using a substrate heater in the patterning of stand-alone features using two precursor compounds, namely a poly(p-phenylene vinylene) (PPV) and a pentacene precursor. The PPV precursor was selected as thermal conversion

leads to the formation of glassy and highly uniform polymer layer several nanometres thick that is able to produce sharp and well defined features similar to those produced in photoresist materials using photo/e-beam lithography methods.[6] Because of these qualities, the PPV precursor was used to demonstrate the ability to pattern well-defined features at high writing speeds by SThL. The pentacene precursor was chosen in order to realise functioning nano-structured organic transistors[8] that have been patterned at far higher speeds than has previously been achieved by our group, demonstrating the versatility of the SThL method.

The concept behind the use of a substrate heater in conjunction with SThL is very simple; the simultaneous sample heating decreases the amount of energy required to reach the precursor conversion temperature, thus facilitating higher writing speeds. While this approach was first proposed by Basu *et al.*[9], here we report experimental evidence of the relationship between sample temperature and the optimum writing speed of SThL, and practically demonstrate how the writing speed of semiconducting pentacene nanoribbons can be increased by a factor of >19, yielding hole-transporting transistors with performance characteristics far superior to those achieved in devices fabricated without the use of substrate heating, and similar to those achieved by conventional hot-plate annealing in inert atmosphere. The substrate heater was also used to significantly increase the speed at which the PPV precursor could be used to write geometrical shapes and define electrode gaps below the micron scale, with a speed increase of approximately 19 times. In the case of the PPV precursor, the resulting PPV structures did not have to exhibit electrical functionality but merely had to adhere to the substrate after the unconverted precursor was removed by a developing step. In order to further demonstrate the feasibility of using SThL as a rapid prototyper we used the PPV precursor as a thermally convertible resist material with the aim indirect low-micron and nanoscale structuring of metallic electrodes[10] (in conjunction with standard wet etching methodologies) and incorporated these into functional devices.

While the results presented here have focussed on the pentacene and PPV precursor materials we anticipate the findings are quite general for the use of SThL with other material systems including semiconducting, insulating and conducting metal-oxides, metal-based conductive nano-inks (for conducting interconnects and electrodes) and many others. The modified SThL method proposed here in combination with suitable materials could provide a unique tool box that could one day be used for the rapid prototyping of nanoscale devices without the need of costly infrastructure.

Experimental

Finite Element Simulations

To explore the expected improvements that the proposed simultaneous sample heating offers, we undertook two-dimensional finite element simulations.[8, 11] Comsol Multiphysics was used for the finite element simulations, with application of the *Heat Transfer in Solids* module and the *Translational Motion* option. The heat transfer equation used in these simulations is:

$$\rho C_p \frac{\partial T}{\partial t} + \nabla \cdot (-\mathrm{k}\,\nabla \mathrm{T}) = \rho C_p(-\mathbf{u} \cdot \nabla \mathrm{T}) \quad (1)$$

Where, ρ = material density, C_p = heat capacity, k = thermal conductivity, T = temperature, and t = time. In the case of thermal equilibrium, where $\frac{\partial T}{\partial t} = 0$ (steady state), Eq. 1 reduces to:

$$\rho C_p(\mathbf{u} \cdot \nabla \mathrm{T}) + \nabla \cdot (-\mathrm{k}\,\nabla \mathrm{T}) = 0 \quad (2)$$

This model takes only takes account of conductive heat transfer; as previous simulations involving heat transfer from a heated probe to a polymer film discounted the effects of radiative heat transfer between the probe and the polymer film.[6]

Mindful of our intended final device structures (i.e. three terminal field-effect transistor), the essential structure of the model comprised a 300 nm thick SiO_2 layer, considered here as the "substrate", along with a 20 nm thick layer of the pentacene precursor.[12] The 300 nm thick SiO_2 is chosen because it resembles the actual gate dielectric used in the transistor fabricated in this work. Schematics of the model setup are shown in **Figure 1(a)-(b)**. As already noted, several parameters govern the amount of heat transferred from the probe to the precursor layer and our primary interest is to identify the maximum speed at which the probe is moved over the precursor film surface while delivering the necessary thermal energy to convert the insulating precursor film to semiconducting pentacene (**Figure 1(c)**). The degree of precursor conversion to semiconducting pentacene can then be experimentally probed by measuring the hole mobility in the resulting transistors. We note that for devices based on unconverted precursor films, no transistor action should be expected due to the highly insulating nature of the precursor films. Importantly, at very low scanning speeds sublimation of the precursor material would be expected, while at very high speeds the depth of the converted precursor is expected to diminish and lead to non-functioning transistors. Optimal hole mobility is expected to be observed in devices in which the precursor is fully converted to pentacene from the surface of the nano-ribbon all the way to the semiconducting pentacene/SiO_2 interface.

To proceed we approximated the description of our precursor materials using parameters from two materials we felt best represented the extreme ends of the conversion process for both materials. On one end of the spectrum we used poly(methyl methacrylate) (PMMA) to simulate the initial amorphous state of the precursor materials[6] as well as the

final state of the converted PPV, while on the other end of the spectrum parameters for crystalline pentacene were used to simulate the converted pentacene precursor . The chemical structures of pentacene, PPV and PMMA are shown in **Figure 1(c)**. The substrate material used in these simulations was SiO_2 which has a thermal conductivity (k) of 1.3 W mK^{-1}, a heat capacity (Cp) of 820 J kg^{-1} K^{-1} and a density (ρ) of 2600 kg m^{-3}. The materials properties of the two materials used as approximations for the pentacene precursor were poly(methyl methacrylate) (PMMA) with k = 0.19 W mK^{-1}, C_p = 1420 J kg^{-1} K^{-1} and ρ = 1190 kg m^{-3}, to simulate the initial amorphous state of the precursor material[1] while for the converted crystalline pentacene state the values of k = 0.58 W mK^{-1}, C_p = 311 J kg^{-1} K^{-1} and ρ = 1300 kg m^{-3}. Both substrate and precursor layer were modelled as semi-infinite planes in which the surface layer and sides of the polymer are thermally insulating whilst the bottom and sides of SiO_2 are connected to a heat source of 20 ℃ (simulating the ambient conditions).[6]

To simulate the effects of simultaneous substrate heating on SThL scan speed, the temperature of the SiO_2 and precursor was initially set and the probe speed required to bring the temperature of the precursor film at the SiO_2 interface up to the target temperature was identified as the maximum scan speed. For all simulations probe temperature was assumed to be constant and equal of 500 ℃. Due to the relatively low conversion temperature of the pentacene precursor (120-160 ℃), the SiO_2 sample starting temperature during the simulations was limited to 90 ℃ - well below the conversion temperature of the precursor to avoid any unwanted conversion that was not directly caused by heating from the probe - and the maximum scan speed was then evaluated for three target temperatures: 120 ℃, 140 ℃ and 160 ℃.

Nanoscale Patterning of Active and Passive Components

To test the validity of the predictions obtained from the finite element simulations we have used thermally convertible organic precursors for the on-demand writing of semiconducting nanoribbons as well as for the patterning of metallic nanogaps. In the case of active organic devices the pentacene precursor was used to produce hole transporting nanoribbons and functional p-channel transistors. For the patterning of nanoscale metal electrodes the thermally convertible precursor poly(*p*-xylene tetrahydrothiophenium chloride), or PXT, was employed as a thermally convertible resist in conjunction with established wet etching protocols to produce metal contacts separated by nanoscale gaps.

Pentacene Precursor

The pentacene precursor selected for this research was 13,6-*N*-Sulfinylacetamidopentacene [**Figure 2(a)**] purchased from Sigma-Aldrich. The precursor was incorporated into transistors by spin casting at 2300 rpm for 60 s the chloroform precursor solution (30 mg/ml) onto Si^{++}/SiO_2 substrates containing prepatterned Au source-drain (S-D) electrodes to a film thickness of 20±5 nm. The AFM system used in this study was the Agilent 5500 integrated with the Anasys SThL NanoTA system using the Anasys ThermaLever EX-AN-200 heatable probes. The substrate heater used in this research was the Agilent Sample Heater specifically designed for use with the Agilent 5500 AFM in conjunction with the LakeShore 332 Temperature Controller which was used to heat samples at a temperature of 85 ℃. SThL patterning was achieved by applying the heatable probe to the precursor surface using normal contact force and scanning at a temperature of 500 ℃ in the usual AFM imaging manner (parallel trace and retrace scan lines of varying numbers to produce block shaped structures) at different speeds between the S-D electrodes set in a perpendicular direction to the electrode interface [**Figure 2(b)**]. At sufficiently low probe speeds, the temperature experienced close to the precursor-substrate interface is high enough to convert the precursor to polycrystalline pentacene. Upon conversion the pentacene

nanostructures become insoluble allowing subsequent removal of the unconverted precursor material by rinsing in a methanol bath. Unfortunately we were unable to obtain any valuable information on the nature of the converted pentacene microstructure as a function of processing conditions primarily due to the extremely small dimensions of the patterned structures.

A schematic structure of the resulting nano-structured transistors is shown in **Figure 2(b). Figure 2(c)** show an AFM image of the actual transistors comprised of a large number of patterned pentacene nanoribbons drawn across the two gold electrodes while **Figure 2(d)** shows a higher magnification of the semiconducting pentacene nanoribbons forming the transistor p-channel. The semiconducting properties of the converted pentacene were then investigated by measuring the current flowing between the S-D electrodes as a function of the gate field.

All charge transport measurements were performed in air and were used as a mean to verify the degree of precursor conversion to semiconducting pentacene for a given scanning speed. Transistor characterisation was achieved using a Keithley 4200 semiconductor parameter analyser and a microprobe station. The current-voltage measurements were undertaken in ambient conditions with a relative air humidity of 40-60 %. The channel length and width of the resulting transistors were 10 μm and 40 μm, respectively, and were composed of approximately 400 parallel semiconducting pentacene nanoribbons. The charge-carrier mobility was extracted using the gradual channel approximation model.[13]

PPV Precursor

The high speed SThL method proposed here was also used for the patterning of metal nanogaps employing the PPV precursor poly(*p*-xylene tetrahydrothiophenium chloride) (PXT) purchased from Sigma-Aldrich [**Figure 3(a)**] as a thermally convertible resist. The

PPV precursor was spin cast onto Si^{++}/SiO_2 substrates to a film thickness of 30±5 nm at 4000 rpm for 180 s using precursor solution (0.25 wt. % in H_2O). Nanoscale patterns were written by high speed SThL in a similar manner to the pentacene precursor by scanning the heated (500 °C) AFM tip along the surface of the PXT film in a series of parallel lines in order to convert it to its insoluble PPV form. It was found that the PXT becomes insoluble (due to partial/full conversion to PPV) at temperatures as low as 110 °C – far lower than the temperature of 200 °C necessary to fully convert the precursor to PPV (which can be achieved by a post-SThL/development vacuum baking step at 200 °C[6]). As a result much higher patterning speeds than those used for pentacene could be achieved, leading to a much higher patterning throughput. **Figure 3(b)** displays the statistical average of the measured maximum patterning speeds of PPV achieved as a function of substrate temperature. It can be seen form this data that the maximum writing speed can be increased by a factor of ~19, from 63 μm s^{-1} for samples maintained at room temperature (~25 °C), to over 1180 μm s^{-1} for samples heated to 85 °C.

Following the successful patterning of PPV on Si^{++}/SiO_2 substrates, PXT films were spincoated onto evaporated electrode layers [a chromium adhesion layer (5 nm) and a gold electrode layer (35 nm)] and patterned by SThL in the same manner as for Si^{++}/SiO_2 substrates described previously. Large area conductive titanium (Ti) pads were evaporated on top of the Au/Cr layers in some instances with the intention of nanopatterning the gold source-drain nanogaps in-between the Ti electrodes. The metal etching was achieved using Sigma-Aldrich Gold Etchant Standard and Chrome Etchant Standard.

Results and Discussion

Finite Element Simulations

Benchmark results for the simulations were performed for the SiO_2 substrate and precursor initially at room temperature (20 °C) and the effect of the contact area was examined using two heated probe widths of 20 nm and 100 nm. A summary of obtained results for both PMMA and pentacene is given in **Table 1**. It can be seen that the maximum speed calculated for PMMA is around 10 times lower than that calculated for Pentacene, a difference attributed to the different thermal properties of the two materials.

Table 1. Benchmark results for the maximum speed at which the three target temperatures are reached at the precursor film/SiO_2 interface when the substrate is maintained at room temperature for both pentacene and PMMA for 20 nm and 100 nm contact widths.

	Writing speed (μm/s)			
T (°C)	Pentacene (Ø 20 nm)	PMMA (Ø 20 nm)	Pentacene (Ø 100 nm)	PMMA (Ø 100 nm)
120	5.39	0.44	12.70	1.14
140	2.81	0.24	10.51	0.84
160	1.73	0.15	7.24	0.57

Figure 4 displays the maximum scan speed as a function of varying substrate temperature for a probe width of Ø 20 nm for the three target temperatures: 120 °C, 140 °C, 160 °C. The scan speeds have been normalised to those at 20 °C (cf. **Table 1**), and as a result they naturally separate into three distinct groupings reflecting the three target temperatures for PMMA and pentacene. For all targeted temperatures the extracted maximum scan speed is found to increase upon simultaneously substrate heating regardless of the target temperature. The general increase in the scanning speed is especially profound for the higher target temperatures, suggesting increases of over 400 % in the temperature range 140-160 °C.

When the probe contact width is increased to Ø 100 nm (i.e. far greater than the precursor film thickness of ~20 nm), the amount of heat energy transferred from the probe increases. Under these circumstances each unit contact area between the probe and the precursor film receives five times the exposure duration during scanning. This effect alone results in a higher scanning speed for all target temperatures (cf. **Table 1**). Generally, as the width of the probe decreases there is a greater proportional increase in the scanning speed for a given substrate temperature. Thus the effect of substrate heating on the scanning speed appears more profound for smaller probe widths owing to the smaller amount of heat transferred from the scanning probe. Since a smaller probe width implies higher feature resolution, the advantage of using simultaneous substrate heating with SThL becomes even more significant.

The important advantages that the simultaneous sample heating has to offer can be further appreciated by comparing two scanning operations performed at the same speed. For example, using a probe width of Ø 20 nm and setting the target temperature at 120 °C, the top speed achieved with simultaneous substrate heating of 90 °C, and using a constant probe temperature of 500 °C, is identical to the speed achieved with the sample maintained at 20 °C and the probe temperature at 1400 °C. From a practical point of view this is highly beneficial as it removes the need for developing highly expensive, custom-built high-temperature SThL probes.

High Speed Patterning of Nanostructured Pentacene Transistors

For substrates maintained at room temperature, p-channel transistors produced at ~32 μm s^{-1} (close to the fastest scan speed at which working transistors could be produced) showed an average hole mobility, calculated using the gradual channel approximation[13], of around 3×10^{-5} cm^2 $V^{-1}s^{-1}$ [**Figure 5(a)**]. Maintaining the same scanning speed (32 μm s^{-1}) but

now simultaneously heating the sample to 85 °C was found to yield transistors with hole mobilities $>1\times10^{-3}$ cm^2 $V^{-1}s^{-1}$ [**Figure 5(b)**]. The latter value equals the hole mobility in transistors fabricated using the same pentacene precursor but converted using conventional hot-plate annealing in nitrogen. We note that no difference in hole mobility is observed between devices produced at the beginning and at the end of the patterning process indicating that the thermal stressing due to continuous application of the heated AFM tip is negligible and/or below our detection limit. Our results demonstrate that SThL can indeed yield transistors in which the performance characteristics are determined by the semiconducting material used rather than the conversion methodology and/or the ambient atmosphere. The dramatic enhancement in hole mobility by nearly two orders of magnitude is attributed to the increase in the temperature experienced by the precursor film leading to improved precursor conversion at the critical dielectric/semiconductor interface. Indeed, and in accordance with Tolk et al.[11], the substrate underneath the precursor layer acts as a heat sink, drawing heat away from the precursor reaction at the interface, and resulting in a layer of unconverted precursor adjacent to the interface. It follows that increasing the substrate temperature helps to reduce the temperature difference between the probe-heated area of the precursor film and the SiO_2 substrate. This allows more complete conversion of the precursor to be achieved.

In order to assess the magnitude of the speed increase achieved by simultaneous substrate heating, we have measured the speed at which the mobility achieved at 32 μm s^{-1} with substrate heated at 85 °C (1×10^{-3} cm^2 $V^{-1}s^{-1}$) [**Figure 5(b)**] decreases to the mobility value measured for transistors produced at the same speed but with the sample maintained at room temperature. Due to the discontinuous speed settings of our AFM system, the highest setting at which we were able to observe functional transistors was 620 μm s^{-1}. This upper limit in the scanning speed is primarily due to the presence of the bulky gold S-D electrodes which in turn make high speed scanning across and over the electrodes unstable and highly

problematic. Despite the high scanning speed (620 μm s^{-1}), however, the hole mobility calculated from the transistors produced with simultaneous sample heating of 85 °C was high and on the order of 3×10^{-4} cm^2 $V^{-1}s^{-1}$ [**Figure 5(c)**]. This value is higher than the hole mobility measured for pentacene transistors produced at 32 μm s^{-1} but with the substrate maintained at room temperature. The evolution of field-effect hole mobility as a function of scanning speed is shown in **Figure 5(d)**. This dramatic increase in the maximum scanning speed of at least 19.4 times higher than that achieved in transistors produced at room temperature, clearly demonstrates the benefits of simultaneous substrate heating in agreement with theoretical predictions and paves the way towards even higher throughput nanopatterning of active materials and devices. Furthermore, and based on this result, one may argue that the maximum writing speed for a sample maintained at 85 °C could well exceed 800 μm s^{-1}.

High Speed Pattering of Metallic Nanogaps

The results in **Figure 3(b)** clearly demonstrate that the scan speed can be dramatically be increased by a factor of ~19 when the sample is heated to 85 °C. The magnitude of speed increase is similar to that achieved in conversion of the pentacene precursor and can be attributed to the similar thermal properties of the particular precursor films. Interestingly, the relationship between substrate and maximum patterning speed is reminiscent of the s-shaped curve predicted by the finite element simulations in **Figure 4**, lending weight to the accuracy of the simulations in predicting the heat transfer behaviour in the model system employed [**Figure 1(b)**].

Most impressive is the quality of the fabricated PPV nanostructures which are found to be highly consistent even at scanning speeds in excess of 1000 μm s^{-1}. To further explore the suitability of these thermally converted PPV structures as a resist for chemical etching,

we have produced pairs of metal S-D electrodes separated by a small gap the length of which was varied from a few hundreds of nanometres to tens of microns. **Figure 6(a)** shows the AFM image of two Au electrodes (35 nm thickness) with a Cr adhesion layer (5 nm thickness) after being developed (see Materials and Methods). The distance between the two electrodes in this case is ~480 nm [see **Figure 6(b)**] but smaller gaps have been obtained. The latter value is primarily determined by the chemical etching step (i.e. undercutting of the metal electrodes during etching) rather than the patterning resolution of the PXT precursor which was found to be in the range 80-100 nm (i.e. roughly equal to the width of the thermal AFM probe used). Since the resolution of a particular SThL system is heavily dependent on the width of the patterning probe, systems using probes with much smaller contact widths[2] should be capable of electrode patterning resolutions far below 100 nm and approach the resolution level of commercial e-beam and high-end photolithography systems.

The versatility of the high speed SThL for the rapid prototyping of nanostructured devices was further demonstrated with the patterning of Au electrodes directly connected to pre-patterned large area Ti electrode pads. The primary purpose of these pads is to aid the contacting of the electrode nanogaps to the macroscopic electrical probes used for connecting the device to the measuring instrumentation. **Figure 6(c)** displays an example of such an Au electrodes patterned between two large Ti pads. Using these sets of electrodes functional transistors based on pentacene have been realised in air without the need of stringent experimental conditions typically required by other high resolution methods such as e-beam and conventional lithography. However, due to the rather narrow channel length and the associated parasitic contact resistances, the level of performance of these pentacene devices is low and well below what has been achieved from the devices shown in **Figure 5**.

Conclusions

We described the development of a high speed SThL method that can be used for the patterning of electrically active as well as passive components using suitable thermally convertible organic precursors. Our approach relies on the simultaneous heating of the precursor film at temperatures significantly above room temperature but below the conversion temperature of the precursor, and the simultaneous application of SThL. Based on this simple approach, the patterning speed of two different organic precursors by SThL can be increased by approximately 19 times. This highly beneficial effect is found to be more pronounced for small diameters probes allowing a significant increase in the writing speed without compromising the patterning resolution which is typically maintained at <100 nm. This improvement allows an areal patterning throughput of ~2×10^5 μm^2/hour for pentacene, all with a rather modest probe temperature of 500 °C. The proposed method is simple, economical and can be fitted retrospectively to any SThL system and/or in conjunction with more complex methods such as multi-probe arrays[14] or higher temperature probes.[5] Finally, the patterning of both electrically active and passive componets can be seen as a significant step towards inexpensive rapid prototyping of nanostructured devices entirely by SThLon demand.

Acknowledgements

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Figure Captions

Figure 1. Three (a) and two (b) dimensional schematics of the basic model used for the simulations. The system comprises of a precursor film (20 nm) on top of a SiO_2 substrate (300 nm) with a thermally resistive boundary layer separating them. The substrate bottom and sides are connected to a heat source of 20℃ to simulate room temperature ambient conditions. The interface with the heated AFM probe is represented by a heat source of a fixed temperature. (c) Chemical structures of pentacene, PPV and PMMA materials used in the simulations.

Figure 2. (a) Chemical structure of the pentacene precursor 13,6-*N*-Sulfinylacetamidopentacene before and after thermal conversion to semiconducting pentacene. (b) Schematic of the bottom-gate, bottom-contact pentacene transistors fabricated by SThL. (c) AFM topography image of a converted pentacene block composed of hundreds of nanoribbon-like structures patterned over two Au electrodes 10 μm apart. (D) A higher magnification AFM topography image from (C). The image reveals the existence of pentacene nanoribbon-like structures with widths comparable to the probe diameter of ~100 nm.

Figure 3. (a) Molecular structures of the PXT (poly(*p*-xylene tetrahydrothiophenium chloride)) precursor which thermally converts to PPV (poly(p-phenylene vinylene)) at temperatures between 120-200 °C. (b) Graph of the maximum scan speed at which insolubilised PPV precursor features were written versus substrate heating temperature. The graph reveals an increase in maximum scan speed for increasing substrate temperature. The relationship between scan speed and substrate temperature is similar to the S-shaped curve predicted by finite element simulations using pentacene.

Figure 4. Theoretical calculations displaying the relationship between the substrate temperature and the maximum scan speed at which each of three target temperature (i.e. 120 °C, 140 °C and 160 °C) is achieved at the precursor/substrate interface for two material systems namely pentacene and PMMA. The scan speeds have been normalised to the maximum scan speed with the substrate maintained at room temperature. The width of the thermal AFM probe used in these calculations was 20 nm.

Figure 5. (a) Transfer characteristics measured for a pentacene transistor produced with a scanning speed of 32 μm s^{-1} and with the substrate maintained at 20 °C with the exception of the black curve labelled "precursor" which was measured at V_D = -50 V prior to precursor conversion. In the latter case no field-effect can be observed since the unconverted pentacene precursor film is highly insulating. (b) Transfer characteristics of a pentacene transistor fabricated with a scan speed of 32 μm s^{-1} and with the substrate temperature maintained at 85 °C. (c) Transfer characteristics of a pentacene transistor produced at 616 μm s^{-1} with the substrate temperature at 85 °C. (d) Measured hole mobility as a function of probe scan speed. The channel length and width for all transistors fabricated were 10 μm and 40 μm, respectively.

Figure 6. (a) AFM topographical image of two Cr/Au (5 nm/35 nm) electrode pads with each measuring 20 μm^2 and separated by an air gap of 480 nm patterned by SThL at a speed of 1000 μm s^{-1} with the substrate temperature of 85 °C. (b) Shows the cross-section profile of the nanogaps indicating a gap width of ~480 nm. (c) Optical image of Au electrodes drawn between sputtered large area Ti contacts. The channel width (W) and length (L) of the electrode structure is 80 μm and 2 μm, respectively.

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Haberle, C. Hagleitner, J. L. Hedrick, D. Jubin, A. Knoll, M. A. Lantz, J. Pentaralkis, H. Pozidis, R. C. Pratt, H. Rothuizen, R. Stutz, M. Varsamou, D. Wiesmann, and E. Eleftheriou, IBM J. Res. Dev. **52**, 493 (2008).

Figures

Figure 1

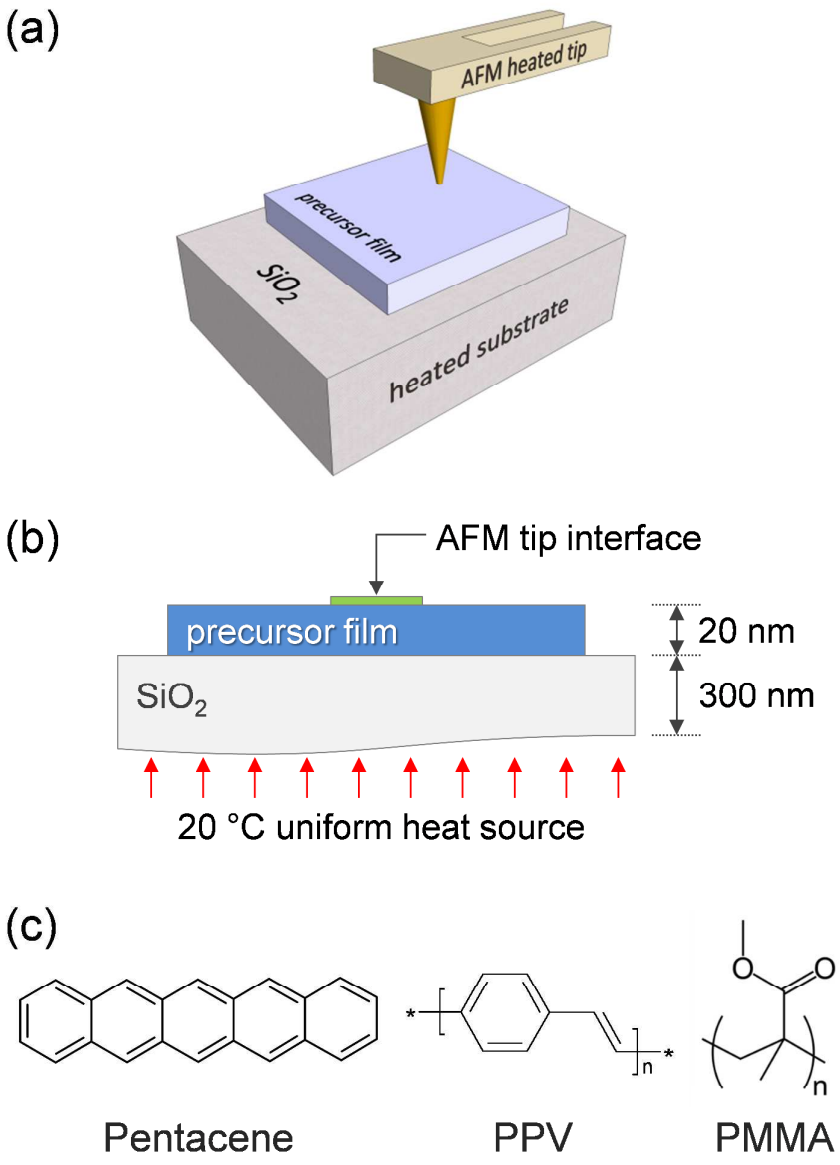


Figure 2

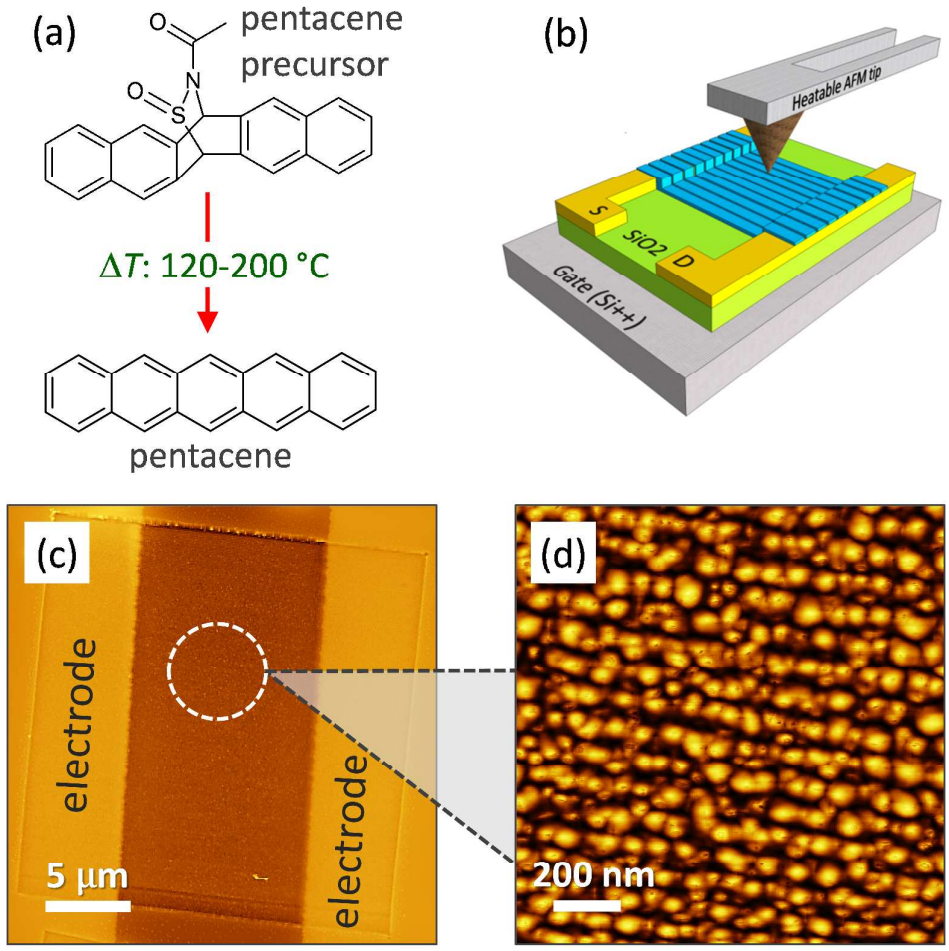

(a)
pentacene
precursor
ΔT: 120-200 °C
pentacene
(b)
Heatable AFM tip
S
SiO2
D
Gate (Si++)
(c)
electrode
electrode
5 µm
(d)
200 nm

Figure 3

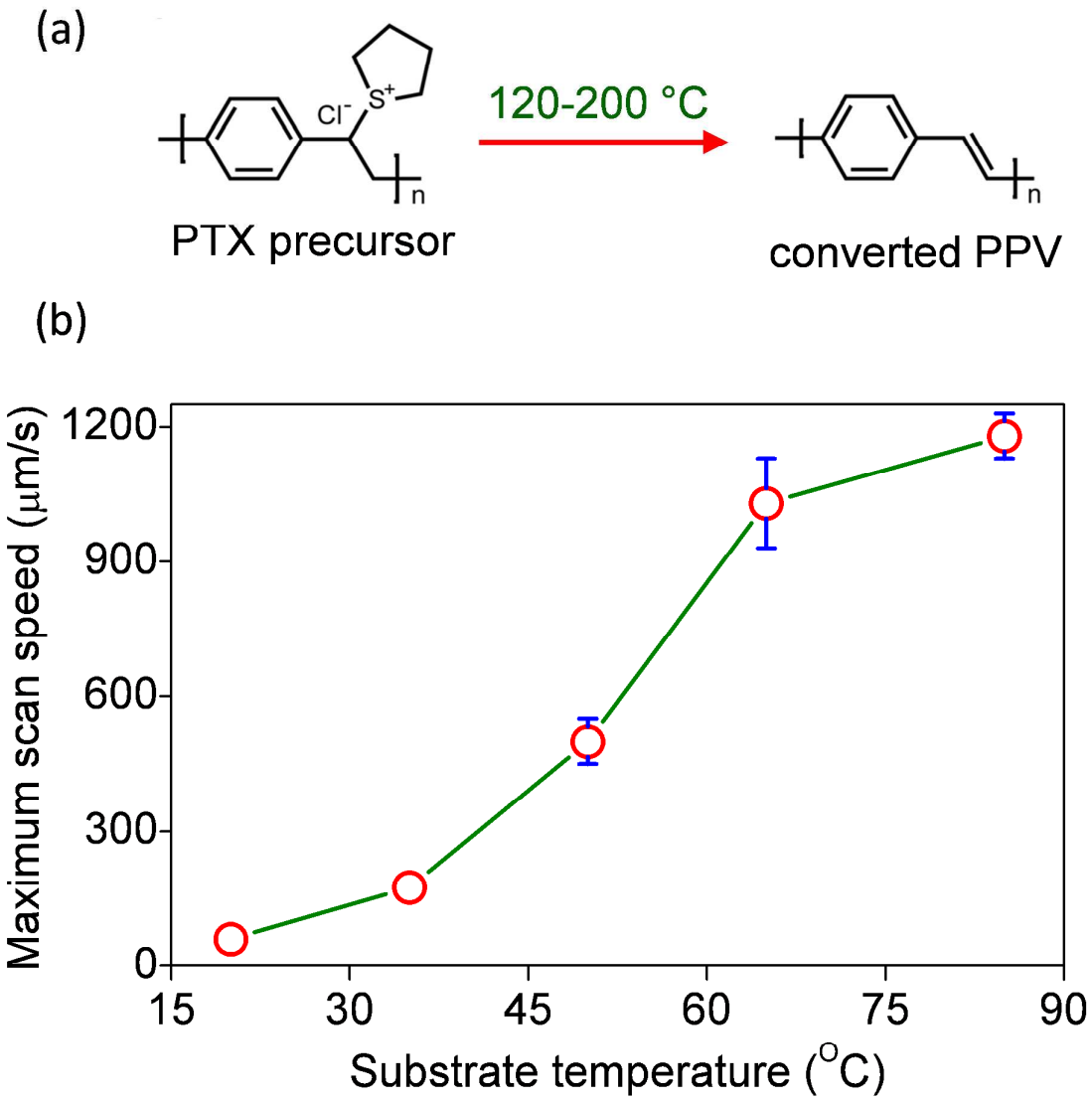

(a)
Cl⁻
S⁺
n
120-200 °C
n
PTX precursor
converted PPV
(b)
Maximum scan speed (μm/s)
0
300
600
900
1200
15
30
45
60
75
90
Substrate temperature (°C)

Figure 4

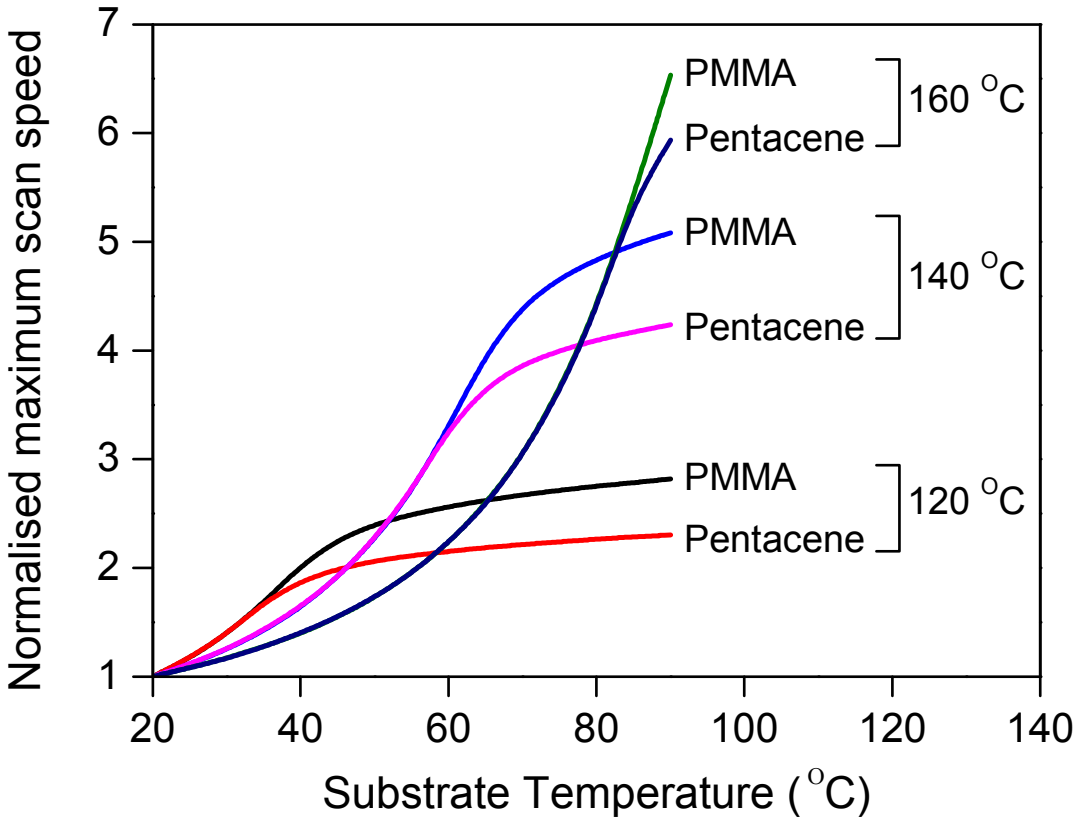

Normalised maximum scan speed
Substrate Temperature (°C)
PMMA
Pentacene
160 °C
PMMA
Pentacene
140 °C
PMMA
Pentacene
120 °C
1
2
3
4
5
6
7
20
40
60
80
100
120
140

Figure 5

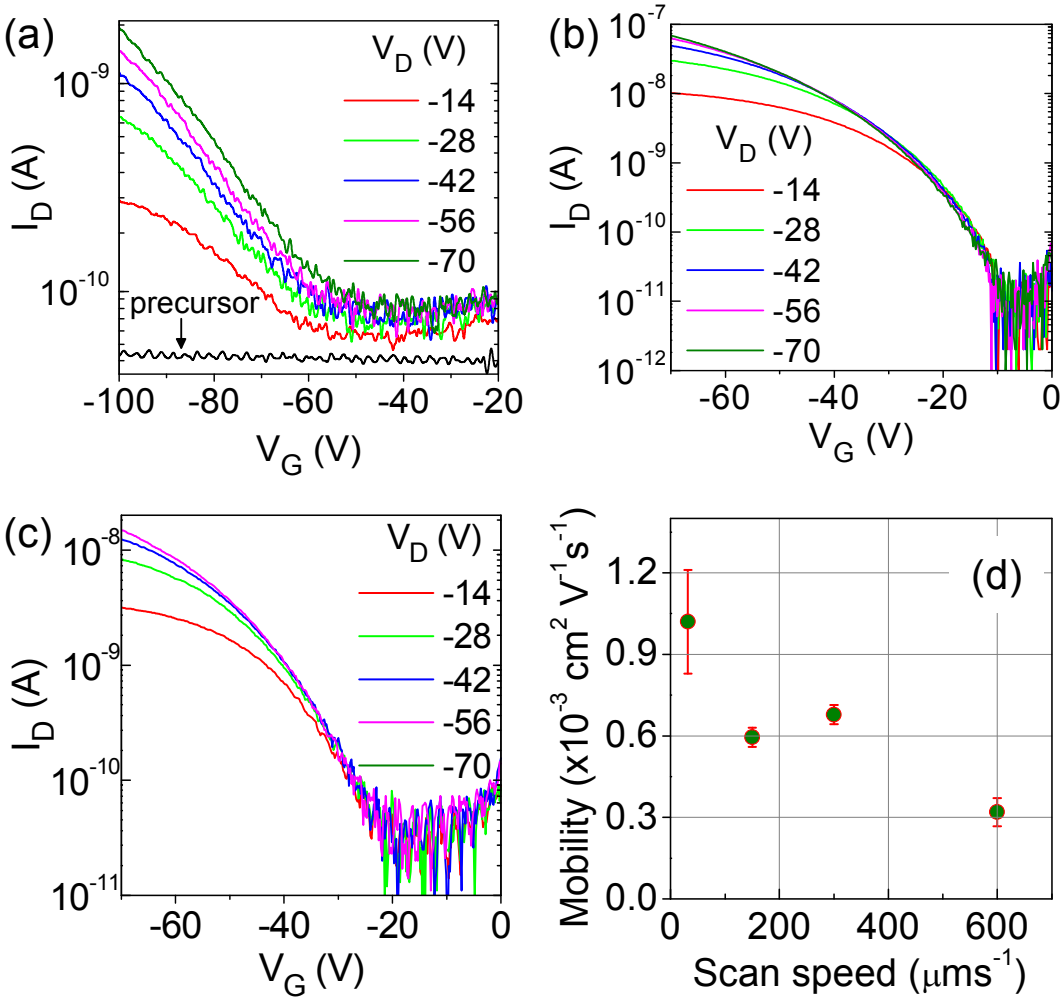
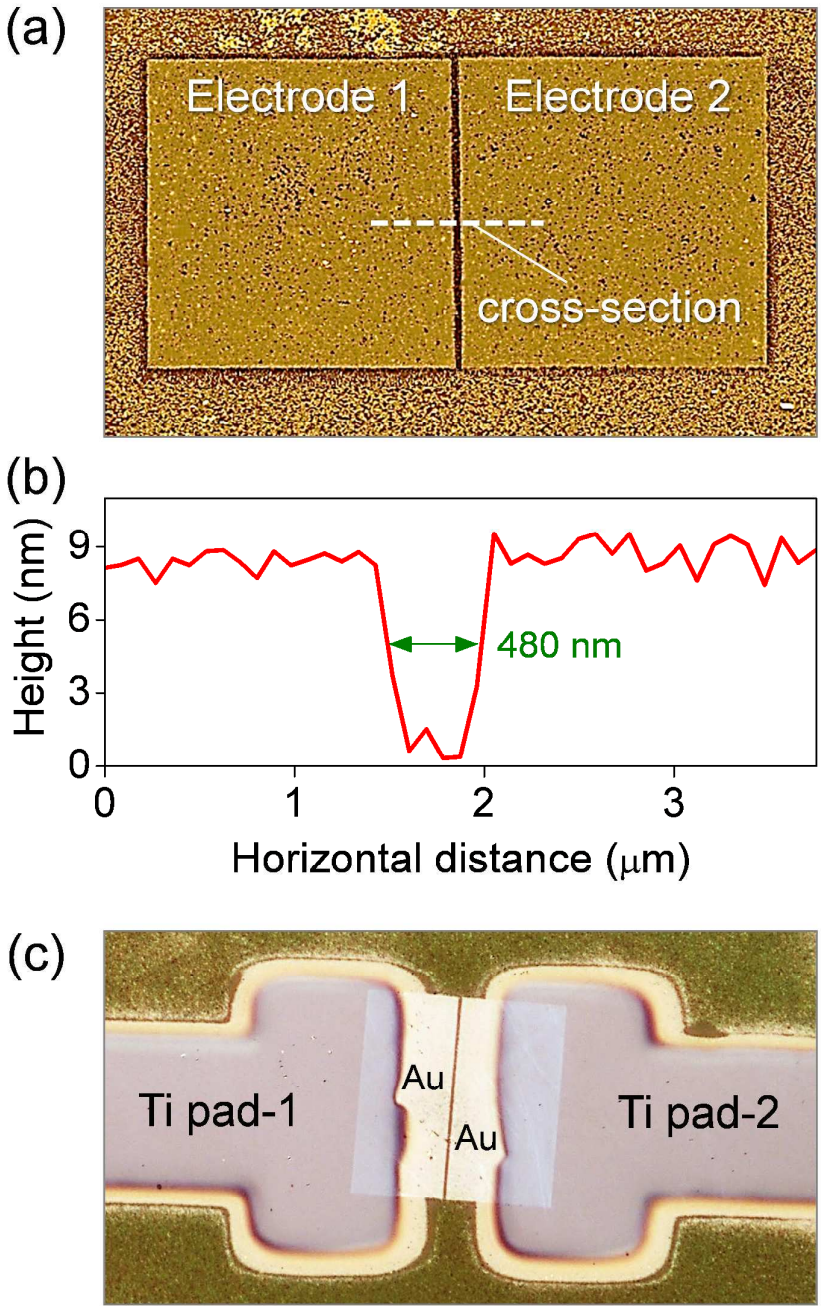


Figure 6


(a)
Electrode 1
Electrode 2
cross-section
(b)
Height (nm)
9
6
3
0
480 nm
0
1
2
3
Horizontal distance (μm)
(c)
Ti pad-1
Au
Au
Ti pad-2