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Development of High-Performance Printed Organic Field-Effect Transistors and Integrated Circuits

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Abstract:

Organic electronics is regarded as an important branch of future microelectronics especially suited for large-area, flexible, transparent, and green devices, with their low cost being a key benefit. Organic field-effect transistors (OFETs), the primary building blocks of numerous expected applications, have been intensively studied, and considerable progress has recently been made. However, there are still a number of challenges to the realization of high-performance OFETs and integrated circuits (ICs) using printing technologies. Therefore, in this perspective article, we investigate the main issues concerning developing high-performance printed OFETs and ICs and seek strategies for further improvement. Unlike many other works in the literature that deal with organic semiconductors (OSCs), printing technology, and device physics, our study commences with a detailed examination of OFET performance parameters (e.g., carrier mobility, threshold voltage, and contact resistance) by which the related challenges and potential solutions to performance development are inspected. While keeping this complete understanding of device performance in mind, we check the printed OFETs' components one by one and explore the possibility of performance improvement regarding device physics, material engineering, processing procedure, and printing technology. Finally, we analyze the performance of various organic ICs and discuss ways to optimize OFET characteristics and thus develop high-performance printed ICs for broad practical applications.

Keywords: Organic field-effect transistors, printing technology, conjugated molecules, integrated circuits, charge transport

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1. Introduction

In the past three decades, organic electronics have experienced rapid development due to its extraordinary potential for large-area, flexible, environmentally friendly, and low-cost electronics, and organic field-effect transistors (OFETs) have been an important building block. OFETs can be utilized for such applications as display, sensing, solar cells, smart labeling, memory, and more complex integrated circuits (ICs),[1] where the fast-emerging bioelectronics will make impressive and widespread use of organic semiconductors (OSCs) and OFETs.[2, 3] Even though numerous techniques have been demonstrated for OFET fabrication, the most promising approach taking best advantage of the unique features of organic electronics is solution-based printing. Compared to those made by vacuum-based processes, printed OFETs still display inferior device performance due to the low carrier mobilities historically observed in the solution processing of conjugated molecules as well as the difficulty in precisely controlling the microstructure of the active layer, resulting in high energetic disorder caused by the printing processes. These make printed OFETs difficult in building high-performance ICs for extensive applications. Fortunately, with the immense effort dedicated to the research on charge-transport and device physics,[4–6] material engineering,[7, 8] and process optimization,[9, 10] the performance-limiting factors are being rapidly overcome, and several high-performance printed OFETs and organic ICs have been reported.[7, 11–13]

In this perspective article, we specifically investigate the route to high-performance printed OFETs and organic ICs. The paper starts with the performance criteria of an OFET (e.g., charge carrier mobility (μ), threshold voltage (V_T), contact resistance (R_C), On/Off ratio (I_{on}/I_{off}), and subthreshold swing (SS)) where the corresponding limitations and possible schemes for performance improvement are examined. Next, our attention is turned to the composition of OFETs and organic ICs. By following the manufacturing sequence of bottom-contact OFET-based ICs, we begin at the initial base of the substrate and end at the elaboration of encapsulation, during which the related issues are separately addressed. After providing an overview of printing technologies and high-performance printable OSCs, we focus on the organic ICs, including basic inverters, more complex circuits (e.g., ring oscillators and logic gates), as well as other ICs and seek strategies for performance development.

2. Performance criteria

To better evaluate OFET performance, the related performance criteria first need to be understood. In the next section, we discuss the principle parameters of OFETs and illuminate their importance in developing high-performance printed OFETs and organic ICs.

2.1 Mobility

A higher mobility provides a larger output current, shorter switching cycles, and a superior On/Off ratio. Due to the very weak van der Waals forces interacting among OSC molecules, the charge transport occurs mostly by hopping. In highly crystalline OSCs such as dioctylbenzothienobenzothiophene (C_8-BTBT) and triisopropylsi-

lylethynyl pentacene (TIPS-pentacene), band-like transport similar to carrier delocalization in inorganic semiconductors has also been reported.[14, 15] This indicates that a high order and high purity of the OSC and a large charge-transfer integral by preferential molecular packing are essential. When a thin OSC film is used as an active layer in an OFET, the apparent mobility is subject to many extrinsic influences (e.g., charge injection,[5] OSC/dielectric interface effects (roughness, dielectric dipoles),[16–19] charge trapping in the OSC film and gate dielectric, related columbic scattering).[20] These factors should be considered to attain high mobility.

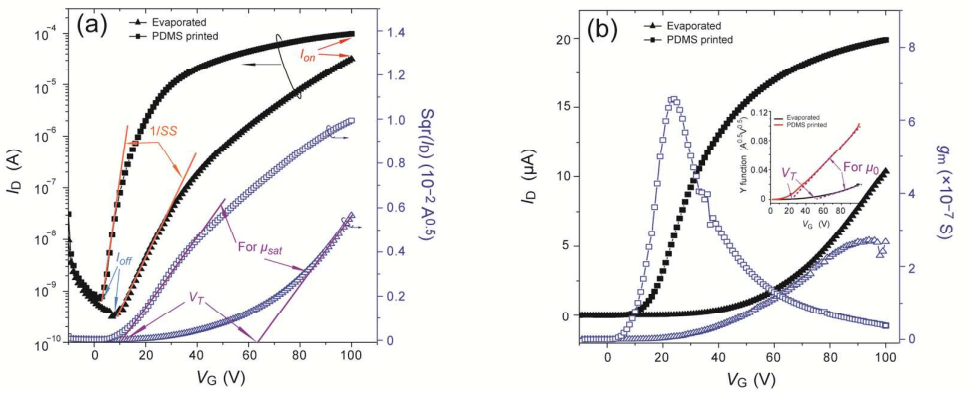

Fig. 1 Illustration of parameter extraction using the conventional technique (a) and Y-function method (b) in saturation and linear regimes, respectively, where the experimental data are taken from two OFETs with metal contacts (Au) fabricated by thermal evaporation and polydimethylsiloxane (PDMS) printing. The inset in (b) shows the Y-function for the evaluation of low-field mobility and threshold voltage.

Until now, the field-effect mobility (μ_{fe}) extracted from the saturation transfer curve has been widely used to characterize OFET mobility, as seen in Fig. 1 (a):[6]

$$\sqrt{I_{Dsat}} = \sqrt{\frac{W}{2L}\mu_{fe}C_i}\left(V_G - V_T\right) \tag{1}$$

where I_{Dsat} is the drain current in the saturation regime; W and L are the channel width and length, respectively; C_i is the gate dielectric capacitance per unit area; and V_G and V_T are the gate voltage and threshold voltage, respectively. This simple technique offers fast mobility estimation without significant impacts from the contact resistance. However, a sufficient linearity for linear fitting is not always reachable,[21] especially for the OFETs that suffer from gate-voltage dependent mobility (e.g., in polymer OFETs)[22, 23] and severe contact impacts (e.g., in bottom-contact OFETs).[5, 24] More reliable alternatives for the evaluation of OFET mobility are desired. The low-field mobility (μ_0) extracted by the Y-function method was found to be free from the degradations arising from contact resistance and interface-related scattering[24] (see inset in Fig. 1 (b)). The Y-function is defined as:

$$Y = \frac{I_{Dlin}}{\sqrt{g_m}} = \sqrt{\frac{W}{L}\mu_0 C_i V_D}\left(V_G - V_T\right) \tag{2}$$

where I_{Dlin} is the drain current in the linear regime, $g_m = \partial I_{Dlin}/\partial V_G$ is the transconductance, and V_D is the drain voltage. The μ_0 exhibited better reliability against μ_{fe} in transport studies that were often based on the mobility's temperature dependences.[15,

[25–27] Another interesting feature of the Y-function method is the direct evaluation of the contact resistance in individual OFETs, which will be discussed below.

2.2 Threshold voltage

Owing to the use of intrinsic OSC and typical accumulation-regime operations, the V_T of OFETs loses its classical meaning in Si metal-oxide-semiconductor field-effect transistors (MOSFETs) and becomes a simply fitting outcome. As stated above, the linear fittings for μ_{fe} and μ_0 deliver V_T as well via the intercepts on the V_G axis (see Fig. 1). However, the better linearity of the Y-function provides greater reliability and better reflects the threshold of charge accumulation in the channel.[28]

High-performance OFETs and organic ICs always demand a small V_T, since the operating voltage can be low. This is highly desirable for portable devices powered by battery, and meanwhile, the power consumption of an IC can be significantly reduced at lower supply voltages. To this end, making the gate dielectric as thin as possible or applying high-k dielectrics increases C_i and, in turn, decreases V_T. This is because the dielectric capacitance per unit area is

$$C_i = \frac{k\varepsilon_0}{t_i} \tag{3}$$

where k is the dielectric constant relative to that of a vacuum (ε_0) and t_i is the dielectric thickness. Note that high-k dielectrics may pose dipolar fields to the adjacent OSC that induces energetic disorder in the transporting carriers near the dielectric/OSC interface, degrading OFET mobility.[16, 17] Moreover, the long relaxation time and high defect density that have been observed in high-k dielectrics may cause large hysteresis and significant charge trapping.

On the other hand, a positive (negative) V_T is desired for n-type (p-type) OFETs, namely accumulation (or enhancement) operating mode, under which the channel is naturally off when V_G does not apply (i.e., zero). Otherwise, an oppositely biased V_G is required to deplete the charge carriers from the OSC film to turn off the channel. If the OSC film is thicker than the maximum depletion thickness, the off-state current increases quickly and the On/Off ratio deteriorates considerably. From an IC design perspective, naturally off OFETs simplify the configuration of the power supply significantly. In order to precisely adjust V_T, the fixed charges (or traps) first need to be minimized in the gate dielectric, at the dielectric/OSC interface,[29] in the OSC film, and even on the backside of the OSC film.[30] To further tune V_T for very low-voltage operations, the work function of the gate electrode should be considered to finely modulate the flat-band voltage.[31, 32]

2.3 Contact resistance

Contact resistance (R_C) is a critical figure-of-merit in developing high-performance printed OFETs, since its relatively high value of kΩ.cm (vs. 0.1 Ω.cm in modern Si MOSFETs) degrades transistor mobility and impedes device downscaling for high-density integration and high-speed operation.[5] Moreover, R_C is a major factor responsible for the poor characteristics of subthreshold swing[33] and device nonuni-

formity and instability.[34, 35]

To decrease R_C, a contact material with an appropriate work function that aligns well with the highest occupied molecular orbital (HOMO) or the lowest unoccupied molecular orbital (LUMO, typically of 3.5–5.5 eV) should be selected for efficient hole- or electron-injection, respectively. This is because the charge injection in OFETs occurs via thermal activation through an energetic barrier at the contact interface, as seen in Fig. 2. In addition to the injection barrier, a small injection area may limit injection efficiency and raise R_C. As will be discussed later, staggered devices (e.g., bottom-gate and top-contact) accommodate larger areas for charge injection and usually exhibit smaller R_C values as compared to coplanar devices (e.g., bottom-gate and bottom-contact devices).[36, 37] After being injected from the source electrode, charge carriers have to access OSC at the contacts, which is another contributor to R_C. Thus, the transport profile therein needs to be improved by optimizing the OSC microstructure, OSC film thickness, and deposition of the source/drain electrodes.[38–42]

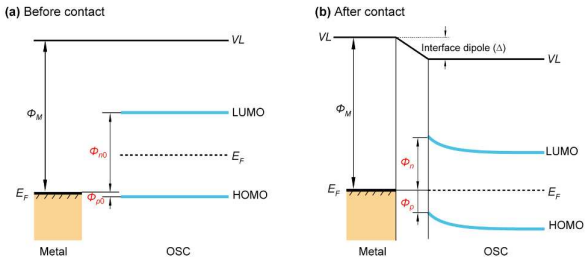

Fig. 2 Energy diagrams of the metal/OSC systems before (a) and after (b) making contact, where Φ_M represents the work function of the contact metal and E_F and VL are the Fermi energy level and the vacuum level, respectively. The theoretically predicted energetic barriers to hole- and electron-injection are Φ_{p0} and Φ_{n0} respectively. An interface dipole (Δ) is induced while making contact. It abruptly changes VL at the interface and consequently alters the hole- and electron-injection barriers from theoretical values to Φ_p and Φ_n, respectively.

The transfer-length method (TLM) has been widely used to evaluate R_C.[5] It relies on the channel resistance, and the relevant parameters (e.g., μ, V_T, and C_i) can vary substantially from device to device for printed OFETs. As a result, the obtained R_C is not accurate. A modified TLM was proposed to improve the extraction reliability and stability, in particular when only few short-L OFETs are available.[43] The R_C evaluated by TLM is only an average value for the whole group of OFETs, and a single OFET (e.g., in a bias-stress test) may need to be concentrated on, as it is difficult to prepare several devices for diverse values of L. The previously mentioned Y-function method is able to estimate R_C for individual OFETs with only one transfer sweep.[24] Besides current-voltage (I-V) methods, the four-point probe[44] and scanning Kelvin probe techniques[45] have been utilized to evaluate R_C as well by directly detecting the potential drops at the source/drain contacts.

2.4 On/Off ratio

This parameter is the maximum ratio of the drain current (often measured in the saturation regime) between the "On" and "Off" states (I_{on}/I_{off}) (see Fig. 1). It characterizes the current modulation capability of an OFET. A higher ratio is desirable, since a stronger I_{on} drives the load more rapidly and a lower I_{off} decreases stand-by leakage and thus reduces static power consumption. For a greater I_{on}/I_{off}, I_{on} needs to be max-

imized and I_{off} minimized. For the former, increasing mobility is a key consideration, and for the latter, proper material synthesis and purification, film thickness optimization, and/or parasitic leakage suppression are important to realize low intrinsic conductivity of the OSC film. Note that a larger ratio of the channel width over channel length (W/L) could increase I_{on} while keeping I_{off} nearly identical, yet it is not an inherent solution to performance improvement.

Here, we would like to emphasize the importance of the back OSC surface that has received scanty attention to date as compared to other OSC surfaces. This is because it was thought that charge transport took place in only a small number of OSC monolayers close to the gate dielectric (i.e., the nominal channel) and that the backside played an insignificant role. This is applicable for charge transport far beyond the threshold (i.e., strong accumulation for mobility evaluation), but it deviates largely for subthreshold transport (i.e., weak accumulation for I_{off} and subthreshold swing, which will be discussed below). In the subthreshold region, the electric field at the OSC film backside can turn the charge transport from bulk depletion to bulk accumulation, leading to a very different I_{off}. As reported by Boudinet et al.,[30] different self-assembled monolayer (SAM) treatments of the OSC film's backside induced dissimilar electric fields that greatly modulated the charge distribution in the OSC film around threshold (see Fig. 3), and the I_{off} and thus I_{on}/I_{off} were altered by several orders of magnitude. For a higher I_{on}/I_{off}, therefore, appropriate backside treatments with minimum native charge accumulation should be considered.

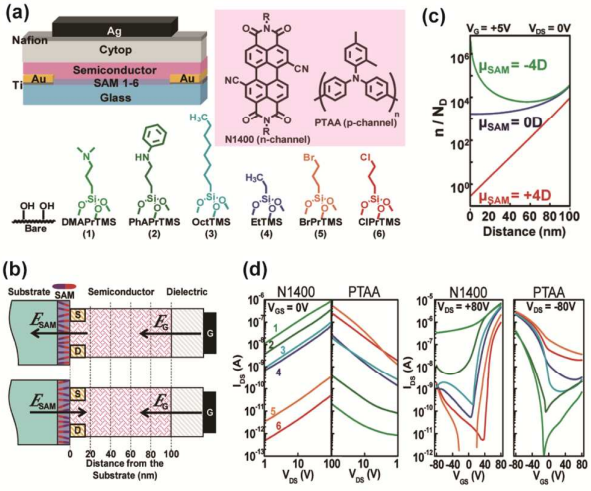

Fig. 3 (a) Schematic representation of the studied OFETs where *n*-type (N1400) and *p*-channel (PTAA) OSCs (chemical structures shown in pink region) and six different SAM precursors (chemical structures shown below) were applied. (b) Schematics of *n*-channel OFETs having negative and positive SAM dipoles on the substrate surface. (c) Charge carrier density ratio as a function of the distance from the SAM substrate surface with different dipole moments (semiconductor thickness=100 nm). (d) *I-V* plots for OFETs with different SAMs measured with a floating gate (left panel) and in the saturation regime (right panel) at the indicated biases. Reproduced with permission.[30] Copyright 2011, ACS.

2.5 Subthreshold swing

As a V_G below V_T is applied, OFETs operate in the so-called subthreshold region, and the subthreshold swing (SS) is measured at the maximum slope of log (I_D) vs. V_G, as seen in Fig. 1:[46]

$$SS = \frac{dV_G}{d(\log I_D)} = \frac{kT}{q}\ln 10\left(\frac{C_i + C_D + C_{SS}}{C_i}\right) \quad (4)$$

where k is the Boltzmann constant, T is the absolute temperature, q is the electron charge, and C_D and C_{SS} are the depletion and surface state capacitances per unit area, respectively. *SS* describes how fast the channel could switch on and off; hence, *SS* should be minimized for fast switching. In addition, a smaller *SS* shrinks V_G spanning required to fully turn the channel on and off (i.e., lower V_T and operating (supply) voltages), and a large *SS* may hinder the scalability of V_T along device miniaturization. At room temperature, the product of $(kT/q)\ln 10$ equals 60 mV so that the lower limit of *SS* is 60 mV/decade if C_D and C_{SS} are both zero. In general, C_D is considered zero for OFETs because of the intrinsic, thin OSC film and the resultant full depletion in the subthreshold region. However, C_{SS} never goes to zero. Rather, large numbers of interface states (with density $N_{SS}=C_{SS}/q$) distributing at the dielectric/OSC interface raise *SS*, typically more than 1 V/decade for printed OFETs.[47]

To decrease *SS*, C_i can simply be increased by thinning the gate dielectric or applying high-k dielectrics to lessen the weight of C_{SS} (cf. Eq. 4). Alternatively, the dielectric/OSC interface can be treated by SAMs[48] or polymers for a lower N_{SS}.[47] A better selection of gate dielectrics (e.g., Cytop, a perfluorinated polymer) and high-quality OSCs are also helpful. It is interesting to see that better charge injection achieved by using a contact interlayer was found to improve *SS*, since adequate charges fill the interface traps more rapidly while the Fermi level sweeps over these energy states.[33] As discussed above, the different properties of the OSC film's backside significantly affect subthreshold transport and do so for *SS* (see Fig. 3(c)). In the subthreshold region, the thin OSC film may be entirely depleted or accumulated. Thereby, the interface states on both sides of the OSC film play similar roles. This has been confirmed theoretically by calculation[49] and device simulations[30, 50] as well as experimentally.[30] Therefore, appropriate treatments of the back OSC surface using SAMs, polymers, passivation, and encapsulation layers could be useful to realize a small *SS*.

2.6 Hysteresis

Strictly speaking, hysteresis is not a device parameter, but it reflects device quality and stability. Hysteresis is usually represented as a V_T shift (ΔV_T) between back and forth V_G sweeping, during which the strong electrical field affects the chemical bonds of the gate dielectric and OSC and creates defects therein. These traps can capture charges for long periods of time. The exact origin of hysteresis in OFETs is still not well understood; however, several explanations have been put forth: (1) trapping and migration of dopant;[51] (2) slow relaxation of polymer dielectrics;[52] (3) dielectric charge storage caused by injection of high-energy carriers; and (4) charge trapping in the OSC film correlated with moisture, impurities, and defects. Small hysteresis is always desirable, because a large ΔV_T may cause misoperation of logic circuits and produce largely deviated output for analog circuits. In this respect, ordered OSC molecular packing, surface treatment of both sides of the OSC film, purification of the dielectric and OSC, and application of dielectrics with short relaxation time as well as

passivation and/or encapsulation are essential.

2.7 Uniformity and stability

Another criterion of OFET performance is uniformity and stability. High uniformity requires all of the precedent parameters to be almost identical from transistor to transistor, which is important to large-scale organic ICs. For instance, the stability of V_T (or ΔV_T) is vital to backplane transistors in active matrix organic light-emitting diodes (AMOLEDs) where transistors supply current to light-emitting pixels so that, under a given biasing condition, the same amount of current is desired to emit the same light intensity. Typically, a ΔV_T less than ±1 V is needed for AMOLEDs using two transistors and one capacitor driving circuit.

For printed OFETs, however, this may prove difficult. Except for the routine attention that should be paid to OSC deposition and surface treatments, printing-related variations in film thickness (especially for the gate dielectric), microstructure (molecular packing, orientation), and charge injection (due to gate/contact misalignment, contact surface roughness, etc.) should be minimized. Annealing at appropriate temperatures is a useful way to improve uniformity, because it removes residual solvent, adsorbed moisture, and impurities; mechanically relaxes the stacked films; and chemically stabilizes all films and their interfaces.[53] With regard to stability, it is often characterized by bias-stress measurements. For instance, continuous V_G bias stress increases hysteresis for the reasons explained above and can degrade *SS* due to defect generation, or it can shift V_T and decrease the output current owing to deep traps within the energy band gap of the OSC. Hence, highly ordered and pure OSC film is indispensable. Moreover, the innate stability of OSCs is also important (i.e., the photo and chemical stability of the conjugated molecule structures and their degradation over time can lead to the deterioration of OFET performance). Finally, passivation and encapsulation are also vital to retaining long-term device stability.

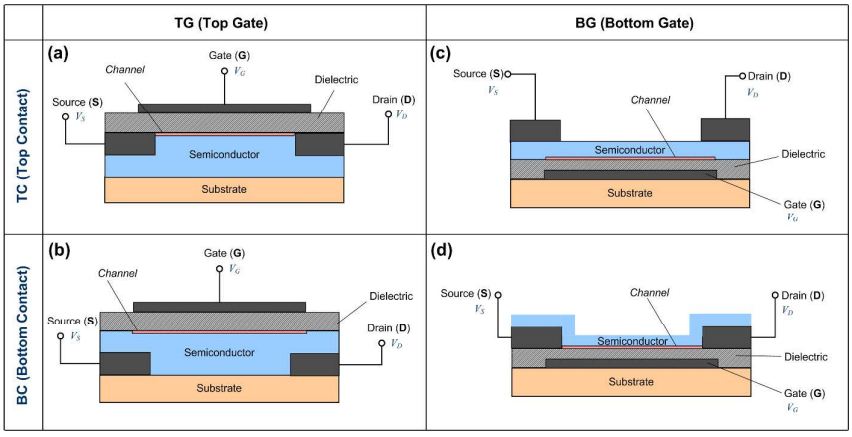

Fig. 4 Section schematic of four configurations of organic transistors. (a) and (b) are top-gate (TG) configured, with top-contact (TC) and bottom-contact (BC) configured source and drain electrodes, respectively. (c) and (d) are bottom-gate (BG) configured, with TC and BC source/drain electrodes, respectively.

3. OFET composition

Here, we examine the OFET components (perhaps not fully printed) one by one and discuss the associated limitations to printing fabrication and performance im-

provement.

3.1 Device structure

Device structure affects not only fabrication feasibility but also device performance. Once the OSC is fixed, an optimal device configuration should be designed with accessible materials and processing facilities. The possible structures of printed OFETs are shown in Fig. 4.

In terms of gate configuration, (a) and (b) have bottom-gate configurations, while (c) and (d) have top-gate configurations. The bottom-gate (BG) architecture has often been utilized in laboratory research because of the commercially available doped Si wafer covered with thermally grown SiO_2, which serve as the BG electrode and dielectric, respectively. Besides ease of use, the advantage of such BG OFETs lies in the fair quality of SiO_2 for OSC deposition that is sensitive to the substrate roughness and surface energy, and various surface treatments can easily be applied.[54] The disadvantages of such a BG configuration include substrate rigidity and the difficulty involved in making ICs because all OFETs share a common gate. If applying substrates other than Si/SiO_2 (e.g., plastic foils), additional BG electrodes and dielectrics as well as via holes for interconnection should be fabricated. However, this leads to the loss of the previously mentioned benefits of BG OFETs. The top-gate (TG) configuration obviously makes it easy to compose ICs, and the gate dielectric acts as a passivation layer that naturally protects the underlying OSC film. However, the relatively rough upper surface of the OSC film causes strong scattering to the surface transporting carriers and lowers the TG OFETs' mobility.[55] Then again, processing a TG dielectric atop an OSC is in principle difficult and harmful, especially for printing. An orthogonal solvent for dielectric printing or coating that does not dissolve or change the OSC properties needs to be selected.

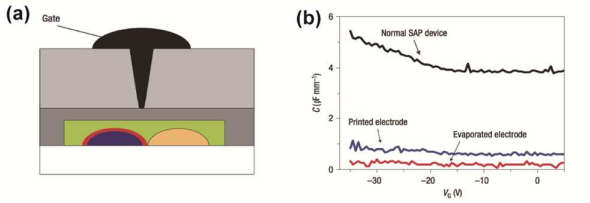

Fig. 5 (a) Schematic of self-aligned gate (SAG) architecture. (b) Capacitance-voltage characteristics of a poly(dioctylfluorene-*co*-bithiophene) (F8T2) OFET with self-aligned printed (SAP) S/D electrodes and unconfined poly(3,4-ethylenedioxythiophene) doped with polystyrene sulfuric acid (PEDOT:PSS) top-gate electrodes (black line). The first S/D electrode was defined by evaporation and photolithography (evaporated electrode), and the second electrode was defined by SAP (printed electrode). Overlap capacitances were measured between the gate and printed (blue line) or evaporated (red line) electrodes in the SAG architecture and in a normal SAP device in which the PEDOT:PSS was printed directly on the PMMA gate dielectric layer (black). Reproduced with permission.[58] Copyright 2007, NPG.

In terms of contact electrodes, there are bottom-contact and top-contact configurations. The bottom-contact (BC) architecture is known for its detrimental effect on the OSC morphology around contacts, which degrades the charge injection and overall transport.[24, 56] Thanks to pre-fabrication before OSC deposition, BC electrodes can be patterned by various techniques with high resolution. The top-contact (TC) configuration does not affect the OSC morphology. Hence, TC OFETs often exhibit better per-

formance than BC ones. However, they require the use of a shadow mask, which increases cost and downgrades patterning resolution (>30 μm). Moreover, TC metallization or deposition atop an OSC is harmful,[57] similar to TG dielectric processing.

Combining gate and contact configurations, there is an alternative classification of device structure: coplanar or staggered. In a coplanar architecture, the source/drain electrodes and the gate dielectric are situated on the same side of the OSC film. This is in contrast to a staggered architecture where the source/drain electrodes and the gate dielectric are located on opposite sides of the OSC film. In general, staggered OFETs deliver better performance than their coplanar counterparts.[5] The main reason is the small charge injection area in coplanar OFETs, where the charge distribution discontinues at the channel ends (sometimes modeled as a depletion transition zone around contacts with very low conductivity), making charge injection sensitive to the injection barrier.[37] However, in staggered OFETs, the overlapping between gate and source/drain electrodes couples, inducing parasitic capacitances that may slow down the operating speed. Noh and coworkers developed a self-aligned gate (SAG) architecture to minimize this detrimental effect and obtained Megahertz operations[58–60] (cf. Fig. 5). Nevertheless, zero and even negative gate/contact overlapping eliminates the aforementioned advantages of the staggered architecture, as observed in novel nano devices.[61–63] The limited charge injection severely degrades device performance, showing as lower μ and higher R_C.[32, 42] Upon these observations, an optimal contact length was proposed that minimizes contact limitations while maintaining the smallest contact size.[42]

3.2 Substrate

The wide variety of substrates determines the special features of organic electronics. In OFET fabrication, substrates serve as not only the mechanical support but also a template for OSC deposition. The latter critically affects the resultant device performance. The substrate surface that is in direct contact with the OSC should be smooth, clean, and with a low surface energy so that surface treatments (SAM, polymer coating) are helpful.[52, 64] Moreover, the substrate itself should be chemically resistive to the solvents used for the subsequent processes and physically stable under tensile/compressive strain and modest heating. Even though Si/SiO_2 and glass provided great accessibility and good quality, they were not compatible with large-area printing for flexible ICs. Thus, attention was turned to plastic (e.g., polyimide, polyethylene naphthalate (PEN), polyethylene terephthalate (PET), and polycarbonate), metal foils, and paper (e.g., film papers, band notes, etc.) substrates,[65–67] on which the OFETs showed comparable performance to those on rigid substrates.[68]

3.3 Source/drain electrodes

A small energetic barrier to charge injection is the primary factor in choosing materials for source/drain (S/D) electrodes. In the early stages of OFETs, research metals with high work functions (*WFs*) (e.g., Au, Ag) were selected for their theoretically predicted small barriers to hole injection as well as easy metallization using thermal evaporation in a vacuum. The low-*WF* metals (e.g., Ca, Al, and Mg) are not stable in

the atmosphere with the presence of oxygen, moisture, and other reactive matter, and careful isolation by inert gas or a passivation layer is required. Consequently, the performance of *n*-type OFETs has been limited by large electron-injection barriers. It was then realized that the interface is never ideal, and a more or less interface dipole always presents, which in principle decreases the S/D electrodes' *WF* so that the hole-injection barrier is elevated and the electron-injection barrier is reduced[69, 70] (cf. Fig. 2). The direction and magnitude of such dipoles depend on the materials applied for the OSC and S/D electrodes and even their deposition order (i.e., TC or BC).[71] An analogous principle was adapted for SAMs and contact interlayers (polymers like poly (3,4-ethylenedioxythiphene) PEDOT:PSS[69] and metal oxides like MoO_3),[33, 72] by which injection properties are effectively improved. Compared to holes, electron injection has received little attention mainly due to the instability of low-*WF* metals and the related interlayers (e.g., tetrakis(dimethylamino)ethylene (TDAE)).[73] Recently, Zhou et al. reported an encouraging breakthrough.[74] An ultra-thin surface modifier of polymers containing aliphatic amine groups polyethylenimine ethoxylated (PEIE) and polyethylenimine (PEI) significantly reduced the *WF* of a wide spectrum of conductors, including ITO, ZnO, FTO, Au, Ag, Al, PEDOT:PSS, and graphene. The test of *n*-type N2200 OFETs with Au contacts showed that the device performance was drastically improved: V_T was decreased from 4.5 V to 0.4 V, and μ was increased from 0.04 cm^2/Vs to 0.1 cm^2/Vs.

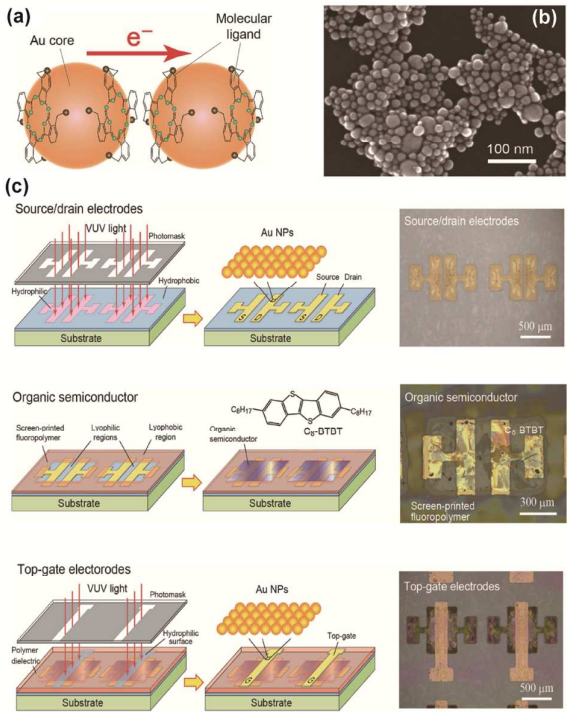

Fig. 6 (a) Schematic illustration of π-junction Au nanoparticles (NPs). The metal core is surrounded by aromatic molecular ligands. (b) Scanning electron microscope image of Au NPs deposited on a substrate. (c) Schematic illustration of OFET array fabrication using the room-temperature printing method. Reproduced with permission.[75] Copyright 2014, Wiley VCH.

Another factor in fabricating S/D electrodes is the charge injection area. Staggered OFETs can afford a larger injection area, as discussed above. If the application of a

coplanar structure is imperative, the area limitation can be alleviated by device design.[76] Xu et al. investigated the contact thickness effects of BG/BC OFETs and found that thicker BC electrodes (10–100 nm) in amorphous-like pentacene OFETs improved device performance with a larger injection area (mostly contact edge). However, for highly crystalline pentacene OFETs, unexpected negative effects were observed, because thicker BC electrodes caused inferior OSC morphology at contacts that predominately limited charge injection.[77]

Following interface injection, the next access transport in OSC bulk at/around contacts contributes to R_C and device nonuniformity and instability. The OSC morphology at the BC contacts needs to be improved by using SAM treatments, and the TC contact processing (printing or metallization) needs to be optimized to minimize damage and contamination to the OSC film. Alternatively, interlayers and reactive metals such as Cu[78] and Ti that provide spontaneous oxide interlayers can be applied.

The final consideration is solution processability. Conductive polymers (e.g., PEDOT:PSS, polyaniline (PANI), and polypyrrole (PPy)) are appealing candidates. Recently, graphite-based and metal nanoparticle (NP) inks were employed in an attempt to provide higher conductivity and low temperature processing. Minari et al. reported fully room-temperature printed C_8-BTBT OFETs with π–junction Au NPs for S/D and gate electrodes.[75] New Au ink was developed using a derivative of metal-free phthalocyanine as the conductive ligand that enabled close contact between Au NPs without annealing (cf. Fig. 6) and led to comparable conductivity to pure Au. The fabricated OFETs exhibited high mobility up to 7.9 and 2.5 cm^2/Vs on plastic and paper substrates. As contact treatment and interlayers are almost indispensable for S/D electrode fabrication, they are more solution processable. Fortunately, SAMs and polymers are based on solutions, so they can be easily printed. For other interlayers, such as metal oxides, solution processing has been reported,[79] and it is currently under extensive study.

3.4 OSC film

The OSC film is an active medium that allows the charge transport to conduct the output current, and it is the most important component in OFETs. Various intrinsic and extrinsic factors—including interaction, orientation, and packing of OSC molecules; material purity; number of grain boundaries in the channel; etc.—affect charge-transport properties. In the framework of Marcus theory, the charge-transfer integral and reorganization energy are crucial to determine an OSC's transport capability, namely carrier mobility. Hence, huge efforts have been dedicated to new OSC synthesis. We will address OSCs in Section 5, but here, our attention is placed on the fundamentals of OSC film and its charge transport.

High purity is desirable, because the presence of impurities interferes with molecular organization during OSC deposition, leading to defects and structural disorders that degrade the transport profile. In addition, impurities can act as trap centers during device operation, causing inferior mobility, nonuniformity, and instability. Structural disorder is significant in small-molecule OSC films. Thus, they should be well purified before device fabrication (e.g., by a train sublimation apparatus used to purify

light-emitting and charge-transport materials for OLEDs). Interestingly, solution-processed small-molecule OSCs such as C_8-BTBT and TIPS-pentacene tend to crystallize, through which impurities are separated out and the rigorous requirement of high purity is relieved.[80] For polymeric OSCs, purification is not easy, yet their morphologies are less sensitive to impurities compared with inorganic crystals and organic small molecules, and the phase separation in OSC solution helps to further reduce the impact of impurities.[26, 81]

Ordered molecular packing with preferential orientation of the OSC is essential to achieve high performance. If molecular packing is disrupted (e.g., by substrate roughness or impurities), grain (or domain) boundaries are created. Deep traps residing in these boundaries can significantly reduce OFET mobility and negatively affect uniformity and stability. Application of a specific solvent, treatment of the substrate surface,[82] and annealing after OSC deposition can help to improve OSC's packing orderliness. Liu et al. analyzed annealing effects on solution-processed *n*-type terrylene tetracarboxdiimide (TDI) and found that the amorphous TDI films became highly crystalline and ordered upon annealing at 180ºC for 10 min,[83] which was evidenced by AFM and XRD results, as shown in Fig. 7. A similar result was observed by Piliego et al., where thermal annealing at 110ºC in a vacuum for 1 h greatly improved OSC morphology and device performance and stability.[53]

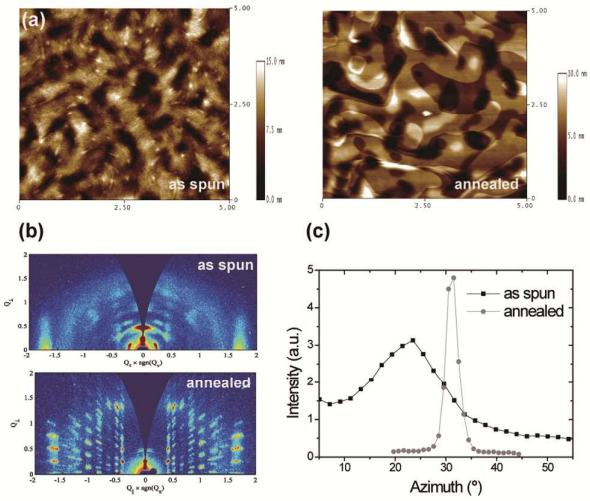

Fig. 7 (a) Tapping mode atomic force microscopy (AFM) image of TDI film, topographic image of as-spun film (left), film annealed at 180°C for 10 min (right). Average surface roughness of the areas taken was 27.8 nm and 18.0 nm, respectively. (b) X-ray diffraction (XRD) patterns of a TDI film on SiO_2 before (a) and after (b) annealing at 180°C. (c) Azimuthal projections of the columnar reflections in (a) and (b). The reflections of the "as-spun" and annealed films are centered at 22.8° and 31.1° with a full width at a half maximum of 13.4° and 2.7°, respectively. Reproduced with permission.[83] Copyright 2010, ACS.

Orientation affects performance in a different way. As the intermolecular electronic conjugation is directional, the largest direction is preferred for charge transport along the source to the drain. Directing the orientation of the OSC is difficult in printing methods due to the uncontrollable solution spreading by Coffee strain effects.[84] Recent research has shown that applying external force and using an appropriate template could lead to well-aligned and -orientated OSC crystals or chains for high mo-

bility. Diao et al. reported a new solution-coating method using a micropillar-patterned printing blade to guide ink recirculation and direct TIPS-pentacene crystal growth.[11] Under the analog principle, Yuan et al. proposed an off-center spin-coating method to align C_8-BTBT crystal in a polystyrene matrix and observed impressive mobility up to 43 cm^2/Vs.[13] Tseng et al. used a nano-grooved SiO_2 substrate for semiconducting poly [4-(4,4-dihexadecy]-4H-cyclopenta[1,2-b:5,4-b′]dithiophen-2-yl)-*alt*-[1,2,5]thiadiazol o [3,4-c] pyridine] (PCDTPT) deposition. This template facilitated the alignment of the polymer chain over a long range and alleviated the necessity of high molecular weight. A high mobility of 23.7 cm^2/Vs was obtained in these polymer OFETs.[12] Based on a nano-grooved substrate, Luo et al. developed a sandwich casting method between two silicon substrates treated by different SAMs. The polymer chains were well aligned upon capillary action, leading to a high mobility of 36.3 cm^2/Vs in PCDTPT (M_n=140 kDa) OFETs, and the mobilities showed strong anisotropic features depending on polymer orientation.[85]

OSC film thickness (t_{SC}) also affects device performance. At very small thicknesses (e.g., t_{SC} <5 nm), the deposited OSC cannot form a continuous film, and the charge transport is limited by percolation. At very large thicknesses (e.g., t_{SC} >100 nm), the bulk traps and amplified roughness of the OSC film as well as the increasing contact resistance may play predominantly detrimental roles. An optimal t_{SC} needs to be determined before massive fabrication. Previous studies have shown that in single-crystal and polycrystalline OFETs, the OSC growth dynamics in a vacuum chamber greatly evolved with deposition.[86, 87] For solution-processed OSC films, the t_{SC} dependences are distinct. Verilhac et al. observed that in staggered (TG/BC) OFETs with spin-coated amorphous OSCs (*p*-type: polytriarylamine derivative (PTAA) and *n*-type: poly[9,9-dioctylfluorene-co-*N*-(4-butylphenyl)-diphenylamine] (TFB)), thickening t_{SC} from 30 nm to 1 μm decreased mobility somewhat but significantly changed V_T and *SS*.[88] In thin-t_{SC} regimes (t_{SC} less than S/D electrode thickness), BC electrodes caused poor OSC morphology near contacts that extended to the channel and degraded *SS*. In thick-t_{SC} regimes, the high contact resistance due to the long distance for vertical access transport and the bulk traps in the amorphous OSC film started to limit the overall transport so that both V_T and *SS* were raised. The optimal t_{SC} was found to be around 200 nm. Different results were reported by Boudinet et al. for OFETs of the same structure but with high-quality polycrystalline OSCs (*p*-type: TIPS-pentacene and *n*-type: Polyera ActivInk™ N1400).[89] As t_{SC} increased from 35 nm (or 45 nm) to 400 nm (or 700 nm), the mobility dropped by two orders of magnitude while V_T remained nearly constant. This was attributed to the poor morphology and defect generation of thick polycrystalline OSC films rather than R_C even if it was also increased by more than one decade. Therefore, the thinnest OSC film was found to be optimal.

3.5 Gate dielectric

The gate dielectric serves as a barrier to the opposite charges on the gate and in the channel coupled by the capacitance C_i. This layer should be a good insulator contain-

ing a small number of mobile and localized charges and traps. A thin dielectric layer (i.e., greater C_i) is always desired to reduce V_T and *SS*, yet this does not go hand in hand with increased gate leakage. It is challenging to obtain a TG dielectric deposited atop the OSC upper surface, which would be rather rough for crystalline OSCs. Thick and conformal dielectrics are required to ensure low leakage. BG dielectrics can be relatively thin (or with an additional barrier),[90] but they should be smooth and with preferential surface energy for OSC deposition.

At the beginning of OFET research, SiO_2 and other inorganic oxides (e.g., Al_2O_3, TiO_2) were widely used. SiO_2 is known for its hydroxyl groups that behave as electron traps, significantly suppressing *n*-type device properties. In addition, they are not suitable for printing. Polymers are the best choices for printed flexible dielectrics because of their native insulating feature and similar mechanical properties to OSCs (i.e., their interface is less sensitive to strain). Until now, a large number of polymer dielectrics have been printed, including polyimide (PI), polyvinylphenol (PVP),[29, 90, 91] photoresists, poly (methyl methacrylate) (PMMA), poly(vinyl alcohol) (PVA), and Cytop.

SAM is an attractive candidate for printed dielectrics. It is unique due to its very small thickness, as thin as one molecular monolayer. Meanwhile, SAM can withstand a high electric field up to 16 MV/cm, comparable and even superior to thermally grown SiO_2 of similar thickness.[92, 93] Therefore, OFETs incorporating SAM dielectrics are able to operate at very low voltages (e.g., 2 V).[94]

Besides single-layer dielectrics, multi-layer systems have attracted great attention due to their capability to tune physical and chemical characteristics. The best-known example is octadecyltrichlorosilane (OTS) on SiO_2 where the OTS treatment greatly improved the performance of pentacene OFETs in terms of μ, *SS*, I_{on}/I_{off}, and uniformity and stability.[95] Polymers (e.g., PAMS-poly(α-methylstyrene)) could play similar roles as OTS on SiO_2.[96] Multi-composite or blended dielectrics have been investigated to increase the dielectric constant (ε). Most polymer dielectrics have low ε (e.g., ε=2.1 for Cytop and ε=2.6 for PMMA), which increases operating voltage. Adding high-ε inorganic components to the polymer matrix (e.g., adding TiO_2 to PVP increases ε from 3.5 to 5.4) and blending low-ε and high-ε polymers (e.g., PMMA and poly(vinylidenefluoride-trifluoroethylene) (P(VDF-TrFE)) are possible strategies.[97, 98]

Another extreme case is electrolytes. Compared to other dielectrics, electrolytes deliver huge C_i up to 1–10 μF/cm^2, which enables OFETs to operate at very low voltages down to 1 V with unprecedentedly high mobility and ambipolar properties due to the very high charge density. Moreover, the extremely high gate field (e.g., 10^7 V/cm) is helpful to eliminate the short-channel effects arising from the increasing lateral field that becomes comparable to the gate field in small-*L* OFETs (e.g., L<1 μm).[99] Despite those advantages, there is a concern regarding electrolyte-gate OFETs: slow dynamic response. This causes large hysteresis during static *I-V* characterizations and slows down the switching speed. Frisbie et al. have achieved encouraging results in this area. They applied various ion gel electrolytes with high ionic conductivity to improve polarization response time. The ion gel-gated poly (3-hexylthiophene-2,5-diyl) (P3HT) OFETs fabricated by aerosol jet printing exhibited both high mobility (1.8 cm^2/Vs) and fast switching speed (1–10 kHz).[100] See the

recent review paper for more detail on this topic.[101]

3.6 Gate electrode

The gate modulates the charge concentration (conductivity) in the OSC film via the electric field, which is the basic operating principle of field-effect transistors. For modern Si MOSFETs, the poly-Si gate has been used for years because of its identical chemical composition and band structure to active Si in the channel as well as its high melting point. It is useful to adjust V_T and enable self-alignment during S/D processing. Along with relentless downscaling, the depletion of the poly-Si gate became a serious issue, and metal gates started to take over. For OFETs, heavily doped Si or metal gates are widely utilized, yet little attention has been paid to their roles in *WF* and conductivity. Chung et al. examined Ti (*WF*=4.89 eV) and Pt (*WF*=5.39 eV) gates for *p*-type pentacene and *n*-type C_{60} OFETs and found that a difference in *WF* of 0.5 eV shifted V_T exactly 0.5 V.[32] This V_T regulation by varying gate *WF* with accessible metals is small for printed OFETs typically operating at high voltages (e.g., 20 V), whereas it is significant for polyelectrolyte OFETs. Kergoat et al. systematically investigated the effect of gate *WF* on electrolyte-gated P3HT OFETs.[31] It turned out that applying Au and Ca gates shifted V_T up to 0.9 V, leading to depletion-mode and enhancement-mode operations. Through tests of various metals with diverse *WF*s, a linear correlation between V_T and the flat-band voltage was observed (cf. Fig. 8).

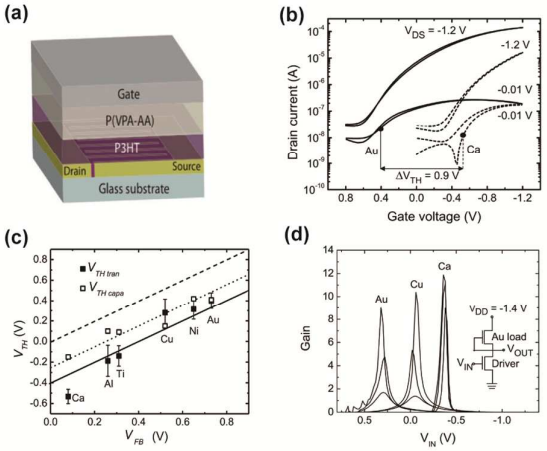

Fig. 8 (a) Schematic representation of the electrolyte-gated OFET with various gate metals. (b) Transfer characteristics in the linear regime (V_{DS}= −0.01 V) and at saturation (V_{DS}= −1.2 V) for electrolyte-gated OFETs with Au (full line) and Ca (dashed line) as gate metal. (c) Variation of the threshold voltage extracted from the capacitance $V_{TH\ capa}$ (empty squares) and transistor measurements $V_{TH\ tran}$ (full black squares) as a function of the flat-band potential. The dotted and full lines are linear fits with a slope of 1 to the data corresponding to capacitance and transistor measurements, respectively. The dashed line represents the ideal case where V_{TH}=V_{FB}. (d) Modification of the signal gain of an inverter with Au as the gate metal for the load and Au, Cu, or Ca as the gate metal for the driver. Reproduced with permission.[31] Copyright 2012, National Academy of Science.

The conductivity of the gate electrode affects the performance of OFETs and organic ICs as well. Han et al. reported that the conductivity was quite low for a few nm-thick Au film thermally deposited atop a dielectric. The gate conductivity increased quickly with gate thickness and finally saturated at a thickness of around 30 nm.[102] The stage delay in a ring oscillator was found to decline from 10^{-3} s to 10^{-5} s as Au gate thickness increased from 9.6 nm to 30 nm. Very recently, Benwadih et al.

developed low-temperature processed graphene ink for gate electrodes.[103] They observed that applying an adhesion component in silver ink decreased the contacting area of Ag flakes with a dielectric (Cytop) and equivalently decreased C_i, while the sheet stacking graphene made much better contact with Cytop. Both *p*-type and *n*-type OFETs showed better performance, and the operating frequency of a seven-stage ring oscillator was increased from 1.2 kHz to 2.1 kHz at a supply voltage of 40 V.

3.7 Interconnects

The fabrication of the preceding device components in a semiconductor fab is called front-end-of-line (FEOL). The fabrication of the subsequent compositions (including interconnects and passivation and encapsulation layers as well as bonding and packing (not discussed here)) is called back-end-of-line (BEOL). Here, we discuss two BEOL components: interconnects and passivation (or encapsulation) layers.

Interconnects are similar to S/D electrodes, but charge injection is no longer an important consideration. Thus, interconnecting materials could be different from those for contacts. High conductivity is desirable for vias and lines. Thick (and/or wide) lines should be used for the power supply, and relatively thinner (and/or narrower) lines are fabricated for signal transmission. By using conductive polymers like PEDOT:PSS or metal NP inks, vias (and via holes) and interconnecting lines can be printed as in S/D electrode printing. When integration becomes large scale, low-*k* dielectrics for multi-layer interconnection should be implemented to eliminate cross talk and reduce parasitic capacitance, which is vital to high-performance ICs.

3.8 Passivation and encapsulation

Passivation and encapsulation are regular steps in manufacturing Si MOSFETs, but they are not always applied to OFETs. The main reason is the early recognition of charge transport in the nominal channel. More and more research studies have shown that high stability and uniformity necessitate proper passivation, because it protects the underlying OSC film from chemical (e.g., moisture and oxygen) and physical attacks.

Various materials have been employed in passivation, including sputtered SiN and polymers (e.g., PVA, polyvinylphenol, PI, Cytop, photo resist). The passivated OFETs exhibited dramatically improved stability in terms of mobility degradation and threshold voltage variation under bias stressing and exposure to air.[105, 106] Recently, Lee et al. reported a uniform and stable inkjet-printed OFET array in which a 1μm-thick photo-acrylate passivation layer improved device stability.[104] After 17 days of storage in air, the mobility of the unpassivated OFETs declined from 0.40 cm^2/Vs to 0.05 cm^2/Vs, whereas the passivated ones showed only a small decrease to 0.23 cm^2/Vs, which was even better than those stored in an N_2 box (see Fig. 9). More surprisingly, the passivated OFETs exhibited great stability under both positive and negative bias stresses with only a tiny V_T shift of 1 V in contrast to the large shifts (−5 V and +13 V for negative and positive V_G bias stress, respectively) for unpassivated OFETs. Moreover, passivation protected the devices during further integration. Therefore, the creation of a full color display based on a printed OFET backplane was

successful.

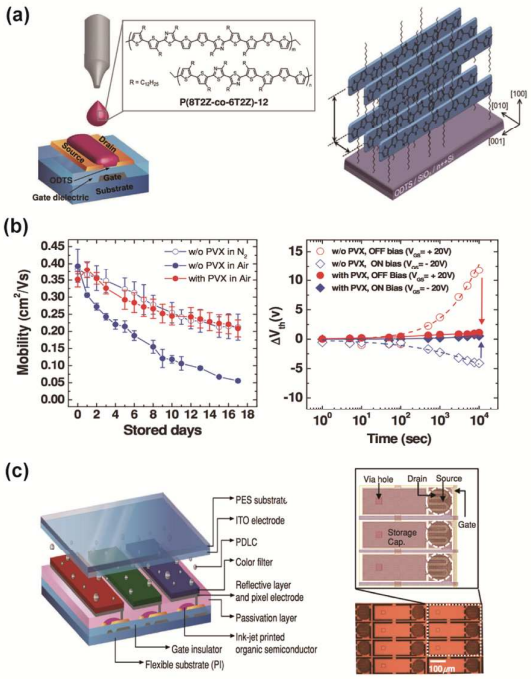

Fig. 9 (a) Left: Inkjet printing scheme of OFET and molecular design for polymer semiconductor P(8T2Z-co-6T2Z)-12 with charge-transfer moieties used in this system. Right: Schematic illustration of molecular ordering in inkjet-printed P(8T2Z-co-6T2Z)-12 polymer semiconductor film. (b) Left: Mobility vs. elapsed time plots of passivated and non-passivated OFETs that were kept either in air or in N_2 ambient. Right: ΔV_{Th} as a function of time under ON bias stress (V_G=–20V, V_{DS}=−10 V) and OFF bias stress (V_G=20 V, V_{DS}=−10 V). Scattered points denote the experimental values, while the solid lines were fitted according to the stretched exponential equations. (c) Left: Schematic three-dimensional view of one PDLC display pixel including OFET drivers for red, green, and blue color display. Right: Pixel array photos taken from optical microscopy, along with detailed scheme of one pixel that contains storage capacitors and three OFETs with interdigitated channels. Reproduced with permission.[104] Copyright 2013, Wiley VCH.

4. Printing technologies

Solution-based processing is naturally suited for low-cost electronics over large-area and flexible substrates. In particular, roll-to-roll printing is appropriate for large-size, low-cost, and large-volume production, which is appealing for applications such as solar cells and displays.[107] The produced films can be directly patterned without using a mask, just like in inkjet printing. It is known that the majority of manufacturing costs for silicon-based devices and ICs are spent on photolithography (multiple steps with relevant photo masks). Direct printing could drastically simplify the OFET fabrication process and greatly reduce the overall cost.

In the following section, we briefly review the printing techniques that have been applied to OFET fabrication. There are two kinds of printing methods according to printing characteristics.[9] One is direct-writing printing where patterning is made by ink ejection without contact, including inkjet printing, spray printing, and screen printing. Another is transfer printing where the patterned targeting material is transferred from a donor to an acceptor substrate, including gravure printing, offset printing, flexography printing, and laser printing. For more detail on printing technologies, see the corresponding review papers.[7, 9, 68, 108]

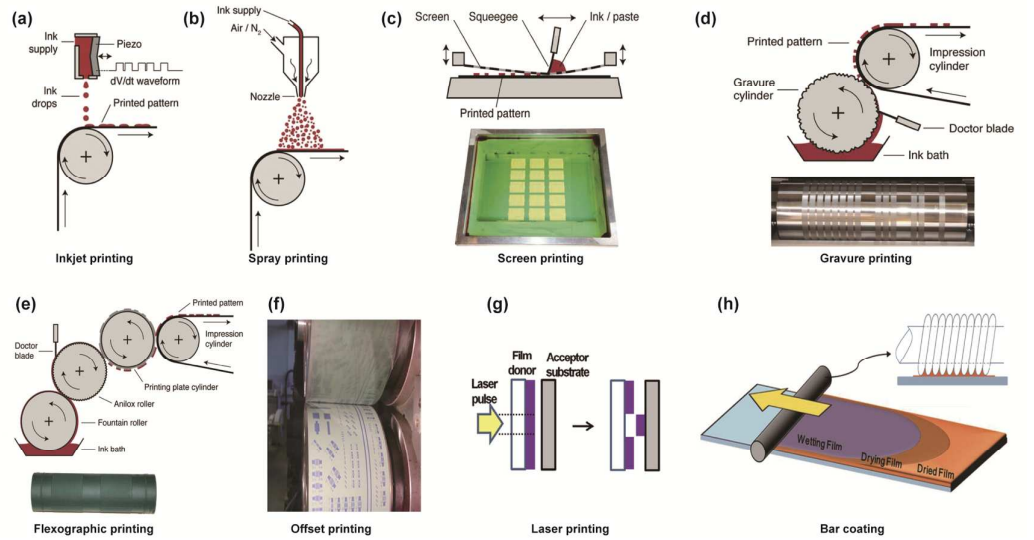

Fig. 10 Schematic of printing technology. (a–e) Reproduced with permission.[108] Copyright 2013, Wiley VCH. (f) Reproduced with permission.[109] Copyright 2005, AIP. (g) Reproduced with permission.[9] Copyright 2013, ACS. (h) Reproduced with permission.[110] Copyright 2013, Wiley VCH.

4.1 Inkjet printing

An examination of the recent literature reveals that inkjet printing is a technique of increasing interest for OFET fabrication. It provides high resolution and ease of formulating inkjet printable inks for a broad spectrum of functional materials. A commonly used inkjet technology is drop-on-demand (DOD) printing, as shown in Fig. 10 (a).

Inkjet printing has been applied to direct-writing conductive polymers, such as PEDOT:PSS and metal NP ink for S/D electrodes and interconnects. The feature size of inkjet-printed components is typically 20–100 μm with droplet volumes of 1–30 picoliter (pL). By using polymer bank[111] and dewetting properties,[112] the patterning size of PEDOT:PSS was shrunk to 5 μm and 500 nm. Meanwhile, the feature size of inkjet-printed Ag NP at a low sintering temperature of 130°C was reduced to 2 μm by employing different precursors.[113] Recently, Teng et al. developed a nanoimprint-assisted inkjet printing method to shrink L down to 750 nm, where nanoimprint was utilized to define submicron patterns on a resist by which Ag S/D electrodes were made by inkjet printing.[114] Cheng et al. greatly downscaled *n*-type OFETs to L=200 nm by inkjet printing Ag *source* electrodes within the gap of photolithographically patterned Au *drain* electrodes,[115] where the small L was obtained upon dewetting Ag ink by a surface modification of predefined Au contacts. By using 50 nm-thick cross-linked Cytop TG dielectric, the N1400 OFETs operated at 5 V with good bias stress stability. Lee et al. optimized the conditions of inkjet printing Ag gate and S/D electrodes for high stability and reproducibility.[116] They found that 30°C (80°C) and 30 μm (80 μm) were the optimal substrate temperature and spacing for gate (HMDS-treated S/D) electrode printing, respectively.

Active OSC films could also be inkjet patterned by either direct printing of OSC inks or patterning of SAMs with different surface energies to induce selective dewetting of OSC material. A major challenge is to control the uneven surface mor-

phology caused by the Coffee strain effect, which leads to poor performance and uniformity. Solvents around the boundary of a deposited droplet on a non-wettable substrate dry faster than those in the center, and the different drying speed produces an uneven film; this is called the Coffee strain effect. Some approaches have been proposed to solve this issue. One is to heat the substrate at a moderate temperature in order to obtain an equal evaporation rate over the entire surface of the droplet and thus control the OSC's microcrystallinity. Lee et al. investigated the droplet morphology of inkjet-printed TIPS-pentacene films.[117] Their results showed that modest heating of the substrate at 46°C and a slight shift of dropping location from the channel center led to a large grain size and well-aligned crystals parallel to the S-D direction, and a mobility of 0.44 cm^2/Vs was obtained. Baeg et al. observed that heating a Si/SiO_2 substrate at 60°C was optimal for the inkjet printing of *n*-type *N*-*N*′-bis(n-octyl)-(1,7&1,6)-dicyanoperylene-3,4:9,10-bis(dicarboximide)(PDI8-CN_2), resulting in great performance (μ_{fe}~0.06 cm^2/Vs, I_{on}/I_{off}~10^6) and uniformity (<10%).[118] The second approach involves using a co-solvent that has different surface tensions and that could create Marangoni flow within the printed droplet. This technique has been successfully employed by Lim and coworkers in inkjet-printed TIPS-pentacene films.[84] Recently, Grimaldi et al. found that a solvent mixture composed of o-dichlorobenzene and chloroform with a ratio of 3:2 was optimal for inkjet printing *n*-type PDI8-CN_2 OSC film, and they noted that the relevant substrate temperature and drop overlapping degree should be accordingly optimized for better reproducibility and OSC microstructure.[119] To overcome Coffee strain effects and improve the crystallinity of inkjet-printed OSCs, Kim et al. also proposed a pattern-induced confined structure (PICS) by which the grain size and crystal form of the inkjet-printed TIPS-pentacene were adjusted by PICSs of various sizes.[120] A method of growing inkjet-printed single-crystal TIPS-pentacene was reported by Kim and co-workers,[121] where a controllable single crystal along the S-D direction was achieved by combing local SAM treatment of the SiO_2 substrate and solvent evaporation optimization.

A process defining via-hole interconnections by inkjet printing of solvent for local etching/dissolution of continuous dielectric and OSC films has been reported as well.[122] Recently, Kwak et al. reported a similar technique to form microwells for inkjet-printed TIPS-pentacene and to improve the OSC's self-organization.[123] See the specific review paper for more details on inkjet printing.[10]

4.2 Spray printing

Spray printing is a cheap and widely used technique for depositing various inks on a variety of substrates with different curvatures (cf. Fig. 10 (b)). In combination with shadow mask or DOD functionality, this technique can be used to pattern OSC and even S/D electrodes. Jang et al. demonstrated all-organic pentacene OFETs using spray-printed PEDOT:PSS S/D electrodes (L=70 μm) where a comparable mobility to those fabricated with Au electrodes was observed.[124] Chan et al. attempted OFET fabrication using spray-printed P3HT.[125] Despite the rather inhomogeneous P3HT films processed by spray printing, they still observed a high mobility of 0.1 cm^2/Vs compa-

rable to that using spin coating. Khim et al. recently reported high-performance *p*-type polymer (P3HT, P2100) and *n*-type small-molecule (N1450) OFETs using spray printing.[126] By controlling the droplet size, nozzle-to-substrate distance, and solvent drying speed during the printing process, highly crystalline OSC films were obtained, and the resultant OFETs showed high mobility comparable to and even higher than that of their spin-coated and inkjet-printed counterparts. Meanwhile, those OFETs displayed high uniformity from device to device, demonstrating the great stability of spray printing.

4.3 Screen printing

In this printing method, ink is pushed through a screen comprising a fine mesh composed of plastic or metal. Patterns are defined by filling the openings of the mesh with a stencil. The screen is coated with the ink using a squeegee, and the mesh is brought into contact with the substrate, thereby pressing the ink through the opening of the screen to define the desired pattern. Hence, more viscous ink is needed for this method compared with inkjet printing. The patterning resolution depends on the size of the openings and the spacing between openings (cf. Fig. 10 (c)). Screen printing has been used to pattern top-level interconnects and electrodes, but it has also been employed to deposit gate dielectric and encapsulation layers. The first printed OFET was made using screen-printed graphite S/D (L=200 μm, 10 μm thick) and gate electrodes.[127] Screen printing was later applied to shrink L=100 μm in BG OFETs[128] and to pattern the gate electrodes and interconnects in TG OFETs.[107] After that, Noguchi et al. demonstrated high-performance pentacene OFETs using a screen-printed shadow mask with a mobility of 0.4 cm^2/Vs and an I_{on}/I_{off} of over 10^5.[129] Recently, Lim et al. fabricated short-L pentacene OFETs (L=30 μm) using screen-printed Ag S/D electrodes and obtained a mobility of 7×10^{-2} cm^2/Vs.[130]

4.4 Gravure printing

Gravure printing is an intaglio printing technique. It employs a metal cylinder comprising engraved or etched pattern cells that are filled with ink provided by an ink fountain where a doctor blade is used to scrape off the excess ink from the cylinder surface. By making contact with the rotating cylinder, the patterns are transferred onto the feeding flexible substrate (cf. Fig. 10 (d)). Gravure printing is a high-throughput technique permitting the production of small features with small thicknesses.

Vornbrock et al. optimized the gravure printing of the OSC film of poly(2,5-bis (3-alkylthiophen-2-yl) thieno [3,2-b]thiophene) (PBTTT). PBTTT OFETs were fabricated with a short L=15 μm defined by inkjet-printed silver S/D contacts and demonstrated a mobility of 0.06 cm^2/Vs, leading to a high operating frequency of 18 kHz.[131] To further improve the operating speed, a very short L<15 μm was achieved by using femtoliter gravure printing, and the mobility in PBTTT OFETs was increased to 0.1 cm^2/Vs.[132] Voiget et al. studied OFETs with sequential gravure printing of P3HT, two TG dielectrics (PMMA and PHEMA), and a TG electrode based on Ag ink. A record mobility of 0.04 cm^2/Vs was observed for such printed P3HT OFETs.[133] High-performance OFETs with gravure-printed TIPS-pentacene demonstrated high

mobility up to 6 cm^2/Vs with great reliability (no operation failure at ultra-low temperatures down to 10 K).[28] A transport modeling revealed that the band-like transport in delocalized states greatly contributed to the overall transport so that higher mobility with more clearly band-like transport is expected for printed OFETs. Recently, Hassinen et al. reported low-voltage operation for polymer OFETs using a gravure-printed OSC (Lisicon SP0300) and dielectric (Lisicon D320).[134] By significantly reducing the dielectric thickness to 200 nm, the inverter based on those OFETs can operate at a low voltage of only 5 V.

4.5 Flexography

The principle of flexography is similar to that of common letterpress techniques, but the printing plate is flexible in flexography, as seen in Fig. 10 (e). This method can print material to nearly all substrates, such as plastic, metal, and paper. Flexography was utilized for OFET fabrication to process S/D electrodes with a small gap (i.e., L) of 16 μm.[135] The fabricated TIPS-pentacene OFETs incorporating PVP dielectric showed a mobility of 0.1 cm^2/Vs and an I_{on}/I_{off} of about 10^5. By combining the two mass printing techniques of flexography and gravure printing, a very short L=10 μm was achieved between PEDOT:PSS S/D electrodes.[136] Flexography has also been used to print OSC films for high-performance *n*-type OFETs.[137]

4.6 Offset printing

At present, offset printing is a widely used commercial method because of its high throughput. In this technique, the ink is brought into contact with a printing plate containing oleophilic/ink-accepting and hydrophilic/ink-repellent surface areas. The ink is selectively transferred onto the oleophilic regions of the printing plate and from there onto the substrate via an intermediate blanket cylinder (cf. Fig. 10 (f)). Offset printing was first applied to OFET fabrication for S/D electrodes of PEDOT:PSS, where TG PTAA OFETs with L=50 μm exhibited a mobility of 3×10^{-3} cm^2/Vs and an I_{on}/I_{off} of 10^3.[68] Next, Choi et al. developed a modified offset printing method for amorphous oxide transistors where the electrode feature size was decreased to 10 μm in width and 6 μm in spacing.[138]

4.7 Laser printing

Recently, laser printing, sometimes called laser-induced forward transfer (LIFT), has been actively applied to OFET fabrication. In this technique, a pulsed laser beam irradiates the donor film (e.g., a glass substrate covered with metal film) where the generated heat gasifies the glass close to the glass/metal interface, leaves the metal film from the substrate, and transfers to the acceptor substrate by pressure (see Fig. 10 (g)). This technique can deposit very different materials, including metal, powder, liquid, OSC etc. For instance, semiconducting copper phthalocyanine (CuPc) and P3HT as well as Ag NP-based S/D electrodes can all be fabricated by laser printing.[139, 140] However, the high energy of the laser may damage the OSC film, and appropriate measures must be taken. Rapp et al. introduced a sacrificial layer of UV-sensitive aryltriazene polymer to protect the laser-printed distyryl-quaterthiophene (DS4T) from

direct irradiation.[141] The same group also found that the stable new oligomer of bis(2-phenylethynyl) end-substituted terthiophene (diPhAc-3T) was not sensitive to laser damage and that a protecting layer was therefore not needed.[142] Another group observed that the thermal energy of laser irradiation might improve the quality of the OSC microstructure and OSC/dielectric interface.[140]

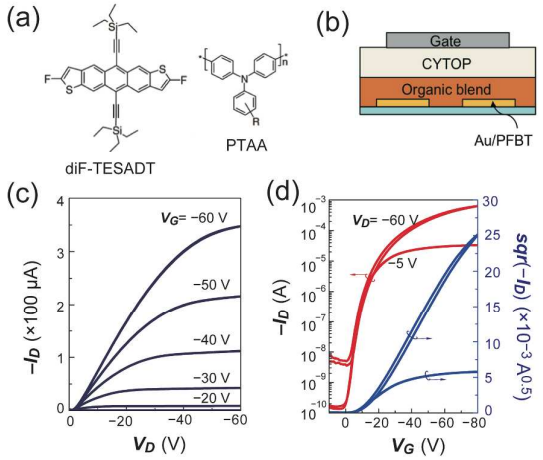

Fig. 11 (a) Molecular structures of diF-TESADT and PTAA. (b) TG/BC device structure. Typical output (c) and transfer (d) characteristics of diF-TESADT:PTAA-based OFETs.

4.8 Bar-coating

Wire-bar-coating is an effective technique capable of depositing very uniform OSC and dielectric layers onto rigid and flexible substrates with high material utilization. It is rather compatible with promising roll-to-roll manufacturing for large-area and low-cost electronics. Bar-coating includes three major steps: (1) deposition of an organic solution just ahead of the coating bar, (2) wet coating the organic solution onto the substrate by horizontally moving the bar along a fixed substrate, and (3) drying the wet film from the edge to the center. The gradual solvent evaporation from the wetted film proceeds without the external centrifugal force that is observed in spin-coating, and it is free from the undesirable fluidic phenomena (e.g., Coffee stain effects) that we often encounter in drop-casting or inkjet printing.[110] This is because a polymer solution is inserted into the spaces between the metal wires so that the thickness of the bar-coated films can be controlled by the wire diameter and the bar moving speed (see Fig. 10 (h)). Khim et al. demonstrated the precisely controlled bar-coated films of conjugated polymer OSCs and polymer dielectrics from 20 nm to 500 nm and applied those films to high-performance OFET arrays and complementary ICs.[110] Highly crystalline conjugated polymer and very smooth dielectric layers were produced by consecutive bar-coating on a 4-inch glass or plastic substrate. The bar-coated TG OFETs with DPPT-TT comprising diketopyrrolopyrrole (DPP), thieno[3,2-b]thiophene (TT), and two thiophene moieties in the repeat unit exhibited a mobility of up to 2.83 cm^2/Vs and excellent device-to-device uniformity with a small standard deviation of 5%–6%. Based on the bar-coated OFETs, high-performance ambipolar inverters (voltage gain >40) and ring oscillators (oscillation frequency of ~25 kHz) were also developed.

Blending small-molecule OSCs with polymers is an attractive approach to enhancing the crystallization of small-molecule OSCs, as the polymer matrix improves the forming properties of the blended solution.[143–146] Here, we demonstrate high-performance bar-coated OFETs with a blend of 2,8-Difluoro-5,11-bis(triethylsilylethynyl) anthradithiophene (diF-TESADT) and PTAA. Figs. 11 (a) and (b) illustrate the chemical structure of diF-TESADT as a small molecule and PTAA as a binding polymer and the schematic diagram of the TG/BC device structure. A solution containing diF-TESADT and PTAA with 1:1 by weight at 4 wt% concentration of solids in tetralin was prepared. Before OSC coating, the surface of patterned Au S/D electrodes (L=20 μm, W=1.0 mm) was modified by immersing in pentafluorobenzene thiol (PFBT) solution to improve charge injection.[145] The OSC solution was then dropped onto one edge of the patterned substrate. Next, a meniscus formed on the solution as the bar was lowered and horizontally transported at 10 mm/s over the substrate. The OSC film was thermally baked at 60^{o}C for 20 min, and the Cytop dielectric layer was formed on top of the active layer. OFET fabrication was completed by thermal evaporation of Al to produce the gate electrode. Figs. 11(c–d) show the output and transfer characteristics of bar-coated diF-TESADT:PTAA OFETs. The good linearity at small values of V_D in the output curves indicates nearly ohmic contacts. We observed a peak mobility of 2.55 cm^2/Vs, which is one of the highest mobilities in the diF-TESADT:PTAA blend system.[143, 144, 146] Additionally we obtained an averaged mobility of 2.33 cm^2/Vs over 20 OFETs with a standard deviation of 0.18 cm^2/Vs and a central V_T=−10.4 V with a small deviation of 0.91 V, indicative of great uniformity of bar-coated OFETs.

5. Printable OSCs

High-mobility printable OSCs are vital to the development of high-performance printed OFETs and organic ICs. In the past few years, several encouraging advances in new OSC synthesis and fabrication technology were reported. For instance, the carrier mobility has reached 100 cm^2/Vs for small-molecule OSCs of C_8-BTBT[13] and around 30 cm^2/Vs for polymeric OSCs of PCDTPT.[12] Such high mobilities could enable expected applications in such areas as wireless communication and data processing. As numerous papers have extensively reviewed the recent advances in OSCs, including printable OSCs,[6–8, 147, 148] here, we briefly revisit some OSCs used for high-performance printed OFETs.

The highest mobility is generally delivered by small-molecule OSCs, among which TIPS-pentacene and C_8-BTBT are the most studied. TIPS-pentacene was first developed by Anthony et al., who substituted the triisopropyl-silylethynyl (TIPS) group on the central 6- and 13-positions of the core of classical pentacene.[149] Compared to pentacene, the reengineered TIPS-pentacene is quite soluble in usual organic solvents, and it exhibits a high crystalline degree after a solution-based deposition. Therefore, a high mobility of over 10 cm^2/Vs[11] and band-like transport properties[15] have been reported for solution-processed or printed TIPS-pentacene OFETs. C_8-BTBT and its similar derivatives (C_n-BTBT) were invented by Takimiya et al.,[150] yet they made extraordinary figure in developing high-mobility printed OFETs from 2008.[26, 151] A dou-

ble-shot inkjet printing technique in combination with local crystallization enabled by droplet confining within a specially designed region led to average and maximum mobilities of 16.4 cm^2/Vs and 31.3 cm^2/Vs, respectively, in C_8-BTBT OFETs.[151] Band-like transport in solution-processed C_8-BTBT OFETs was also reported,[26] and recently, the mobility record was refreshed by Prof. Bao's group at Stanford University, and the maximum mobility was boosted up to 43 cm^2/Vs (and 10^2 cm^2/Vs in supporting information) using an off-center spin-coating method.[13] These results indicate that a high mobility of over 100 cm^2/Vs is possible for printed OFETs. Moreover, bis(tetracene) derivatives recently demonstrated great potential for printable OSCs, providing high mobility (6.1 cm^2/Vs), high solubility, and great air stability (over 4 months without clear deterioration in mobility or On/Off ratio).[152]

Conjugated polymers are well suited for printed OFETs owing to the ease of solution preparation and their amorphous properties. They have typically provided relatively lower mobilities than the small-molecule OSCs, yet they recently made considerable progress.[153] High mobilities have been found in some semi-crystalline polymers like P3HT, poly (3,3'-dialkyl-quaterthiophene) (PQT), and PBTTT. However, more attention needs to be paid to the control of crystal size, alignment, and orientation. Recently, donor-acceptor (D-A) copolymers attracted great attention for their exceptionally high mobility, small band gap, high stability, and low sensitivity to film morphology as well as ambipolar charge-transport properties. They are copolymers with alternating electron-deficient and electron-rich units along the backbone. *n*-type naphthalenediimide and bithiophene (PNDI2OD-T2)[137] and *p*-type cyclopentadithiophene and benzothiadiazole (CDTBTZ)[154] copolymers are two examples that exhibited high electron- and hole-mobility up to 0.8 cm^2/Vs and 5.5 cm^2/Vs, respectively. For the latter, a high mobility of over 20 cm^2/Vs was achieved using polymer self-assembly discussed above, and further mobility improvement was also demonstrated upon electronic contact optimization.[85] The copolymers based on the electron-deficient unit of DPP also received great interest, and a high mobility of 10 cm^2/Vs was reported.[155] In addition to DPP, copolymers based on the unit of thiophene-flanked benzodipyrrolidone (BPT) have also received attention.[156]

6. Organic ICs

After the fabrication of individual OFETs, they are connected to build a circuit or an IC. Next, we shall discuss organic ICs and their performance development.

6.1 CMOS inverter

Complementary MOS (CMOS) is a primary architecture for present microelectronics, as it permits a broad input noise margin, large output spanning, and strong driving capability with small power consumption. Now, the CMOS inverter is a standard vehicle to test device performance and verify the feasibility of composing complex ICs. An organic CMOS inverter consists of an *n*-type OFET (*n*-FET) and a *p*-type OFET (*p*-FET), as seen in Fig. 12a. It charges and discharges the load capacitor *C* to either the supply voltage (V_{dd}) or zero by alternatively switching on the *p*-FET or the *n*-FET, depending on whether the input is low or high. Since one of the two OFETs is always

off and the current flowing from the power supply to the ground is very low (only static leakage), CMOS circuits dissipate very little power.

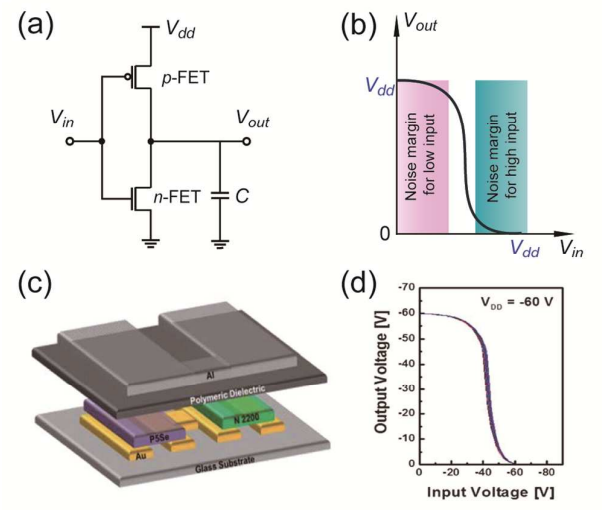

Fig. 12 (a) Schematic of an organic CMOS inverter. (b) Typical voltage transfer curve of the organic inverter. (c) Device schematics of TG/BC CMOS inverter based on P5Se/N2200 OFETs. (d) VTCs with 20 scans at V_{dd}=−60V. Reproduced with permission.[157] Copyright 2012, RSC.

Fig. 12 (b) shows the typical voltage transfer curve (VTC) of a CMOS inverter. Such a VTC offers a large noise margin to ICs. For instance, input (V_{in}) could be anywhere between 0 V and *n*-FET's V_T to perfectly output V_{out}=V_{dd} (termed pull-up). Likewise, V_{in} could be anywhere between V_{dd} plus *p*-FET's V_T to output V_{out}=0 V (pull-down). Therefore, perfect "0" and "1" outputs can be produced by somewhat imperfect inputs. This is recognized as a regenerative property of CMOS logic, enabling complex ICs to function properly while connecting noisy loads or facing strong interferences. A narrow and steep transition region in a VTC curve is desirable to maximize the noise margin (ideally of 1/2 V_{dd}) and minimize power consumption. Therefore, a high mobility and large I_{on}/I_{off} for both OFETs are essential. On the other hand, the transition is better situated at or near $V_{dd}/2$ to maximize the two noise margins, which requires the *I*-*V* characteristics of the two OFETs to be closely matched. Layout design contributes in part to this symmetry (e.g., a wider channel width *W* is allocated to *n*-FET for a higher output current due to its relatively smaller mobility compared to *p*-FET). However, the unbalance caused by the asymmetric V_T cannot be fixed in this way, and it needs to be solved by the strategies discussed above. Khim et al. reported a highly stable CMOS inverter based on inkjet-printed polymer OFETs, as seen in Figs. 12 (c–d). Compared to P3HT, poly(3,3″,3‴,3⁗-tetradodecyl-2,5′:2′,2″:5″,2‴-pentaselenophene) (P5Se) exhibited greater stability upon exposure to air and under bias stress.[157] Gili et al. employed self-aligned printing (SAP) to produce a short *L*=400 nm by using SAP inkjet printing Au S/D electrodes. The obtained CMOS inverter operated at 10 V.[158] To simplify the fabrication process and improve alignment accuracy, a one-step self-aligned imprint was developed by Li and coworkers.[159] This technique permits a one-time definition of channel geometry, S/D electrodes, OSC film, and gate electrodes using a single

imprinting stamp.

If three CMOS inverters are connected in a series, their corresponding VTCs will be delayed in sequence, as shown in Figs. 13 (a) and (b). A propagation delay (τ_d) is defined as the time required for a signal to propagate from one gate to the next, and it is the average delay of pull-up and pull-down. The τ_d of an inverter can be expressed as:

$$\tau_d \approx \frac{CV_{dd}}{4}\left(\frac{1}{I_n}+\frac{1}{I_p}\right) \tag{5}$$

where I_n is the maximum on-state current for *n*-FET taken at V_G=V_{dd}, and I_p is the maximum on-state current for *p*-FET taken at V_G=−V_{dd}. The pull-down delay is $CV_{dd}/2I_n$, and the pull-up delay is $CV_{dd}/2I_p$. Thereby, the average delay is expressed as Eq. 5. A larger current (I_n, I_p) discharges/charges the load faster, yet theoretically, this cannot be accomplished by increasing V_{dd} due to the current saturation. A more practical method would be to increase the OFET mobility and change the device configuration (e.g., larger W/L and C_i). The load C in Fig. 13 (a) represents the overall capacitance connected to the output node that comes from interconnecting lines and next gates. A better OFET and IC design as well as the application of a low-*k* dielectric for interconnects can lower C. The τ_d will be discussed below for ring oscillators.

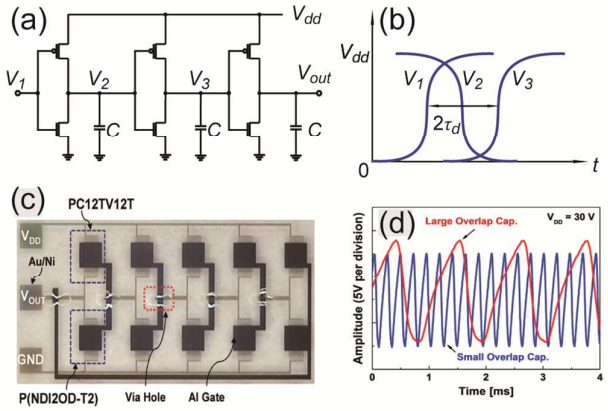

Fig. 13 (a) Schematic of three inverters connected in series and (b) their voltage transfer curves where the delay passing two inverters is illustrated. (c) Photograph of five-stage ring-oscillator consisting of CMOS inverters using *p*-type alkyl-substituted thienylene vinylene (TV) and dodecylthiophene (PC12TV12T) and *n*-type P(NDI2OD-T2) polymer OSCs. (d) Output voltage oscillation characteristics at V_{DD} = 30 V. Reproduced with permission.[160] Copyright 2013, Elsevier.

6.2 Ring oscillators

If the output terminal of the final gate in Fig. 13 (a) is connected to the input terminal of the first gate, the initial input signal will negatively feed back after passing through three inverters and reach a status to continuously work as an oscillator. This is called a ring oscillator. It may constitute any odd number of inverters, yet the overall delay $\tau_{d\text{-}total}$=$n\tau_d$ increases, with n being the stage number and the oscillating frequency f_{osc}=1/($n\tau_d$). Similar to CMOS inverters, ring oscillators have been widely used as testing vehicles. A higher f_{osc} signifies a smaller τ_d and thus greater performance. Fig. 13 (c) shows an inkjet-printed ring oscillator on a plastic substrate reported by Baeg et al. To reduce the operating voltage, they applied a blended polymer dielectric with a

7:3 wt% mixture of PMMA and high-*k* P(VDF-TrFE).[160] Through analysis of the parasitic capacitance effects caused by the overlapping between gate and S/D electrodes, they found that large overlapping significantly reduces f_{osc}, as seen in Fig. 13 (d). Smaal et al. utilized mixed SAM to tune the *WF* of Au S/D electrodes and found that OFET charge injection significantly affects τ_d.[161] Note that those are optimizations within individual OFETs, and additional attention should be paid to circuit design and fabrication for higher f_{osc}.

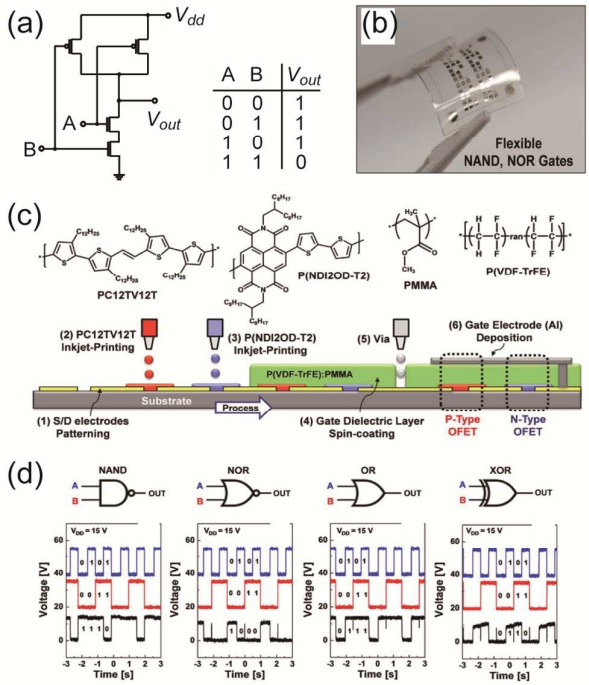

Fig. 14 (a) Schematic and truth table of NAND logic gate. (b) Photograph of flexible printed logic gates on a PEN substrate. (c) Schematic process flow for fabrication of CMOS inverters and logic gates based on TG/BC OFETs, where the upper section shows the molecular structures of applied polymers. (d) Experimental results of various printed flexible logic gates. Reproduced with permission.[162] Copyright 2013, IEEE.

6.3 Logic gates and power consumption

Once a CMOS inverter is operational, more logic gates (e.g., NOT AND (NAND), NOT OR (NOR)) can be directly achieved. According to CMOS logic architecture, there are two complementary transistor networks: the *n*-network and the *p*-network. For instance, connecting two *n*-FETs in series and linking two *p*-FETs in parallel constructs a NAND gate (see Fig. 14 (a)) where each *n*-FET in the *n*-network is paired with a *p*-FET in the *p*-network while their connecting modes are always complementary. Only if the two *n*-FETs are "ON" (with high inputs or logic "1" for A and B) at that time, the two *p*-FETs are both "OFF," and the output is pulled down to zero (i.e., logic "0"). Otherwise, if either of the *n*-FETs is turned off (input logic "0"), the paired *p*-FET is accordingly turned on so that the output is pulled up to V_{dd} (i.e., logic "1"). This is the function of NAND logic. Other logic gates can be constructed in similar ways, and subsequently, complex logic circuits can be built based on these building blocks. Recently, Baeg et al. demonstrated flexible CMOS logic gates using inkjet-printed polymer OFETs.[162] Using a blended polymer dielectric, the various printed logic gates work quite well at a supply voltage of 15 V (see Figs. 14 (b–d)).

As the integration scale increases, the power consumption becomes a serious issue. For a CMOS inverter, in every switching cycle, the charge CV_{dd} is transported from the power supply to the load C, and thus, at every second, the overall transported charge is $kCV_{dd}^2 f$, where k(<1) is the active factor denoting the activity degree of all gates in an IC and f is the clock frequency. The dynamic power is:

$$P_{\text{dynamic}} = V_{dd} \times \text{average current} = kCV_{dd}^2 f \quad (6)$$

From this formula, a smaller V_{dd} could significantly reduce P_{dynamic}. However, the same or higher output current is desired at a lower V_{dd}, so the device size (smaller L and W) needs to be reduced and/or the mobility increased. It is interesting to note that a smaller device size and consequently smaller chip size can help to reduce the parasitic capacitance C within OFETs (gate dielectric capacitance and gate/contact parasitic capacitance) and in interconnects. Device miniaturization is highly desirable to reduce P_{dynamic}. When the inverter is on standby, it consumes only static power through the leakage current as:

$$P_{\text{static}} = V_{dd} I_{off} \quad (7)$$

Lower values of I_{off} and/or V_{dd} are important for keeping P_{static} small. The total power consumption is:

$$P_{\text{total}} = P_{\text{dynamic}} + P_{\text{static}} \quad (8)$$

Smaal et al. analyzed the dissipated power of a 19-stage ring oscillator and found that P_{dynamic} is proportional to f and P_{static} is around 36.1 μW at V_{dd}=10 V.[161] In the highly stable printed CMOS inverter reported by Khim et al.,[157] they observed negligible P_{static} due to the very low I_{off}, yet P_{dynamic} increased quickly from 50 nW to 25 μW and 80 μW for V_{dd} =20 V, 60 V, and 80 V, highlighting the importance of supply voltage diminution for reducing power consumption.

6.4 Other complex ICs

Based on the previous successful developments of device engineering and fabrication technology, complex ICs can be designed and fabricated for extensive applications, as have been expected for organic electronics. Radio-frequency identification devices (RFIDs) are a promising application, and the research on OFET-based RFIDs is fast evolving and approaching commercialization. Kjellander et al. optimized a fabrication process and circuit design for this purpose.[163] They optimized inkjet printing of the blended OSC of TIPS-pentacene and PS and then applied it to one droplet deposition for four OFETs, where the circuit design was accordingly optimized to eliminate cross talk among those OFETs. In this way, the parameter variation and the circuit size were significantly reduced, enabling the proper function of 8-bit RFID transponders (see Fig. 15(a)). More appealing designs are based on CMOS technology. Schwartz et al. examined CMOS-based static and dynamic shift registers made by inkjet printing on a flexible PEN substrate.[164] Their results showed that static design fits slow functions like latching, while dynamic design is more suited for high-frequency operations, and the latter exhibited more advantages in footprint and

power utilizations (cf. Fig. 15 (b)). Jacob et al. systematically investigated the digital and analog modules of RFIDs using printed organic CMOS technology.[165] They firstly optimized fabrication processes regarding *p*-type TIPS-pentacene printing and charge injection in *n*-type Polyera ActivInk™ OFETs as well as surface treatment effects, and they obtained very stable and well-matched device characteristics that enabled a seven-stage ring oscillator operating at 1.2 kHz at V_{dd}=40 V. They then validated the basic RFID modules one by one, including a high-frequency rectifier, logic circuits like flip-flop, and comparators, as seen in Fig. 15 (c). Compared to digital circuitry, analog modules are often difficult to realize. Maiellaro et al. succeeded with high-gain operational transconductance amplifiers (OTAs) based on printed organic CMOS technology.[166] Their OTAs fabricated on plastic foil exhibited an open-loop gain of up to 50 dB and a gain-bandwidth product of 1.5 kHz, which enabled the functionality of a switched-capacitor comparator with an input frequency of up to 50 Hz (cf. Fig. 15 (d)).

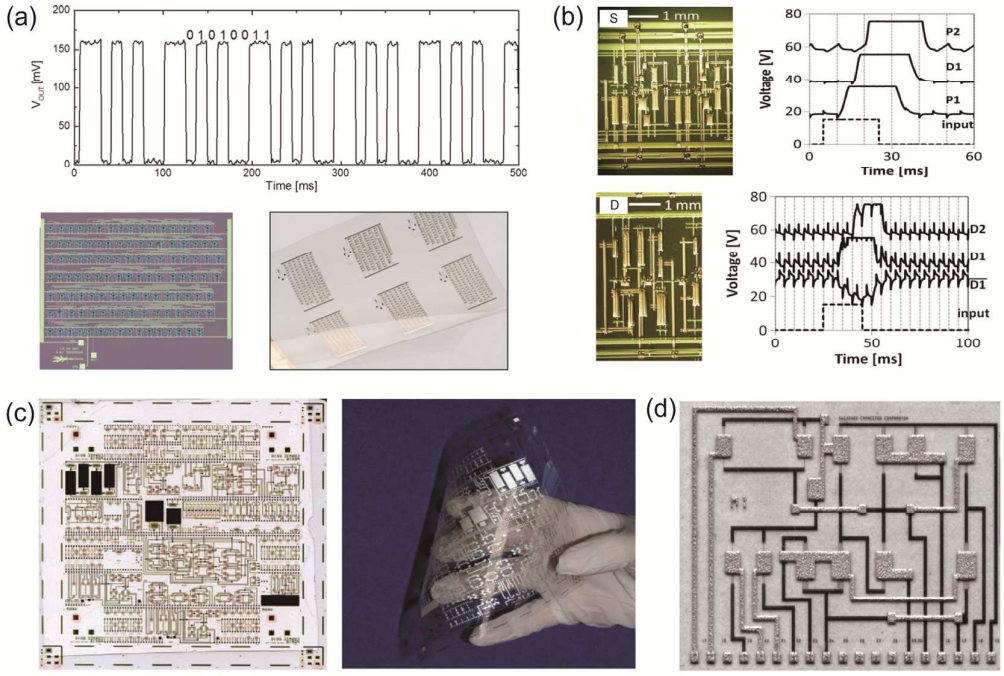

Fig. 15 (a) Upper: Output oscillations for an 8-bit RFID transponder. Lower: Left is crossed polarized micrograph of an 8-bit RFID transponder, "single-droplet" design. The blue colored circles are the inkjet-printed OSC blend. Each droplet covers one logic gate consisting of 2–4 transistors. Right is the photograph of four 8-bit RFID transponder chips, with "single-droplet" design, on plastic foil. One transponder has a footprint of 34 mm^2. Reproduced with permission.[163] Copyright 2013, Elsevier. (b) Upper: Optical micrograph of a single stage of the master–slave flip-flop shift register, and measured input (dotted line) and outputs (solid lines), with a 10-ms clock and supply voltage of 20 V. Curves are offset by 20 V for clarity. Lower: Optical micrograph of a single dynamic shift-register stage and measured input and outputs, with a 5-ms clock and supply voltage of 20 V. Reproduced with permission.[164] Copyright 2013, IEEE. (c) Pictures of an 11 cm*11 cm plastic foil with printed single devices and complementary digital and analog circuits. Reproduced with permission.[165] Copyright 2013, Elsevier. (d) Photograph of the switched capacitor comparator based on the folded-cascade transconductance amplifier. Reproduced with permission.[166] Copyright 2013, IEEE.

7. Summary

In summary, the current paper presented a prediction of the development of

high-performance OFETs and organic ICs. Based on the starting point of performance criteria, we examined all of the device components one by one and discussed the related limitations and challenges while seeking possible strategies for further performance improvements. Then, we revisited printing technologies and high-performance printable OSCs, discussing recent progress and prospective developments. Finally, we addressed the applications of printed OFETs for high-performance ICs and how device characteristics affect composed IC performance and explained the evolution of printed ICs.

From the developments discussed above, it is clear that the fast-evolving OSC and processing technology have boosted the carrier mobility up to 100 cm^2/Vs in OFETs, much higher than that of amorphous silicon-based transistors and comparable to that in poly-silicon devices. Such high mobilities should be sufficient for a wide variety of applications, even for telecommunications that demands high-frequency operation. However, the actual commercialization of printed OFETs and ICs still faces a number of challenges. An important challenge is the lack of fundamental understanding of charge-transport and operating principles of OFETs, perhaps due to the large diversity in OSCs, gate dielectrics, contact materials, device structures, and fabrication techniques. Therefore, reliable and versatile device models and fabrication methods should be developed in the future to massively manufacture high-performance OFETs and organic ICs for practical use.

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