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Metal-driven interface engineering enables multi-functionality in $SrTiO_3$ memristor devices

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The choice of metal electrode and the possible modifications to the metal/oxide interface morphology critically influence the behavior of the active switching layer in memristive devices. However, this interplay remains largely unexplored and poorly understood. Here, we systematically investigate various commercially popular metal electrodes and correlate their interfacial characteristics with $SrTiO_3$ perovskite logic memristor devices. Using high-angle annular dark-field (HAADF) STEM imaging, we reveal that thicker and chemically active interfacial layers formed by Ag, Al, and Co electrodes enhance oxygen vacancy modulation, leading to pronounced negative differential resistance (NDR) behavior, larger resistive switching windows, and higher I_{on}/I_{off} ratios. Conversely, thinner interfaces formed by Pd and Ti, as well as Cr, Cu, and Ni, exhibit weaker or absent NDR and reduced switching contrast. Atomistic simulations combining density functional theory (DFT) and quantum transport calculations show that metals with low oxide formation enthalpies promote the formation of interfacial oxide layers, enabling oxygen-vacancy redistribution that modulates electron injection into $SrTiO_3$. In contrast, sharp and symmetric interfaces suppress vacancy-driven conductance modulation, consistent with the experimentally observed absence of pronounced switching and NDR. Our findings underscore the pivotal role of interface engineering in enhancing $SrTiO_3$ memristors for multifunctional memory and neuromorphic applications.

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Introduction

Resistive switching devices, commonly known as memristors,[1] are at the forefront of emerging memory and neuromorphic computing technologies due to their non-volatility, high scalability, low power consumption, and analog switching behavior that mimics synaptic plasticity.[2–5] Among various material platforms, transition metal oxides (TMOs), such as SrTiO3, stand out for their well-understood defect chemistry, perovskite stability, and compatibility with CMOS processes.[6–10] While extensive research has been devoted to tailoring switching properties *via* stoichiometry control and doping in the oxide layer,[11–16] comparatively little attention has been paid to the influence of the metal/oxide interface, despite its critical role in charge injection, redox dynamics, and interface-driven switching mechanisms.[17–19] In particular, the choice of metal electrode profoundly impacts the interfacial chemistry, potential barrier profile, and defect dynamics at the interface, which are key factors governing device behaviors such as the RS window, endurance, variability, and electrical bistability, including negative differential resistance (NDR).[20,21] However, a systematic investigation into how different metal electrodes modulate NDR and resistive switching properties in $SrTiO_3$-based devices has been largely unexplored. This knowledge gap is especially significant, given that NDR, an important nonlinear phenomenon that enables oscillations, signal amplification, and neuron-like behavior, has been sporadically reported in oxide memristors,[22–24] with little mechanistic insight into its origin or dependence on interface structure. Moreover, neuromorphic functionalities such as short-term plasticity and adaptive learning, central to the development of brain-inspired computing, are often demonstrated in isolated device configurations without understanding how electrode materials influence their manifestation. Bridging this gap is essential for the rational design of multifunctional memristors that integrate memory storage with cognitive computing capability.

In this study, we systematically explore the effect of the metal electrode selection on the resistive switching and nonlinear electrical behavior of metal/$SrTiO_3$-based memristive devices by comparing Pd, Cr, Ti, Cu, Ni, Ag, Al, and Co metal electrodes. We demonstrate that the emergence and strength of both NDR and resistive switching behavior are strongly

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dependent on the interfacial properties, which are modulated by the interfacial chemical reactivity and oxidation tendencies of the metal. Using high-angle annular dark-field (HAADF) STEM imaging, we reveal a direct correlation between interfacial layer thickness and the degree of NDR, resistive switching window, and I_{on}/I_{off} ratio. To shed light on the origins of resistive switching behavior, we perform density functional theory (DFT) calculations and quantum transport simulations. Beyond memory performance, we further show that devices with thicker and more reactive interfaces exhibit learning-forgetting-relearning behavior, suggesting an interfacial origin for synaptic plasticity modulation. These findings collectively reveal that interfacial engineering *via* electrode selection is a powerful yet underexplored lever for tuning nonlinear and memory properties in oxide memristors. Our work not only deepens the mechanistic understanding of resistive switching and NDR in $SrTiO_3$ devices but also establishes a unified framework linking electrode choice to device functionality, offering a pathway to co-optimize memory and neuromorphic performance through strategic material selection.

Results and discussion

Fig. 1a illustrates a schematic representation of our multi-functional devices, where the $SrTiO_3$ film is sandwiched between top and bottom metal electrodes. We cut a fresh device using a focused ion beam (FIB) and fabricated 80 nm-thick lamellae (Fig. 1b). Then, we acquired high-angle annular dark field (HAADF) cross-sectional scanning transmission electron microscope (STEM) images. The images confirm that the structure of the device indeed corresponds to a vertically stacked Metal/$SrTiO_3$/substrate. The $SrTiO_3$ thin film has a physical thickness of $\sim$15 nm. Also, acquired high-resolution cross-sectional transmission electron microscopy (TEM) images of the device, which confirm the correct crystalline structure of the $SrTiO_3$ film (Fig. 1c). The selected area electron diffraction (SAED) pattern of $SrTiO_3$ was recorded along the^{001} zone axis. The pattern exhibits sharp, evenly spaced diffraction spots arranged in a square symmetry, consistent with the cubic perovskite structure (Fig. 1d). Initially, we investigated the device structure of the $SrTiO_3$ device with a Co top electrode. The high-resolution cross-section morphology image and energy-dispersive spectrometer (EDS) depth profile of the $SrTiO_3$ thin film are shown in Fig. 1e. The image confirms that the structure of our device corresponds to a vertically stacked Au/Co/$SrTiO_3$ heterostructure (shortly Co/$SrTiO_3$), and the EDS maps confirm the distribution of Sr, Ti, O, Au, and Co in the heterostructure. The current–voltage (*I–V*) characteristics of the Co/$SrTiO_3$ device at room temperature show typical NDR behavior. Next, we changed the minimum bias voltage window ranging from -5 to -1 V, fixing the maximum bias voltage at 7 V (Fig. 1g). The device showed unipolar NDR behavior, and the *I–V* characteristics showed significant dependence on minimum voltage value, as at small voltages, NDR behavior is not visible, and with increasing voltage to $V_{min} = -5$ V, we observed the most robust NDR behavior. As shown in Fig. 1h, the NDR window showed dependence on bias width, where the peak and valley voltages (*e.g.*, V_P and V_V) shifted to more positive voltages over increasing minimum bias voltage. Peak and valley voltage evolution over the bias window width is extracted (dots), and the fitted curve (solid line) shows an exponential behavior (Fig. 1i). Similarly, peak to valley (PVR) shows exponential increases over the bias window width (Fig. 1j) as it enhanced from 1 to 2.2 at $V_{min} = -5$ V (equal to bias window of 10 V). This exponential evolution of peak/valley voltages and PVR with increasing bias window can be attributed to enhanced electric-field-driven carrier transport across the metal/$SrTiO_3$ interface, possibly resulting in field-dependent tunneling[25] and trap-assisted conduction.[26]

Building on the foundational material and structural characterization presented in Fig. 1, we next examined how the choice of top metal electrode influences the electrical behavior of our metal/$SrTiO_3$ devices. To systematically explore this, we first fabricated $SrTiO_3$ devices using both noble and active metals, including Pd, Ti, Ag, Al, and Co as electrodes. Then, the electrical characteristics for each device were measured at $T = 25$ °C and ambient conditions. Devices incorporating Pd and Ti electrodes exhibited Schottky-like *I–V* characteristics without any indication of NDR behavior (Fig. 2a). Current index of various metal/$SrTiO_3$ devices extracted at peak current and normalized to the reference device with the Co electrode. The index in the left column indicates relative current levels across different metal electrodes under identical conditions. In contrast, clear NDR features were observed in devices with Ag, Al, and Co electrodes, with the effect intensifying in the order Ag $<$ Al $<$ Co. Applying a negative voltage sweep to -5 V results in a transition from the high-resistance state (HRS) to the low-resistance state (LRS), while a positive voltage sweep to 5 V resets the device back to the HRS. Devices with Pd and Ti electrodes exhibited weak resistive switching, whereas significantly enhanced switching behavior was observed for devices with Ag, Al, and Co electrodes (Fig. 2b). To understand the origin of these differences, we conducted high-angle annular dark-field (HAADF) scanning transmission electron microscopy (STEM) to examine the interface between each metal and the $SrTiO_3$, as shown in Fig. 2c. The Pd and Ti formed very sharp and abrupt interfaces with minimal structural or chemical modification of the underlying $SrTiO_3$. In contrast, Ag, Al, and Co formed progressively thicker and more diffuse interfacial regions. Note that representative HADDF-STEM images are shown here, with a comprehensive set of images for each metal provided in Fig. S1. Interestingly, while the NDR and switching effects became stronger with increasing interface thickness, the NDR window, the voltage range over which NDR occurs, did not increase monotonically. The widest NDR window was observed for Ag-based devices, followed by a gradual narrowing in Al and Co devices, despite their thicker interfaces. This suggests a non-linear relationship where an optimal interfacial thickness may exist for maximizing the voltage range of NDR operation. Nonetheless, the most pronounced NDR (*e.g.*, as measured by the PVR value) and the

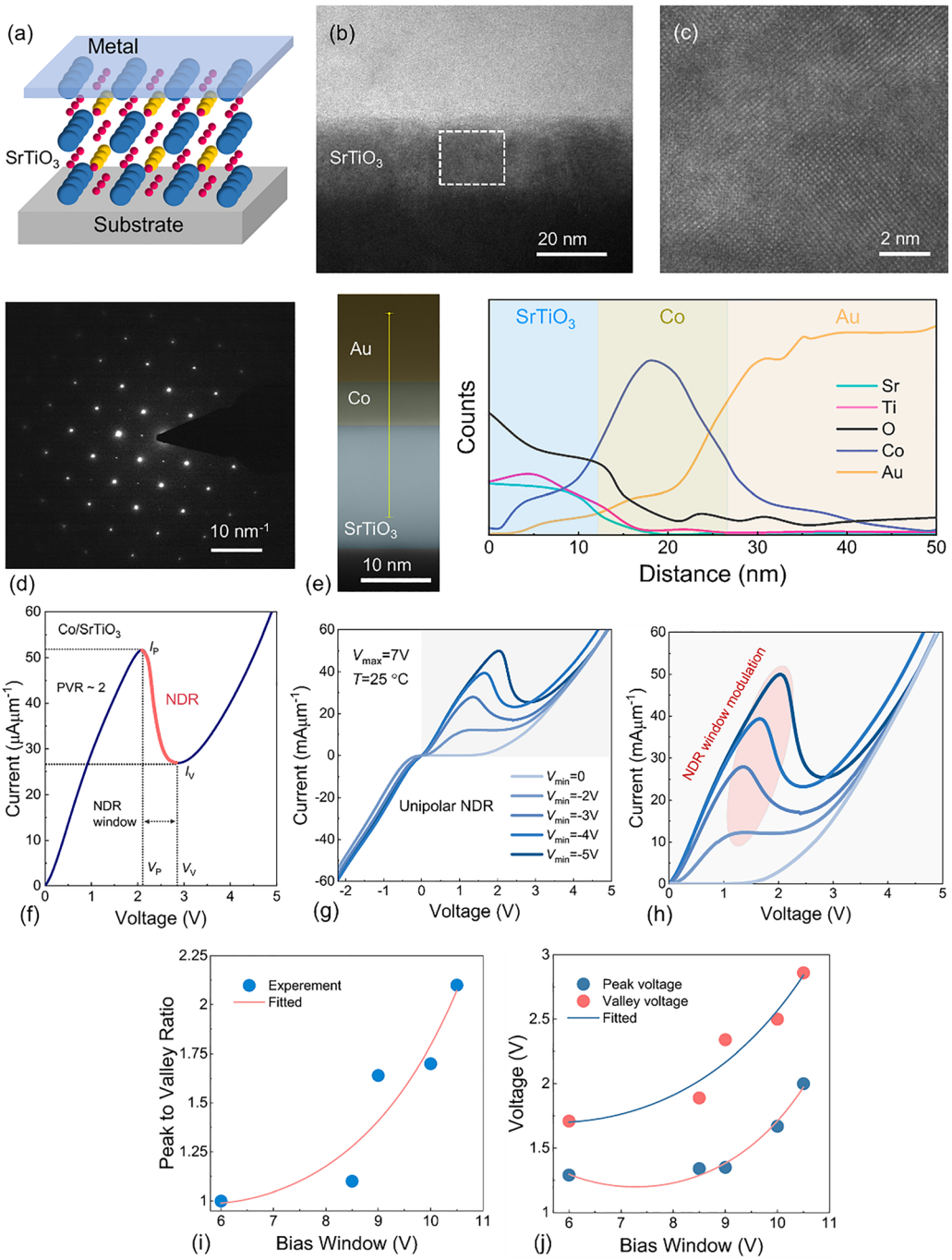

Fig. 1 Structural and electrical characterization of the Metal/$SrTiO_3$ heterojunction NDR devices. (a) Schematic of the Metal/$SrTiO_3$ heterojunction. (b) A cross-sectional HADDF-STEM image of the Metal/$SrTiO_3$ heterojunction. (c) The HR-TEM image of $SrTiO_3$ illustrates its crystalline structure, and (d) shows the electron diffraction patterns from the corresponding region. (e) EDS depth profile, (f) *I*–*V* characteristics of the device with sharp and thick interfaces. (g) Unipolar NDR behavior of *I*–*V* characteristics with different V_{min}, with (h) zoomed NDR area. (i) and (j) Extracted and fitted peak/valley voltages and PVR values over the Bias window.

strongest resistive switching behavior (*e.g.*, the largest I_{on}/I_{off} ratio) were achieved in Co-based devices, which had the thickest interfacial layer among all the samples studied. Additional electrodes, including Cr, Cu, and Ni, were also evaluated, all of which exhibited Schottky-like *I*–*V* characteristics without showing any NDR behavior (Fig. S2). In addition, these electrodes exhibited comparatively weaker resistive switching performance than the more active counterparts, such as Ag, Al, and Co (Fig. S3). Fig. 2d-f presents the quantitative dependence of PVR, the NDR window, and the I_{on}/I_{off} ratio *versus* interfacial thickness, respectively. The observed correlation between interface thickness and electrical performance suggests a

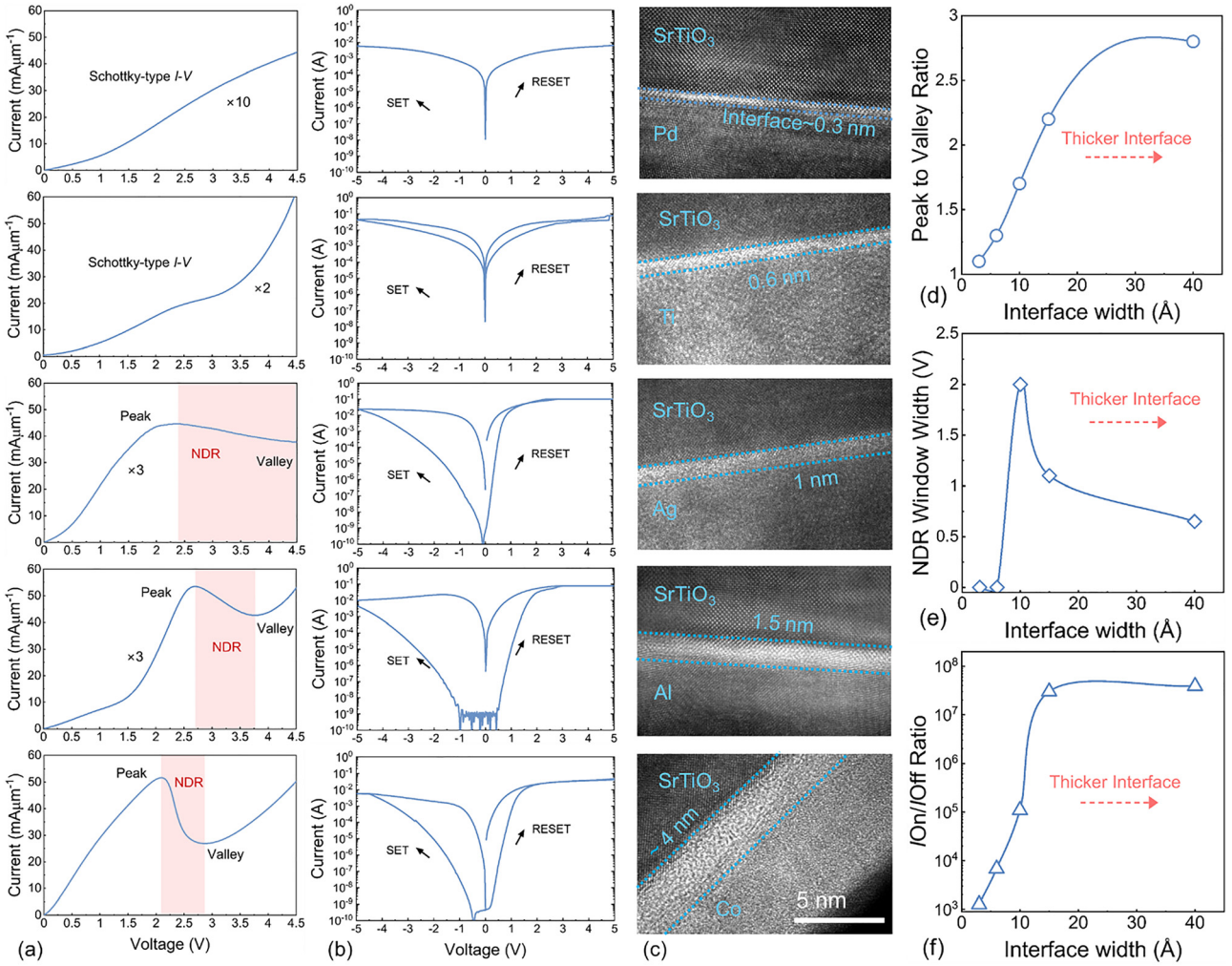

Fig. 2 Electrical characteristics and interface-dependent performance of metal/$SrTiO_3$ heterojunctions. (a) *I*–*V* characteristics, (b) memory performance, (c) a cross-sectional HADDF-STEM image of the $SrTiO_3$ heterojunction with Pd, Ti, Ag, Al, and Co. (d) PVR and (e) NDR window width, and (f) I_{on}/I_{off} ratio over interface width. The current index in the left column for various metal/$SrTiO_3$ devices is normalized to the reference device with the Co electrode.

mechanism in which the interface itself acts as an active layer, facilitating NDR and resistive switching. Thicker interfacial regions are likely to support increased defect formation,[27] particularly oxygen-vacancy generation[16] at the metal/$SrTiO_3$ interface. The error bar plot for the interface width variation of different metals is shown in Fig. S4. In some devices with Co electrodes, a local dome-shaped feature is observed at the Co/$SrTiO_3$ interface (Fig. S5). We attribute the dome-like interfacial region to localized oxidation of the electrode at the $SrTiO_3$ interface, likely driven by oxygen migration under high electrical bias. This leads to a non-uniform redistribution of oxygen vacancies and corresponding changes in the local stoichiometry, which modulate the interfacial injection barrier and give rise to the observed resistive switching and NDR behavior. In this picture, the switching originates from the dynamic evolution of the interface rather than from the formation and rupture of conductive filaments. By contrast, devices with sharper and more chemically stable interfaces, such as Pd and Ti, do not exhibit similar behavior, likely because they do not support comparable interfacial defect evolution or vacancy redistribution. It is important to note that oxide formation tendency does not translate into a strictly monotonic electrical response. While increasing interfacial oxide thickness generally enhances NDR strength and switching performance, the NDR window does not follow the same trend, indicating a more complex dependence on interface properties. This suggests the existence of an optimal interfacial regime where the balance between defect density and carrier transport maximizes device performance. Accordingly, the proposed design framework should be interpreted as a trend-based guideline rather than a strictly monotonic rule, ensuring a physically grounded and non-overgeneralized understanding. Furthermore, possible contributions from other mechanisms, such as thermal effects, trap-assisted tunneling (TAT), and interface barrier modulation, were carefully considered in interpreting the observed unipolar NDR. Thermal effects are unlikely to dominate, given the relatively low operating currents and the high reproducibility of the switching behavior. Similarly, TAT typically leads to

smooth nonlinear conduction rather than the distinct unipolar NDR observed here. While interface barrier modulation can influence carrier injection, in our devices, it is intrinsically governed by bias-driven oxygen vacancy migration within the interfacial oxide layer. Accordingly, the unipolar NDR behavior is primarily controlled by oxygen vacancy dynamics, with other mechanisms contributing only likely in secondary positions. We clarify that the NDR under positive bias and the resistive switching under negative bias originate from the same interface-controlled oxygen vacancy dynamics, rather than distinct mechanisms. Under negative bias, oxygen vacancies migrate toward the interface, reducing the barrier and inducing the SET transition (HRS to LRS). Under positive bias, partial vacancy redistribution away from the interface leads to a non-monotonic modulation of the injection barrier, resulting in NDR within a limited voltage range. Depending on the sweep amplitude and device history, this same process can either manifest as NDR or evolve into a full RESET. Overall, both behaviors are consistently explained by bias-dependent interfacial oxygen vacancy redistribution. To assess the possible influence of $SrTiO_3$ thickness on the *I–V* characteristics, we performed cross-sectional STEM imaging, the results of which reveal a uniform $SrTiO_3$ layer ($\sim$15 nm) with highly similar morphology across different samples used for device fabrication, confirming consistent film growth (Fig. S6). Together, these findings underscore the critical role of interfacial engineering in oxide-based nanoelectronic devices. By carefully selecting the electrode material and controlling the interface structure, it is possible to modulate key nonlinear electrical behaviors, offering a powerful approach to optimizing device functionality for applications in memory, logic, and neuromorphic computing.

Fig. 3 provides a comparative evaluation of resistive switching performance in devices with five different top metal electrodes: Pd, Ti, Ag, Al, and Co. In Fig. 3a, retention measurements over 10 000 seconds for representative active and noble metals, Co and Al, and Pd are shown. Our observations show that while the low-resistance state (LRS) remains relatively stable across all devices, the high-resistance state (HRS) varies significantly with metal type. This can be attributed to the fact that LRS conduction is dominated by bulk or intrinsic channel properties, whereas HRS is more sensitive to interfacial electronic structure, trap states, and potential barrier height, factors that vary with metal reactivity and interface chemistry. Despite this variation, all devices exhibit well-separated and stable resistance states, with minimal drift, confirming reliable non-volatile memory characteristics. Endurance results in over 200 cycles (Fig. 3b) further confirm stable switching across all devices, with clearly maintained HRS and LRS states throughout repeated SET/RESET operations. A notable distinction is observed in I_{on}/I_{off} ratios (Fig. 3c), which differ significantly with electrode type. Devices using Co and Al, and Ag electrodes exhibit the highest switching ratios, respectively, while Pd, Ti, Cu, Cr, and Ni show more moderate contrast. The interfacial properties primarily govern this difference. Co, Al, and Ag are chemically active metals that are more prone to forming native oxides or undergoing interfacial reactions with the oxide surface, leading to thicker or more electronically modulated interface layers. These altered interfaces likely enable enhanced charge trapping, barrier modulation, or local redistribution of defect states, resulting in stronger resistive switching. In contrast, Pd, Ti, and Ag form sharper or more inert interfaces that suppress such effects, leading to weaker RS behavior. Also, the distributions of V_{SET} and V_{RESET} (Fig. S7), show good consistency across cycles and among devices. This uniformity suggests stable interface-driven switching mechanisms, irrespective of the electrode metal used.

This enhanced performance in Co and Al devices is attributed to the active chemical nature of these metals, which promotes stronger interfacial interactions with the switching layer, likely $SrTiO_3$. Both Al and Co are known to readily form native oxides or undergo interfacial redox reactions, resulting in thicker and more chemically reactive interfacial layers, a feature also observed in HAADF-STEM analysis discussed in earlier sections. These interfacial layers can serve as reservoirs or facilitators for oxygen vacancy generation and migration, which are key to forming and rupturing conductive filaments in resistive switching devices.[28,29] Furthermore, the reactive interfaces in Co and Al devices help stabilize the formation and dissolution of conductive paths, thereby enhancing the contrast between HRS and LRS, improving retention stability, and enabling sharper and more reproducible switching events. In contrast, devices with noble or less reactive metals like Pd and Cr, *etc.*, tend to form sharp, clean interfaces with minimal intermixing, limiting the formation of oxygen vacancies and suppressing filamentary conduction. Furthermore, the dome-shaped Co contact and its conformal interface with the $SrTiO_3$ layer (Fig. S5), likely formed by the extensive migration/accumulation of oxygen between the electrode and $SrTiO_3$. This observation further substantiates our hypothesis by directly linking interfacial morphology to the enhanced resistive switching and the pronounced NDR behavior. To evaluate device-to-device reproducibility, we performed statistical analysis of the key performance metrics, PVR, I_{on}/I_{off} ratio, and NDR window width, across 20 devices for each metal electrode, as summarized in Fig. 3d–f. The distributions show a high degree of consistency within each metal group, with most devices exhibiting closely clustered values for all three parameters. This narrow spread not only confirms the robustness of the measured characteristics but also reinforces the systematic trends observed across different metals. In particular, the clear separation between electrode types indicates that the electrical behavior is governed by intrinsic, metal-dependent interface properties rather than stochastic variations.

To gain insights into the interface-modulated resistive switching in $SrTiO_3$ devices, we perform a set of atomistic simulations. Firstly, we calculate reaction enthalpies for the oxide formation at Pd, Ti, Co, Ag, and Al electrodes using density functional theory (DFT) (Fig. S8). The lowest formation enthalpies (the oxide is the most likely to form) are obtained for Al_2O_3, Co_3O_4, and TiO_2. This finding indicates that the dome-like region observed by the measurements may correspond to

an oxide formed at the metal-$SrTiO_3$ interface. Similarly, a higher formation enthalpy of PdO is in line with the sharp Pd–$SrTiO_3$ interface.

Having identified electrodes with the highest potential of interface modulation, we construct models of resistive switching in devices with a sharp interface, taking the Pd electrode as an example, and in devices in which an oxide layer is likely to form, such as in Al-based devices. The model is based on DFT calculation, performed on static device atomistic structures, which are subsequently passed to a quantum transport solver that outputs a current value for a given applied voltage. In both cases, we assume that $SrTiO_3$ is sub-stochiometric, *i.e.*, contains a small amount (around 3.8%) of oxygen vacancies that are generated during the process shown in Fig. 2a. These oxygen vacancies migrate towards/from the Au electrode upon the application of positive (negative) bias at the top electrode. Such migration may lead to the conductance modulation, as demonstrated in Ref. 30 We construct structures with vacancies accumulated at one of the electrodes (Pd or Au), or, in the case of Al-based devices, at the Au electrode, at the Al_2O_3–$SrTiO_3$ interface, and within the Al_2O_3 layer. Additionally, we consider only the crystalline $SrTiO_3$ with the TiO_2 termination, as it has been demonstrated that this termination is likely to exhibit interface-type switching.[30]

First, we assess the possibility of vacancy migration-induced resistive switching in Pd–$SrTiO_3$–Au devices. As demonstrated in Fig. S9, the current values calculated at −1 V for the two vacancy distributions differ marginally. At the positive bias of 0.5 V, the currents differ by two orders of magnitude, but they are both in the low current range. Based on these results, we exclude the possibility of resistive switching solely *via* vacancy migration in the Pd–$SrTiO_3$–Au device, which is fully consistent with the device's *I*–*V* characteristics shown in Fig. 2b. The reason for such behavior can be attributed to the lack of an interfacial region at one of the electrodes and the similar work functions of these two electrodes,[31] leading to a rather symmetric device where the conduction modulation cannot be achieved by oxygen vacancy migration.

Next, we analyze the conductance modulation in Al–$SrTiO_3$–Au devices with oxygen vacancies present at different locations. In this case, we assume that a thin (1.5 nm-long) layer of Al_2O_3 is formed at the Al–$SrTiO_3$, as suggested by TEM measurements and calculated oxide formation enthalpies. The highest current for both polarities is obtained for the structure with vacancies located within the Al_2O_3 layer (Fig. 4a). As revealed by the local density of states (LDOS) plot, the injection of electrons from the Al electrode into the conduction band of $SrTiO_3$ is facilitated in this case, as the oxygen vacancies in Al_2O_3 make this layer conductive. On the other hand, the current is the lowest in the case of vacancies accumulating at the opposite, Au electrode (Fig. 4b). In this case, the Al_2O_3 layer acts as a barrier for electron transport. The large On/Off ratio (for both the positive and negative biases) for these two configurations (Fig. 4d) is consistent with the *I*–*V* measurements presented in Fig. 2b. Additionally, the configuration of vacancies grouped at the Al_2O_3–$SrTiO_3$ interface exhibits a moderately large current (Fig. 4c and d), as the transport through the Al_2O_3 layer is now promoted by the tunneling *via* oxygen vacancy states at the interface. We have therefore demonstrated that the modulation of the oxygen content through oxygen vacancy migration is a plausible mechanism of resistive switching in devices where an oxide is formed at one of the interfaces. Moreover, we note that

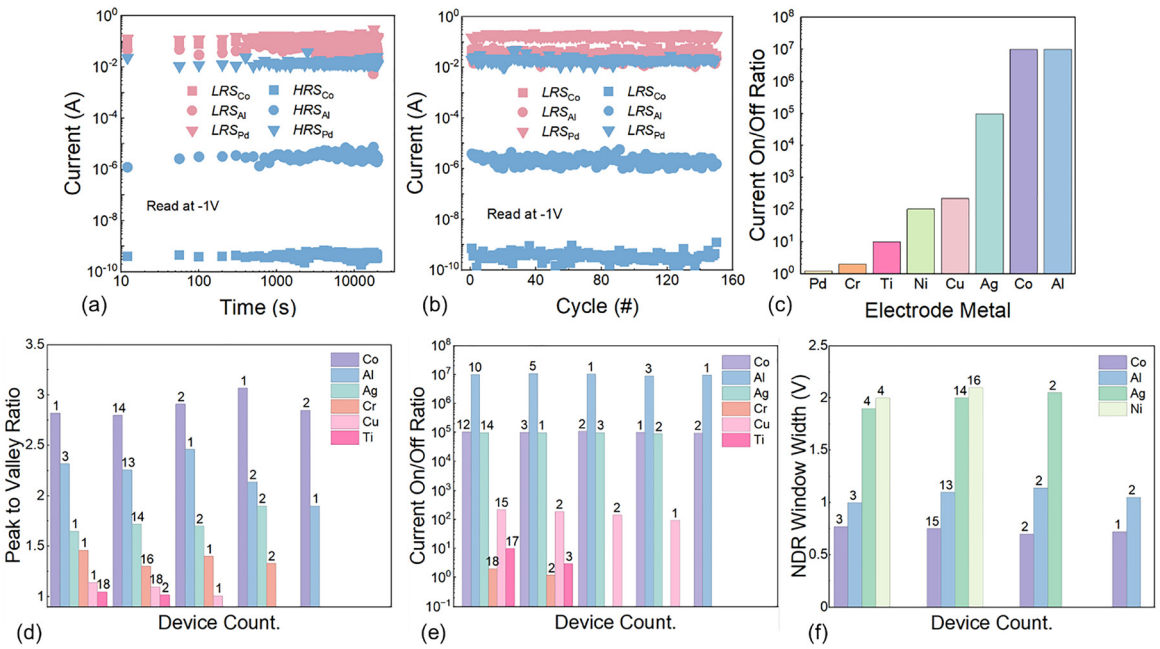

Fig. 3 Retention, endurance, and switching characteristics of $SrTiO_3$ devices with different metal electrodes. (a) retention, and (b) endurance performance of three representative metals with thin Pd, and thicker Co and Al interfaces. (c) Current on/off ratio, and (d)–(f) PVR, current On/Off ratio and NDR window, respectively.

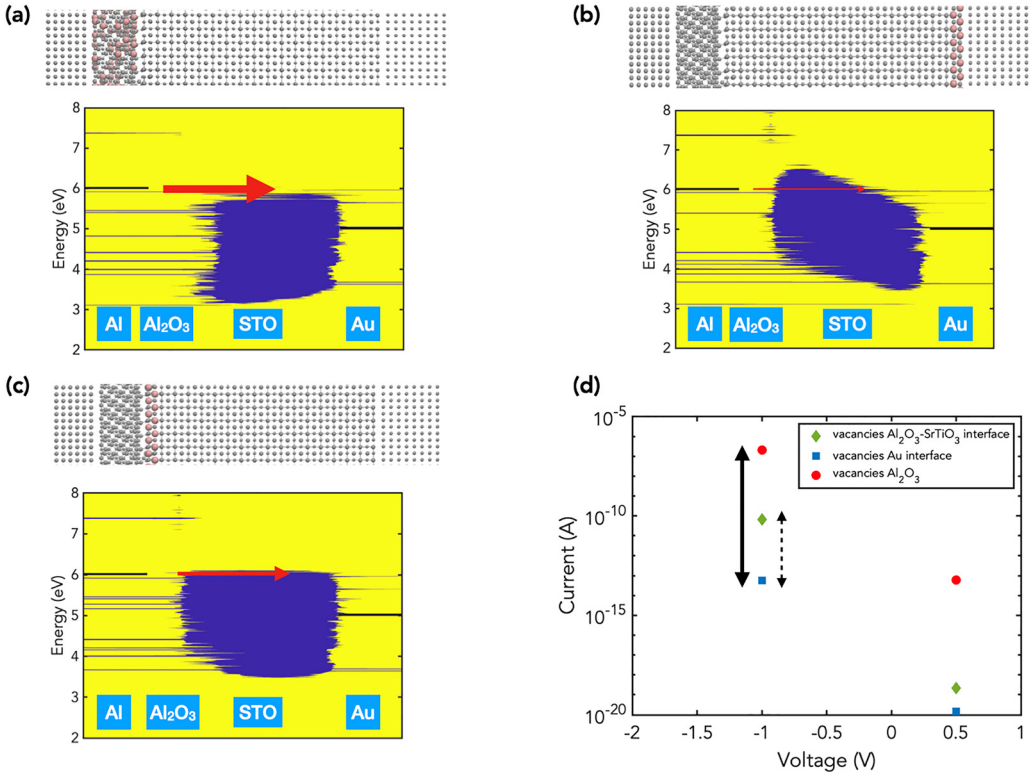

Fig. 4 Atomistic modeling and transport characteristics of Al–Al_2O_3–$SrTiO_3$–Au devices with oxygen vacancies. (a) The atomistic structures and the corresponding local density of states (LDOS) plots for Al–Al_2O_3–$SrTiO_3$–Au devices with oxygen vacancies (shown in pink) located in the Al_2O_3 interfacial layer, (b) at the $SrTiO_3$–Au interface, and (c) at the Al_2O_3–$SrTiO_3$ interface. Yellow and blue regions denote high and low DOS, respectively. The red arrows indicate the electron transport from the Al electrode into the $SrTiO_3$, while the black horizontal lines indicate the Fermi levels of the electrodes at −1 V applied to the Al electrode (1 V applied to the Au electrode). (d) Current for the devices in a–c, calculated at −1 V, and 0.5 V voltages. Vertical arrows indicate On/Off ratios. STO is used as the standard abbreviation for $SrTiO_3$ in the figures.

the direction of the vacancy migration is aligned with the biasing scheme used in Fig. 2b, strengthening our model further. As an alternative mechanism, changing the width of the interfacial oxide layer may also lead to resistive switching behavior. Exploring this phenomenon, however, goes beyond the scope of this work.

As summarized in Table 1 and compared with prior $SrTiO_3$-based devices, our results highlight an improvement in achieving multifunctional device performance. In most reported studies, devices tend to exhibit either resistive switching or NDR behavior individually; when both are present, one functionality is typically compromised, resulting in reduced I_{on}/I_{off}

Table 1 Comparison of $SrTiO_3$-based memristors and NDR logic devices, including material form, device structure, switching behavior, and key performance metrics

Device structure	Film form/thickness (nm)	Switching mode/voltage (V)	I_{on}/I_{off}	Endurance	Retention (s)	PVR	NDR window width (V)
$Pt/SrTiO_3/Pt$[10]	Amorphous/100	Filamentary/−1.5	10^3	—	—	1.5	0.75
$Pt/SrTiO_3/Pt$[13]	Amorphous/10	Interfacial/−1.5	10^2	10^5	10^4	1.3	0.55
$Ag/SrTiO_3/Ag$[15]	Crystalline/—	Interfacial/—	10^2	—	10^2	—	—
$Pt/Nb:SrTiO_3/Al$[19]	Polycrystalline/—	Interfacial/0.3	10^6	—	10^3	—	—
$Ag/SrTiO_3/Pt$[32]	Crystalline/100	Interfacial/0.24	$<10^3$	—	—	—	—
$Au/SrTiO_3/Nb:SrTiO_3$[33]	Crystalline/35	Filamentary/—	<10	—	—	1.3	1
$Ag/Mn:SrTiO_3/Ti$[34]	Crystalline/—	Filamentary/1.2	~10	10^2	5×10^3 s	—	—
$Pt/SrTiO_3/SRO/Pt$[35]	Crystalline/100	Filamentary/—	$\sim 10^4$	$\sim 10^2$	10^4s	<1.5	0.5
$Ag/SrTiO_3/Pt$[36]	Amorphous/53	Filamentary/0.3	—	10^2	~10	—	—
$Pd/SrTiO_3/MgO/LSMO$[37]	Crystalline/38	Interfacial/2.5	$\sim 10^2$	10^6	10^4s	—	—
$Au/Nb:SrTiO_3/Au$[38]	Crystalline/500	Interfacial/−1.25	$\sim 10^5$	10^4	$>10^4$s	—	—
$Au/Nb:SrTiO_3$[39]	Crystalline/500	Interfacial/−1.5	$>10^4$	$\sim 10^4$	10^9s	1.1	2.5
$Pt/TiO_2/SrTi_{0.99}Nb_{0.01}O_3/Pt$[40]	Crystalline/—	Interfacial/—	~10	3×10^3	—	1.9	2.5
This work	Crystalline/15	Interfacial/−0.5	$>10^7$	150	10^4	2.9	1
This work	Crystalline/15	Interfacial/−1	$>10^5$	150	10^4	2.25	1

ratios or relatively weak NDR characteristics (commonly 1.1 < PVR < 1.9). In contrast, our devices demonstrate both strong resistive switching ($I_{on}/I_{off} > 10^7$) and pronounced NDR (PVR up to 2.9), while maintaining stable retention. This balanced performance is achieved through a straightforward and practical strategy based on metal selection and interface engineering. Overall, these results suggest that carefully controlled interface formation can provide an effective route to simultaneously optimize memory and nonlinear functionalities in $SrTiO_3$-based devices.

Conclusion

In summary, our comprehensive study elucidates the decisive role of metal electrode choice and interfacial morphology in modulating the resistive switching, negative differential resistance, and potentially neuromorphic properties of metal/$SrTiO_3$-based memristors. We demonstrate that active metals, such as Co and Al, form thicker interfacial layers that facilitate enhanced oxygen vacancy dynamics, thereby producing more pronounced NDR features, larger switching windows, and improved I_{on}/I_{off} ratios. In contrast, some metals such as Pd, Ni, Cr, and Ti may yield thinner interfaces with diminished switching performance. Our results reinforce the conclusion that the rational interface engineering *via* electrode selection offers a powerful strategy to tailor multifunctional memristive devices, paving the way for optimized memory and brain-inspired computing systems.

Methods

Device fabrication

The $SrTiO_3$ thin film was grown on $SrTiO_3$ (001) substrates using the pulsed laser deposition (PLD) at 650 C in $\sim 10^{-3}$ Torr. The electrode area (60 μm × 60 μm) was determined using electron-beam lithography on $SrTiO_3$ thin film, followed by thermal deposition of the top electrode metal/Au (10/80 nm) and bottom electrodes Au (80 nm) under the vacuum pressure of $\sim 10^{-6}$ Torr. Finally, a metal lift-off was carried out to remove extra metals and achieve drain and source electrodes.

Characterization and measurement

HADDF-STEM imaging and EDX analysis were performed at 200 kV using Seron AIF 2100 and Philips CM30. Electrical characteristics were measured using a Keithley 4200 parameter analyzer and RIGOL DG5072 arbitrary waveform generator, digital oscilloscope, in an ambient probe station under dark conditions. The *I–V* measurements were carried out at the read voltage of approximately −1 V, a compliance current of 10^{-3} A, and a voltage sweep rate of 0.2 V s^{-1}. The I_{on}/I_{off} ratio was extracted at −1 V. The PVR was defined as the ratio of the peak current to the valley current (I_{peak}/I_{valley}), while the NDR window was determined from the voltage difference between the valley and peak positions (V_{valley}–V_{peak}).

Computational details

All electronic structure calculations are performed using the density functional theory (DFT) method, implemented in the CP2K code[41] with its Gaussian-type orbitals (GTOs). Formation enthalpies of oxides E_{form} are calculated as:

$$E_{form} = aE(\text{oxide}) - bE(\text{metal}) - \frac{1}{2}cE(O_2),$$

where E(oxide), E(metal), and $E(O_2)$ are the energies per number of functional units of oxides, corresponding metals, and the oxygen gas, while a, b, and c are integer multiples that ensure the balance between the species involved in the reaction. The oxygen gas is modeled by placing an O_2 molecule in a 10 Å-large cubic box. Before constructing devices, bulk structures of the electrodes, oxides, and crystalline $SrTiO_3$ are created. These blocks are then attached by optimizing the distance between each of them, and applying the strain (along the directions perpendicular to the transport direction) to the electrodes and the interfacial layer, so that they match the dimensions of $SrTiO_3$. Structural relaxations are performed using the L-BFGS minimization method, with a double-ζ polarization (DZVP) basis set[42] and the PBE functional.[43] Convergence criteria of 4.5×10^{-4} Ha $bohr^{-1}$ for forces and 3×10^{-3} bohr for the geometry change are used. The plane-wave cutoff is set to 500 Ry, while a cutoff of 60 Ry is employed to map the GTOs onto the plane-wave grid. To generate the Hamiltonian and overlap matrices that serve as inputs to transport calculations, a single-ζ polarization basis set[42] is used to minimize the computational costs. The Hamiltonian elements smaller than 1×10^{-6} Ha are excluded from the transport calculations. The electronic current through the constructed devices is computed *via* the quantum transmitting boundary method (QTBM) in the coherent limit of transport.[44] To correct for the band gap underestimation of DFT, the Hubbard (DFT+U) correction[45] with the parameter U–J = 9 eV is applied to the 3d orbitals of Ti. Open boundary conditions are applied along the transport direction to allow for electron injection and to determine the transmission function through devices.

Conflicts of interest

There is no conflict of interest to declare.

Data availability

The data that support the findings of this work are available from the corresponding author upon reasonable request. All data requests will be handled by SM.SE., who can be contacted at sattari@iue.tuwien.ac.at.

Supplementary information (SI): TEM images of the metal/$SrTiO_3$ heterostructure, *I–V* characteristics of the $SrTiO_3$ device, cross-sectional SEM image of the $SrTiO_3$ device, RESET voltage distribution of the $SrTiO_3$ device, formation enthalpies of oxides formed at the metal-$SrTiO_3$ interfaces, and

computational modeling (LDOS and transport) of Pd–$SrTiO_3$–Au devices. See DOI: https://doi.org/10.1039/d6tc00552g.

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