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Deuterium-enabled stabilization of metal/oxide interfaces *via* suppressed oxygen diffusion in BEOL-compatible InGaZnO thin-film transistors

Woosub Byun,[a] Tae-Hyun Kil,[b] Bong Ho Kim,[c] Yunseok Kim,[de] Hwanyeol Park,*[de] Jun-Young Park*[bf] and Dae-Myeong Geum *[a]

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This study systematically investigates the influence of post-metallization annealing (PMA) ambient on the electrical and interfacial properties of a-IGZO thin-film transistors (TFTs) incorporating BEOL-compatible tungsten (W) contacts. The devices were annealed at 300 °C and 350 °C using oxygen rapid thermal annealing (O_2 RTA) and high-pressure deuterium annealing (HPDA). The HPDA-treated devices exhibited enhanced electrical performance, including reduced subthreshold swing (74 mV dec^{-1}), increased I_{on}/I_{off} ratio, and lowered contact resistance ($R_C W$ = 5.74 Ω cm). These improvements are attributed to the passivation of interfacial defects and the formation of W–D bonds, which effectively suppress interfacial oxidation. Furthermore, based on density functional theory (DFT) calculations, it was noted that HPDA promotes W–D bond formation, which can play an important role as an oxygen diffusion barrier. These theoretical results give a physical basis for the dual role of deuterium in defect passivation and suppression of interfacial oxidation at the W electrode, consistent with the HPDA observations of decreased W 4f binding energy and reduced WO_x formation.

1. Introduction

As CMOS technology approaches its scaling limits, alternative integration approaches have gained increasing attention to sustain improvements in performance and functionality. Among these, monolithic three-dimensional (M3D) integration offers a promising solution by enabling vertical stacking of devices, thereby reducing interconnect delays and enhancing system density and speed.[1–3] To realize such integration at the back end of line (BEOL), the use of low-temperature and high-mobility channel materials is essential. Amorphous indium-gallium-zinc oxide (a-IGZO), a representative oxide semiconductor (OS), has emerged as a compelling candidate for BEOL-compatible transistors due to its low processing temperature, high carrier mobility, and negligible off-state leakage current.[4–11] These properties make IGZO particularly attractive for stacked memory and logic systems in M3D architectures.

However, as device dimensions shrink and the total resistance becomes increasingly dominated by the source/drain contact resistance (R_C), optimizing the metal/oxide interface has become a critical challenge.[12–14] Several methods, including ozone treatment and interlayer insertion, have been proposed to engineer the metal–oxide interface and reduce R_C.[13,15] However, these approaches are not suitable for large-area applications and may involve complicated process steps. While post-annealing techniques using oxygen (O_2)[16] and nitrogen (N_2) atmospheres have been widely studied, hydrogen (H_2)-based treatments have recently gained attention due to their ability to passivate oxygen-related defects and defect states in IGZO. Forming gas annealing (FGA) and high-pressure hydrogen annealing (HPHA), both utilizing H_2, have shown improvements in electrical performance and stability.[15–19]

Recently, deuterium (D_2), a stable isotope of hydrogen, has attracted attention due to its superior thermal, chemical, and electrical stability. While its passivation mechanism is analogous to that of H_2, D_2 exhibits greater stress immunity due to its larger atomic mass (*e.g.*, Si–D *vs.* Si–H), which enables more durable suppression of defect generation under stress conditions. Accordingly, high-pressure deuterium annealing (HPDA) has been introduced and demonstrated to outperform

[a] Department of Electrical and Computer Engineering, Inha University, 100 Inha-ro, Michuhol-gu, Incheon 22212, Republic of Korea. E-mail: dmgeum@inha.ac.kr
[b] ParkLab Semiconductor Inc., 1 Chungdae-ro, Seowon-gu, Cheongju-si, Chungcheongbuk-do 28644, Republic of Korea
[c] Semiconductor R&D Center, Samsung Electronics, Co. Ltd., Giheung, South Korea
[d] Department of Electronic Materials, Devices, and Equipment Engineering, Soonchunhyang University, Asan City, Chungcheongnam-do 31538, Republic of Korea. E-mail: phy3654@sch.ac.kr
[e] Department of Display Materials Engineering, Soonchunhyang University, Asan City, Chungcheongnam-do 31538, Republic of Korea
[f] School of Electronics Engineering, Chungbuk National University, 1 Chungdae-ro, Seowon-gu, Cheongju-si, Chungcheongbuk-do 28644, Republic of Korea. E-mail: junyoung@cbnu.ac.kr

conventional hydrogen-based approaches in channel defect passivation.[20–22] Nevertheless, the majority of D_2-related studies have been limited to improvements in the bulk or the gate dielectric/channel interface properties. In contrast, its role in modifying R_C at the metal/IGZO interface, an increasingly dominant component in scaled TFTs, remains underexplored. Moreover, a holistic understanding of how HPDA concurrently modulates both the gate insulator/channel and metal/channel interfaces has yet to be established. This lack of insight hampers the broader adoption of D_2-based treatments in BEOL-compatible integration schemes.

Therefore, a systematic investigation into the dual-interface effects of HPDA is necessary to elucidate the underlying reaction pathways and their impact on electrical characteristics. In particular, understanding how D_2 affects interfacial oxidation, R_C, effective channel length deviation (ΔL), and subthreshold swing (SS) is critical to realizing reliable oxide-based transistors under thermal and integration constraints. In this work, we present a comprehensive analysis of HPDA as a post-metallization treatment to suppress interfacial oxidation and enhance the switching characteristics in tungsten (W)/a-IGZO TFTs. By comparing against conventional O_2 rapid thermal annealing (RTA), we demonstrate that HPDA significantly reduces R_C by forming stable W–D bonds and preventing the formation of oxidized tungsten species (WO_x), while simultaneously passivating interface traps at the gate dielectric/channel interface. This dual-interface engineering strategy enables simultaneous contact and channel optimization, offering a robust and scalable pathway for high-performance, BEOL-compatible oxide electronics.

2. Experimental details

Fig. 1a illustrates the fabrication procedure and corresponding surface morphologies of the IGZO-based devices investigated in this work. The devices were constructed on a heavily doped n^+-Si substrate (5×10^{18} cm^{-3}), which simultaneously functioned as the global back-gate electrode. A 15 nm-thick Al_2O_3 gate dielectric was deposited *via* atomic layer deposition (ALD), followed by RF sputtering of a 30 nm-thick IGZO channel layer. Mesa isolation was achieved by wet etching using an HCl : DI = 1 : 6 solution. Source and drain (S/D) contacts were defined by DC sputtering of 80 nm-thick tungsten (W) and patterned through a standard lift-off process. To evaluate the impact of post-fabrication annealing on device characteristics, two distinct treatments were applied: RTA in an O_2 ambient (1 Torr, 250 sccm) and HPDA with $N_2 : D_2$ = 96% : 4% gas under 10 bar pressure, both conducted at 300 and 350 °C for 1 hour.

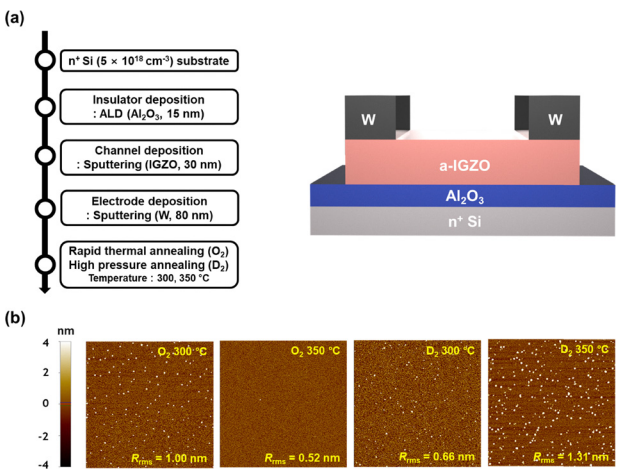

Fig. 1 (a) Schematic process flow of the a-IGZO TFT with a W contact, and (b) atomic force microscopy images of IGZO films annealed in O_2 at 300 °C and 350 °C, and D_2 at 300 °C and 350 °C.

Fig. 1b shows the atomic force microscopy (AFM) images of IGZO films subjected to O_2 RTA and HPDA treatments at 300 °C and 350 °C, respectively at the 3D Convergence Center of Inha University. A clear divergence in surface morphology is observed depending on the annealing ambient. For the O_2-annealed samples, the root mean square roughness (R_{rms}) decreased from 1.00 nm to 0.52 nm with increasing temperature, indicating enhanced film densification and surface smoothing facilitated by oxygen-driven removal of weakly bonded surface species.[23,24] This densification is likely to suppress surface-related scattering and improve interface quality with the gate dielectric. In contrast, the D_2-treated samples exhibited increasing R_{rms} values, from 0.66 nm to 1.31 nm, with rising temperature. This roughening can mainly be attributed to the thermally activated reduction of In_2O_3 by deuterium, leading to the formation of metallic indium clusters at the IGZO surface.[25,26] While this reaction enhances bulk conductivity by increasing free electron concentration, the concurrent degradation in surface flatness may introduce additional carrier scattering, particularly at the back-channel region.

All first-principles calculations were carried out within Kohn–Sham density functional theory (DFT) using the plane-wave projector augmented-wave (PAW) method as implemented in VASP.[27,28] Exchange–correlation effects were treated with the Perdew–Burke–Ernzerhof (PBE) generalized-gradient approximation[29] augmented by the D3 dispersion correction of Grimme to account for long-range interactions important at the oxide/metal interfaces.[30] Brillouin-zone integrations employed Monkhorst–Pack *k*-point meshes.[31] We used a plane-wave cut-off of 400 eV, SCF energy tolerance of 10^{-5} eV, and force convergence of 0.02 eV $Å^{-1}$. These settings follow recent tungsten/oxide interface studies and are sufficient to converge energetic trends relevant to adhesion and diffusion processes. To determine the transition state, we used the nudged elastic band (NEB) method.[32] Detailed calculation methods are explained in the supplementary information.

3. Results and discussion

To evaluate the material properties under different annealing ambients, carrier concentration was extracted from Hall-effect measurements, as shown in Fig. 2a. In comparison to the O_2 annealed devices, the HPDA-annealed device showed more than double the carrier concentration, suggesting that

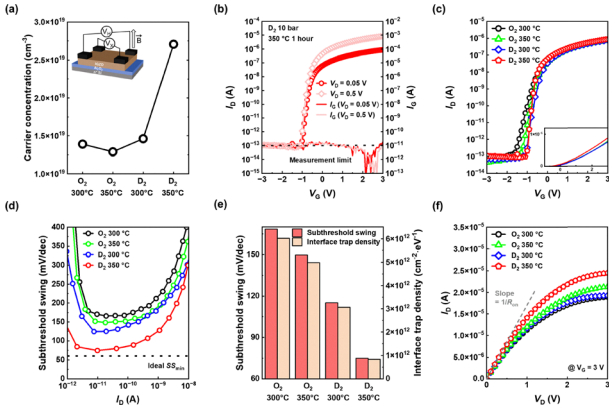

Fig. 2 (a) Hall-effect measurement results showing the variations in carrier concentration as a function of annealing ambient, with a schematic of the setup shown in the inset. I_D–V_G curves of the a-IGZO TFTs (b) for 350 °C HPDA devices and (c) as a function of different annealing ambients on a logarithmic scale (linear scale as shown in the inset figure). (d) Extracted SS *versus* I_D, (e) minimum value of SS and interface trap density (D_{it}), and (f) I_D–V_D curves of the a-IGZO TFT depending on the annealing ambient.

diffusion of D_2 into the IGZO channel effectively increases the conductivity of the IGZO channel. The increased carrier concentration can be attributed to the incorporation of deuterium into the IGZO matrix.[33]

$$H^+ + O^{2-} \rightarrow OH^- + e^- \quad (1)$$

As described in eqn (1), hydrogen (or deuterium) species in the H^+ (or D^+) state can generate conduction band electrons by bonding with lattice oxygen. This mechanism supports the interpretation that the conductivity improvement observed in the HPDA-annealed devices is primarily driven by donor-like behavior of the deuterium species introduced during annealing.

Then, to assess the electrical characteristics of the IGZO TFTs, representative transfer characteristics were measured at two drain voltages (V_D = 0.05 V and 0.5 V). Fig. 2b shows the transfer characteristics of the devices annealed by HPDA at 350 °C, and Fig. S1 shows the corresponding characteristics for the devices annealed at 300 °C and 350 °C by O_2 RTA and at 300 °C by HPDA. The electrical characteristics of the fabricated IGZO TFTs were characterized using a Keithley 4200A-SCS semiconductor parameter analyzer at room temperature under dark conditions. The devices exhibited minimal variation in both threshold voltage (V_T) and SS across the two conditions, reflecting stable turn-on behavior, robust electrostatic gate control, and low trap-assisted leakage under varying lateral electric fields. The off current (I_{off}) remained unchanged, and the gate leakage current (I_G) consistently stayed within the picoampere range near the measurement limit, confirming excellent insulating properties of the gate oxide without dielectric degradation.

Fig. 2c presents the transfer characteristics (I_D–V_G) of the devices, and Fig. S2 shows the uniformity and their corresponding mean values, measured for 10 samples with different annealing ambients. The measurements were performed with V_D fixed at 0.05 V, while V_G was swept from −3 V to 3 V. To evaluate the V_T, the constant-current method was employed, where V_T is defined as the V_G at which I_D reaches 100 nA × W L^{-1}. The average extracted V_T values were 0.66 V, 0.61 V, 0.65 V and 0.53 V for the O_2 300, O_2 350 °C, D_2 300 and D_2 350 °C samples, respectively. Fig. S3a presents the box plot of V_T for each ambient, evaluated using 10 samples at each temperature. The overall shift in V_T was relatively small, indicating that both O_2 and D_2 annealing effectively passivate the oxygen-related defects within the IGZO channel layer and maintain stable subthreshold operation. The on/off current ratio (I_{on}/I_{off}) was calculated by measuring the drain current at V_G–V_T = ±2 V. All devices exhibited robust switching characteristics with I_{on}/I_{off} ratios exceeding 10^6, indicating negligible degradation during fabrication and effective activation of the channel through post-annealing. Among the samples, the device subjected to HPDA at 350 °C exhibited the highest I_{on}/I_{off} ratio of 7.83 × 10^6, reflecting enhanced channel conductivity under this condition. This improvement might primarily result from the increased electron concentration in the IGZO layer induced by D_2 diffusion. Compared to O_2 annealing, the D_2-treated devices exhibited higher carrier densities, likely due to more effective passivation of oxygen-related defects and the incorporation of deuterium species.[34,35] As the HPDA temperature increases, deuterium incorporation becomes more pronounced, contributing additional free electrons to the conduction band.[21] Notably, the D_2-annealed device at 350 °C exhibited an increased I_{on} while maintaining a sharp SS compared to the O_2-annealed device. This observation suggests that D_2 annealing effectively passivates deep trap states at the gate dielectric/IGZO interface, contributing to enhanced electrostatic control.

Additionally, SS and interface trap density (D_{it}) were evaluated to examine how the annealing ambient influences the Al_2O_3/IGZO interface. eqn (2) was used to determine SS, which is directly impacted by D_{it}, and eqn (3) was used to extract D_{it}.[36] These investigations made it possible to quantitatively assess how the annealing ambient affects the overall electrical performance of the devices, as well as the quality of the interface.

$$SS = \frac{\partial V_G}{\partial \log I_D} \quad (2)$$

$$D_{it} = \frac{C_{ox}}{q}\left(\frac{q \cdot SS \cdot \log(e)}{kT} - 1\right) \quad (3)$$

here, C_{ox} is the gate oxide capacitance per unit area, q is the elementary charge, k is the Boltzmann constant, and T is the Kelvin temperature. The theoretical values for 15 nm-thick Al_2O_3 were utilized in the calculations: C_{ox} = 5.31 × 10^{-7} F cm^{-2}, q = 1.60 × 10^{-19} C, k = 1.38 × 10^{-23} J K^{-1}, and T = 300 K.

Fig. 2d shows the variation in SS as a function of I_D, and Fig. 2e shows the extraction of D_{it} for the fabricated IGZO TFTs under different ambients. All samples exhibited typical U-shaped SS behavior, and the average of the extracted SS values was 168,

150, 115, and 75 mV dec^{-1} for the O_2 300, O_2 350 °C, D_2 300, and D_2 350 °C samples, respectively, with the corresponding D_{it} values of 6.02 × 10^{12} cm^{-2} eV^{-1}, 4.98 × 10^{12}, 3.07 × 10^{12}, and 8.43 × 10^{11} cm^{-2} eV^{-1}. Fig. S3b presents the box plot of SS for each ambient, evaluated using 10 samples at each temperature. A consistent reduction in SS and D_{it} was observed with increasing annealing temperature across both ambient types, indicating thermally assisted passivation of the interface traps. In comparison to O_2 at 350 °C, HPDA at 350 °C yields the lowest SS and more than an order of magnitude reduction in D_{it}, suggesting better electrostatic gate control and more efficient passivation of interface states at the Al_2O_3/IGZO interface. This enhanced passivation is potentially associated with O–D bond formation, which can neutralize oxygen-related defect sites and dangling bonds.[20,21] The improved interface characteristics achieved through HPDA are expected to play a key role in ensuring electrical reliability and long-term operational stability in OS TFT applications.

Although HPDA increases the back-channel surface roughness observed by AFM, as shown in Fig. 1b, it does not necessarily conflict with the enhanced SS and decreased D_{it}. The gate-induced conduction channel in our back-gated structure is mostly formed near the Al_2O_3/IGZO interface, where interfacial trap states control SS. Therefore, the SS improvement under HPDA is consistent with enhanced trap passivation at the Al_2O_3/IGZO interface, while the roughness increase primarily reflects changes at the back-channel surface.

Furthermore, Fig. 2f shows the output characteristics of IGZO TFTs under various annealing conditions measured by sweeping V_D from 0 to 3 V at V_G = 3 V, and Fig. S4 shows the output curves measured at different V_G. All devices exhibited clear linear-to-saturation transitions, suggesting stable channel formation and effective carrier injection. Among all conditions, the device annealed under HPDA at 350 °C exhibited the highest output current and the steepest slope in the low-V_D region. To quantitatively assess this behavior, the on-resistance (R_{on}) was extracted from the linear regime of the output curves.[37] The extracted values were 6.22, 6.06, 6.01, and 5.11 Ω m for devices annealed in O_2 at 300 °C, O_2 at 350 °C, D_2 at 300 °C, and D_2 at 350 °C, respectively. This reduction may reflect contributions from both enhanced channel conductivity consistent with Hall-effect measurements in Fig. 2a and improved carrier injection at the S/D contacts. These contributions are quantitatively separated using TLM analysis in Fig. 3.

To decouple the contributions of channel resistance and contact resistance to the overall R_{on} values, we carried out an analysis of the sheet resistance (R_{sh}) of the IGZO TFTs under different annealing ambients by using the transmission line method (TLM). The inset in Fig. 3a displays the TLM fitting curves at V_G–V_T= 0 V, where the slope corresponds to R_{sh} and the y-intercept provides the R_C value. The extracted R_{sh} values were 479.4, 473.2, 472.6, and 476.4 kΩ □$^{-1}$ for the O_2 300 °C, O_2 350 °C, D_2 300 °C and D_2 350 °C samples, respectively, as shown in Fig. 3a. Thus, it is suggested that the observed reduction in R_{on} under HPDA is unlikely to originate from changes in intrinsic channel properties. Instead, the performance enhancement observed in the D_2 350 °C sample is more

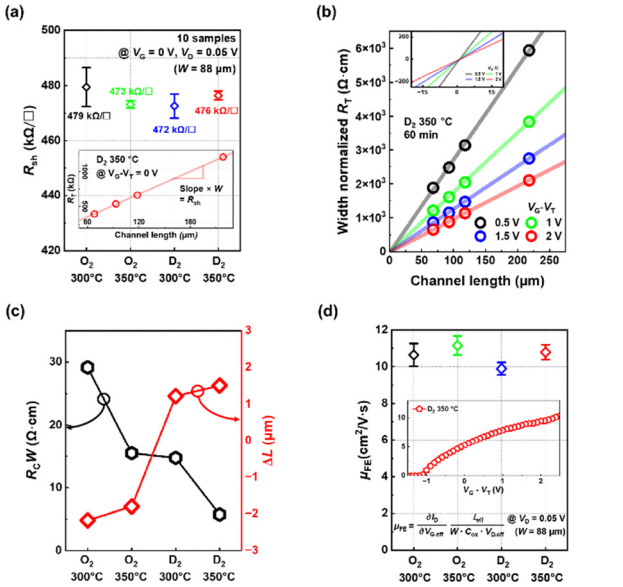

Fig. 3 (a) Comparison of the sheet resistance (R_{sh}) with different annealing ambients; the TLM linear fitting graph at HPDA 350 °C is shown in the inset. (b) Graph of width normalized R_T–L obtained by TLM at HPDA 350 °C, with parameters depending on the annealing ambient. (c) Width normalized R_C and ΔL, and (d) μ_{FE} at different annealing ambients; μ_{FE} *versus* V_G–V_T of HPDA 350 °C is shown in the inset.

reasonably attributed to changes at the contact interface. This result implies that D_2 annealing, particularly under HPDA conditions, may promote favorable interfacial reactions at the W/IGZO junction, thereby lowering R_C and enhancing the overall device performance.

So, as shown in Fig. 3b, to analyze the contact properties independently from parasitic channel effects, total resistance (R_T) was extracted at V_D = 0.05 V while sweeping V_G–V_T from 0.5 V to 2 V in 0.5 V increments. Devices with various channel lengths (L = 68, 93, 118, and 218 μm) were employed to derive R_T as a function of L. These R_T values were width-normalized ($R_T \times W$) and linearly fitted to obtain R_C and ΔL using the TLM. The effective channel length (L_{eff}) was calculated using eqn (4):

$$L_{eff} = L - \Delta L \quad (4)$$

here, ΔL quantifies deviations from the designed channel length. A positive ΔL indicates lateral diffusion of the S/D contact into the channel, effectively shortening L_{eff}, while a negative ΔL suggests current crowding near the contacts, which makes the channel appear longer than designed. Such behaviors are frequently observed in OS TFTs with back-gate structures.[14,38,39] Fig. 3b presents the extracted R_C and ΔL values for the 350 °C HPDA annealed device, while Fig. S5 shows the corresponding data for devices annealed at 300 °C and 350 °C by O_2 RTA, and at 300 °C by HPDA. As shown in the inset plot, R_C and ΔL were determined from the y- and x-intercepts of the R_T-L fitting curves, respectively. The excellent linearity in these fits demonstrates the accuracy of the extraction and the uniformity of the W/IGZO contact across the samples.

Fig. 3c compares the extracted values of $R_C W$ for IGZO TFTs subjected to different annealing conditions. Among the four conditions, the device annealed under high-pressure D_2 ambient at 350 °C exhibited the lowest $R_C W$, decreased by approximately 80% compared to the O_2 300 °C sample (29.17 to 5.74 Ω cm). Given that the channel R_{sh} remained nearly unchanged across all conditions (Fig. 3a), the observed reduction in $R_C W$ results from improvements in the metal/oxide interface, rather than changes in channel conductivity. This reduction is attributed to D atoms passivating interfacial defect states by replacing oxygen-related defects and metal-hydroxyl bonds with more stable metal–deuterium (M–D) bonds.[20,33,40,41] These reactions reduce the density of trap states at the metal-to-semiconductor (MS) interface, thereby enhancing the electron injection efficiency across the contact.[42] Furthermore, D_2 exposure during annealing may promote the formation of tungsten deuteride (W–D_x) phases at the contact interface, which can relieve local strain and suppress the formation of resistive tungsten oxides that are typically induced by O_2 annealing.[43] Notably, the device annealed with D_2 at 350 °C exhibits the lowest R_C among all samples, confirming that HPDA significantly improves charge injection at the metal/IGZO interface, which is consistent with earlier enhancements in I_{on} and R_{on}. These effects, when combined with deuterium-driven interfacial stabilization that suppresses interfacial oxidation and promotes more stable W–D-related bonding, result in a significant reduction in $R_C W$ under HPDA. This demonstrates that a D_2-containing ambient can engineer a chemically stable, low-resistance W/IGZO contact without affecting the structural integrity of the channel.

The extracted ΔL values were −2.17, −1.8, 1.22 and 1.51 μm for the O_2 300 °C, O_2 350 °C, D_2 300 °C and D_2 350 °C samples, respectively. The negative ΔL values observed in the O_2-annealed devices are attributed to current crowding near the S/D contact edges - a common phenomenon in back-gate TFT structures. As the annealing temperature increases, the improvement of the W/IGZO interface through thermally driven oxidation moderately reduces R_C, which in turn alleviates current crowding and thereby reduces the deviation between the physical channel length and L_{eff}.[44] This trend is reflected in the smaller magnitude of ΔL at 350 °C compared to 300 °C. Thus, the gradual shift of ΔL toward zero in O_2-annealed devices indicates improved electron injection efficiency due to enhanced interfacial quality, even though the contact remains non-ideal.

In contrast, HPDA-treated devices exhibited consistently positive ΔL values, measured as 1.22 μm at 300 °C and 1.51 μm at 350 °C, clearly distinguishing them from the O_2-annealed counterparts. This behavior is closely linked to the enhanced channel conductivity induced by the deuterium–oxygen reaction described in eqn (1), which significantly increases the free carrier concentration during HPDA, and the resulting reduction in resistivity facilitates lateral current spreading beyond the nominal S/D junction edges, effectively widening the conduction region and shifting the L_{eff} inward. This leads to a larger positive ΔL, indicating overextension of the current path into the S/D region. Such ΔL expansion is consistent with the mechanism proposed by Shi *et al.*,[45] where hydrogen incorporation leads to the formation of a high-electron-density interfacial layer near the contact, effectively modifying the injection and shortening L_{eff}. The observed trend aligns well with the Hall measurement results in Fig. 2a, reinforcing the interpretation that HPDA enhances both carrier transport and contact characteristics. Therefore, the positive ΔL under HPDA reflects not only the increase in channel conductivity but also a structural transition toward more ohmic-like carrier injection, both of which are key to improving overall device performance.

Then, to calculate the field-effect mobility (μ_{FE}), the effective V_D ($V_{D.eff}$) and effective V_G ($V_{G.eff}$) were utilized from eqn (5)–(7), with corrections for R_C and L_{eff}.[14]

$$V_{D.eff} = V_D\left(1 - \frac{R_C}{R_{TOT}}\right) \quad (5)$$

$$V_{G.eff} = V_G\left(1 - \frac{R_C}{2R_{TOT}}\right) \quad (6)$$

$$\mu_{FE} = \frac{\partial I_D}{\partial V_{G.eff}} \frac{L_{eff}}{W \cdot C_{ox} \cdot V_{D.eff}} \quad (7)$$

As shown in Fig. 3d, the extracted μ_{FE} values for the O_2-annealed devices were 10.64 and 11.14 $cm^2\ V^{-1}\ s^{-1}$ at 300 °C and 350 °C, respectively, while the D_2-annealed devices yielded 9.89 and 10.78 $cm^2\ V^{-1}\ s^{-1}$ under the same conditions. The inset plots the V_G-dependent μ_{FE} behavior for the HPDA 350 °C device, confirming that the mobility remains relatively stable across the measured bias range. Despite clear improvements in I_{on} and reduced R_{on} under HPDA, the mean and variance of μ_{FE} show no substantial enhancement across the four conditions. This decoupling between current gain and mobility suggests that the observed electrical improvement is largely driven by a reduction in $R_C W$ rather than intrinsic channel transport.

AFM analysis supports this interpretation by revealing significant surface roughening in the HPDA-treated samples. Deuterium exposure disrupts the In–O–In bonding network by reducing In_2O_3, an essential part of the conduction path, into metallic indium clusters,[25] thereby fragmenting the continuous channel structure near the back surface. Significantly, SS is mainly controlled by electrostatic gate control and trap states at the buried Al_2O_3/IGZO interface, where the gate-induced percolation path forms in this back-gate structure, while the roughening and indium cluster formation are localized at the exposed back-channel surface. Thus, even if the back-channel surface becomes rougher, SS can be improved through interfacial trap passivation. This structural degradation increases carrier scattering and offsets the potential mobility gain expected from higher carrier density. Consistently, the nearly unchanged TLM-extracted R_{sh} can be explained as the result of competing effects, where the HPDA-driven increase in electron concentration is counteracted by roughness-induced scattering, resulting in a comparable R_{sh} across the different annealing conditions. In summary, while HPDA effectively lowers $R_C W$ and suppresses trap states to boost current performance, its benefit to mobility is limited by deuterium-induced disruption of the conduction path at the IGZO back-channel surface. Therefore, the dominant electrical improvement under

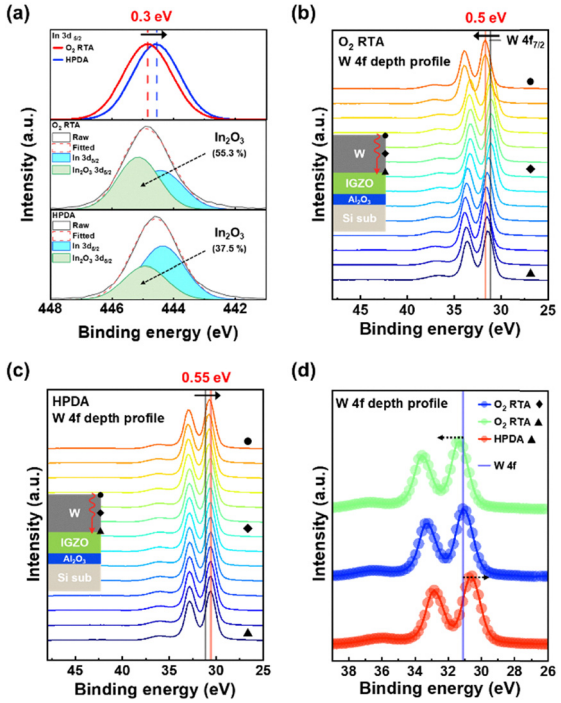

Fig. 4 XPS analysis of IGZO TFTs: (a) a comparison of the In 3d peaks for the devices treated by RTA and HPDA at the top, and the deconvolution of the In 3d peaks of the RTA-treated devices in the centre and HPDA-treated devices at the bottom; W 4f depth profile of the (b) RTA-treated devices and (c) HPDA-treated devices; (d) comparison of the W 4f peaks at the points of RTA ◆, ▲, and HPDA ▲.

HPDA is more consistently attributed to contact optimization together with improved Al_2O_3/IGZO interface electrostatics, rather than an intrinsic reduction in R_{sh}.

This highlights the critical need for surface engineering or passivation to preserve interfacial integrity and fully exploit the mobility potential of HPDA-treated oxide semiconductors.

To elucidate the origin of the limited μ_{FE} enhancement under HPDA despite reduced R_{on} and increased carrier concentration, Fig. 4a presents the In $3d_{5/2}$ core-level spectra at the IGZO back-channel surface. Compared to the O_2-annealed sample, which exhibits a peak at 444.8 eV, the HPDA-treated sample reveals a distinct downward shift to 444.5 eV, corresponding to a $\sim$0.3eV reduction in binding energy. This spectral evolution indicates that deuterium-induced chemical reduction transforms high-binding-energy In_2O_3 into low-binding-energy elemental indium.[46] To quantify this transformation, each spectrum was deconvoluted into In and In_2O_3 components. The O_2-annealed film exhibits 55.3% In_2O_3 content, whereas the HPDA film shows a significantly reduced fraction of 37.5%. This 18% decrease in In_2O_3 content suggests that deuterium introduces additional free carriers and alters the chemical backbone of the amorphous IGZO network. Given that In_2O_3 constitutes a primary percolative subnetwork for electron conduction in the amorphous phase, its local depletion results in a fragmented transport path. The formation of metallic indium clusters simultaneously introduces morphological discontinuities and local potential barriers that enhance carrier scattering, especially near the back-channel surface. Therefore, the observed stagnation in μ_{FE} despite favorable $R_C W$ and I_{on} improvements can be attributed to this chemically driven loss of conduction continuity. These results emphasize that, for HPDA to be effective in boosting both carrier concentration and transport efficiency, concurrent strategies for maintaining In_2O_3 chemical bonding at the back-channel surface must be implemented.

To further examine the interfacial evolution induced by the annealing ambient, Fig. 4b shows the XPS depth-profiled W $4f_{7/2}$ spectra of the O_2-annealed device. As the sputtering depth increases from the surface toward the W/IGZO interface, a characteristic shift in binding energy is observed. Specifically, the binding energy decreases gradually from the top electrode surface and then increases again near the metal/semiconductor interface, with a total upward shift of approximately 0.5 eV at the boundary. This upward shift suggests the presence of WO_x near the interface, likely formed during the O_2 RTA process. The W $4f_{7/2}$ peak of metallic W is generally found in the 31.2 to 31.8 eV range, whereas WO_x exhibits higher W $4f_{7/2}$ binding energies, typically in the 32.8 to 35.8 eV range, depending on the oxidation state.[46] As no such shift is observed in the central bulk of the W electrode, the oxidation is confined to the interfacial region. This localized chemical change at the contact interface reflects the diffusion of oxygen from the IGZO side during thermal annealing under O_2 ambient. The depth-dependent analysis of the W 4f peak indicates that the W/IGZO interface is chemically modified by O_2 annealing, potentially influencing the electrical and structural characteristics of the contact.

In contrast to the O_2-annealed sample, the HPDA-treated device exhibited no noticeable variation in the W $4f_{7/2}$ binding energy across the sputtering depth, as shown in Fig. 4c. Unlike the upward energy shift observed near the W/IGZO interface under O_2 annealing, the W 4f signal in the HPDA sample remained constant throughout the electrode depth. Instead, a uniform shift of approximately 0.55 eV was observed compared to the reference W peak, indicating a consistent modification of the W chemical state across the entire electrode.[47] Yu *et al.* found that higher annealing pressures greatly increase the depths of deuterium incorporation in dielectric films, which is consistent with this interpretation.[42] The uniform compositional change seen in the W electrode is therefore thought to be caused by a similar pressure-driven diffusion mechanism.[48] This result also suggests that no interfacial oxidation occurs under HPDA conditions and that the W electrode maintains chemical uniformity without depth-dependent changes. The absence of localized binding energy fluctuation implies that the W/IGZO contact remains chemically stable under D_2 ambient, in contrast to the interfacial oxidation observed in the O_2-annealed counterpart.

In summary, Fig. 4d compares the W 4f spectra at the center and W/IGZO interface for both annealing conditions. In the O_2-annealed sample, a distinct binding energy shift is observed at the interface, consistent with interfacial oxidation. In contrast, the HPDA-treated sample shows no such variation, confirming

the chemical uniformity of the W electrode. To further investigate these effects, we conducted DFT calculations. Fig. S6 presents the calculated partial density of states (PDOS) of tungsten before and after deuterium incorporation, together with the optimized atomic structures. In the pristine W structure (Fig. S6a), the PDOS is characterized by relatively localized states near the Fermi level, indicating that the electronic states are predominantly confined to tungsten d-orbitals with limited hybridization. By contrast, the introduction of deuterium (Fig. S6b) induces a substantial redistribution of electronic states across the entire energy window. The PDOS of W in the doped configuration exhibits broader and more delocalized features, while the distinct overlap between the W-states and the D-states suggests the formation of coherent hybridized orbitals. This hybridization can be interpreted as direct evidence of W–D chemical bond formation, which not only modifies the local electronic environment but also stabilizes the deuterium within the lattice.

A further important feature revealed by the PDOS is the shift in the d-band center (ε_d). In the pristine system, ε_d is located at −1.81 eV, whereas in the D-doped system it moves upward to −1.69 eV, *i.e.*, closer to the Fermi level. According to the d-band model, such an upward shift reflects an increase in the average energy of the W 5d electrons, leading to weakened binding strength of adsorbates relative to the undoped case. This theoretical prediction is consistent with the experimental XPS spectra shown in Fig. 4d, where the binding energy of the W 4f peaks shifts toward lower values upon deuterium doping. The combined DFT and experimental results therefore provide a coherent picture: incorporation of deuterium leads to electronic delocalization, hybridization between W and D orbitals, and an increase in the d-band center, all of which contribute to the experimentally observed reduction in binding energy.

Additionally, Fig. 5 illustrates the calculated oxygen diffusion pathways and corresponding diffusion barriers at the W/a-IGZO heterointerface with and without deuterium incorporation. In the W/a-IGZO structure in Fig. 5a and c, the oxygen atom migrates relatively easily for three diffusion pathways: path a to path c, exhibiting a comparatively low diffusion barrier. In contrast, once deuterium is introduced into the heterostructure, the corresponding diffusion barrier increases significantly, as shown in Fig. 5b and d. This increase can be attributed to the strong interaction between the deuterium atoms and lattice oxygen, which effectively reduces the number of available weakly bonded oxygen species. As a result, oxygen migration toward the W layer can be substantially hindered by deuterium incorporation.

The higher barrier observed in the D-doped heterostructure suggests that deuterium incorporation plays a crucial role in suppressing oxygen transport across the interface. Given that oxygen diffusion into the W electrode is a primary origin of interfacial WO_x formation, the elevated barrier implies that D doping provides a kinetic protection mechanism against interfacial oxidation. This mechanistic picture is consistent with our experimental findings that high-pressure deuterium annealing stabilizes the W/IGZO interface by reducing interfacial trap states. In other words, deuterium atoms passivate electronic defects in the oxide materials and chemically and kinetically inhibit oxygen diffusion toward the W layer, thereby suppressing the undesirable formation of resistive WO_x phases. As a result, these findings highlight that deuterium plays two beneficial roles: it electronically passivates defect states while simultaneously suppressing oxygen migration pathways, thereby ensuring both chemical and electrical stability of the W/a-IGZO heterostructures.

Finally, the a-IGZO TFTs in different annealing ambients were evaluated for gate-bias stress reliability. Fig. 6a and b show the findings of the positive bias stress (PBS) and negative bias stress (NBS), respectively, with V_D maintained at 1 V, while the stress was applied at intervals of 500 s up to 5000 s (V_G = 7 V for PBS and V_G = −7 V for NBS). Under all annealing conditions, both PBS and NBS induced a negative shift in V_T, indicating that donor-like charge generation or positive-charge accumulation outweighs the opposing electron-trapping process. To clarify the mechanism under each stress condition, the bulk-related and interface-related contributions can be considered separately.

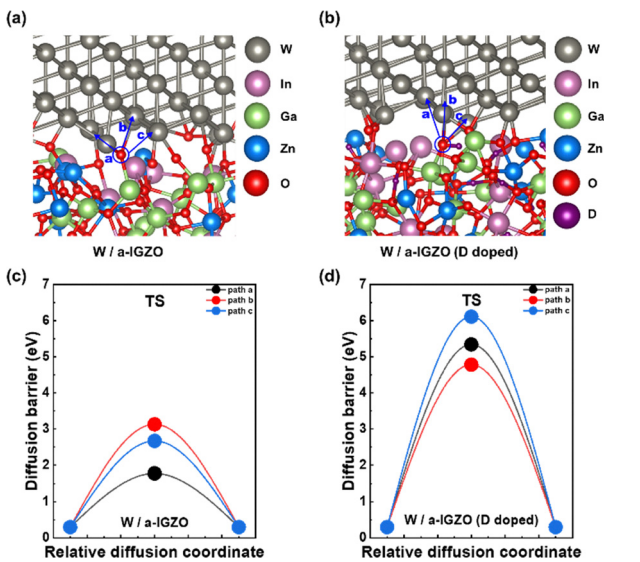

Fig. 5 (a and b) Oxygen diffusion pathways for (a) W/a-IGZO and (b) W/a-IGZO (D doped) heterostructures. Color scheme: grey, W; pink, In; light-green, Ga; blue, Zn; red, O; purple, D. (c and d) Diffusion barrier of oxygen migration for (c) W/a-IGZO and (d) W/a-IGZO (D doped). The pathway a to c is labeled in (a) and (b).

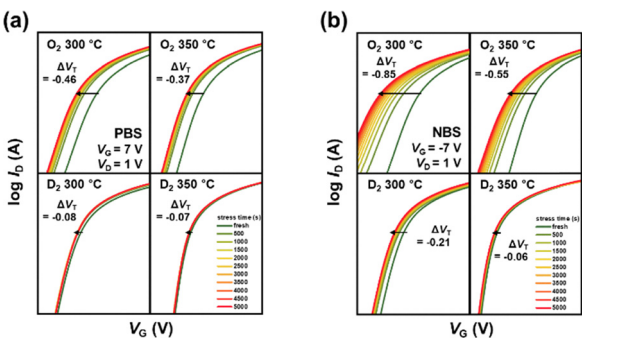

Fig. 6 Transfer characteristics of the a-IGZO TFTs during (a) positive bias stress and (b) negative bias stress at V_D = 0.05 V.

Under PBS, the negative V_T shift is likely associated mainly with the ionization of oxygen-related defect sites in the IGZO bulk, which can increase the density of donor-like states and free electrons. In this case, the opposing positive V_T shift caused by electron trapping at the GI/IGZO interface is considered to be a secondary contribution.[49] Under NBS, the negative V_T shift can be understood in terms of two concurrent contributions, namely field-assisted migration of positively charged oxygen-related defect species toward the GI/IGZO interface and hole trapping at the interface. Among these, defect migration may play the more dominant role, as the resulting positive-charge accumulation near the interface is consistent with enhanced electron induction in the channel. The improved bias-stress stability observed after HPDA may be understood in direct relation to these pathways. Passivation of oxygen-related defect sites in the IGZO bulk is likely associated with suppression of the defect-ionization process under PBS, while reduction of interfacial trap states at the Al_2O_3/IGZO interface may reduce the contributions from charge trapping and field-assisted defect accumulation under NBS. Taken together, these results suggest that HPDA mitigates bias-stress instability by weakening both the bulk-related contribution under PBS and the interface-coupled contribution under NBS, leading to a smaller V_T shift than that observed after O_2 RTA.

Fig. 7 schematically summarizes the proposed mechanisms by which HPDA influences the a-IGZO TFT stack. Upon exposure to high-pressure deuterium, D atoms diffuse into both the IGZO bulk and its interfaces, where they engage in multiple chemical pathways. In the IGZO matrix, deuterium likely bonds with lattice oxygen or oxygen vacancies, contributing additional free carriers while suppressing defect states. At the back-channel surface, the formation of In-rich clusters is accompanied by roughening of the local surface, suggesting partial reduction of In_2O_3. Simultaneously, at the gate insulator interface, deuterium is presumed to neutralize dangling bonds and reduce trap densities, resulting in enhanced electrostatic gate control. At the contact region, D incorporation leads to the formation of W–D bonds at the W/IGZO interface, chemically stabilizing the electrode and mitigating oxygen-induced interfacial oxidation. This structural preservation is expected to

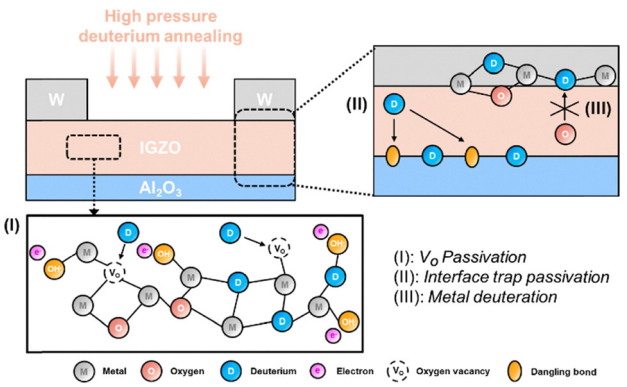

Fig. 7 Proposed mechanism of the IGZO TFTs after the HPDA process.

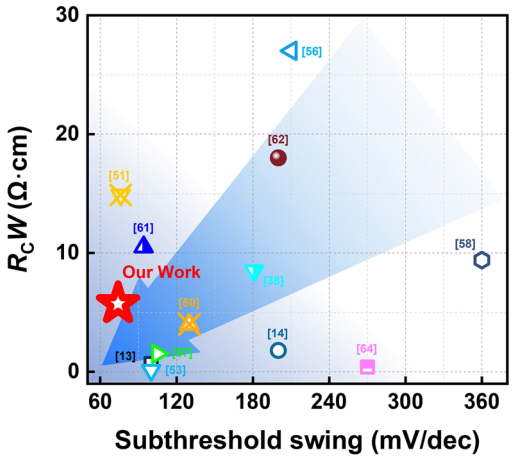

Fig. 8 Comparison of our work and various references: R_CW *vs.* SS.

suppress R_C. While each effect is localized, their combination suggests that HPDA enables a noticeable enhancement of the device characteristics, offering a viable post-metallization treatment for BEOL-compatible TFT integration.

Fig. 8 benchmarks the R_CW performance of this work against previously reported IGZO TFTs, highlighting the unique advantage of the HPDA-treated W contact. Table S1 provides a comparison of major device parameters from previous studies, enabling a clear overview of the performance differences in the fabricated TFTs.[50–66] The proposed process achieves one of the lowest R_CW values (5.74 Ω cm at 350 °C) among reported BEOL-compatible devices, outperforming even noble-metal-based contacts such as Au, which often suffer from CMOS-integration limitations. Notably, previous studies on W-contact focused on factors such as IGZO thickness[50] or interlayer engineering,[51] but lacked a systematic assessment of annealing effects on R_CW. By clearly linking R_CW trends to annealing ambient and temperature, this study demonstrates that precise thermal activation under a deuterium-rich environment is essential for minimizing interfacial resistance while preserving CMOS compatibility. This positions HPDA as a reliable post-metallization strategy for scalable oxide device integration in monolithic 3D architectures.

4. Conclusions

In this work, the effects of O_2 RTA and HPDA at 300 °C and 350 °C were systematically investigated in BEOL-compatible a-IGZO TFTs employing W electrodes. Among the investigated conditions, HPDA at 350 °C produced the most favorable device characteristics, reducing D_{it} to 8.43 × 10^{11} cm^{-2} eV^{-1} and improving SS to 75 mV dec^{-1}, while also lowering R_CW to 5.74 Ω cm. These results indicate that HPDA is more effective than O_2 RTA in improving both the Al_2O_3/IGZO dielectric interface and the W/IGZO contact interface. The improved electrical characteristics, together with the reduced W 4f binding-energy shift and suppressed WO_x formation observed by XPS, consistently suggest that deuterium plays an important role in suppressing interfacial oxidation and enhancing contact

stability. DFT calculations further support this interpretation by showing that deuterium incorporation can stabilize the W/IGZO interface and increase the oxygen diffusion barrier. Taken together, these results demonstrate that HPDA is an effective route for improving electrostatic control and contact characteristics in BEOL-compatible oxide TFTs and provides a useful strategy for low-temperature oxide-semiconductor integration in advanced BEOL platforms.

Author contributions

Woosub Byun: writing – original draft, investigation, formal analysis, data curation, visualization. Tae-Hyun Kil: formal analysis, visualization, resources, writing – review & editing. Bong Ho Kim: formal analysis, visualization, resources, writing – review & editing. Yunseok Kim: formal analysis, visualization, writing. Hwanyeol Park: conceptualization, writing – review & editing. Jun-Young Park: conceptualization, writing – review & editing. Dae-Myeong Geum: conceptualization, supervision, project administration, resources, writing – review & editing.

Conflicts of interest

There are no conflicts of interest to declare.

Data availability

The data that support this article are available from the corresponding author upon reasonable request.

References cited in the supplementary information (SI) have been listed in the article's reference list. Supplementary information is available. See DOI: https://doi.org/10.1039/d6tc00357e.

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