Journal of Materials Chemistry C

ROYAL SOCIETY OF CHEMISTRY

REVIEW

View Article Online
View Journal

Cite this: DOI: 10.1039/d6tc00317f

Recent progress in alternative metals for advanced interconnects

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With the continued downscaling of semiconductor devices such as transistors and memory devices, metal interconnects have become increasingly critical for transmitting electrical signals required for data processing. Recently, metal interconnects have played a critical role in enhancing computing performance, particularly through advanced packaging technologies that accelerate the progress of artificial intelligence (AI) computing. Copper (Cu) is widely used as an interconnect material due to its low bulk resistivity of 1.68 μΩ cm. However, as the physical dimensions of interconnects shrink below 10 nm, the resistivity of Cu increases significantly, a phenomenon known as the "resistivity size effect." The increasing resistance of interconnects leads to resistance–capacitance (RC) delays, which decrease the operation speed of transistors and memory devices. Consequently, the rising resistance of metal interconnects at small dimensions hampers the progress of fast, efficient AI computing, where data volumes are growing exponentially. This increase in resistivity originates from enhanced electron scattering at surfaces and grain boundaries at reduced physical dimensions. To overcome the resistivity size effect, metals with short electron mean free paths (EMFPs) are required to reduce scattering. Therefore, the exploration of alternative interconnect materials is essential. In this review, we address the requirements for advanced interconnect materials and compare the properties of potential candidates for reducing RC delays. We also summarize the challenges in developing alternative metals and fabrication methods, categorized into single-elementary metals, binary intermetallic compounds, ternary metals, and emerging topological semimetals. Finally, we provide an outlook on the development of next-generation interconnect materials.

Received 30th January 2026,
Accepted 18th March 2026

DOI: 10.1039/d6tc00317f

rsc.li/materials-c

1. Introduction

With the evolution of artificial intelligence (AI) based computing, the demand for efficient processing of massive volumes of data has increased significantly.[1–5] This trend necessitates faster

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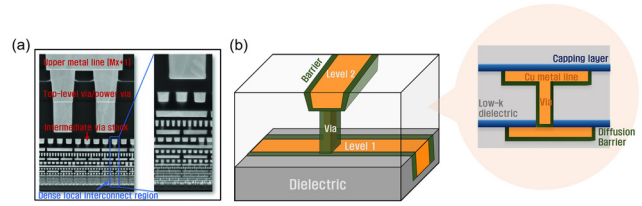

Fig. 1 Interconnect architectures in advanced and vertically stacked IC systems. (a) Cross-sectional view of an advanced chip showing FEOL transistors and multilevel BEOL interconnects, where local interconnects connect devices and global interconnects route signals; RC delay in the multilevel interconnect stack becomes a key bottleneck at advanced nodes. Reprinted with permission from ref. 19, Copyright 2022, IEEE. (b) Level 1 and 2 interconnect schematic illustrating a Cu line and *via* in a low-*k* dielectric with diffusion barrier and capping layers.

computing speeds, enhanced accuracy, and higher throughput, thereby driving innovative advancements in semiconductor device performance.[4,6,7] For decades, Moore's law has guided the semiconductor industry, enabling continuous improvements in the areal density of complementary metal–oxide–semiconductor (CMOS) transistors.[8–10] However, lateral transistor scaling based on shorter channels has slowed and is approaching its physical limits. Moreover, interconnects that transmit electrical signals among these high-density transistors introduce resistance–capacitance (RC) delay, which has emerged as a major bottleneck for further advances in computing performance.[11–13] Consequently, overall signal delay is now governed primarily by the interconnect RC delay rather than by the switching speed of transistors. The delay is expected to pose an even more severe bottleneck in vertically stacked multi-chip systems (*i.e.*, three-dimensional stacking), which have been recently introduced through advanced packaging technologies. Semiconductor devices using vertical stacking architectures, such as high-bandwidth memory (HBM), employ through-silicon vias (TSVs) to connect vertically stacked chips, enabling parallel and multiple data processing.[14–16]

Integrated circuit (IC) manufacturing is conventionally divided into front-end-of-line (FEOL), middle-of-line (MOL), and back-end-of-line (BEOL) processes.[17,18] Fig. 1a shows a cross-section of an advanced chip with FEOL-integrated transistors.[19] Multiple overlying metal layers contain local interconnects for transistor coupling and global interconnects for signal distribution. The transistor performance has been enhanced through channel-length scaling and the introduction of advanced gate dielectrics.[20–22] However, interconnects comprising multilevel layers and interlayer dielectrics largely determine RC delay which has become a major bottleneck at advanced technology nodes.[23] Fig. 1b illustrates the interconnect configuration between levels 1 and 2, showing a copper (Cu) interconnect with diffusion barrier and capping layers.

Reducing RC delay requires lowering interconnect resistance and capacitance.[24–27] While capacitance reduction has been extensively addressed through the use of low-*k* dielectrics and air-gap integration, interconnect resistance has emerged as the more critical challenge in advanced technology nodes.[28–30] In early generations of ICs, aluminum (Al) served as the interconnect metal because of its relatively low resistivity (ρ_0) and excellent process compatibility.[31,32] However, with continued device scaling, Al interconnects suffered from increased delay and severe electromigration, which ultimately limited their reliability.[31,33] To overcome these issues, Cu was introduced into manufacturing by IBM in 1997, and it rapidly replaced Al as the industry standard due to its lower bulk resistivity and superior conductivity.[30,34–36]

Meanwhile, interconnect reliability remains a decisive factor in nanoscale semiconductor devices. Cu exhibits superior electromigration resistance compared to Al, and electromigration and diffusion persist as primary failure modes as linewidths are scaled down to the nanometer regime.[31,37] Under high current densities, Cu interconnects undergo atomic transport, leading to the formation of voids in depletion regions and hillocks in accumulation sites, which can result in open-circuit failures or leakage paths. Consequently, diffusion barriers and

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liners such as Ta/TaN and TiN have been introduced to suppress atomic migration; however, these layers also reduce the effective volume of Cu, thereby increasing the overall resistance.[38,39]

More importantly, the resistivity of Cu lines increases significantly at the scaled dimensions required for technology nodes beyond 10 nm. Fig. 2a and b summarize how Cu resistivity ρ_0 depends on thickness and microstructure.[40] In Fig. 2a, resistivity is plotted against Cu layer thickness, where filled symbols represent room-temperature measurements and open symbols correspond to data acquired at 4.2 K. The legend classifies the Cu datasets according to processing conditions, such as different annealing temperatures and the presence of Ta interlayers; the resulting offsets indicate that variations in microstructure can significantly shift ρ_0 at comparable thicknesses. Fig. 2b replots the same dataset as ρ_0 *versus* grain size (g), revealing that much of the scatter observed in Fig. 2a collapses into a clear grain-size-dependent trend. This behavior indicates that grain boundary scattering largely governs sample-to-sample variations in resistivity at a given thickness. Finally, Fig. 2c compares single-crystal (SC), large-grain (LG), and small-grain (SG) Cu at 298 K, demonstrating that improved crystallinity (*i.e.*, larger grain size) shifts the resistivity scaling curve downward. However, ρ_0 continues to increase at reduced thicknesses and rises much more rapidly below 50 nm—a phenomenon known as the resistivity size effect, in which surface and interface scattering become increasingly dominant.[41,42]

To mitigate the resistivity size effect, alternative interconnect materials must possess a shorter electron mean free path (EMFP) than Cu. Specifically, the EMFP of Cu is approximately 39 nm; when feature sizes are scaled below this value—and particularly below 10 nm—this relatively long EMFP leads to significantly enhanced scattering.[43,44] Additionally, ideal candidates should not require liner or barrier layers, which reduce the volume fraction of metal lines.[13] Finally, these materials must maintain compatibility with existing semiconductor device fabrication processes.

In this review, we provide a comprehensive overview of the fundamental properties and nanoscale electron transport characteristics of various metal candidates. These materials are categorized into single-element metals, binary alloys, and ternary systems. We compare their intrinsic material properties and integration-related aspects—including barrier/liner scaling, process compatibility, and reliability—to identify viable interconnect materials for future technology nodes. Ultimately, this review aims to clarify current limitations and outline future directions for interconnect technologies in next-generation semiconductor devices.

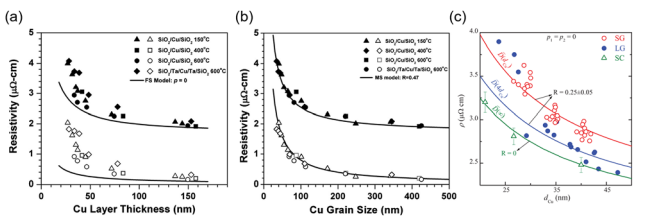

Fig. 2 Cu resistivity scaling governed by thickness and microstructure. (a) ρ *versus* Cu thickness for SiO_2/Cu/SiO_2 under different processing conditions (symbols), with FS fits (p = 0). (b) The same data replotted as ρ *versus* grain size, highlighting a grain boundary-controlled trend with MS fits (R = 0.47). Reprinted with permission from ref. 40. Copyright 2010, American Physical Society. (c) ρ Scaling at 298 K for small grain, large grain, and single crystal Cu, showing reduced ρ with improved crystallinity but a remaining rise at small dimensions. Reprinted with permission from ref. 41. Copyright 2011, American Physical Society.

2. Resistivity size effect

2.1 Matthiessen's rule

The electrical resistivity of metals originates from multiple scattering mechanisms; therefore, isolating their individual contributions is critical for evaluating the performance and reliability of nanoscale devices. Matthiessen's rule[45] is commonly employed to represent total resistivity (ρ_{total}) as a linear combination of independent bulk scattering terms:

$$\rho_{total}(T) = \rho_{ph}(T) + \rho_{imp} + \rho_{def} \quad (1)$$

The phonon contribution, ρ_{ph}, increases nearly linearly with temperature and dominates at elevated temperatures. In contrast, the impurity-related resistivity (ρ_{imp}) and the defect-related resistivity (ρ_{def}), arising from structural defects such as dislocations or vacancies, remain essentially temperature-independent. These components constitute background terms that become relatively more important at low temperatures. While this additive form provides a reasonable description of bulk metals, it is insufficient when the conductor dimensions are comparable to the EMFP, as additional scattering processes contribute significantly. Under such conditions, the probability of electron reflection at grain boundaries and diffuse scattering at surfaces increases dramatically. Consequently, a size-dependent term must be incorporated into the total resistivity to account for these nanoscale phenomena.

Fig. 3 illustrates the physical picture of electron scattering as interconnect dimensions and grain sizes decrease, highlighting how transport properties are governed by the EMFP. In Fig. 3a, electron–phonon scattering is shown for materials with long and short EMFPs, representing the intrinsic scattering behavior of the bulk materials. When the EMFP is longer than the grain size, electron–phonon scattering dominates and is the primary factor determining the metal resistivity. However, when the EMFP is comparable to or smaller than the grain size, electrons also experience significant scattering at grain boundaries and surfaces. Fig. 3b illustrates the electron scatterings for large and small EMFPs. When the intrinsic EMFP is comparable to or larger than the grain size, significant additional scattering occurs at grain boundaries and surfaces. In metals with a large EMFP (like Cu), this long path is not preserved; instead, the effective EMFP is severely truncated by frequent encounters with grain boundaries and interfaces. This is represented by the shortened green arrows, indicating that transport has become

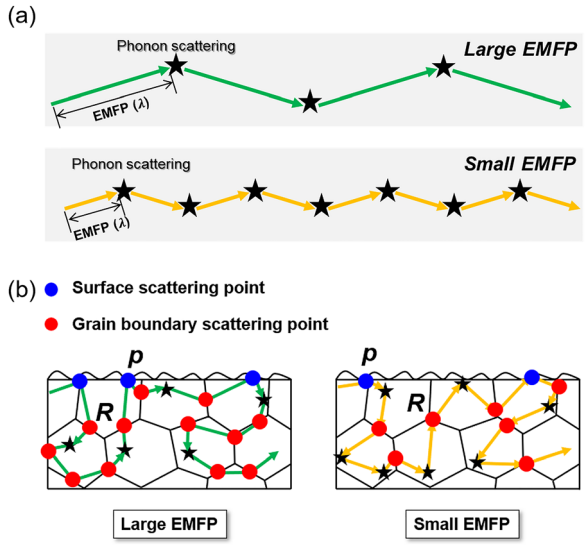

Fig. 3 Schematic illustration of how electron mean free path (EMFP, λ) governs resistivity scaling. (a) In bulk transport, a larger EMFP implies fewer phonon scattering events over a given distance, corresponding to lower bulk resistivity, while a smaller EMFP indicates more frequent bulk scattering. (b) Under dimensional scaling, when the film thickness and grain size approach or fall below λ, electrons are more likely to encounter surfaces (specularity p) and grain boundaries (reflection R) before bulk scattering, making resistivity strongly dependent on interfaces and microstructures; materials with a shorter EMFP exhibit a smaller incremental penalty from additional boundary scattering, leading to weaker resistivity degradation.

highly sensitive to the microstructure, which drives a sharp increase in resistivity.

Conversely, in metals where the intrinsic EMFP is already smaller than the grain size, the electron path is primarily limited by bulk scattering from the start. While additional scattering at grain boundaries and surfaces still occurs, the length of the small EMFP is largely maintained (represented by the yellow arrows). Consequently, these additional scattering events do not increase the resistivity as substantially as they do in the large-EMFP case. Therefore, metals with long EMFPs lose their low-resistivity advantage at small dimensions, whereas metals with small EMFPs exhibit a much weaker 'size effect'. This demonstrates that alternative materials for future interconnects must possess a short intrinsic EMFP.

As a result, the product of bulk resistivity (ρ_0) and EMFP (λ) has been proposed as a useful figure of merit (FOM) for assessing interconnect materials under aggressive scaling, because it captures how strongly a material is expected to suffer from size driven scattering. These scaling-dependent electron scattering behaviors have been analysed using semiclassical transport frameworks, such as the Fuchs–Sondheimer (FS) surface scattering model and the Mayadas–Shatzkes (MS) grain boundary scattering model, which extend Matthiessen's rule to capture size-dependent resistivity.[42,46]

2.2 Mayadas–Shatzkes (MS) and Fuchs–Sondheimer (FS) models

The resistivity increase of metallic conductors at reduced dimensions can be analysed within the semiclassical Boltzmann transport equation (BTE), with boundary effects incorporated through the FS and MS models. The FS model accounts for surface scattering *via* explicit boundary conditions, while the MS model describes grain boundary scattering using a probabilistic approach. The two models form complementary descriptions of the dominant scattering factors in thin metallic films and interconnects.[42,46,47]

In the FS model, the steady-state condition ($\partial f/\partial t = 0$) and the relaxation time approximation are applied to the BTE. Since the electric field drives current along the in-plane direction, a spatial variation is considered only across the film thickness. At the two film surfaces $s = 0$ and $s = a$, the incident and reflected electron distribution functions are related through the specularity parameter:

$$C^{+}(v_z, 0) = pC^{-}(-v_z, 0) \quad (2)$$

$$C^{-}(v_z, a) = pC^{+}(-v_z, a) \quad (3)$$

where $C = f - f_0$ is the deviation of the distribution function from equilibrium. The parameter ranges from 0 to 1, with $p = 1$ denoting perfectly specular reflection and $p = 0$ completely diffuse scattering. Solving the reduced BTE under this boundary condition yields the FS resistivity expression:

$$\rho_{FS} = \rho_0 \left[1 - \left(\frac{3\lambda}{2d}\right)(1-p)\int_1^{\infty}\left(\frac{1}{t^3} - \frac{1}{t^5}\right)\frac{1-\exp(-kt)}{1-p\exp(-kt)}\mathrm{d}t\right]^{-1} \quad (4)$$

where $k = d/(\lambda t)$, λ is the bulk EMFP, and d is the film thickness. The effective value of p is governed by the interfacial structure and chemistry, where smoother interfaces favor more specular reflection, whereas roughness, disorder, or strong interfacial electronic coupling randomizes electron momentum and suppresses p.[48]

The MS model captures grain boundary scattering by considering each boundary as a partially reflecting barrier with reflection probability (R) and transmission probability $1 - R$. Within the relaxation time approximation, the combined scattering rate is expressed as follows:

$$\frac{1}{\tau^*} = \frac{1}{\tau} + 2F(k \cdot \hat{n}) \quad (5)$$

where τ is the background relaxation time, F is the additional transition rate introduced by the boundaries, k is the electron wavevector, and $\hat{n}$ is the boundary normal. Introducing the dimensionless parameter,

$$\alpha = \frac{\lambda}{g}\frac{R}{1-R} \quad (6)$$

With λ being the bulk EMFP and g being the average grain size, the resulting resistivity relative to the bulk is given by:

$$p\frac{\rho}{\rho_0} = \left[1 - \frac{3}{2}\alpha + 3\alpha^2 - 3\alpha^3 \ln\left(1 + \frac{1}{\alpha}\right)^{-1}\right] \quad (7)$$

The reflection coefficient R depends strongly on grain-boundary character; for instance, low-energy coherent boundaries tend to exhibit lower reflection, whereas random

high-angle boundaries act as stronger scattering centers due to larger potential steps and local charge accumulation. Such scattering can be mitigated through grain-boundary engineering, including dopant or impurity segregation that reduces the effective potential barrier and suppresses reflection.[49,50] Since both surface and grain-boundary scattering coexist in real materials, the total resistivity is typically expressed by considering these mechanisms concurrently. A compact form commonly used for scaling analysis is based on Matthiessen's rule:

$$\rho_{tot} \approx \rho_0 + \Delta\rho_{FS} + \Delta\rho_{MS} \quad (8)$$

where $\Delta\rho_{FS}$ and $\Delta\rho_{MS}$ denote the excess resistivity contributions from surface and grain boundary scattering, respectively. This expression serves a convenient basis for quantitative modelling, while more comprehensive formulations have been developed to incorporate both effects simultaneously and have been demonstrated in previous studies.[41,51]

It is worth noting that p and R are not strictly intrinsic constants of a given metal; instead, they depend strongly on interfacial morphology, microstructure, and the properties of surrounding materials. In contrast, the EMFP is primarily determined by the bulk electronic structure and is generally regarded as the fundamental intrinsic parameter controlling the extent of resistivity scaling.

2.3 Figure of merit (FOM)

Due to the resistivity size effect, the use of the $\rho_0\lambda$ product has been established as a universal figure of merit (FOM) for interconnect evaluation. Resistivity variations with decreasing feature size have been analysed using the FS and MS models, establishing $\rho_0\lambda$ as a practical metric for assessing interconnect performance. Since both surface and grain boundary scattering contributions scale with $\rho_0\lambda$, this product provides a convenient way to quantify the dimensional dependence of resistivity in confined geometries and serves as a useful screening criterion for alternative conductors in scaled interconnects.

Fig. 4 categorizes candidate interconnect materials for evaluating their FOM values. The candidates are organized into four groups that are referenced throughout this review. The single-element metal group includes transition and noble metals that have been widely explored as near-term replacements. The binary system group encompasses both solid-solution alloys and ordered intermetallic compounds, where the composition can be tuned to adjust $\rho_0\lambda$, while integration constraints such as diffusion, thermal stability, and patterning are simultaneously evaluated.[52,53] The ternary system group includes compound conductors, such as MAX phases and delafossite ABO_2 materials, where the composition and crystal structure provide additional degrees of freedom for optimizing transport properties.[54,55] Finally, the emerging concept group includes materials at an early stage of interconnect exploration; these are discussed primarily in terms of their electronic transport characteristics and are included to highlight potential future research directions rather than near-term integration.[56]

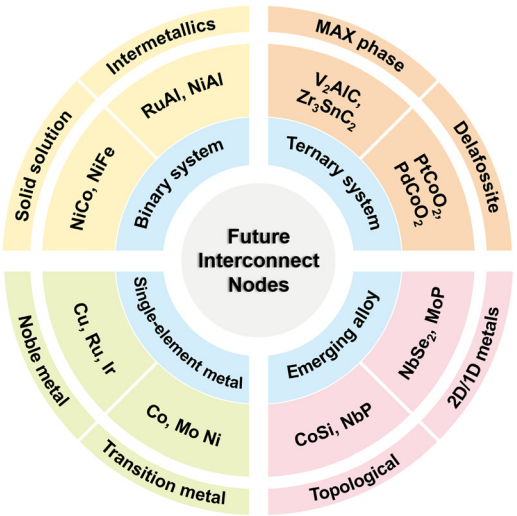

Fig. 4 Conceptual map categorizing candidate interconnect materials for future interconnect nodes prior to FOM-based screening, highlighting the transition from conventional conductors to emerging alternatives at reduced dimensions.

Table 1 Representative room-temperature values of bulk resistivity ρ_0, EMFP (λ), and for selected elemental metals. Adapted with permission from ref. 43. Copyright 2016, AIP Publishing. Adapted with permission from ref. 57. Copyright 2017, AIP Publishing. Adapted with permission from ref. 58. Copyright 2020, AIP Publishing. Adapted with permission from ref. 59. Copyright 2005, IEEE

Element	Crystal structures	$\rho_{0,rt}$ ($\mu\Omega$ cm)	λ_{rt} (nm)	$\lambda \times \rho_0$ (10^{-16} Ω m^2)
Cu[43]	fcc	1.678	39.9	6.70
Al[43]	fcc	2.650	18.9	5.01
Rh[43]	fcc	4.7	6.88	3.23
Ir[43]	fcc	5.2	7.09	3.69
Ni[43]	fcc	6.93	5.87	4.07
Pt	fcc	10.6[57]	2.8[57]	3.4[58]
Co[43]	hcp	6.2	11.8/7.77	7.31/4.82
Ru[43]	hcp	7.8	6.59/4.88	5.14/3.81
Os[43]	hcp	8.9	7.20/4.87	6.41/4.33
Mo[43]	bcc	5.34	11.2	5.99
Nb	bcc	14.75[59]	2.36[58]	3.56[59]

Representative values of ρ_0, λ, and their product are summarized in Table 1 for various materials.[43,57] Table 1 allows for comparison of bulk resistivity and the corresponding transport length scale across candidate conductors.[58,59] Cu exhibits low bulk resistivity but a long EMFP of approximately 39 nm, resulting in a relatively large $\rho_0\lambda$ and strong sensitivity of resistivity to dimensional confinement.[43] In contrast, ruthenium (Ru) and iridium (Ir), with EMFPs of approximately 6 nm and 8 nm, respectively, have higher ρ_0 values but significantly smaller $\rho_0\lambda$ values. This translates to a much more gradual resistivity increase under scaling. These comparisons underscore that bulk resistivity alone is insufficient for describing transport at the nanoscale; the EMFP is a critical parameter for evaluating conductor performance.

As shown in Fig. 2, the resistivity of Cu increases significantly as the film thickness decreases. The influence of the

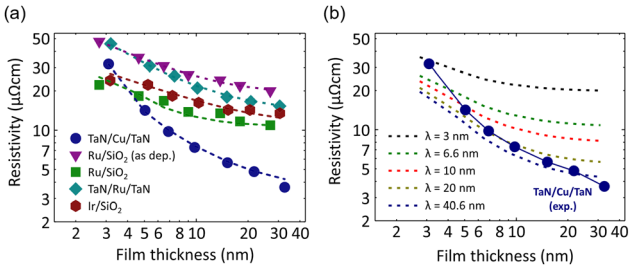

Fig. 5 EMFP driven crossover in thickness dependent resistivity scaling. (a) ρ_0 *versus* film thickness for Cu, Ru, and Ir stacks, showing weaker scaling in Ru and Ir and a crossover at ultrathin thicknesses. (b) TaN/Cu/TaN data compared with model curves for different EMFPs (λ), where a shorter λ gives a smaller scaling induced resistivity increase at a fixed $\rho_0\lambda$. Reprinted with permission from ref. 57. Copyright 2017, AIP Publishing.

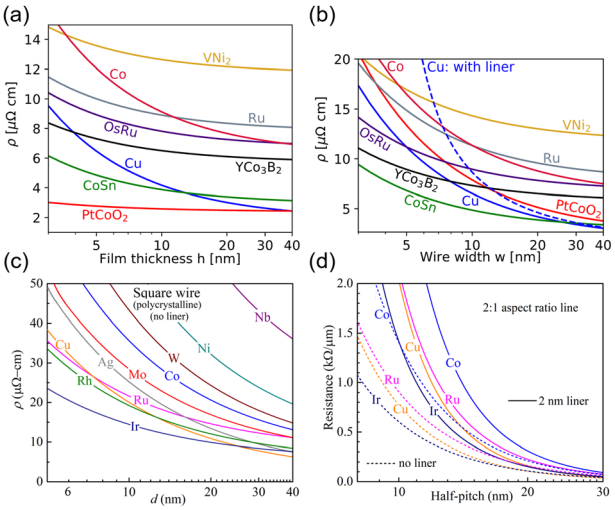

Fig. 6 Computational screening of interconnect resistivity scaling beyond $\rho_0\lambda$. (a) Film resistivity projections incorporating an anisotropic electron structure through r_{film}, highlighting deviations from the simple $\rho_0\lambda$ trend. (b) Wire resistivity projections using r_{wire}, comparing scaling behaviors across candidate metals relative to Cu with a liner. (c) Predicted resistivity scaling of elemental metals as a function of dimension. (d) Geometrical scaling penalty from barrier/liner integration, showing the reduction of effective conducting cross-section at a small half-pitch. (a) and (b) Reprinted with permission from ref. 61. Copyright 2022, American Physical Society. (c) and (d) Reprinted with permission from ref. 58. Copyright 2020, AIP Publishing.

EMFP becomes particularly evident when the thickness-dependent scaling of Cu is compared with that of Ru and Ir.[57,58] Their shorter EMFPs lead to a much weaker thickness dependence of resistivity compared to Cu. The resistivities of Ru and Ir reach comparable values to Cu and can eventually fall below it when the thickness is reduced to approximately 5 nm (Fig. 5a).[57] Fig. 5b supports this crossover by overlaying the experimental TaN/Cu/TaN trend with model curves calculated for varying EMFP values; it demonstrates that a shorter EMFP results in a significantly smaller scaling-induced resistivity increase.[60] In this model, λ is varied while the product $\rho_0\lambda$ is held constant; consequently, the baseline resistivity shifts upward because a smaller λ implies a larger ρ_0 under this constraint. This crossover indicates that metals with intrinsically small λ, and thus small $\rho_0\lambda$, can exhibit lower resistivity at nanoscale dimensions.

Computational studies have extensively extended the use of the product $\rho_0\lambda$ values to explore interconnect materials based on density functional theory (DFT) across a broad set of candidate materials.[58,61] DFT calculations have predicted resistivity ρ_0 and the product of resistivity and electron mean free path $\rho_0\lambda$ for both single-element metals and compounds across various film thicknesses. Comparative screening across elemental metals summarizes which conductors are expected to retain low resistivity at reduced dimensions.[61] Fig. 6a shows the predicted resistivity (based on DFT calculations) as a function of film thickness, highlighting the characteristic increase in resistivity as the thickness decreases. Most materials exhibit a significant increase in resistivity below 10 nm. However, $PtCoO_2$ displays an extremely weak size effect that outperforms Cu, making it a promising candidate for thin-film applications. This behavior is attributed to the large EMFP of $PtCoO_2$ ($\sim$110 nm), which leads to relatively weak electron scattering when the grain size is large. However, this advantage does not extend to wire geometries, where additional sidewall scattering can substantially alter the scaling behavior. In this regard, comparing the FOM for thin films does not fully capture the electrical behavior at all small-scale geometries.[61]

To address the limitations of thin-film FOM comparisons, resistivity scaling coefficients r_{film} and r_{wire} were recently introduced as geometry-specific descriptors. In this framework, the conventional FOM $\rho_0\lambda$ is replaced by r_{film} for films and by r_{wire} for wires, where r_{wire} additionally accounts for scattering from sidewalls across both width and height surface normals.[61] Accordingly, Fig. 6b presents resistivity as a function of wire width w, emphasizing that wire scaling can deviate significantly from film scaling because electrons encounter multiple boundary orientations rather than just the top and bottom surfaces.[61]

Fig. 6c and d further highlight realistic predictions of resistivity variations as a function of dimension for both square wires and lines with a 2 : 1 aspect ratio.[58] In Fig. 6d, the dashed and solid curves distinguish between two specific scenarios: cases without a liner and those with a finite liner thickness. In the latter case, the presence of a liner reduces the available conductor volume (the effective cross-sectional area), thereby increasing the overall resistance. This distinction is critical for evaluating the practical performance of interconnect materials in highly scaled integrated circuits. Table 2 applies these descriptors to highlight how electron transport characteristics vary according to specific device geometries.[61,62]

3. Conductor candidates

3.1 Single-element metals

Single-element metals—including noble metals, such as Ru, Ir, and Rh, as well as transition metals like Co and Mo—have been extensively investigated as prospective replacements for Cu in advanced interconnect technologies (Table 1).[43,57]

Table 2 Calculated transport parameters for selected intermetallic compounds and oxides, including $\rho_0\lambda$, r_{film}, and r_{wire}. Adapted with permission from ref. 61. Copyright 2022, American Physical Society. Adapted with permission.[62] Copyright 2023, AIP Publishing

Material	ν_F [10^6 m s^{-1}]	λ [nm]	ρ_0 [μΩ cm]	$\rho_0\lambda$ [$\times10^{-16}$ Ω m^2]	r_{film} [eV per atom]	r_{wire}	Cohesive energy
Cu[61]	1.2	34.8	1.8	6.7	6.1	6.2	3.4
Cr_2AlC[61]	0.3	5.6	14.5	8.0	3.4	6.5	4.9
IrRu[61]	0.7	6.2	8.3	5.1	3.3	5.1	8.4
CuPt[61]	0.8	11.2	6.1	6.8	3.3	5.1	4.6
$NiIr_3$[61]	0.4	3.4	10.1	4.8	3.2	3.5	6.5
VPt_2[61]	0.5	5.4	8.1	4.9	3.0	3.8	5.8
IrRh[61]	0.7	5.8	6.6	3.6	3.0	3.5	6.4
OsRu[61]	0.7	6.5	6.5	4.2	3.0	3.0	7.4
$MoNi_2$[61]	0.4	5.7	12.8	5.7	2.8	3.5	5.2
$CrNi_2$[61]	0.3	2.9	25.9	4.8	2.7	3.4	4.4
CoSn[61]	0.6	19.6	2.9	5.9	2.6	2.6	4.4
VNi_2[61]	0.3	3.9	13.9	4.5	2.5	3.5	5.0
YCo_3B_2[61]	0.4	7.6	5.7	5.1	2.1	2.2	5.6
$ScCo_3B_2$[61]	0.4	5.5	8.1	5.9	2.0	2.0	5.7
$PtCoO_2$[61]	0.9	110.4	1.8	13.3	0.5	7.3	5.0
CuTi[62]	0.7	9.8	19	9.56	9.14	10.17	4.33

Their attractiveness stems from their inherently short EMFP, favorable resistivity scaling behavior, and superior resistance to electromigration relative to Cu. Although their bulk resistivities are typically higher than that of Cu, these characteristics allow them to surpass Cu performance as dimensions shrink to the nanoscale, where electron scattering becomes the dominant factor.[13]

The primary limitation of Cu interconnects originates from their intrinsically long EMFP of ~39 nm. This leads to a severe escalation in resistivity once the metal thickness reaches the sub-20 nm regime, where surface and grain-boundary scattering dominate transport. In contrast, alternative metals such as Ru (5.7 nm), Ir (7.1 nm), Rh (6.9 nm), Co (9.8 nm), and Mo (~11 nm) possess substantially shorter EMFPs, rendering their electrical resistivity significantly less sensitive to geometrical confinement.[43,57]

As shown in Fig. 7a, comparative screening data from experimental reports reveal that these short-EMFP metals maintain lower effective resistivity than Cu/TaN stacks at reduced thicknesses, despite their higher bulk resistivity values.[63] Notably, the plotted resistivity values correspond to integrated metal stacks fabricated primarily by physical vapor deposition (PVD) or atomic layer deposition (ALD), thereby capturing realistic contributions from interface, surface, and liner-induced scattering. This trend highlights that intrinsic electronic transport length scales, rather than bulk resistivity alone, govern interconnect performance in the deeply scaled regime. This underscores the scaling advantage of short-EMFP conductors for future BEOL integration.[63–65]

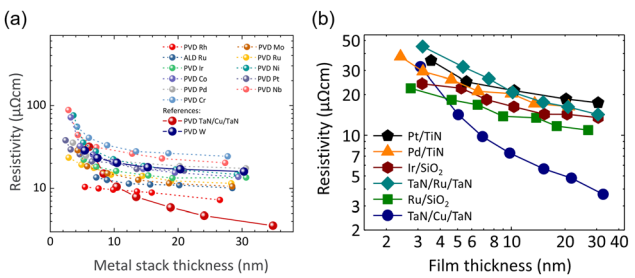

Fig. 7 Thickness-dependent resistivity of single-element metals. (a) Screening comparison showing that short EMFP metals (Ru, Ir, Rh, Co, and Mo) exhibit weaker resistivity scaling than Cu despite higher bulk resistivity. Reprinted with permission from ref. 63. Copyright 2024, AIP Publishing. (b) Liner-integrated comparing thickness-dependent resistivity of Cu- and Ru-based stacks. Reprinted with permission from ref. 57. Copyright 2017, AIP Publishing.

Fig. 7b presents a direct integration-level comparison of thickness-dependent resistivity for candidate interconnect metals incorporated within realistic liner or substrate stacks.[57] To reflect BEOL-relevant conditions, all metal films were deposited *via* PVD and subsequently annealed to stabilize the microstructure and promote grain growth prior to electrical characterization. The Cu/TaN reference exhibits a pronounced upturn in resistivity as the film thickness is reduced below 15 nm, indicating a severe size effect arising from the combination of a long EMFP and the necessity of diffusion barriers.

In contrast, Ru-based stacks (such as Ru/SiO_2 and TaN/Ru/TaN) show significantly weaker thickness dependence, maintaining lower resistivity in the ultrathin regime. Similarly, Ir/SiO_2 and Pd/TiN stacks exhibit moderated scaling behavior compared to Cu/TaN. These results demonstrate that short-EMFP metals preserve their scaling advantage even in liner-integrated configurations, confirming their practical viability for advanced interconnect applications beyond the limits of Cu.

Fig. 8a demonstrates that Ru thin films deposited by chemical vapor deposition (CVD) is strongly contingent on substrate chemistry and post-deposition annealing.[66] Oxygen incorporation in as-deposited films on oxide substrates leads to poor conductivity; however, annealing at 400 °C reduces defect scattering and restores electrical performance. On TiN substrates, annealing significantly lowers the grain boundary reflection coefficient, further confirming the critical role of thermal treatments in mitigating size effects.

Similarly, Fig. 8b highlights Mo films deposited by PVD and ALD. While both techniques exhibit resistivity escalation in the sub-10 nm regime, annealing consistently improves conductivity.

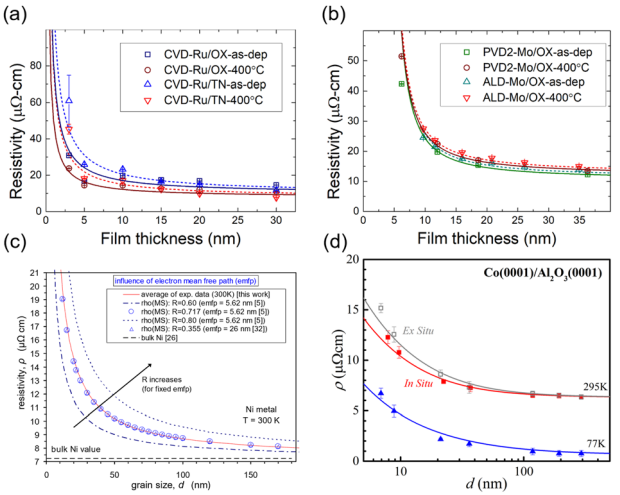

Fig. 8 Grain boundary and interfacial effects on resistivity scaling in single-element metals. (a) Thickness-dependent resistivity of CVD Ru films showing strong substrate and annealing effects. (b) Resistivity scaling of PVD- and ALD-grown Mo films, with improved conductivity after annealing. Reprinted with permission from ref. 66. Copyright 2023, Elsevier. (c) Grain-size-dependent resistivity of Ni thin films following the MS model. Reprinted with permission from ref. 67. Copyright 2021, Springer Nature. (d) Grain-size-dependent resistivity of epitaxial Co (0001)/Al_2O_3 (0001). Reprinted with permission from ref. 68. Copyright 2019, AIP publishing.

Notably, ALD-grown films provide enhanced uniformity and superior performance at the thinnest dimensions.[66] These observations collectively emphasize the importance of microstructural engineering. Deposition chemistry and thermal processing are not merely peripheral steps; they critically influence grain boundary scattering and, consequently, determine overall device-level performance.

Additional insight is provided by Fig. 8c, which illustrates the resistivity variations of Ni thin films as a function of grain size at 300 K, combining averaged experimental data with MS model analysis.[67] The solid symbols represent experimental resistivity values, while the dashed lines correspond to MS model predictions for various grain-boundary reflection coefficient R, at a fixed EMFP of 5.62 nm. The data reveal a pronounced increase in resistivity as the grain size decreases, confirming that grain-boundary scattering dominates transport in the fine-grained regime.

Notably, even for a metal with an intermediate EMFP such as Ni, resistivity remains highly sensitive to the grain-boundary reflection coefficient. This indicates that microstructural factors can outweigh intrinsic bulk transport properties. This result underscores that effective interconnect scaling requires deliberate control over grain size and crystallographic texture, in addition to selecting materials with favorable EMFP values.

Fig. 8d illustrates how surface conditions and the measurement environment critically influence resistivity scaling in transition-metal interconnects, specifically exemplified by epitaxial Co(0001) films on Al_2O_3(0001).[68] The pronounced discrepancy between *in situ* and *ex situ* measurements highlights the high sensitivity of Co to surface oxidation and contamination. Such effects introduce additional interfacial scattering mechanisms beyond intrinsic grain-boundary scattering. At room temperature, the resistivity decreases rapidly with increasing grain size and approaches a weakly size-dependent regime only at sufficiently large dimensions. In contrast, low-temperature measurements suppress phonon scattering, thereby isolating the intrinsic size-effect behavior. Overall, the trends observed in Ru, Mo, Ni, and Co indicate that microstructural engineering must extend beyond simple grain-size control to include interface quality and process integration, as these factors ultimately govern resistivity at advanced interconnect dimensions.

Electromigration reliability constitutes another decisive factor for interconnect performance. Atomic diffusivity follows an Arrhenius relationship, where the migration energy scales directly with the material's cohesive energy.[69] Consequently, metals with higher cohesive energies generally possess lower diffusivities and longer electromigration lifetimes.[70] Cu, with a cohesive energy of 3.5 eV per atom, corresponds to an activation energy of 0.8 eV, reflecting its limited structural stability at high current densities.[71] In contrast, Ir and Ru—possessing cohesive energies between 7.1 and 8.0 eV per atom—exhibit activation energies approaching 1.1 eV, which is consistent with significantly enhanced durability. Mo (6.8 eV per atom) also offers robust stability, while Co (5.2 eV per atom) provides intermediate reliability—outperforming Cu, though not matching the levels of Ru.[72] These intrinsic properties align with experimental results demonstrating that barrier/liner-free Ru interconnects exhibit lifetimes far exceeding those of conventional Cu.[73]

From a process-integration perspective, Ru remains the most mature candidate. Both CVD and ALD methodologies can yield continuous Ru films down to 2 nm in thickness, making it highly compatible with advanced BEOL integration.[74,75] Co is already employed in high-volume production environments, particularly for liners and *via* metallization, benefiting from established process expertise.[76,77] While Mo presents a promising balance of resistivity scaling and cohesive energy, its widespread industrial adoption is pending for the development of viable high-volume deposition routes.[78,79] Conversely, Ir and Rh offer compelling scaling benefits but are hampered by scarcity, high costs, and deposition challenges. Pt is similarly restricted by both cost constraints and significant integration complexity.[80]

In summary, single-element metals with intrinsically short EMFPs and elevated cohesive energies provide superior performance compared to Cu in nanoscale interconnects. Among these, Ru emerges as the most technologically practical option, combining favorable scaling with superior electromigration resistance. Co and Mo deliver complementary strengths and are likely to be integrated within hybrid or multi-material schemes, whereas Ir, Rh, and Pt, while theoretically promising, remain constrained by economic availability and manufacturing hurdles. Realizing reliable, scalable interconnects at sub-10 nm technology nodes will require coupling these materials with advanced interface design, process optimization, and strategic alloying.

3.2 Binary intermetallic compounds

Binary intermetallic compounds and ordered alloys have recently gained significant attention as credible successors to both Cu and elemental metals in advanced interconnects. Their promise arises from a combination of intrinsically short EMFP, elevated cohesive energies, and ordered crystal lattices that inherently minimize random alloy scattering. This synergy enables the suppression of the resistivity size effect while simultaneously enhancing electromigration resistance and thermal stability, making intermetallic compounds strong contenders for sub-10 nm technology nodes.

As illustrated in Fig. 9a, the FOM ($\rho_0\lambda$) is plotted against cohesive energy, serving as a proxy for electromigration robustness.[63] Promising compounds cluster in favorable regions of this map, including Al-based alloys (Al_3Sc, Al_2Cu, and $CuAl_3$), Ru-based systems (RuAl and GaRu), and ordered intermetallic compounds such as NiAl. These materials combine short EMFPs with strong atomic bonding, enabling suppressed resistivity scaling while maintaining high resistance to atomic diffusion. Notably, NiAl and RuAl exhibit $\rho_0\lambda$ values substantially lower than that of Cu while sustaining cohesive energies comparable to those of refractory metals, indicating a more optimal balance between electrical conductivity and reliability for advanced interconnect applications.

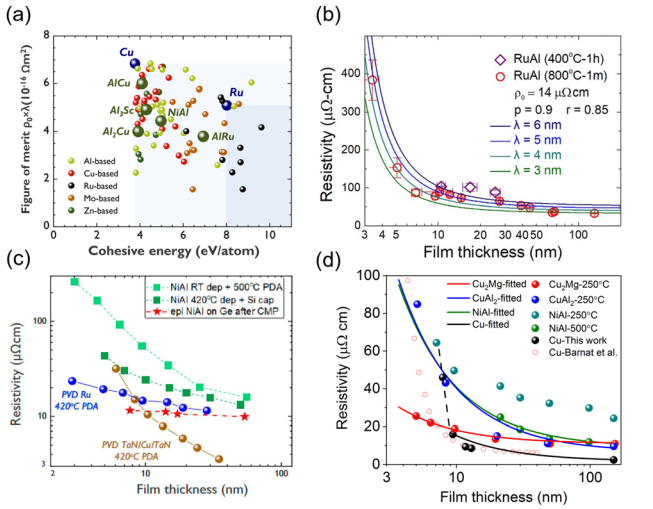

Fig. 9 Resistivity scaling and materials screening of binary intermetallic compounds for advanced interconnects. (a) Screening of binary intermetallic compounds using the FOM ($\rho_0\lambda$) *versus* cohesive energy, highlighting promising Al-based, Ru-based and NiAl-type compounds combining favorable scaling potential and strong atomic bonding. Reprinted with permission from ref. 63. Copyright 2024, AIP Publishing. (b) Thickness-dependent resistivity of RuAl thin films, showing weak scaling behavior governed by a short EMFP and high surface specularity, together with excellent thermal stability after annealing. Reprinted with permission from ref. 81. Copyright 2024, AIP Publishing. (c) Resistivity scaling of NiAl thin films demonstrating the impact of microstructural engineering, where back-thinning and epitaxial growth significantly reduce resistivity at nanoscale thicknesses. Reprinted with permission from ref. 84. Copyright 2023, IEEE. (d) Benchmark comparison of selected binary intermetallic and alloy systems, showing that NiAl, $CuAl_2$, and Cu_2Mg outperform Cu in the sub-10 nm regime. Reprinted with permission from ref. 53. Copyright 2021, AIP Publishing.

RuAl: resistivity scaling and thermal robustness. Among the screened candidates, RuAl emerges as a particularly promising interconnect material. As shown in Fig. 9b, RuAl thin films exhibit a bulk resistivity of approximately 14 μΩ cm and a markedly suppressed resistivity increase as the thickness decreases.[81] The RuAl thin films were deposited *via* co-sputtering, followed by post-deposition annealing to form the ordered intermetallic phase prior to electrical characterization. The experimental data are well described by combined FS and MS models using a short EMFP (λ = 3–6 nm) and a high surface specularity ($p \approx 0.9$), indicating predominantly specular surface scattering. Although the grain-boundary reflection coefficient remains non-negligible ($R \approx 0.85$), its impact is mitigated by the intrinsically short transport length scale of RuAl, resulting in significantly weaker resistivity scaling compared with Cu.

Importantly, RuAl maintains stable resistivity after post-deposition annealing at temperatures up to 900 °C, demonstrating exceptional thermal robustness. Severe degradation is observed only above 1000 °C, primarily due to oxidation and silicide formation. This combination of a low $\rho_0\lambda$ product, strong atomic bonding, and outstanding thermal endurance positions RuAl as a compelling candidate for barrier-free or liner-free interconnect integration.

NiAl: microstructure engineering *via* back-thinning. NiAl, another promising intermetallic compound, demonstrates that resistivity scaling can be substantially improved through process-driven microstructural engineering.[82,83] As shown in Fig. 9c, NiAl thin films deposited by PVD exhibit markedly reduced resistivity when a back-thinning strategy is employed.[84] In this approach, a thick film is first deposited to promote significant grain growth during annealing, followed by thinning *via* chemical–mechanical polishing while preserving the enlarged grains.

This method effectively decouples grain size from film thickness, suppressing grain-boundary scattering in the ultra-thin regime. As a result, epitaxial NiAl grown on Ge substrates achieves resistivities as low as 11.5 μΩ cm at 7.7 nm and 10.6 μΩ cm at 17.2 nm, outperforming PVD Ru of comparable thickness. These results confirm that ordered intermetallic compounds can surpass conventional metals when the microstructure is deliberately engineered, highlighting process-enabled pathways toward Cu-replacement interconnects.

Benchmarking results highlight clear differences among Cu, Cu–Mg, $CuAl_2$, and NiAl (Fig. 9d). Pure Cu exhibits the steepest resistivity increase as the thickness is reduced, reflecting its severe size-effect.[53] Alloying Cu with Mg moderates this trend, leading to a noticeably weaker resistivity scaling; however, Cu–Mg remains inferior to ordered intermetallic compounds at scaled dimensions. In contrast, $CuAl_2$ and NiAl show substantially gentler resistivity increases across the entire thickness range, despite their higher bulk resistivities. Notably, NiAl maintains the lowest effective resistivity among the compared materials at small thicknesses after annealing. This indicates that crystallographic ordering and reduced disorder scattering

provide a more robust route to suppressing the size effect than Cu-based alloying alone.

NiCo solid solution: a unique case among alloys. In contrast to ordered compounds, the disordered phase of solid solutions typically exhibits elevated resistivity due to disorder-induced scattering. According to Nordheim's rule, this effect scales with the differences in atomic potential and d-band filling between constituent elements. Alloys with large electronegativity mismatches or dissimilar d-band centers suffer from significant broadening of electronic states, leading to higher residual resistivity.

As shown in Fig. 10a, the progression from the binary NiCo alloy to the quinary NiFeCoCrMn high-entropy alloy reveals a systematic enhancement of electronic disorder.[85] While NiCo retains relatively sharp Bloch spectral features, the incorporation of additional elements progressively broadens the band structure and smears the Fermi surface, indicating reduced quasiparticle lifetimes. This band smearing reflects strong elastic scattering arising from chemical disorder, which shortens the EMFP and fundamentally limits electrical conductivity in concentrated solid-solution and high-entropy alloys. Fig. 10b further demonstrates that Ni and Co possess closely aligned d-band centers (offsets of only 0.1–0.2 eV) and similar exchange splitting, which minimizes electronic disorder. In contrast, elements like Cr or Mn deviate by >0.5 eV, introducing localized states that increase scattering. This electronic compatibility explains why NiCo, despite its nature as a disordered solid solution, maintains a significantly lower residual resistivity than more complex high-entropy alloys.

Importantly, a single-phase hexagonal close-packed (HCP) NiCo alloy has recently been successfully deposited, which exhibits a $\rho_0\lambda$ value of approximately 5.7×10^{-16} Ω m^2, comparable to that of ordered intermetallics such as NiAl and far superior to Cu (2.3×10^{-15} Ω m^2).[86] Its short EMFP ($\sim$5 nm) significantly mitigates size effects; while the resistivity of Cu rises sharply below 20 nm due to its long EMFP, NiCo maintains a stable resistivity of approximately $\sim$20 $\mu\Omega$ cm even at a thickness of 9 nm, outperforming Cu/TaN stacks at comparable dimensions (Fig. 10c). This advantage is reinforced in Fig. 10d, where NiCo aligns more closely with ordered intermetallic compounds than with conventional solid solutions, combining high cohesive energy ($\sim$5.1 eV per atom) with low resistivity. Microstructural evidence in Fig. 10e further confirms that epitaxial NiCo grown on Al_2O_3 can form single-phase HCP crystal structures, validating that these intrinsic electronic advantages can be realized experimentally.

Taken together, NiCo represents a rare case where a solid-solution alloy demonstrates scaling characteristics comparable to ordered intermetallic compounds. Its synergy of a short EMFP, favorable FOM, and high cohesive energy positions it as a compelling post-Cu candidate, bridging the gap between single-element metals and ordered alloys. RuAl combines favorable resistivity scalability with exceptional thermal stability, while NiAl leverages process-driven approaches—such as back thinning and epitaxial growth—to achieve record-low resistivities. Additional compounds, including $CuAl_3$ and $ScAl_3$, further expand the available materials design space, particularly in the sub-10 nm regime.[87–89] Looking forward, key challenges include the development of industrially scalable deposition routes, ensuring compatibility with low-k dielectrics, and balancing performance against material cost and availability. With continued progress in these areas, binary intermetallic compounds and related alloys hold substantial promise as practical and scalable replacements for Cu-based interconnects.[29,90,91]

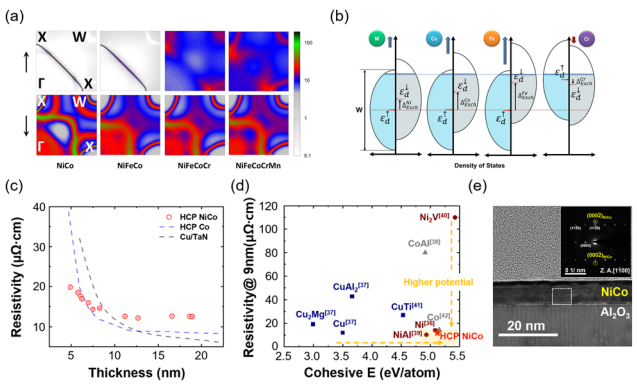

Fig. 10 Electronic origins and scaling behavior of low-resistivity solid-solution alloys. (a) Evolution of the electronic structure from binary NiCo to multicomponent NiFeCoCrMn, illustrating increased band smearing with compositional complexity. (b) Schematic comparison of d-band alignment and exchange splitting, showing the minimal electronic mismatch in NiCo compared with Cr- and Mn-containing alloys. Reprinted with permission from ref. 85. Copyright 2019, Springer Nature. (c) Thickness-dependent resistivity of NiCo films demonstrating reduced size effects relative to Cu/TaN stacks. (d) Benchmark of resistivity *versus* cohesive energy, placing NiCo close to ordered intermetallic compounds and distinct from conventional solid solutions. (e) Cross-sectional TEM image of epitaxial NiCo on Al_2O_3, confirming high structural quality and sharp interfaces. Reprinted with permission from ref. 86. Copyright 2025, American Chemical Society.

3.3. Ternary systems

Investigations into ternary compounds have expanded as the limitations of conventional interconnect metals have become evident at reduced dimensions. These systems provide ordered structures and anisotropic conduction pathways that modify electron scattering compared with elemental or binary materials. Two representative categories have been studied in detail: MAX phases, which are layered carbides and nitrides, and oxides of the delafossite type.

The relationship between antisite defect formation energy and electronegativity difference is presented in Fig. 11a.[92] The vertical axis shows the formation energy of M–A antisite pairs, and the horizontal axis shows the electronegativity difference between the M and A elements. MAX phases such as Cr_2AlC and Ti_2AlC fall in the low formation energy region of about 2.1 to 2.7 eV, whereas Zr_3SnC_2 and Hf_3SnC_2 appear above 5 eV. As the electronegativity difference increases from roughly 0.1 to 0.7, the antisite pair formation energy increases, indicating that larger chemical contrast between M and A elements makes M–A exchanges energetically less favorable. It is noted that M–A exchanges are energetically more accessible than M–X or A–X exchanges, which is consistent with the different bonding environments in MAX phases.

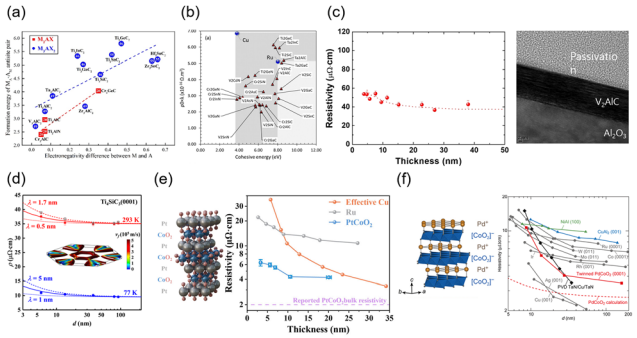

Fig. 11 Ternary compounds for scaled interconnects: MAX phases and delafossite oxides. (a) Screening map linking electronegativity difference to antisite defect formation energy in MAX phases, indicating that M–A exchanges are more favorable than M–X or A–X exchanges and that A-site volatility can affect stoichiometry. Reprinted with permission from ref. 92. Copyright 2021, Elsevier. (b) *Ab initio* screening of cohesive energy and $\rho_0\lambda$, highlighting thermodynamically, stable MAX phases with $\rho_0\lambda$ comparable to or lower than Cu and Ru. Reprinted with permission from ref. 96. Copyright 2021, American Physical Society. (c) Resistivity scaling of sputtered V_2AlC films with a cross-sectional TEM image confirming the layered structure on Al_2O_3. Reprinted with permission from ref. 97. Copyright 2021, American Chemical Society. (d) Epitaxial Ti_4SiC_3 (0001) films showing nearly thickness-independent resistivity at 293 K and 77 K. Reprinted with permission from ref. 98. Copyright 2021, AIP Publishing. (e) Delafossite layered conduction concept and $PdCoO_2$ thin-film transport, including annealing-induced improvement and microstructure-limited resistivity. Reprinted with permission from ref. 99. Copyright 2025, John Wiley and Sons. (f) Resistivity scaling of epitaxial $PtCoO_2$ down to a few nanometers, compared with effective Cu with barriers and Ru. Reprinted with permission from ref. 100. Copyright 2025, AIP Publishing.

This defect tendency is relevant to synthesis because disordering and A site loss can promote non-stoichiometry during high temperature processing, especially when A elements are volatile.[93,94] In addition, transport in MAX phases is closely tied to the bonding network within the carbide or nitride slabs, so antisite disorder that perturbs the local bonding environment can influence the electronic conduction pathways.[95]

Ab initio screening results are provided in Fig. 11b, which plots cohesive energy against the product $\rho_0\lambda$ for MAX phases, with Cu and Ru shown as reference metals.[96] For these references, Cu exhibits $\rho_0\lambda$ values ranging from 6.7 to 6.8 $\times$ 10^{-16} Ω m^2, while Ru shows 5.1 $\times$ 10^{-16} Ω m^2. Specific MAX phases are also highlighted: Ti_2GeC has a cohesive energy of 7.6 eV per atom with $\rho_0\lambda$ = 6.1 $\times$ 10^{-16} Ω m^2, Ti_2SiC has a cohesive energy of 7.8 eV per atom with $\rho_0\lambda$ = 6.1 $\times$ 10^{-16} Ω m^2, and V_2AlC has a cohesive energy of 7.9 eV per atom with $\rho_0\lambda$ between 4.1 and 5.3 $\times$ 10^{-16} Ω m^2. Overall, the figure highlights that 69 thermodynamically stable MAX phases satisfy a Cu-based benchmark, defined as having both a lower $\rho_0\lambda$ than Cu and a cohesive energy exceeding 3.8 eV per atom.

The resistivity scaling behavior of V_2AlC films was experimentally reported.[97] Fig. 11c shows resistivity variations as a function of film thickness, with the red fitting curve summarizing the weak thickness dependence over the 5–50 nm range. In particular, between thicknesses of 50 and 10 nm, the resistivity remains essentially constant. Even at a thickness of 6 nm, the film exhibits a resistivity of approximately 49 $\mu\Omega$ cm, remaining within the same range as thicker films rather than increasing sharply under geometric confinement. The EMFP of V_2AlC, estimated to be 11–13.6 nm, is sufficiently short that additional surface and grain-boundary scattering contributions remain limited. The accompanying cross-sectional transmission electron microscopy (TEM) image directly reveals the V_2AlC layer deposited on an Al_2O_3 substrate, together with a passivation overlayer, confirming the intended layered stack used for the scaling comparison.

Resistivity scaling characteristics of another epitaxial layer are addressed in Fig. 11d, where Ti_4SiC_3(0001) layers exhibit resistivity values that vary only weakly across nearly two orders of magnitude in thickness.[98] Fig. 11d plots the resistivity as a function of film thickness, measured *in situ* in vacuum at 293 K (red squares), in liquid N_2 at 77 K (blue circles), and *ex situ* in air at 293 K (open gray squares). At room temperature, the resistivity is 35.2 $\pm$ 0.4 $\mu\Omega$ cm at 92.1 nm and 37.5 $\pm$ 1.1 $\mu\Omega$ cm at 5.8 nm, showing minimal variation despite a large change in thickness. At 77 K, the resistivity decreases to 9.5 $\pm$ 0.2 $\mu\Omega$ cm at 92.1 nm and 11.0 $\pm$ 0.4 $\mu\Omega$ cm at 5.8 nm. These data demonstrate that while resistivity decreases with decreasing measurement temperature, it remains largely independent of the film thickness. To further visualize the reduced size effect, Fig. 11d overlays FS model curves under the assumption of completely diffuse surface scattering (p = 0). Under this condition, the plotted curves correspond to λ = 0.5, 1.1, and 1.7 nm at 293 K and λ = 1, 3, and 5 nm at 77 K, illustrating how a short effective λ is consistent with the weak thickness dependence. Because the films are epitaxial, grain-boundary scattering is expected to be negligible in interpreting the thickness trend. The inset further shows the calculated Fermi surface, color-coded by Fermi velocity, highlighting the intrinsic electronic structure underlying the transport behavior.

Delafossite oxides, such as $PdCoO_2$ and $PtCoO_2$, have been reported to exhibit quasi-two-dimensional transport largely confined to the noble metal layers. This unique electronic structure enables an ultralow bulk in-plane resistivity on the order of a few $\mu\Omega$ cm. Fig. 11e illustrates the layered crystal structure of $PtCoO_2$ alongside its thickness-dependent transport characteristics.[99] The resistivity of $PtCoO_2$ increases only gradually as the film thickness is reduced from 20.1 nm to 3.3 nm, remaining below benchmark metals across the entire thickness range. Notably, at 5.6 nm, the resistivity of $PtCoO_2$ is six times lower than that of effective Cu. Furthermore, the resistivity of $PtCoO_2$ increases by a factor of only 1.5 when thinning from 20.1 nm to 3.3 nm, whereas effective Cu exhibits a seven-fold increase between 19.8 nm and 5.7 nm.

Fig. 11f shows a structural schematic of delafossite $PdCoO_2$ alongside a thickness-dependent comparison of in-plane resistivity at 300 K.[100] Measured $PdCoO_2$ thin-film resistivity is plotted as red squares and benchmarked against epitaxial thin films of high-conductivity elemental metals, NiAl, and $CuAl_2$, while a PVD TaN/Cu/TaN stack is included as a reference interconnect structure. In the relatively thick regime (d = 13.8, 27.8, and 161.3 nm), the $PdCoO_2$ films show resistivities lower

than those of the compared epitaxial alloys and elemental metals, with the exception of Ag and Cu, indicating favorable transport when the geometric confinement is modest. As the thickness is further reduced, the $PdCoO_2$ resistivity increases and overtakes several elemental-metal trends by $d = 8.7$ nm. It is important to note that delafossite oxides exhibit an extremely weak size effect in thin-film form, a characteristic attributed to their exceptionally large EMFP of ~110 nm. However, this scaling advantage diminishes in nanowire geometries. In such confined structures, the increased frequency of electron scattering at the sidewalls—relative to the top and bottom surfaces—dominates the transport mechanism, leading to a more pronounced resistivity escalation.

3.4 Topological semimetals

Topological materials have recently emerged as one of the most promising classes of compounds in condensed matter physics and electronic materials research.[101,102] Owing to the topological characteristics of their band structures, they exhibit distinct transport behaviors compared to conventional metals or semiconductors.[101,103] In particular, topological semimetals (TSMs) feature band crossings that form Dirac cones or Weyl nodes, leading to the presence of topologically protected conduction channels (Fig. 12a).[103,104] These channels are inherently resistant to scattering and can support quasi-ballistic transport.[105] Such properties are highly attractive for nanoscale interconnects, where conventional metals suffer from severe resistivity increases upon dimensional scaling.[101–109]

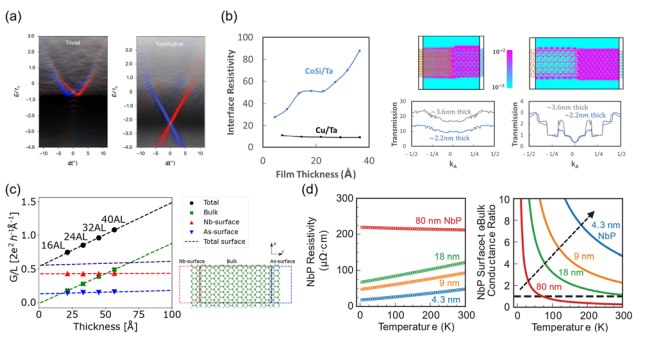

Fig. 12 Surface-dominated transport in topological semimetals. (a) Schematic band structures trivial and topological states, showing gapped bands in the trivial phase and Dirac cone-like crossing with topological surface states in the topological phase. Reprinted with permission from ref. 109. Copyright 2023, Spring Nature. (b) Calculated LDOS, interface-specific resistivity, and momentum-resolved transmission *versus* the thin film thickness for Cu/Ta and CoSi/Ta interfaces, revealing bulk-dominated transport in Cu/Ta and thickness-independent, surface-dominated transport in CoSi/Ta. Reprinted with permission from ref. 110. Copyright 2024, Springer Nature. (c) Ballistic conductance per unit length (G/L) *versus* thickness (atomic layers), separated into bulk and surface contributions, showing dominant surface conduction in ultrathin films. Reprinted with permission from ref. 112. Copyright 2024, Springer Nature. (d) The thickness- and temperature-dependent resistivity and surface-to-bulk conductance ratio of NbP films, demonstrating surface-dominated transport in ultrathin regimes. Reprinted with permission from ref. 114. Copyright 2025, AAAS.

CoSi is a representative topological semimetal that highlights the unique scaling behavior of surface-dominated transport.

Although its bulk density of states (DOS) near the Fermi level is relatively low—leading to limited bulk conduction—the presence of topological surface states enables current transport to be dominated by surface channels.[110,111] This behavior is revealed by interface resistivity scaling and transmission simulations as shown in Fig. 12b. In the bulk-like regime (larger thickness), the CoSi/Ta interface exhibits a significantly higher resistivity than Cu/Ta due to the reduced bulk DOS of CoSi. However, as the thickness is scaled down to a few nanometers, the bulk contribution rapidly diminishes and surface conduction becomes dominant, resulting in a pronounced reduction in the interface resistivity. In contrast, Cu/Ta remains bulk-carrier dominated; thus, thickness scaling enhances interfacial scattering and either maintains or worsens the resistance.

The transmission probability is plotted as a function of the transverse momentum k_A for different film thicknesses (Fig. 12b). For Cu/Ta, increasing the thickness from ~2.2 nm to ~3.6 nm leads to higher transmission due to increased bulk carrier participation. In contrast, CoSi/Ta exhibits nearly thickness-independent transmission, demonstrating that transport is governed by robust surface channels rather than bulk states.[110] NbAs provides another compelling example of a Weyl semimetal in which surface conduction becomes increasingly dominant as the thickness is reduced. Fig. 12c presents the conductance contributions as a function of thickness expressed in atomic layers (ALs), where the horizontal axis denotes the number of atomic layers and the vertical axis shows the ballistic conductance per unit length (G/L).[112] For a 16 AL film (corresponding to ~2.1 nm), approximately 76% of the total conductance originates from surface states, while only 24% is contributed by the bulk. Even at 40 AL (~5.7 nm), surface conduction remains responsible for more than half of the total conductance. These results indicates that, as the film thickness decreases, electrical transport becomes increasingly dominated by surface channels.[112]

NbP has recently been identified as another promising topological semimetal candidate, exhibiting unconventional thickness- and temperature-dependent resistivity scaling.[113,114] Fig. 12d shows the resistivity of NbP films as a function of temperature for various thicknesses, along with the corresponding surface-to-bulk conductance ratio. Thick NbP films (80 nm) exhibit nearly temperature-independent resistivity, consistent with disorder-dominated bulk conduction. In contrast, thinner films (18, 9, and 4.3 nm) display distinct metallic behavior, with resistivity decreasing as the temperature decreases. Remarkably, sub-5 nm NbP films exhibit resistivities up to six times lower than those of bulk NbP. At these reduced dimensions, NbP outperforms both Cu and Ru thin films of comparable thicknesses, highlighting its potential as a high-conductivity alternative for advanced interconnects.[63,114,115] The right panel in Fig. 13d shows the surface-to-bulk conductance ratio as a function of temperature. As the thickness decreases, the ratio increases dramatically, indicating a crossover from bulk-dominated to surface-dominated transport.

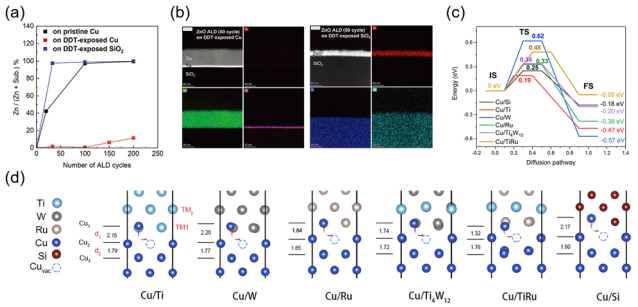

Fig. 13 Selective ZnO atomic layer deposition and Cu interfacial barriers. (a) XPS-derived Zn atomic fraction *versus* the ALD cycle number on pristine Cu, DDT-exposed Cu, and DDT-exposed SiO_2, showing suppressed ZnO growth on DDT-treated Cu and rapid saturation on SiO_2. (b) Cross-sectional STEM and EDS maps of ZnO deposited by ALD on DDT-exposed SiO_2, showing uniform ZnO growth. Reprinted with permission from ref. 130. Copyright 2023, John Wiley and Sons. (c) DFT-calculated Cu diffusion reaction pathways at Cu/transition metal (TM) and Cu/Si interfaces, comparing interfacial diffusion barriers from initial (IS) to final (FS) states. (d) Interfacial atomic structures of Cu/TM and Cu/Si systems after Cu diffusion, where interlayer distances (d_1 and d_2) indicate the degree of diffusion suppression. Reprinted with permission from ref. 131. Copyright 2025, Elsevier.

In summary, NbP demonstrates a unique scaling behavior where thinner films exhibit lower resistivity—a robust, surface-dominated conduction mechanism that persists across a wide temperature range. This contrasts sharply with conventional metals, which invariably suffer from resistivity escalation as dimensions scale down.[111,112,114,116] Nonetheless, several limitations remain. First, many TSMs exhibit higher bulk resistivity than Cu or Ru, which can lead to performance losses if surface conduction is not sufficiently activated.[63,114] Second, most TSMs are susceptible to surface oxidation and degradation under ambient conditions, raising concerns regarding long-term reliability.[117,118] Third, large-area growth, orientation control, and CMOS BEOL compatibility are still at relatively early stages.[119,120] Future research must therefore focus on overcoming these challenges to realize the intrinsic topological transport properties of TSMs in practical device fabrication environments.

4. Advanced barriers and liners

4.1 Problems with traditional Ta/TaN: thickness overhead

The shrinkage of interconnect dimensions leads to a sharp increase in current density.[121] The high current density induces Joule heating, which elevates the temperature and accelerates electromigration, thereby reducing the mean time-to-failure of the interconnects.[122,123]

Cu intrinsically has a high diffusion coefficient, making it prone to penetrate the surrounding dielectric during high-temperature processing or device operation.[123,124] The activation energy for Cu diffusion in SiO_2 is reported to be approximately 0.2–0.9 eV,[53] which is lower than that of most other metals.[122,123] As a result, severe reliability issues such as leakage path formation and short-circuiting can occur.[125] In addition, Cu reacts with oxygen to form copper oxides (CuO_x), further degrading electrical performance.[123,125,126]

To suppress such problems, barrier and liner layers have been introduced. These layers block Cu diffusion, improve interfacial adhesion, and enhance both electrical and mechanical stability, while also preventing oxygen penetration.[123] To date, Ta and TaN have been the most widely used barrier/liner materials for Cu interconnects.[123,127]

However, as feature sizes scale down to tens of nanometers or below, the volumetric fraction of barrier/liner layers becomes significant, reducing the effective conductive cross-sectional area and thereby increasing line resistance. Conversely, thinning the barrier below 3 nm drastically deteriorates its diffusion-blocking ability, leading to severe reliability degradation.[122,123,127]

As device dimensions continue to scale, alternative approaches such as selective barriers, Co/Ru liners, and barrierless Ru have been proposed.[127] This evolution underscores the inability of conventional Ta/TaN barriers to fundamentally resolve the thickness overhead issue.

Although DFT calculations have identified several alternative materials with high theoretical Cu diffusion barriers, their practical effectiveness is often reduced under real processing conditions due to polycrystalline microstructures and grain-boundary-mediated diffusion. Consequently, translating idealized theoretical predictions into manufacturable barrier solutions remains a nontrivial challenge.[128,129]

4.2 Thin metallic barriers

To overcome the thickness overhead problem of Ta/TaN barriers, it is essential to develop ultrathin passivation layers that can mitigate electromigration while maintaining strong diffusion-blocking capabilities.[123,125,127]

Recent studies have revealed that Ru can effectively suppress Cu diffusion at significantly lower thicknesses than Ta/TaN, positioning it as a promising candidate for next-generation barriers.[127] Nevertheless, as long as Cu-based interconnects rely on barrier architectures within conventional damascene structures, unavoidable trade-offs between device performance and pattern scalability will persist. To address this, the use of ultrathin Ru barriers *via* area-selective ALD (AS-ALD) has recently been reported. Specifically, ZnO films can be grown selectively by ALD using dodecanethiol as an inhibitor; the resulting Ru/ZnO bilayer serves as an effective Cu diffusion barrier for advanced Cu interconnects (Fig. 13a and b).[130]

First-principles calculations provide insight into Cu diffusion behavior at various metal and alloy interfaces (Fig. 13c).[131] Cu/Si and Cu/Ti exhibit very low diffusion barriers (~0.25 and ~0.19 eV), indicating weak diffusion resistance. Cu/Ru and Cu/Ti_4W_{12} show moderate barriers (~0.33–0.34 eV), while Cu/W has a higher barrier (~0.48 eV). Notably, the Cu/TiRu interface exhibits the highest diffusion barrier (~0.62 eV) along with a deep final-state energy (~0.57 eV), suggesting a thermodynamically stable interface and strong suppression of Cu migration. These results demonstrate the complementary roles of Ru (low resistivity and process compatibility) and W (strong diffusion blocking), with TiRu alloys synergistically combining

these advantages. The enhanced diffusion resistance is further supported by relaxed interfacial atomic structure analysis (Fig. 13d).[131]

4.3 2D materials: graphene, h-BN, and MoS_2

Recently, atomically thin two-dimensional (2D) materials have emerged as promising alternatives to conventional Cu diffusion barriers and liners.[132] 2D materials are bonded by van der Waals forces between layers, resulting in weak interfacial interactions with Cu, which can effectively reduce electron scattering.[133] Their atomically thin yet dense structure, combined with superior mechanical strength and chemical stability, makes them highly suitable for next-generation interconnect integration.[132,133]

Graphene. Graphene, an atomically thin sp^2-bonded carbon layer, offers excellent chemical stability and is a promising Cu diffusion barrier. As a monolayer ($\sim$3 Å), graphene minimizes the thickness of high-resistivity barriers, thereby maintaining low Cu interconnect resistivity, since its intrinsic resistivity contributes negligibly.[134] Graphene/Cu structures also exhibit higher current density tolerance and breakdown voltage than bare Cu, indicating improved reliability. However, diffusion blocking strongly depends on graphene quality, as defects and grain boundaries provide Cu diffusion paths, while high-quality, large-grain graphene effectively suppresses Cu transport. Consequently, Cu/graphene structures show significantly enhanced time-to-failure lifetimes. Under a constant electric field of 7.0 MV cm^{-1} at 100 °C, mono-, bi-, and trilayer graphene barriers demonstrate comparable or superior time-to-failure relative to 2–4 nm TaN barriers. Increasing graphene layers further extends lifetime, confirming that stacked graphene effectively mitigates Cu diffusion and dielectric degradation (Fig. 14a).[135]

Hexagonal boron nitride (h-BN). Hexagonal boron nitride (h-BN), while electrically insulating, is an effective Cu diffusion barrier due to its atomically smooth, dense, and chemically inert structure. It suppresses both surface and interfacial Cu diffusion, reducing void and hillock formation, current crowding, Joule heating, and electromigration degradation.[136] As shown in Fig. 14b, Cu interconnects passivated with an angstrom-thin h-BN layer retain structural integrity after current stressing, whereas unpassivated Cu exhibits severe voids and hillocks.[137] Notably, such failure features appear only in regions without h-BN coverage, directly confirming its role in enhancing electromigration reliability. However, poor Cu wettability on h-BN can cause non-uniform Cu growth, indicating that h-BN is most effective when combined with complementary liners or surface treatments. Nevertheless, the poor wettability of Cu on h-BN can lead to non-uniform Cu growth, suggesting that h-BN is most effective when integrated in combination with complementary liners or surface treatments.[138]

Transition metal dichalcogenides (TMDs). Transition metal dichalcogenides (TMDs) such as MoS_2, WS_2, and TaS_2 are layered materials with van der Waals bonding, enabling direct growth on dielectrics and ALD-compatible BEOL integration.[139,140] Their atomic thinness, chemical stability, and

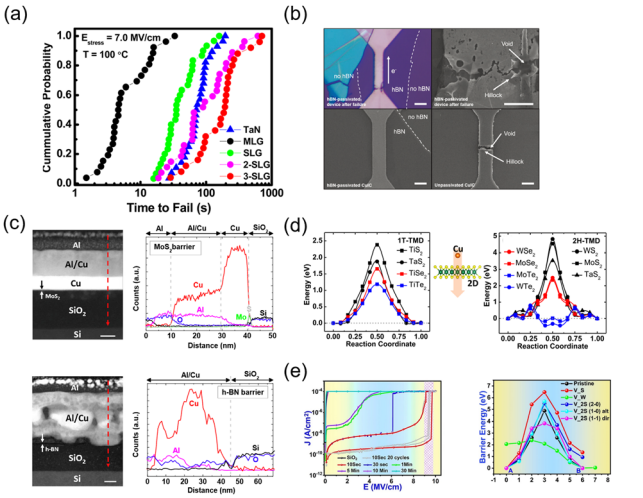

Fig. 14 Two-dimensional material barriers for Cu interconnect reliability. (a) Time-to-failure lifetime comparison under electric-field stress for Cu interconnect structures employing conventional TaN and graphene diffusion barriers. Monolayer and stacked graphene barriers exhibit comparable or improved reliability relative to TaN despite atomic-scale thickness, highlighting the limitation of conventional barrier scaling. Reprinted with permission from ref. 135. Copyright 2015, American Chemical Society. (b) Post-mortem optical and SEM analyses of h-BN-passivated and unpassivated Cu interconnects after current stressing, showing suppressed void and hillock formation in h-BN-covered regions. Reprinted with permission from ref. 137. Copyright 2021, John Wiley and Sons. (c) Cross-sectional STEM images and EDS line-scan profiles of Cu interconnects incorporating MoS_2, and h-BN diffusion barriers, highlighting improved Cu blocking by MoS_2. Reprinted with permission from ref. 123. Copyright 2017, Spring Nature. (d) DFT-calculated Cu diffusion energy barriers across single-layer TMDs in 1T and 2H phases. Reprinted with permission from ref. 39. Copyright 2020, AIP Publishing. (e) *J*–*E* characteristics of WS_2 diffusion barriers deposited under different growth conditions (left) and DFT-calculated Cu diffusion energy barriers in pristine and defect-containing WS_2 (right). Reprinted with permission from ref. 60. Copyright 2025, Elsevier.

mechanical robustness make them promising combined barrier/liner materials. Experiments show that MoS_2 forms a continuous barrier between Cu and dielectrics, significantly suppressing Cu diffusion and extending time-to-failure lifetimes, outperforming h-BN (Fig. 14c).[123]

First-principles calculations reveal that 2H-phase TMDs (*e.g.*, MoS_2 and WS_2) exhibit very high Cu diffusion barriers (3–4 eV), far exceeding those of 1T-phase TMDs (1–2 eV) as shown in Fig. 14d.[39] MoS_2 is particularly attractive due to its high diffusion resistance and low interfacial scattering. Reliability studies further show that even defect-containing WS_2 retains substantial diffusion-blocking capability.[39] Overall, TMDs emerge as strong candidates to replace conventional Ta/TaN barriers, with MoS_2 being the most extensively validated, although challenges remain in scalable growth, low-temperature processing, and damascene integration.[39,60,123,140]

4.4 Self-assembled monolayers (SAMs) and high-entropy alloys

Beyond 2D materials, molecular barriers such as self-assembled monolayers (SAMs) have been explored as ultrathin Cu diffusion

barriers.[141] SAMs form single-molecule-thick layers whose surface properties can be tailored by terminal functional groups. While silane-based SAMs bond strongly to oxide surfaces, their organic backbones may permit Cu diffusion. Aminosilane SAMs improve barrier performance through Cu–NH_2 coordination, enhancing adhesion and diffusion suppression. Despite their atomic-scale thickness, SAMs face challenges in thermal stability, plasma resistance, and mechanical robustness, motivating hybrid organic–inorganic barrier designs.[141–144]

Meanwhile, high-entropy alloys have emerged as promising inorganic diffusion barriers. Composed of multiple metallic elements in near-equiatomic ratios, high-entropy alloys exhibit severe lattice distortion and chemical disorder that hinder Cu migration. High-entropy alloy thin films demonstrate strong Cu diffusion suppression, high thermal stability, and favorable resistivity compared with Ta/TaN.[143,145]

5. Integration and process compatibility

5.1 Dry-etching challenges

Dry etching is a physical–chemical method that utilizes high-energy ions and plasma-induced radicals to remove surface atoms. This approach offers high anisotropy and precise process control, enabling the fabrication of high-aspect-ratio structures with minimal undercutting—qualities that have made it indispensable in IC manufacturing.[146,147]

However, direct dry etching of Cu remains practically infeasible due to several intrinsic limitations. First, Cu's chemical inertness results in low reactivity with plasma radicals; even under halogen-based plasmas (*e.g.*, Cl_2 and HBr), etch rates are extremely low.[148] Second, Cu-based etch by-products such as $CuCl_x$ and CuF_x exhibit low volatility, leading to surface residue and redeposition.[148,149] Third, the lack of self-limiting passivation layers on Cu complicates profile tuning and anisotropy control.[149] Furthermore, poor selectivity against masks and plasma-induced surface damage often lead to increased resistivity and degraded reliability.[150]

Consequently, the industry employs the dual damascene process, where dielectric patterns are etched first and then filled with Cu. While this bypasses direct metal etching, it relies heavily on chemical mechanical polishing, which increases costs and reduces throughput. Moreover, chemical–mechanical polishing-induced defects, such as Cu dishing and dielectric erosion, impair planarity and exacerbate RC delay.[149–152]

5.2 Recent progress in dry-etching

To address the limitations of Cu interconnects, extensive research has focused on next-generation metals such as Ru, Mo, Co, and NiCo. These materials exhibit low resistivity and, unlike Cu, can form volatile etch by-products, enabling direct dry etching.[113,153]

Ru is particularly attractive because it forms volatile RuO_4 under O_2-based plasma, allowing direct metal etching without a diffusion barrier. As shown in Fig. 15a, nearly vertical Ru lines

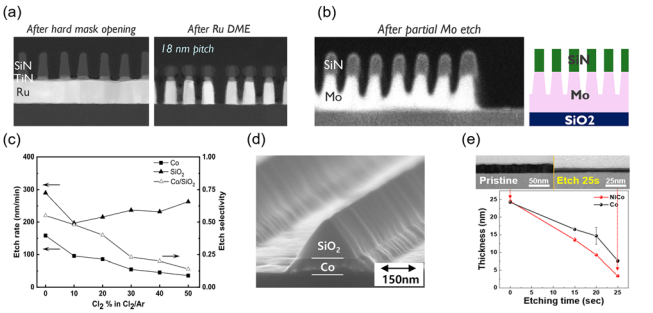

Fig. 15 (a) Cross-sectional TEM images of 18 nm pitch Ru gratings after SiN/TiN hard mask opening and after Ru direct metal etching, demonstrating nearly vertical Ru line profiles enabled by cyclic Ru etch and oxide removal processes. (b) Cross-sectional image of partially etched Mo lines after Cl_2/O_2 plasma etching, illustrating the feasibility of direct Mo patterning for ultrafine interconnect fabrication. Reprinted with permission from ref. 154. Copyright 2022, AIP Publishing. (c) Etch rates of Co thin films and SiO_2 hard masks, and the corresponding etch selectivity as a function of Cl_2 concentration in Cl_2/Ar plasma, indicating effective Co dry etching with sufficient selectivity to SiO_2. (d) Cross-sectional SEM image of Co thin films etched under Cl_2/Ar plasma conditions, confirming uniform etch profiles and direct patterning capability. Reprinted with permission from ref. 155. Copyright 2024, Elsevier. (e) SEM images and thickness evolution of NiCo thin films as a function of dry etching time under $BCl_3/Cl_2/O_2$ plasma, demonstrating controlled etching behavior and favorable etch uniformity. Reprinted with permission from ref. 86. Copyright 2025, American Chemical Society.

with an 18 nm pitch are achieved using a SiN hard mask, demonstrating excellent etch anisotropy and pattern fidelity. This capability could significantly simplify or replace conventional damascene and chemical–mechanical polishing-based processes.[154]

Mo also shows favorable etching behavior under Cl_2/O_2 plasma. Cross-sectional images (Fig. 15b) reveal well-defined trench profiles beneath a SiN hard mask, indicating that Mo can be patterned directly while preserving dielectric integrity. This expands process flexibility and enables sub-32 nm pitch interconnects with reduced process complexity.[154]

Co has similarly been demonstrated to undergo controllable dry etching. As shown in Fig. 15c, the increasing Cl_2 concentration in Cl_2/Ar plasma enhances the Co etch rate while maintaining sufficient selectivity over SiO_2. The etching mechanism (Fig. 15d) involves the formation of volatile metal chlorides, producing smooth profiles and well-defined Co/SiO_2 interfaces, in contrast to Cu.[155]

Similarly, it has been reported that NiCo alloys can be selectively dry-etched under halogen-based plasma conditions.[86] NiCo thin films were dry-etched using a BCl_3 (100 sccm)/Cl_2 (25 sccm)/O_2 (10 sccm) gas mixture at a chamber pressure of 10 mTorr, a bias power of 500 W, and a source power of 100 W. Under these conditions, the average etch rate of the NiCo thin films was approximately 0.79 nm s^{-1}. As shown in Fig. 15e, the change in the remaining metal thickness with etching time indicates that NiCo exhibits faster and more uniform etching behavior than pure Co films. Cross-sectional imaging before and after etching further confirms the improved profile control and etch uniformity. These results support the potential of NiCo as a

next-generation interconnect metal by combining favorable electrical properties with patterning compatibility.

5.3 Need for co-optimization of deposition, patterning, and reliability

In the fabrication of next-generation ultrafine-pitch interconnects, treating deposition, patterning, and reliability as independent modules has reached its practical limits. Instead, the simultaneous co-optimization of these three pillars is now indispensable for continued scaling.[156]

In conventional Cu-based damascene structures, Ta/TaN barriers and liners introduce thickness overhead that constricts the conductive cross-sectional area, directly increasing resistance. Emerging schemes, such as Ru-based barrierless interconnects, aim to eliminate this overhead. However, while the bulk Ru resistivity is typically 14.0–14.5 μΩ cm, integrated Ru lines often exceed 16 μΩ cm due to grain-size effects and enhanced interfacial scattering. This disparity highlights that material selection alone is insufficient; deposition uniformity and interfacial engineering must be co-optimized with patterning strategies to realize the full benefits of advanced metals.[157,158]

Furthermore, conventional damascene processes inevitably cause plasma-induced damage to low-*k* dielectrics. Alternative integration approaches, such as top-*via* architectures, pattern metal lines and vias first before filling them with pristine low-*k* materials or air gaps, significantly mitigating PID. While these architectures enable barrier-free integration and enhanced stability, they face mechanical challenges during chemical-mechanical polishing and potential void formation during filling. Additionally, localized patterning damage can still accelerate long-term degradation mechanisms, including electromigration and time-dependent dielectric breakdown. Ultimately, these coupled effects underscore the necessity of a holistic co-optimization approach across materials and integration schemes.[159–163]

6. Device packaging advances

6.1 AI-specific computing architectures

The rapid evolution of AI computing has fundamentally redefined interconnect requirements, shifting the primary system bottleneck from logic scaling to memory bandwidth and communication density. As shown in Fig. 16a, the training compute for state-of-the-art AI models has increased exponentially over the past decade, demanding massive parallelism across thousands of accelerators. This shift places unprecedented pressure on data movement between logic, memory, and compute nodes, making interconnect bandwidth density, latency, and energy efficiency the critical constraints for sustained AI acceleration.[164–167]

In parallel, the trajectory of microprocessors reveals the limits of logic-centric scaling (Fig. 16b). While transistor counts still follow Moore's law, single-thread performance and clock frequencies have plateaued due to the breakdown of Dennard

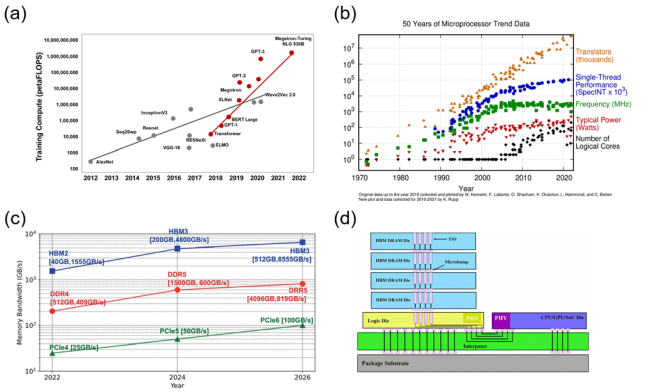

Fig. 16 System-level drivers for advanced interconnect and packaging technologies in AI computing. (a) Exponential growth of AI training compute over the past decade, highlighting the increasing demand for memory bandwidth and interconnect density. Adapted from NVIDIA GTC 2022 Keynote.[167] (b) Long-term microprocessor trends showing continued transistor scaling alongside stagnating single-thread performance and rising power consumption retrieved from Karl Rupp.[170] (c) Comparison of memory bandwidth scaling, illustrating the superior trajectory of HBM relative to DDR and GDDR for AI workloads. Reprinted with permission from ref. 172. Copyright 2024, John Wiley and Sons. (d) Schematic of 2.5D/3D integration employing TSV-based HBM stacks. Reprinted with permission from ref. 179. Copyright 2025, Springer Nature.

scaling.[9,168–171] This has forced an architectural shift toward heterogeneous integration and advanced packaging to deliver system-level performance gains.

While HBM remains the only viable path for sustaining AI workloads (Fig. 16c), its capacity limits have sparked interest in disaggregated memory systems. However, disaggregation often incurs significant latency penalties and reduced effective bandwidth, reinforcing the necessity of high-density, low-latency on-package interconnects over remote memory expansion.[172–174]

The integration of HBM relies on advanced packaging, such as TSVs and redistribution layers (RDLs), which face frequency-dependent transmission losses—from parasitic capacitance at low frequencies to inductive effects above 10 GHz. Consequently, emerging architectures are embracing 2.5D and 3D integration (*e.g.*, Intel's Foveros) to minimize interconnect length and maximize density (Fig. 16d). Moving forward, the core computer-memory fabric for AI will remain HBM-centric, supported by TSV/RDL scaling, hybrid bonding, and advanced interconnect materials tailored for nanoscale operation.[175–183]

6.2 Three-dimensional (3D) integration and vertical vias: demand for ultrathin, reliable interconnects

The success of 3D logic–memory integration depends critically on the scaling and reliability of vertical interconnects, specifically TSVs. These vias must simultaneously serve as low-resistance electrical pathways, efficient thermal conduits, and robust mechanical structures. As integration density rises, TSVs are scaling from tens of microns down to the sub-micron regime, where conventional Cu-based structures encounter intrinsic limitations.[184,185,190]

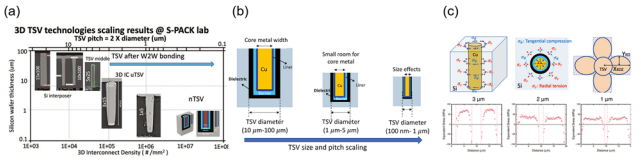

Fig. 17 Scaling challenges of through-silicon vias (TSVs) for 3D integration. (a) Evolution of TSV scaling, showing the transition from conventional microscale TSVs to ultra-thin and nanoscale TSVs with rapidly increasing interconnect density. (b) Schematic illustration of TSV miniaturization, highlighting the reduced conductive cross-section and the growing impact of barrier/liner layers at small diameters. (c) Thermo-mechanical stress distribution around scaled TSVs, demonstrating increased stress concentration and enlarged keep-out zones as the TSV diameter decreases. Reprinted with permission from ref. 186. Copyright 2024, IEEE.

Fig. 17a illustrates this aggressive scaling trajectory: while early interposers utilized 50–100 μm diameter TSVs, recent ultra-thin TSVs (uTSVs) have reached ~3 μm, with future nanoscale TSVs (nTSVs) projected to exceed a density of 10^7 mm^{-2}. However, as shown in Fig. 17b, miniaturization drastically reduces the effective conductive cross-section. While barriers and liners are negligible in wide TSVs, they consume a disproportionate volume at sub-5 μm diameters. Furthermore, Cu resistivity escalates severely due to its long EMFP of ~39 nm as classical size effects begin to dominate.[186]

Thermo-mechanical reliability further constrains scaling. The coefficient-of-thermal-expansion mismatch between Cu and Si induces significant stress in the substrate (Fig. 17c).[186] As diameters shrink, stress concentrations intensify, enlarging keep-out zones and degrading nearby transistor performance. These challenges motivate the search for Cu-replacement conductors—such as Ru, Co, or intermetallic compounds like RuAl—which possess shorter EMFP and higher cohesive energies. Such materials may enable barrier-free or ultrathin-liner integration, suppressing size-dependent resistivity while improving electromigration resistance. Ultimately, next-generation AI systems will require innovations in interconnect metals and bonding schemes to overcome these structural and material limits.[153,187–189]

6.3 Linking material choice to system-level performance and packaging requirements

The choice of interconnect materials affects not only line resistivity and electromigration resistance but also system-level performance and packaging feasibility.[191,192] As device architectures move toward chiplet integration, 3D stacking, and heterogeneous packaging, interconnects must satisfy electrical, thermal, mechanical, and process-integration requirements.

Metals with a shorter EMFP, such as Ru and Co, allow narrower interconnects without excessive resistivity scaling, reducing RC delay and energy per bit. This improves effective bandwidth and lowers latency in memory-bound architectures like HBM-enabled AI accelerators. In contrast, Cu suffers severe size-effect penalties across multiple interconnect tiers, degrading throughput and increasing power consumption.[86,121,162]

Packaging constraints further influence material selection. Redistribution layers, TSVs, and hybrid-bonded interfaces require metals that form continuous ultrathin films, adhere to diverse substrates, and remain stable under thermal cycling.[193] Barrier-free or ultrathin-liner approaches using Ru or RuAl enhance density while reducing process complexity and chip-area overhead.[187,194] Materials with higher cohesive energy and stress tolerance also improve mechanical reliability, mitigating cracks, delamination, and KOZ expansion in 3D stacks.[195]

Ultimately, interconnect materials must be evaluated in the context of packaging architectures. A metal that performs well in isolated BEOL metrics may underperform under packaging stress, whereas a slightly higher-resistivity metal may enable better system efficiency by improving bonding yields or allowing thinner barriers.[196–198] Aligning material properties with heterogeneous stacking and energy-efficient bandwidth delivery is critical to sustaining performance growth in AI systems.[4]

7. Future outlook and conclusions

The continued scaling of interconnects into the sub-10 nm regime exposes fundamental limitations of Cu-based metallization.[199] As shown in Fig. 18a, while Cu exhibits the lowest bulk resistivity among common metals, its long EMFP of 39 nm makes it highly susceptible to size-effect-induced resistivity increases.[200] In contrast, metals such as Ru, Mo, and certain intermetallic compounds possess shorter EMFPs (5–10 nm) and higher cohesive energies, reducing scattering and improving electromigration resistance. However, Fig. 18a also underscores that no elemental metal is without trade-offs: Ag suffers from agglomeration, Al lacks EM stability, W requires thick barrier/liner stacks, and Ni exhibits thermal instability. Thus,

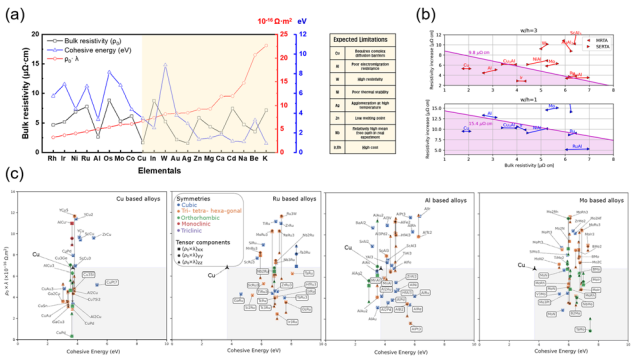

Fig. 18 Material-level limits and screening criteria for nanoscale interconnect conductors. (a) Comparison of elemental metals highlighting the trade-off between bulk resistivity, EMFP, and cohesive energy, illustrating the intrinsic limitations of Cu-based interconnects. Adapted with permission from ref. 52. Copyright 2023, John Wiley and Sons. (b) Resistivity scaling under geometric confinement for different line aspect ratios, showing that short EMFP metals and ordered intermetallic compounds maintain lower resistivity in narrow geometries. Reprinted with permission from ref. 200. Copyright 2023, American Physical Society. (c) Mapping of binary alloys and intermetallic compounds in cohesive energy–figure-of-merit space, identifying ordered compounds as favorable candidates beyond elemental metals. Reprinted with permission from ref. 87. Copyright 2025 by the authors.

bulk resistivity alone is an insufficient metric for evaluating advanced interconnect suitability.[43,57,201,202]

Geometrical confinement further amplifies resistivity challenges in nanoscale interconnects. Fig. 18b evaluates resistivity increases for varying aspect ratios using two Boltzmann transport models: the momentum relaxation time approximation (MRTA) and the self-energy relaxation time approximation (SERTA). For narrow, tall lines (w/h = 1), both models predict that Cu and Al exceed the acceptable resistivity threshold ($\sim$15 μΩ cm), rendering them unsuitable for dense interconnect routing. Conversely, short-EMFP materials like Ru, RuAl, and Mo remain below this limit. Ordered intermetallics, such as NiAl and RuAl, further benefit from suppressed alloy-disorder scattering, maintaining favorable scaling even at higher bulk resistivities.[87]

Mapping binary alloys and intermetallics in cohesive-energy *versus* $\rho_0\lambda$ space highlights the advantages of ordered compounds (*e.g.*, RuAl, NiAl, $CuAl_3$, and $ScAl_3$), which combine strong atomic bonding with low $\rho_0\lambda$, yielding robust electromigration resistance and suppressed size-effect resistivity as shown in Fig. 18c.[87] Ordered intermetallic compounds such as RuAl, NiAl, $CuAl_3$, and $ScAl_3$ cluster in a favorable region characterized by both strong atomic bonding and low $\rho_0\lambda$ values, indicating a rare combination of electromigration robustness and suppressed size-effect-induced resistivity. In contrast, disordered Cu-based alloys typically fail to reduce scattering effectively, highlighting the critical role of crystallographic order in optimizing both transport and reliability. However, it is noteworthy that the disordered phase of HCP NiCo exhibits an exceptionally small size effect, positioning it as a promising candidate for next-generation interconnect materials.

Replacing Cu with short-EMFP metals (Ru, Mo, and Co) or ordered intermetallics offers a clear path to mitigating resistivity scaling, while their higher cohesive energies enhance electromigration resistance. Complementary barrier and liner strategies remain essential: ultrathin metallic barriers, 2D layers (graphene and h-BN), and SAMs can provide angstrom-scale diffusion blocking without significantly reducing the conductive area. High-cohesion metals such as Ru and RuAl may even enable barrier-free integration, improving both density and reliability.[43,53,63,123,134,143,194,203]

From a processing perspective, deposition and etching compatibility remain critical. ALD and CVD can produce continuous Ru and Co films below 3 nm; however, stoichiometric intermetallics like NiAl and RuAl require precise chemical and crystallographic control.[13,204] On the etching side, the limited volatility of Ru and intermetallics necessitates advanced techniques such as atomic layer etching (ALE).[154,205] Thermomechanical stress also compounds resistivity penalties in narrow geometries, where high current density and thermal-expansion mismatch accelerate failure.[121,195]

Looking forward, interconnect evaluation must go beyond bulk resistivity. A refined figure of merit integrating ρ_0, EMFP, surface and grain boundary scattering, cohesive energy, and barrier thickness is needed to link material properties directly to delay, energy, and reliability. Barrier minimization emerges as a key strategy: metals and intermetallics with high cohesive energies can enable barrier-free or ultrathin-liner integration, enlarging the effective conductive area and reducing interfacial scattering. Co-optimization of materials and processes---including deposition, etching, and hybrid wafer-to-wafer bonding—will be essential to ensure manufacturability and BEOL compatibility at scale.[187,189,205]

Ultimately, no single property—low resistivity, short EMFP, or strong bonding—can define the ideal interconnect. Future nanoscale wiring will rely on the convergence of advanced conductors, ultrathin barriers (or barrier-less), and integration-aware process strategies, co-optimized to deliver high electrical performance, mechanical reliability, and manufacturability at scale.[113,192,203]

Conflicts of interest

There are no conflicts to declare.

Data availability

No primary research results, software or code have been included and no new data were generated or analysed as part of this review.

Acknowledgements

This work was supported by the Technology Innovation Program (RS-2025-02220654, RS-2025-02219463, and RS-2023-00234833) funded by the Ministry of Trade, Industry, and Energy (Korea), and the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (RS-2021-NR060141). This work was also supported by the Ajou University research fund.

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