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Flexible RRAM utilizing CdSe quantum dot–P4VP composites and graphene layers

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We developed a flexible RRAM device for neuromorphic systems using a CdSe quantum dot–P4VP (poly-4-vinylpyridine) composite with a graphene interfacial layer for superior reliability and flexibility. Exhibiting linear synaptic updates, the device achieved an 87.41% MNIST pattern recognition accuracy, showing great potential as a synaptic device for wearable AI systems.

Introduction

The rapid expansion of the Internet of Things (IoT) and advanced bio-healthcare sensors has generated an exponential increase in distributed data, creating an urgent need for edge computing to process information at its source.[1,2] This demand is particularly pronounced in wearable and implantable artificial intelligence (AI) systems, where real-time analysis is critical for health monitoring and user safety. However, progress in this field remains constrained by the von Neumann architecture, which suffers from a bottleneck between physically separated processing and memory units.[3–6] This bottleneck leads to excessive energy consumption and latency, while reliance on cloud computing introduces privacy risks, especially for sensitive biometric data.[7]

Neuromorphic computing offers a compelling alternative by emulating the brain's architecture, where memory and processing are inherently co-located within a vast network of neurons and synapses.[8] In this paradigm, synaptic devices play a pivotal role by modulating connection strength between neurons, analogous to biological learning and memory.[9,10] To serve effectively as artificial synapses, devices must meet stringent criteria: non-volatility, high integration density, low-power operation, fast switching, endurance over many cycles, and above all, linear and symmetric analogue conductance modulation.

A variety of emerging non-volatile memory devices—including flash memory, ferroelectric RAM (FeRAM), phase-change memory (PCM), magnetoresistive RAM (MRAM), and resistive RAM (RRAM)—have been explored as synaptic candidates.[11] Among them, RRAM is considered the most promising due to its simple two-terminal structure, high integration density, nanosecond switching, and analogue resistance modulation.[11–14] Furthermore, when implemented in a crossbar array, RRAM can directly perform in-memory vector–matrix multiplications (VMM) by exploiting Ohm's and Kirchhoff's laws, enabling highly parallel and energy-efficient neuromorphic operations.[13–15,39]

Despite these advantages, conventional RRAM fabricated on rigid substrates such as silicon or glass has limited utility for next-generation wearable electronics, which demand mechanical flexibility and resilience under repeated deformation.[16–20] Efforts to integrate RRAM on polymer substrates have encountered severe challenges, including thermomechanical incompatibility, interfacial delamination, and significant performance degradation under strain.[17,18] More critically, the stochastic formation and rupture of conductive filaments, the core mechanism of resistive switching, induce large variability in resistance states.[16] This variability hinders reliable multi-level conductance tuning, a fundamental requirement for neuromorphic learning.

To address these issues, hybrid nanocomposites composed of semiconductor quantum dots (QDs) dispersed in polymers have been proposed as active switching layers.[21,22] QDs provide discrete charge-trapping sites that promote more controlled filament growth, improving switching stability. However, QD-based RRAM devices have yet to demonstrate sufficient durability under mechanical stress,[23] and their synaptic performance in neuromorphic tasks has remained insufficiently validated.[24]

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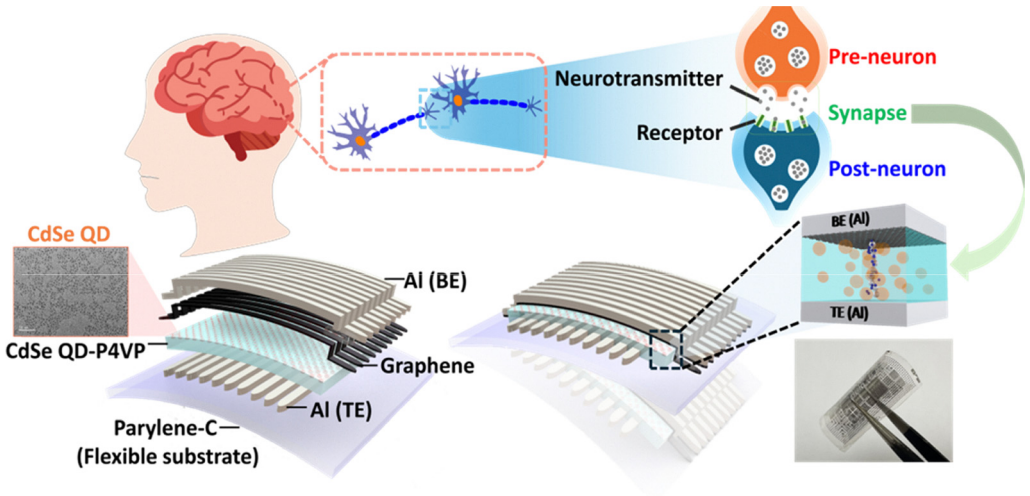

Fig. 1 Schematic illustration, structural characterization, and optical image of the CdSe QD–P4VP based flexible RRAM device. The schematic depicts the multilayer Al/graphene/CdSe QD–P4VP/Al stack on a flexible parylene-C substrate. The TEM image confirms the morphology and uniform dispersion of the synthesized CdSe QDs, while the optical photograph highlights the fabricated flexible RRAM device after integration.

As a complementary strategy, this work introduces graphene as a functional interfacial layer.[25] Owing to its atomically thin yet continuous structure, graphene can act as an effective diffusion barrier that suppresses the migration of the active electrode material into the switching medium, thereby enhancing long-term stability.[26–28,40] In addition, its mechanical compliance is expected to dissipate local stress and mitigate interfacial delamination, which are critical concerns during repeated bending.[26,28] These possible advantages are systematically examined in the following sections, where experimental results clarify how such effects manifest in practice.

In this work, we present the fabrication and systematic characterization of a high-performance flexible RRAM device that integrates a CdSe QD–P4VP (poly-4-vinylpyridine) nanocomposite switching layer with an engineered graphene interfacial layer (Fig. 1). The incorporation of QDs is shown to be critical for achieving stable resistive switching, while the graphene interlayer enhances both electrical reliability and mechanical robustness by acting as a diffusion barrier and a mechanically compliant buffer layer. Building on these materials and device-level improvements, we further demonstrate analogue synaptic functionalities with highly linear and symmetric conductance modulation. Neural network simulations based on the experimentally measured characteristics yield an MNIST classification accuracy of 87.41%, underscoring the strong potential of this hybrid device architecture as a key enabler for next-generation wearable and flexible neuromorphic systems.

Experimental

Materials

Cadmium oxide (CdO, 99.99%), selenium (Se, 99.999%), and oleic acid (OA, 90%) were purchased from Alfa Aesar. Trioctylphosphine (TOP, >85%) was purchased from TCI. 1-Octadecene (ODE, 90%) was purchased from Acros Organics. Poly(4-vinylpyridine) (P4VP, M.W. ~60 000) was purchased from Sigma-Aldrich.

Synthesis of CdSe QDs

CdSe QDs were synthesized following a modified literature method.[29] A mixture of CdO (0.102 g), OA (1.23 mL), and ODE (14 mL) was degassed under vacuum at 120 °C for 1 h in a three-neck flask. The solution was then heated to 180 °C under a nitrogen atmosphere until it became clear. Separately, Se (0.0205 g) was dissolved in TOP (0.15 mL) and ODE (2 mL). After the Cd precursor became transparent, the solution was heated to 240 °C, and the Se precursor was swiftly injected. After 1 min, the heating mantle was removed, and the reaction mixture was rapidly cooled. Methanol was added to precipitate the QDs, followed by centrifugation (6500 rpm, 10 min). The precipitate was redispersed in toluene and reprecipitated with methanol; this purification step was repeated three times.

Preparation of CdSe QD–P4VP solutions

Purified CdSe QDs were dispersed in chloroform containing 1 wt% P4VP, maintaining a QD : P4VP weight ratio of 1 : 2. The solution was stirred at 300 rpm for 30 min and briefly sonicated (10 s) to ensure homogeneous dispersion.

Fabrication of memory devices

Flexible RRAM devices were fabricated on parylene-C-coated Si substrates. A 10 μm-thick parylene-C film was deposited on a 2.5 × 2.5 cm^2 p-type Si wafer as a flexible base. A 200 nm-thick Al bottom electrode was then deposited by e-beam evaporation through a stainless-steel shadow mask (minimum linewidth 100 μm and deposition rate 0.4 Å s^{-1}). A CdSe QD–P4VP solution (0.8 mL) was spin-coated onto the bottom electrode at 5000 rpm for 40 s, followed by annealing at 85 °C for 30 min.

For devices with a graphene interlayer, CVD-grown graphene was transferred using a PMMA-assisted wet transfer process. After PMMA coating, graphene was delaminated from the Cu foil with $FeCl_3$ solution, rinsed with deionized water and dilute HF, and transferred onto the QD–P4VP layer. PMMA was

removed with acetone, and residual backside graphene was eliminated by O_2 reactive ion etching (RIE). Finally, a 200 nm-thick Al top electrode was deposited through a second shadow mask by the same method, completing the Al/graphene/QD–P4VP/Al stack. Raman spectroscopy (D/G ratio = 0.37) and sheet resistance measurements ($\sim$209 Ω sq^{-1}, CV $\approx$ 4–5%) of the transferred graphene are provided in Fig. S7 and S8 (SI).

Characterization

The synthesized CdSe QDs were characterized to evaluate their optical and structural properties. UV-vis absorption spectra were obtained using a UV-vis spectrophotometer (UV-2600i, Shimadzu), and photoluminescence (PL) spectra were recorded with a spectrofluorometer (FluoroMax Plus, HORIBA). The crystal structure was analysed by X-ray diffraction (XRD, SmartLab, Rigaku), and the chemical composition was examined by X-ray photoelectron spectroscopy (XPS, Nexsa, Thermo Fisher Scientific). Transmission electron microscopy (TEM, JEM-2010, JEOL) was employed to obtain high-magnification images, size distributions, and selected-area electron diffraction (SAED) patterns. The energy band diagram was determined using ultraviolet photoelectron spectroscopy (UPS, Nexsa, Thermo Fisher Scientific).

To investigate the structural and compositional characteristics of the fabricated devices, cross-sectional imaging and elemental analysis were performed. High-resolution cross-sectional images of the multilayer structure were obtained by spherical aberration-corrected scanning transmission electron microscopy (Cs-STEM), while elemental distributions of each thin-film layer were confirmed by energy-dispersive X-ray spectroscopy (EDS) mapping.

Electrical characterization was performed using a semiconductor parameter analyser (Keithley 4200-SCS). Direct current (DC)–voltage sweeps were conducted to evaluate resistive switching under different P4VP concentrations and device configurations (with or without QDs and the graphene interlayer). In addition, pulse measurements enabled by the same analyser were used to investigate synaptic functionalities, including long-term potentiation/depression (LTP/LTD), analogue weight updates, and system-level neuromorphic performance.

Mechanical flexibility was evaluated by programming devices into either a high-resistance state (HRS) or a low-resistance state (LRS), followed by repeated bending at a radius of 5 mm (corresponding to a 1 cm diameter). Resistance states were measured at predefined intervals to assess stability, and robustness was determined by the ability to maintain distinct HRS and LRS values after cyclic bending.

Results and discussion

Device operation results

To validate the quality of the core components, the synthesized CdSe QDs were comprehensively characterized. Fig. 2(a) shows the UV-vis absorption and PL spectra, with an excitonic absorption peak at 558 nm (bandgap 2.22 eV) and a sharp emission at 569 nm, indicative of high-quality, monodisperse QDs. The inset optical image also confirms the expected yellow emission under UV illumination. The XRD pattern (Fig. 2(b)) matches the cubic CdSe reference (JCPDS no. 19-0191), with peaks at 25.4°, 42.2°, and 49.8° assigned to the (111), (220), and (311) planes. XPS analysis further verified the Cd 3d (405.2 and 412 eV) and Se 3d (53.8 and 54.4 eV) peaks, consistent with reported values.[30,31] TEM and SAED (Fig. 2(e and f)) revealed uniformly distributed nanoparticles with high crystallinity, while size distribution analysis yielded an average diameter of 3.64 ± 0.42 nm (Fig. 2(g)). UPS measurements established the valence and conduction band edges at −6.09 eV and −3.87 eV, respectively, as shown in Fig. 2(h) and Fig. S1(SI).

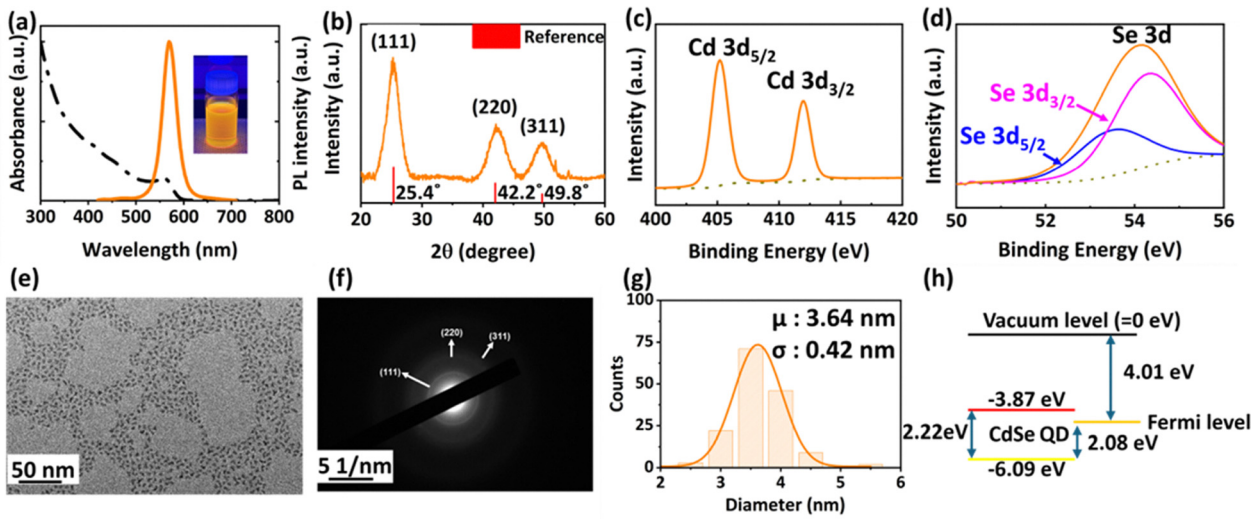

Fig. 2 Optical, structural, and electronic characterization of CdSe QDs. (a) Absorption (dash-dotted line) and PL (solid line) spectra. The inset shows a photograph of the CdSe QD solution under 365 nm UV illumination. (b) XRD pattern of the CdSe QDs (orange line) along with the JCPDS reference for cubic CdSe (no. 19–0191, red line). XPS spectra of Cd 3d (c) and Se 3d (d). (e) TEM image. (f) SAED pattern. (g) Size distribution histogram obtained from TEM analysis with a Gaussian fitting curve. (h) Energy band diagram derived from UPS measurements.

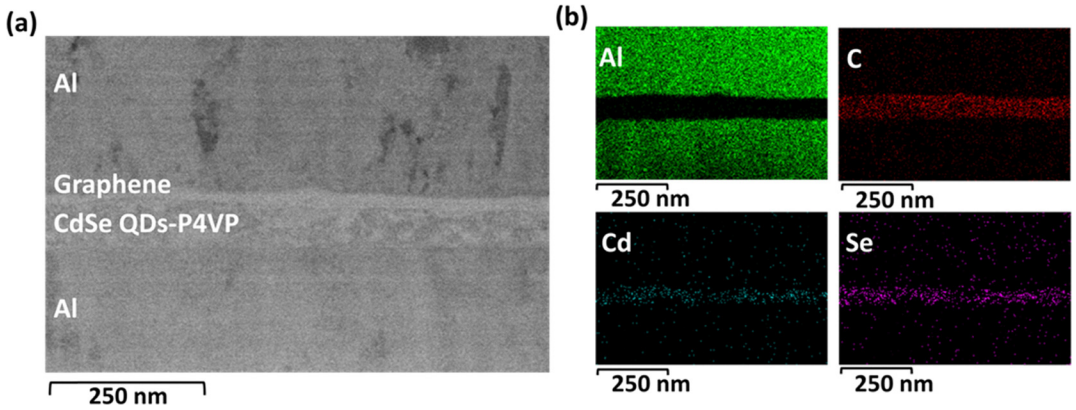

Fig. 3 (a) Cross-sectional TEM image and (b) EDS elemental maps of the fabricated Al/graphene/CdSe QD:P4VP/Al flexible RRAM device.

With the structural and optical properties of the CdSe QDs thoroughly characterized, device integration was subsequently confirmed. Cross-sectional TEM (Fig. 3(a)) clearly resolved distinct layers from the bottom to the top electrode with well-defined interfaces, while energy-dispersive X-ray spectroscopy (EDS) mapping (Fig. 3(b)) confirmed the spatial distributions of Al, C, Cd, and Se, validating the successful fabrication of the designed heterostructure.

To evaluate the effect of CdSe QDs and the graphene layer, three types of devices were fabricated: P4VP only, CdSe–P4VP without graphene, and CdSe–P4VP with graphene (Fig. 4). Devices without CdSe QDs showed no resistive switching (Fig. 4(a)), while those with CdSe QDs exhibited switching behaviour (Fig. 4(b and c)). The addition of a graphene interlayer significantly improved performance, enabling stable switching over 300 consecutive DC cycles (Fig. 4(d)), corresponding to an ~17-fold improvement in DC endurance compared with the device without graphene.

Statistical analyses further highlight the benefits of the graphene layer. The cumulative distribution function (CDF) plot (Fig. 4(e)) shows narrower LRS and HRS distributions for devices with graphene (CV = 0.43 for the HRS and 0.21 for the LRS) compared with those without graphene (CV = 0.97 and 1.07). SET and RESET voltages also became more uniform: for graphene-integrated devices, the mean SET and RESET voltages were +2.06 V and −0.85 V with standard deviations of 0.77 V and 0.37 V, whereas devices without graphene exhibited +2.78 V and −0.52 V with larger deviations of 1.09 V and 0.37 V (Fig. 4(f)). These results confirm that the graphene interlayer narrows switching distributions, improves voltage uniformity, and enhances cycle-to-cycle (C2C) stability and overall reliability.

The observed improvements can be attributed to the multifunctional role of graphene as a robust interfacial layer. Electrically, its atomically thin yet continuous structure acts as a diffusion barrier, suppressing uncontrolled Al ion migration into the QD–P4VP layer. This regulation of ion transport prevents stochastic filament overgrowth and abnormal events such as negative set or random back-switching. Mechanically, graphene provides compliance at the interface, dissipating local stress and suppressing delamination during repeated bending. Its high thermal conductivity[34] also disperses Joule heating generated during repetitive switching, reducing interfacial damage (a quantitative thermal estimation is provided in the SI). Together, these electrical, mechanical, and thermal effects promote more uniform filament formation and rupture, leading to enhanced C2C stability, improved endurance, and reliable operation under mechanical deformation.

For practical application in flexible electronics, the device was fabricated on a freestanding 10 μm-thick parylene-C film peeled from a temporary Si wafer. In the flat state, stable non-volatile memory characteristics were confirmed, with HRS and LRS retention exceeding 10^4 s and a robust on/off ratio above 10^4 at a 0.1 V read voltage (Fig. 4(g)). Mechanical robustness was further verified by cyclic bending at a radius of 5 mm: resistance states measured every 100 cycles demonstrated stable LRS retention up to 300 cycles, while maintaining an on/off ratio above 10^4 throughout (Fig. 4(h)). Together, these results establish the Al/graphene/CdSe QD–P4VP/Al/parylene-C structure as a promising platform for high-performance, flexible non-volatile memory applications. A detailed mechanical scaling analysis of the neutral plane position, strain-induced band modulation, and flexoelectric effects under bending is provided in the SI.

Switching mechanism: forming process

The forming process corresponds to the first SET operation in a pristine device. When electrons are injected in the low-voltage regime, they are readily captured by trap states at the QD surface or at the QD–polymer interface (Fig. 5(a)). Trapped charges within the CdSe quantum dots play a pivotal role in generating localized electric field enhancement. This charge accumulation establishes localized space charge regions that modify the electrostatic potential landscape of the composite film. According to Poisson's equation, the presence of such excess charges induces a redistribution of the electric field, concentrating the external field lines around the charged QDs. In addition, the dielectric mismatch between CdSe ($\varepsilon \approx 9$–10) and the P4VP matrix ($\varepsilon \approx 3$–4) further amplifies this effect through Maxwell–Wagner–Sillars interfacial polarization, causing the QDs to behave as "nano-lenses" for the applied field. A finite-element simulation (Sentaurus TCAD) supporting this field-concentration effect is provided in Fig. S4 (SI), where the

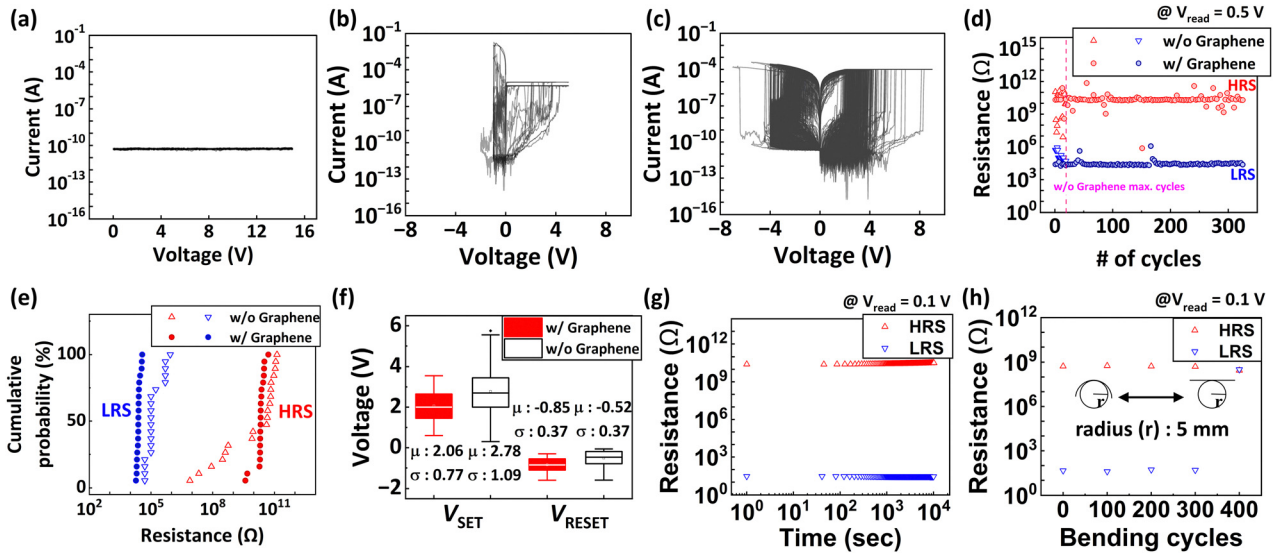

Fig. 4 Electrical characteristics of RRAM devices based on P4VP-only, CdSe QD–P4VP, and CdSe QD–P4VP with a graphene interlayer. DC current–voltage (*I–V*) switching curves for the (a) P4VP-only device, (b) CdSe QD–P4VP device without a graphene interlayer, and (c) CdSe QD–P4VP device with a graphene interlayer. (d) Endurance characteristics of the CdSe QD–P4VP devices with and without the graphene interlayer. (e) Cumulative distribution function (CDF) of the high-resistance state (HRS) and the low-resistance state (LRS). (f) Statistical distributions of the SET and RESET voltages for devices with and without the graphene interlayer. (g) Data retention properties of the graphene-integrated device. (h) Results of the mechanical bending test for the flexible RRAM device.

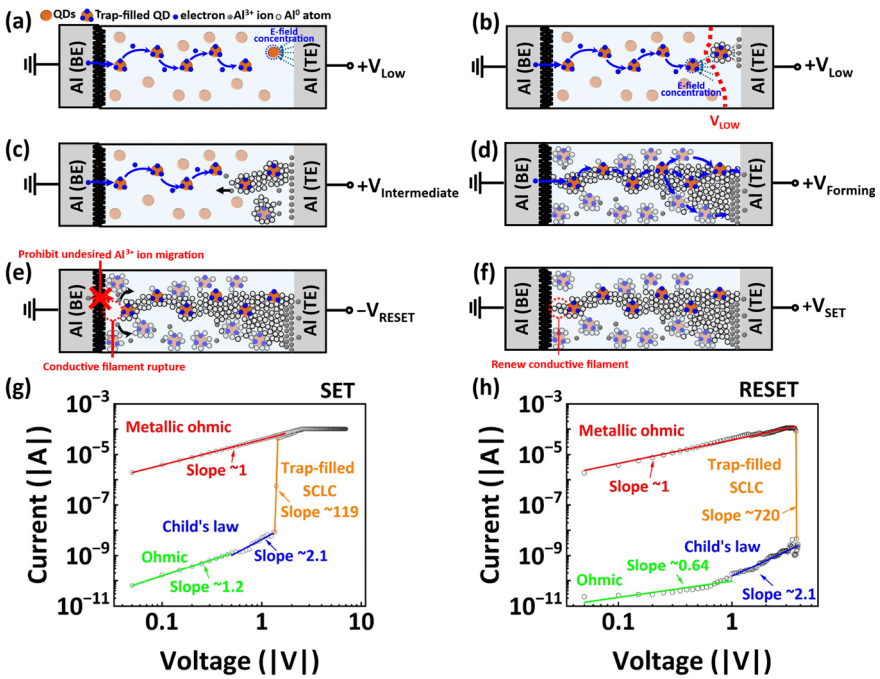

Fig. 5 Switching and conduction mechanism of the Al/graphene/CdSe QD–P4VP/Al RRAM device. Schematic illustration of the switching mechanism at various stages: (a and b) at a low positive voltage, (c) at an intermediate positive voltage, (d) during the forming process, (e) during the RESET process, and (f) during the SET process. Log–log plot of the DC *I–V* characteristics for the (g) SET and (h) RESET operations, confirming that the conduction is governed by the space-charge-limited-current (SCLC) mechanism.

maximum local electric field reaches 19.58 MV cm^{-1} around the QD–insulator interfaces.[32,33] The resulting local field enhancement significantly lowers the barrier for electrochemical oxidation of Al at the top electrode and accelerates the drift of Al^{3+} ions into the active layer (Fig. 5(b)).

Under increasing bias, these Al^{3+} ions are progressively reduced by excess electrons trapped at QD sites, leading to the formation of metallic clusters, as shown in Fig. 5(c). Filament nucleation begins near the anode, where Al oxidation occurs, and clusters coalesce as they propagate toward the

cathode under the applied field. In the final stage, the intense electric field near the cathode promotes additional cluster formation, enabling the merging of the anode-initiated filament with cathodic clusters. This bridging event establishes a continuous conductive filament spanning both electrodes, which produces the abrupt current increase observed during the forming transition (Fig. 5(d)). In this way, the synergistic effects of charge trapping and dielectric contrast not only promote localized field enhancement but also define the spatial progression of filament growth, culminating in reproducible resistive switching in the QD–polymer nanocomposite system.

In contrast, in thick polymer films without QDs, the formation of conductive filaments is strongly suppressed. First, the low trap density delays the transition to space-charge-limited conduction, limiting the extent of carrier localization. Second, the absence of dielectric contrast leads to a nearly uniform electric field distribution, preventing any specific site from reaching the critical field required for Al oxidation and ion migration. Third, without discrete QD surfaces, there are no preferential sites for the accumulation and reduction of Al^{3+} ions, making heterogeneous nucleation highly unfavorable. As a result, stable filament seeds cannot be generated; even if transient conductive paths form, they tend to disperse or rupture randomly, precluding reproducible resistive switching and leaving the device in an insulating state until dielectric breakdown occurs.

Switching mechanism: reset process

When a negative bias is applied to the top electrode, current flows through the preformed metallic filament. Due to its asymmetric geometry—thicker near the top electrode and thinner near the bottom electrode—the filament experiences a locally enhanced current density in the narrow bottom region. This results in localized Joule heating, which accelerates the re-oxidation of metallic Al^0 back into Al^{3+} and weakens the filament structure (Fig. 5(e)). The conductive path ruptures preferentially near the bottom electrode, restoring the high-resistance state. Simultaneously, the release of previously trapped charges within the QDs further suppresses carrier transport, reinforcing the RESET transition. The graphene interlayer positioned at the bottom electrode effectively blocks undesired migration of Al^{3+} ions from the BE during the RESET process, while allowing the intended filament rupture near the bottom region. This selective ion blocking facilitates a smoother transition to the high-resistance state by ensuring controlled dissolution of the thinnest portion of the filament.

Switching mechanism: set process

In contrast to the pristine forming step, the subsequent SET process after RESET is no longer dominated by nucleation but rather by filament regrowth. Residual Al clusters and partially reduced metallic remnants remain embedded between QDs after filament rupture. These residual structures serve as preferential sites for renewed filament growth under positive bias, significantly lowering the activation barrier for ion migration and reduction (Fig. 5(f)). As a result, the SET voltage in subsequent cycles is reduced compared with the initial forming voltage, and the switching dynamics become more reproducible.

Importantly, the graphene interlayer located at the bottom electrode provides both electrical and mechanical reinforcement. Electrically, its atomically thin yet continuous structure acts as a barrier that suppresses uncontrolled diffusion of Al^{3+} ions, guiding more uniform and localized filament growth. Mechanically, its compliance mitigates interfacial stress and protects the electrode–nanocomposite interface from degradation during repeated filament formation and rupture. Consequently, whereas the initial forming step is nucleation-driven, subsequent SET cycles are governed by growth-assisted filament restoration, reinforced by the stabilizing role of graphene. This combined mechanism underpins the enhanced cycle-to-cycle stability and long-term reliability observed in graphene-integrated devices. Post-switching TEM and EDS mapping across pristine, LRS, and HRS states confirmed the formation and rupture of Al-based conductive filaments, supporting the metallic Al filament mechanism (Fig. S6, SI).

Conduction mechanism

To investigate the conduction mechanism of the flexible RRAM, the DC *I–V* curves were analysed. Fitting of the log–log *I–V* curves for SET and RESET operations revealed distinct conduction regimes. During the SET operation, current transport in the HRS can be divided into three regions, as shown in Fig. 5(g). In the low-bias regime, the slope of ~ 1 corresponds to ohmic conduction, where transport is dominated by thermally generated carriers through the polymer matrix. In this region, injected carriers contribute negligibly, and no significant filament growth occurs.

As the voltage increases, the slope transitions to ~ 2, characteristic of trap-controlled space-charge-limited conduction (SCLC). In this regime, injected carriers are captured by trap states associated with the CdSe QDs, leading to localized space charge formation and internal field enhancement *via* Maxwell–Wagner–Sillars polarization. These effects facilitate the reduction of Al^{3+} ions, which are supplied not only from the anode but also from previously ruptured filament tips. The ions nucleate into metallic clusters at QD sites, progressively reconnecting fragmented conductive paths.

At higher voltages, the slope sharply increases to ~ 119, signifying the trap-filled SCLC regime. With most traps saturated, the localized electric field at the advancing filament tip becomes extremely intense, enabling rapid coalescence of metallic clusters. This process bridges the gap between partially preserved clusters and the cathode, resulting in the abrupt current surge that defines the SET transition into the low-resistance state (LRS).

Thus, the observed sequence of conduction regimes—ohmic (slope $\sim$ 1), trap-controlled SCLC (slope $\sim$ 2), and trap-filled SCLC (slope $\sim$ 119)—captures the progressive stages of the SET process: incubation by carrier injection, stepwise filament regrowth through cluster nucleation, and final bridging to restore a continuous conductive filament across the electrodes. A quantitative trap density analysis across 87 devices (3263 valid cycles), confirming that the extracted N_t remains consistently within the 10^{14}–10^{16} cm^{-3} range, is provided in Fig. S5 (SI).

In the LRS, conduction begins with metallic ohmic behaviour (slope $\sim$ 1), as shown in Fig. 5(h). During the RESET

operation, the slope abruptly increases to ~720, reflecting filament destabilization driven by localized Joule heating and Al re-oxidation. As the voltage is swept down, the slope gradually decreases to ~2, indicating trap-controlled SCLC through QD-related trap states. With a further voltage decrease, the slope returns to ~1, signifying complete filament rupture and recovery of the HRS.

Neuromorphic computing applications

To evaluate the potential of the flexible CdSe QD:P4VP-based RRAM device for neuromorphic computing applications, its synaptic characteristics were investigated using two distinct pulse programming schemes. All measurements were performed using repetitive read-SET-read or read-RESET-read sequences to observe conductance changes with high temporal resolution. For all experiments, the read operation employed a 0.5 V, 150 μs pulse with a fixed interval of 100 μs.

In the identical pulse programming (IDP) scheme, the SET and RESET operations were performed using 32 identical positive pulses (2.2 V, 5 μs) and 32 identical negative pulses (−2.5 V, 75 μs), respectively. Under these conditions, the device exhibited a characteristic sigmoidal profile of conductance modulation. During long-term potentiation (LTP), the conductance increased sharply due to the formation and strengthening of conductive filaments, followed by gradual saturation. Conversely, a symmetric decreasing trend was observed during long-term depression (LTD).

In the second scheme, incremental step pulse programming (ISPP), a linearly ramped voltage sequence was used to induce gradual conductance modulation. SET pulses ranged from +1.70 V to +2.60 V in 0.02 V steps, while RESET pulses ranged from −1.82 V to −2.76 V in −0.02 V steps. Each pulse width was fixed at 70 μs. This approach ensured a nearly constant electric field gradient, resulting in uniform and symmetric conductance modulation across both LTP and LTD processes. Consequently, the conductance change per pulse (ΔG) exhibited excellent linearity and consistency—key characteristics for analogue weight updates. The ISPP scheme enabled the reliable resolution of 48 intermediate conductance states over an ~6.5 μS window, corresponding to an effective synaptic resolution of approximately 6 bits.

The conductance modulation behaviour under IDP and ISPP is presented in Fig. 6(a) and (b), respectively. The fitted curves were employed as weight update functions to evaluate and compare the system-level on-chip learning accuracy of each scheme. To evaluate the practical utility of the fabricated devices, a classification simulation was performed using the binarized MNIST dataset. As shown in Fig. 7(a), a fully connected neural network was constructed with 784 input neurons and 10 output neurons. Each synapse was implemented using a differential pair of RRAM devices (G^+ and G^-) to represent both positive and negative weights. During training, SET or RESET pulses proportional to the error in each output neuron were applied without employing a write–verify feedback loop, reflecting a realistic on-chip learning scenario. Weight updates were directly governed by the fitted curves extracted from experimental pulse–conductance data.

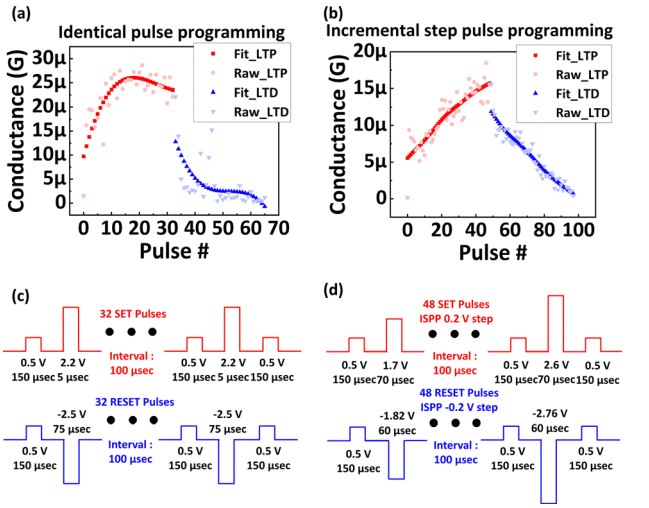

Fig. 6 Synaptic conductance modulation characteristics of the Al/graphene/CdSe QD:P4VP/Al RRAM device using (a) identical pulse programming (IDP) and (b) incremental step pulse programming (ISPP) schemes. Corresponding applied pulse sequences for (c) IDP and (d) ISPP, showing the SET (positive) and RESET (negative) pulse waveforms along with the interleaved read pulses (0.5 V, 150 μs) used for conductance monitoring.

As shown in Fig. 7(b), a classification accuracy of 73.98% was obtained using the IDP-based weight update, whereas the ISPP-

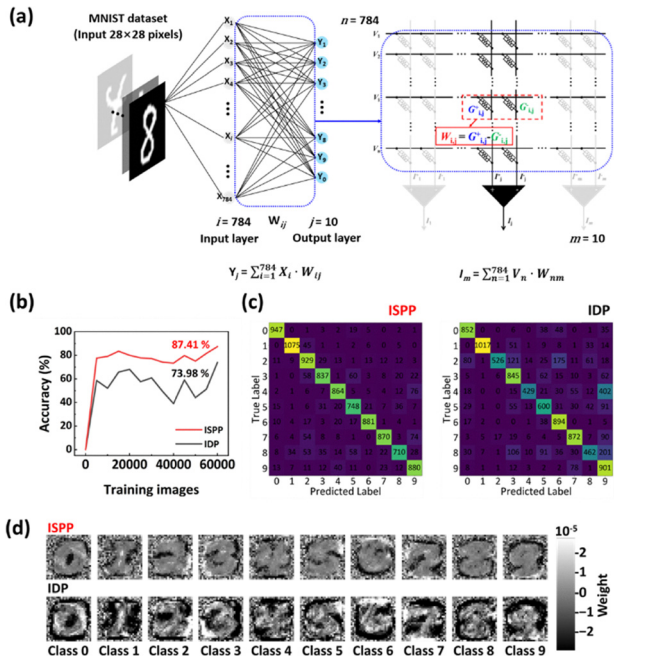

Fig. 7 Neuromorphic system simulation for MNIST classification using CdSe QD:P4VP RRAM devices. (a) Schematic of the fully connected neural network and the corresponding RRAM-based neuromorphic architecture. (b) Classification accuracy achieved using synaptic conductance modulation from both IDP and ISPP schemes. (c) Confusion matrix for the classification results after training. (d) Synaptic weight maps of the output neurons (digits 0–9) learned during training.

based approach achieved a significantly higher accuracy of 87.41%. This improvement is attributed to the enhanced linearity and symmetry of the ISPP scheme, which enabled more precise and reliable synaptic updates. The confusion matrix (Fig. 7(c)) and synaptic weight maps (Fig. 7(d)) further illustrate that ISPP-based training produced more distinct and recognizable digit features. These results experimentally demonstrate that the Al/graphene/CdSe QD–P4VP/Al-based flexible RRAM device is a promising candidate for high-performance analogue synaptic devices in neuromorphic systems. Monte Carlo simulations assessing the sensitivity of classification accuracy to device-to-device variability and read noise confirmed that the worst-case accuracy remains above 81% under realistic conditions (Tables S1 and S2, SI). The estimated synaptic update energy under ISPP conditions was approximately 4 nJ per SET pulse and 1.8 nJ per RESET pulse (SI).[35–38]

Conclusions

In this work, a high-performance flexible RRAM device based on an Al/graphene/CdSe QD–P4VP/Al structure was fabricated and systematically evaluated. The introduction of a graphene interfacial layer effectively suppressed Al ion diffusion and reduced interfacial stress, resulting in stable switching over 300 cycles and mechanical robustness after 300 bending cycles. The resistive switching behavior was explained by filament formation and rupture, governed by charge trapping in CdSe QDs and Al ion redox reactions, consistent with the space-charge-limited conduction model. Notably, the device exhibited linear and symmetric conductance modulation under incremental step pulse programming (ISPP), enabling precise analogue weight updates. A recognition accuracy of 87.41% in MNIST classification confirms its viability as a synaptic element for neuromorphic computing.

Overall, this study demonstrates the potential of integrating CdSe QDs and graphene interlayers to realize flexible, reliable, and neuromorphically capable RRAM devices for next-generation intelligent electronics.

Author contributions

B. Kim and J. Moon: conceptualization, data curation, formal analysis, and writing – original draft; S. Lee, S. Kim, H. Choi, and D. W. Park: data curation and writing – review and editing; D. Kim and Y. Kim: funding acquisition, writing – review and editing, supervision validation, and resources.

Conflicts of interest

There are no conflicts to declare.

Data availability

All data supporting the findings of this study are available within the article and its supplementary information (SI), which includes UPS analysis, TCAD electric field simulation, trap density analysis, post-switching TEM/EDS mapping, Raman spectroscopy and sheet resistance data of transferred graphene, Monte Carlo variability simulation results, and synaptic update energy estimation. Additional raw measurement data and analysis scripts are available from the corresponding author upon reasonable request. See DOI: https://doi.org/10.1039/d5tc03937a.

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