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Interface carrier transport in van der Waals heterostructures: roles of bubbles, annealing, and electric field screening

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van der Waals (vdW) two-dimensional (2D) materials are pivotal for advancing high-performance electronic and optoelectronic devices in the post-Moore era. However, their practical performance is severely limited by interface quality, which poses a critical bottleneck. Herein, we systematically investigate the electrical response of vdW interfaces under electric fields, thermal annealing, and alternating current excitation, thereby establishing a theoretical basis and technical pathway for interface optimization. Specifically, using peak force tunneling amperemeter (TUNA) atomic force microscopy (AFM), we directly observe that interface bubbles impede interlayer carrier transport in vdW heterostructures. Furthermore, thermal annealing investigations reveal a non-monotonic modulation of the rectifying behavior in the heterostructure. Additionally, electric field distribution simulations provide insights into the mechanisms for the attenuation or screening of vertical electric fields across various vdW interfaces. Overall, this work offers a rigorous, actionable framework integrating physical insights and application needs, with significant implications for precise interface design, optimized thermoelectric processing windows, and reliable integration of wafer-scale 2D material devices.

1. Introduction

van der Waals (vdW) two-dimensional (2D) materials, owing to their atomic-scale thickness, tunable bandgaps, strong light–matter interactions, and weak interlayer coupling,[1–5] have emerged as ideal candidates for next-generation electronics, optoelectronics, sensors, and quantum devices in the post-Moore era.[6–9] Their material-as-device structural advantage is particularly pronounced in applications such as heterogeneous integration, flexible electronics, and wafer-scale device fabrication.[10–13] However, interface quality hinders the transition of vdW 2D materials from laboratory prototypes to industrial-scale manufacturing. Unlike conventional semiconductors that form stable interfaces through strong covalent bonds, vdW materials rely on physical adsorption and weak interlayer interactions for stacking. As a result, their interfaces are highly susceptible to contamination from transfer residues, interface bubbles, surface impurities, and lattice mismatch.[14–17] Although these microscopic interface defects do not disrupt the crystal lattice itself, they profoundly influence carrier transport, contact resistance, band alignment, and device stability,[18–20] acting as an invisible killer that limits performance uniformity, manufacturing yield, and long-term reliability. As such, interface engineering constitutes a critical research focus for both fundamental studies and the industrialization of 2D materials.

Currently, research on vdW interfaces primarily centers on three key directions. First, the influence of interface structure on device performance. Numerous studies have revealed how interface bubbles, polymer residues, interlayer twist angles, and wrinkles influence carrier mobility,[21] band structure,[22] interlayer coupling,[23] and photoluminescence properties.[24,25] In vertical heterostructure device arrays, physical isolation at the interface can completely suppress interlayer charge transfer,[19] resulting in poor uniformity across the array. Second, the development of interface optimization strategies. Techniques such as thermal annealing,[26,27] residue-free transfer,[28–30] and ultra-flat transfer[31,32] are all pursued with the common goal of

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achieving atomically clean interfaces. Among these, thermal annealing has drawn particular interest because of its compatibility with silicon back-end-of-line (BEOL) processes. However, its narrow thermal processing window and reported side effects, such as atomic interdiffusion at elevated temperatures, present significant challenges.[33–36] Third, maintaining atomically flat contact interfaces over centimeter-scale or wafer-scale areas,[37,38] suppressing interface stress-induced structural reconstruction, and achieving spatially uniform electrical performance.[39–41] Addressing these issues represents both a frontier in fundamental research and a critical milestone for industrial-scale manufacturing.

Although significant progress has been made in understanding the relationship between interfaces and device performance, existing studies still exhibit clear limitations. Most research has focused on the behavior of interfaces and surfaces in single vdW 2D materials under electrical characterization,[21,42–44] with little systematic investigation into the co-evolution of stacked vdW interfaces under dynamic operating conditions, such as electric fields, thermal stress, or alternating current signals. In particular, at the heterostructure device level, there remains a lack of quantitative comparisons and mechanistic insights into how interface quality influences electrical stability and functional retention. Moreover, while the distribution, attenuation, and screening behavior of vertical electric fields at the intrinsic, atomically sharp interfaces of pristine vdW materials have been studied,[45,46] the corresponding behavior at artificially engineered interfaces formed during device fabrication has not been systematically explored. This knowledge gap severely hinders precise control over interface charge distribution and the rational design of band engineering strategies.

This work systematically investigates the electrical response and evolution of vdW heterostructure interfaces under various physical stimuli. First, we employ peak-force tunneling amperemeter (TUNA) atomic force microscopy (AFM) to visualize the distinct impacts of interface bubbles on interlayer carrier transport. Second, we apply controlled thermal annealing to reveal the non-monotonic evolution of rectifying characteristics. Finally, by integrating electric field distribution simulations, we systematically analyze the screening effects and field distribution characteristics across different types of interfaces. This study not only provides new insights into the intrinsic relationship between interface microstructure and macroscopic device performance but also delivers experimental evidence and practical guidance for optimizing interface engineering and enhancing reliability in wafer-scale 2D devices.

2. Experimental methods

2.1 Fabrication and characterization of vdW 2D material devices

Few-layer MoS_2 and WSe_2 were exfoliated from bulk crystals *via* mechanical cleavage and precisely stacked using a dry-transfer technique to fabricate WSe_2/MoS_2 heterostructure, respectively. Ti/Au (10 nm/100 nm) metal contacts were then deposited onto the devices using photolithography combined with electron-beam evaporation to form electrical contacts. To characterize the electrical properties of surfaces and interfaces in the 2D material heterostructure, WSe_2/MoS_2 devices were placed in an AFM system. Under peak force TUNA mode (fA-level current detection sensitivity, a noise floor below 100 fA, an amplifier bandwidth of 15 kHz, and a gain range of 10^7–10^{10} V A^{-1}), a probe bias of +3 V (positive polarity) was applied to the conductive AFM tip to acquire nanoscale maps of peak current distribution across the surface, focusing on vertical interlayer transport in the WSe_2/MoS_2 stack. Conductive AFM measurements were performed in air using SCM-PIT-V2 probes (Pt/Ir-coated, nominal tip radius $\leq$25 nm), with a peak force setpoint of 20 nN and a scan rate of 0.5 Hz. To further investigate the impact of thermal treatment on interface properties, WSe_2/MoS_2 heterostructure devices were annealed in a tube furnace under an argon/hydrogen (Ar/H_2) mixed atmosphere (67% Ar and 33% H_2, with a total flow rate of 450 sccm) at a pressure of 3 torr. The annealing was performed post-fabrication, after the deposition of Ti/Au metal contacts. Sequential annealing steps were carried out: the temperature was ramped up at 15 °C min^{-1} from room temperature to 300 °C, held for 2 hours, and then cooled naturally to room temperature. This was followed by a second annealing cycle, ramping up at 15 °C min^{-1} to 450 °C, held for 2 hours, and cooled naturally. After each annealing step, the direct current (DC) current–voltage characteristics of the devices were measured.

To evaluate rectification under dynamic conditions, alternating current (AC) characterization was performed on the same WSe_2/MoS_2 heterostructure devices using a voltage-divider configuration. A function generator delivered a clean sinusoidal voltage with peak-to-peak amplitude (V_{pp}) of 6 V and frequency of 200 Hz. The generator output impedance was set to 50 Ω with corresponding termination. The device was connected in series with a fixed load resistor of 4.7 MΩ. The voltage appearing across this load resistor (V_{out}) was acquired using one channel of a digital storage oscilloscope. The input waveform was simultaneously monitored *via* a separate channel using the same probe configuration. All AC measurements were conducted at room temperature in ambient air. Critically, the excitation conditions, 6 V_{pp} amplitude, 200 Hz frequency, 4.7 MΩ load, and probe configuration, were kept identical for the as-fabricated device and after each annealing step (300 °C and 450 °C), ensuring that any observed changes in output waveform shape and rectification quality arise solely from modifications to the heterostructure interface rather than variations in the measurement setup.

2.2 Electric field distribution simulation at interfaces of vdW 2D materials

In this work, we adopt a simplified electrostatic model in COMSOL Multiphysics to investigate the spatial distribution of the effective electric field under an externally applied vertical electric field. While a fully atomistic description would require first-principles calculations, our framework approximates the

strong intra-layer covalent bonding (S–Mo–S in MoS_2 and Se–W–Se in WSe_2) by placing fixed positive and negative charge densities at discrete planes corresponding to the atomic positions within each monolayer. Specifically, each monolayer is modeled as a 0.67 nm thick slab (approximating the interlayer spacing in bulk TMDs). In COMSOL Multiphysics simulations, the charge distribution within 2D TMD layers is modeled as a uniform surface charge density (σ), applied to infinitesimally thin boundary planes positioned at the atomic layers within the structural slab. Specifically, for an N-type MoS_2 layer, a positive surface charge density (σ_{Mo}) is applied to the central plane (the Mo atomic layer), while negative surface charge densities (σ_S) are applied at symmetric positions above and below (corresponding to the top and bottom S atomic layers, respectively). Conversely, for a P-type WSe_2 layer, an opposite charge polarity configuration is adopted: a negative surface charge density (σ_W) is applied to the central plane (the W atomic layer), and positive surface charge densities (σ_{Se}) are applied at the positions of the Se atomic layers above and below. To ensure overall electrical neutrality for each material, the net charge within each unit cell is zero, satisfying the conditions $\sigma_{Mo} + 2\sigma_S = 0$ and $\sigma_W + 2\sigma_{Se} = 0$. The magnitude of these sheet charges is chosen to reproduce the known macroscopic dielectric constant of the material ($\varepsilon_r \approx 4$ for multilayer MoS_2 and similar for WSe_2), calibrated such that the internal electric field oscillations and average screening match reported values from literature for pristine vdW layers. The interlayer regions (either vdW gap in homostructures or the tunable air gap emulating bubbles in heterostructures) are treated as vacuum ($\varepsilon_r = 1$) with zero charge density. By capturing the key features of our model, we avoid the need to impose complex boundary conditions. Although the entire structure is three-dimensional, the bubble is sufficiently large in the x–y plane. We can therefore approximate the bubble as infinitely extended when investigating the electric field distribution inside it. This allows the full three-dimensional structure to be studied using a one-dimensional model, in which the two directions perpendicular to the one-dimensional axis are treated as infinitely large by default in the software. This is equivalent to applying periodic boundary conditions in three-dimensional space.

This fixed-sheet-charge representation is appropriate and advantageous for the dielectric screening problem under consideration for several reasons. First, it captures the essential physics of polarization screening in layered vdW materials without requiring computationally intensive atomic-scale resolution: the discrete charge planes mimic the strong intra-layer dipoles and polarization response, leading to periodic oscillations of the electric field inside each monolayer (as observed in our results) and effective attenuation of the field across multiple layers, consistent with macroscopic dielectric behavior. Second, this approach directly highlights the role of dielectric contrast (high-ε_r TMD *vs.* low-ε_r air/vacuum) in voltage division and field enhancement/dilution within bubbles, which is the key mechanism we aim to elucidate. Unlike purely macroscopic models that treat each layer as a uniform dielectric without internal structure, our method retains some microscopic character (layered charge separation) to better reproduce the non-monotonic field behavior in the air gap as its thickness varies from sub-nm to tens of nm.

3. Results

3.1 Classification of interfaces in vdW 2D materials

Interfaces in vdW 2D materials can be broadly categorized into intrinsically atomically sharp interfaces (Fig. 1a) and artificially engineered interfaces (Fig. 1b and c). Intrinsic atomically sharp interfaces are typically obtained by mechanical exfoliation of bulk crystals and exhibit atomic-level flatness and exceptional cleanliness, serving as an ideal benchmark for evaluating the intrinsic performance of devices. In contrast, artificially engineered interfaces are formed during transfer, stacking, and micro/nanofabrication processes, which often introduce interface contaminants (Fig. 1b) and structural defects (Fig. 1c). Contaminants primarily originate from residues of transfer media, environmental adsorbates, or impurities introduced during processing atmospheres. Structural defects often arise from lattice imperfections inherent to chemical vapor deposition (CVD) growth or from localized damage induced by subsequent microfabrication steps. This work systematically investigates the evolution of electrical behavior in these distinct interfaces under the combined influence of electric and thermal fields. We focus on elucidating their differential impacts on key performance metrics, including carrier transport efficiency, rectification characteristics, and electrical stability. The findings aim to provide theoretical

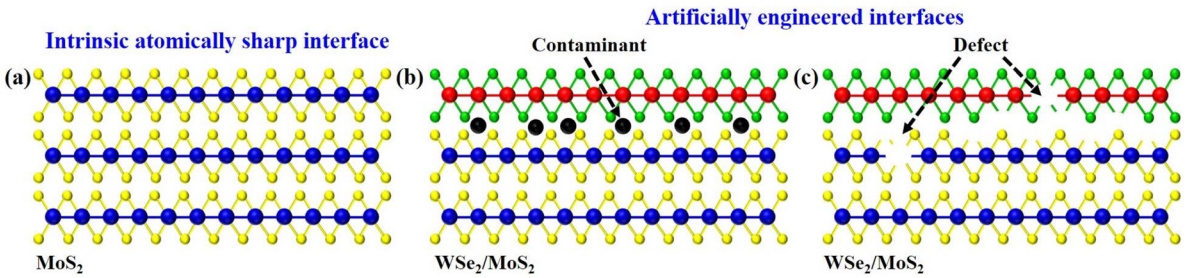

Fig. 1 Classification of interfaces in vdW 2D materials. (a) Intrinsic atomically sharp interfaces. (b and c) Artificially engineered interfaces, including interface contaminants and interface defects.

insights and design guidelines for interface engineering toward high-performance and highly reliable vdW 2D material devices.

3.2 Correlation between interface quality and surface peak current in vdW 2D material heterostructure

WSe_2/MoS_2 vdW heterostructure devices containing interface bubbles were fabricated on SiO_2/Si substrate using standard photolithography patterning followed by metal evaporation and lift-off processes. These bubbles, unintentionally introduced during mechanical exfoliation and dry-transfer stacking of the 2D flakes, serve as natural testbeds for probing the sensitivity of interlayer charge transport to nanoscale interface imperfections. To quantitatively assess their impact, the devices were characterized using conductive AFM operated in peak force TUNA mode, which enables simultaneous acquisition of topographical and nanoscale current maps with high spatial resolution and minimal sample damage.

In the measurement configuration schematically depicted in Fig. 2a, which illustrates the electrical setup with tip bias on WSe_2 and grounding on MoS_2 to probe vertical transport, a +3 V bias (positive polarity) was applied to the conductive AFM tip in contact with the top WSe_2 layer, while the underlying MoS_2 flake was electrically grounded through a metal contact. The resulting AFM topography (Fig. 2b) clearly reveals three well-defined interface bubbles labeled 1, 2, and 3, with vertical heights of 24.5 nm, 26.4 nm, and 29.2 nm, respectively. Critically, the corresponding peak current map (Fig. 2c), acquired concurrently under identical conditions, shows a complete absence of measurable current (0 pA) across all three bubble regions. In stark contrast, the surrounding flat regions exhibit robust and spatially uniform conduction, confirming that the loss of current is directly correlated with the presence of the bubbles rather than material degradation or contact failure.

While a monolayer of WSe_2 or MoS_2 is only approximately 0.7 nm thick, bubble-induced gaps reaching tens of nanometers in height create separations over 30 to 40 times larger. These distances (24.5–29.2 nm) far exceed the decay length of electronic wavefunctions in 2D semiconductors, effectively eliminating interlayer orbital hybridization. To quantify this, consider a simple rectangular barrier tunneling model where the transmission probability P scales as $\exp(-2\kappa d)$, with decay constant $\kappa \approx \sqrt{2m\varphi}/\hbar$. Using reasonable parameters for TMD–air interfaces (effective mass $m \approx$ electron mass, barrier height $\varphi \approx 4$ eV based on work functions), $\kappa \approx 10\ \mathrm{nm}^{-1}$. Assuming Δd corresponds to a characteristic bubble height of 26.4 nm, the calculation yields $\exp(-\approx 528) \approx 10^{-229}$, corresponding to a suppression of the tunneling probability by more than 200 orders of magnitude. This estimate, while approximate and neglecting factors like effective mass renormalization or band structure details, confirms the near-total transport suppression observed in the current maps. Consequently, the vertical current is nearly extinguished in these regions, this complete suppression of vertical current in bubble regions suggests that the large separations strongly inhibit interlayer orbital overlap and tunneling. Achieving atomically clean, conformal, and flat interfaces throughout the heterostructure stack is therefore not merely an ideal but an absolute prerequisite for unlocking the intrinsic electronic and optoelectronic properties of 2D materials.

3.3 Correlation between interface quality and electrical properties of vdW 2D material heterostructure under thermal annealing treatment

Thermal annealing is a well-established and effective technique for cleaning surfaces and interfaces in vdW 2D heterostructures, and it is fully compatible with BEOL processes in silicon-based integrated circuit fabrication.[26,27,38] In this work, WSe_2/MoS_2 vertical heterostructure diodes were fabricated *via* standard photolithography and metal deposition, followed by post-fabrication annealing in a tube furnace under an Ar/H_2 ambient at varying temperatures.

Current–voltage characteristics were systematically measured at three stages: as-fabricated (before annealing), after annealing at 300 °C, and after annealing at 450 °C, as summarized in Fig. 3a, with each based on a single forward–reverse sweep from −3 V to +3 V. The as-fabricated device exhibited poor electrical performance, delivering only 0.05 nA at +3 V with a modest rectification ratio of approximately 5,

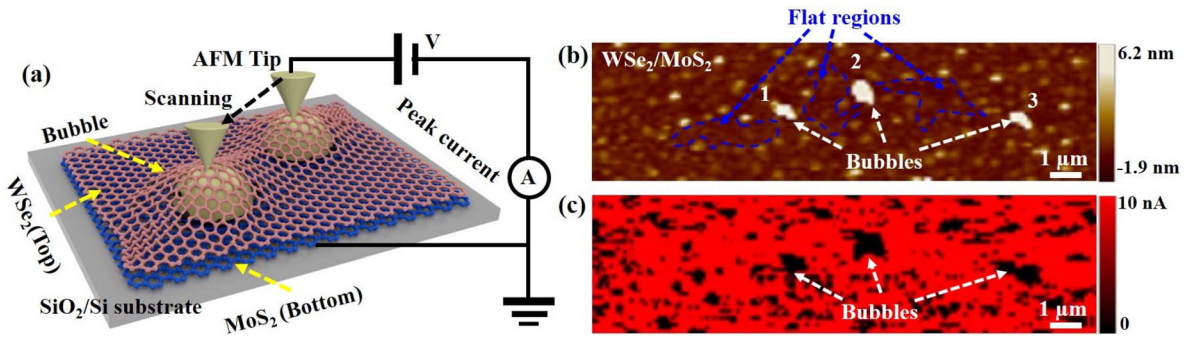

Fig. 2 Surface current distribution characteristics of vdW 2D material heterostructures. (a) Schematic illustration of surface current measurement on a vdW heterostructure with interface bubbles. (b and c) AFM topography and corresponding surface peak current map of a WSe_2/MoS_2 heterostructure.

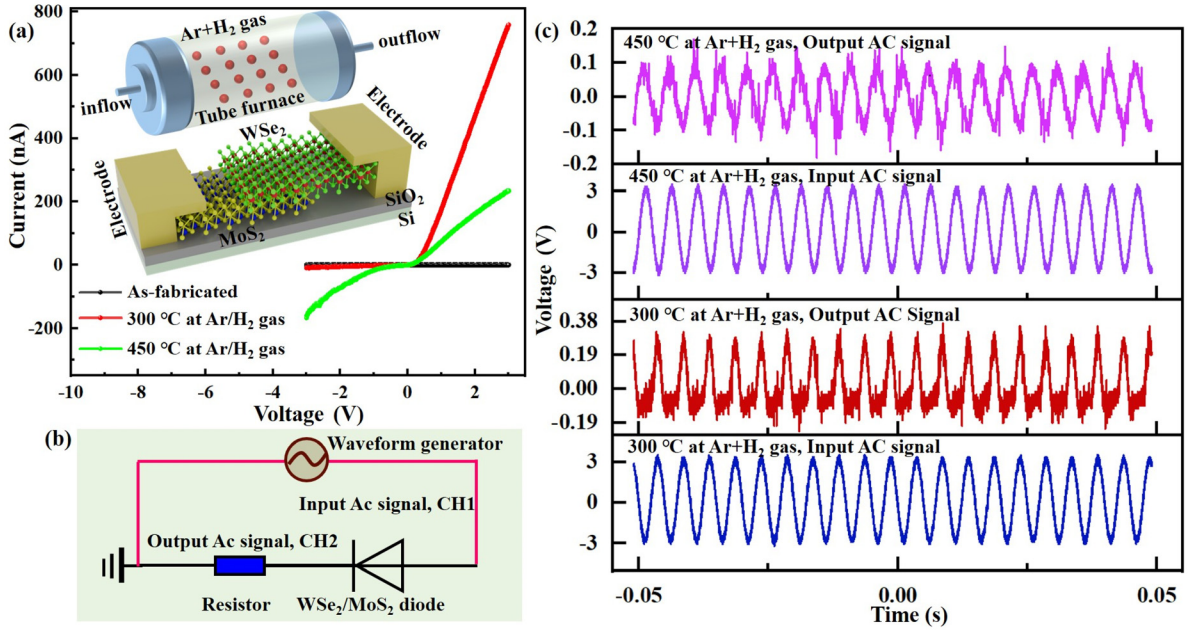

Fig. 3 Thermal annealing induced interface evolution in WSe_2/MoS_2 heterostructure and its impact on rectification behavior. (a) Current–voltage characteristics measured after annealing at different temperatures. The upper inset presents a schematic of the annealing process in a tube furnace, while the lower inset depicts the structural layout of the WSe_2/MoS_2 device. (b) Circuit configuration for AC signal testing of the heterostructure diode. (c) Output signal waveforms recorded under identical sinusoidal input conditions, highlighting the pronounced degradation of rectification performance after high-temperature annealing.

defined as the ratio of forward current $I(+3\ \mathrm{V})$ to the absolute reverse current $|I(-3\ \mathrm{V})|$ without averaging over multiple sweeps. Upon annealing at 300 °C, the forward current surged by over four orders of magnitude to 758.7 nA at +3 V, and the rectification ratio improved dramatically to 85 using the same calculation, clear hallmarks of a functional p–n junction with strong forward conduction and effective reverse blocking. This marked enhancement is attributed to the thermal removal of residual polymers from the transfer process and potential migration and coalescence of interface bubbles, hypothesized based on improved carrier transport and prior reports,[26,27] which could collectively yield a cleaner, more intimate, and atomically flat vdW interface.

However, further increasing the annealing temperature to 450 °C led to significant performance degradation: the current at +3 V dropped to 234 nA, and the rectification ratio collapsed to just 1.4. This deterioration is consistent with prior reports of thermally activated atomic interdiffusion in heterostructures,[33–36] though our attribution relies on electrical evidence rather than direct materials characterization. We hypothesize two interrelated potential mechanisms: first, interdiffusion of chalcogen atoms (Se and S) across the WSe_2/MoS_2 interface, blurring the p–n junction; second, diffusion of metal atoms, notably Ti from the contacts, into the semiconductor channels, introducing defects. To validate the above assertion, future work should employ characterization techniques to visualize interfacial intermixing or profile elemental distributions. Together, these processes reconstruct the interface energy landscape, suppress the built-in electric field, and render carrier transport nearly symmetric, effectively transforming the diode into an ohmic-like or quasi-homogeneous junction. While these single-sweep results highlight clear trends, repeat *I–V* sweeps (at least two per condition) would be valuable in future studies to address potential hysteresis, such as differences between forward and reverse scans due to trapping, or stability issues, ensuring the observed degradation is reproducible and not sweep-dependent.

To further confirm the evolution of junction asymmetry observed in DC measurements, AC rectification tests were performed under identical excitation conditions as detailed in section 2.1. A 6 V peak-to-peak, 200 Hz sinusoidal input was applied across the series combination of the heterostructure diode and a 4.7 MΩ load resistor (Fig. 3b). The voltage developed across the load (V_{out}) and the input waveform were recorded concurrently on the oscilloscope. As shown in Fig. 3c, the device annealed at 300 °C produced a clear half-wave rectified output, whereas the waveform after 450 °C annealing closely followed the input sinusoid, indicating near-complete loss of rectifying behavior.

These results underscore a critical trade-off in thermal processing of 2D heterostructures. Moderate annealing, such as at 300 °C, optimizes interface quality and unlocks high-performance diode behavior, whereas excessive temperatures may trigger detrimental interface intermixing that irreversibly degrades electronic functionality. Therefore, precise control of annealing parameters, particularly temperature and ambient atmosphere, is essential for harnessing the full potential of vdW heterostructures in next-generation electronic and optoelectronic applications.

3.4 Electric field distribution at interfaces of vdW 2D materials

Fig. 4 presents a high-precision electrostatic model developed using COMSOL Multiphysics to investigate how the size of interface bubbles influences the spatial distribution of the effective electric field in vertically stacked vdW 2D heterostructures. In contrast to existing theoretical studies in the literature,[45,46] which typically focus on ideal, defect-free, single-component systems such as pristine MoS_2 or graphene, our work innovatively introduces a tunable air gap to emulate the interface bubbles commonly present in real devices. We investigated the MoS_2/MoS_2 homostructure and the WSe_2/MoS_2 heterostructure, respectively. In our model, positive and negative charges are fixed at their respective atomic lattice sites (S–Mo–S or Se–W–Se), and each monolayer is assigned a thickness of 0.67 nm, enabling the macroscopic continuum framework to effectively capture atomic-scale charge polarization characteristics.

In the MoS_2/MoS_2 homostructure (Fig. 4a), under an externally applied vertical electric field, the effective electric field within the air gap exhibits pronounced size dependence. When the gap is extremely small (for example, 1 nm), the electric field in the gap is significantly higher than the average field inside the adjacent MoS_2 layers. As the gap widens, this field gradually decreases and, beyond a transition gap thickness of approximately 41 nm, drops below the field strength (Mo atom) inside the MoS_2 layers on either side. This behavior can be understood through dielectric voltage division. MoS_2 possesses a relatively high relative permittivity ($\varepsilon_r \approx 4$),

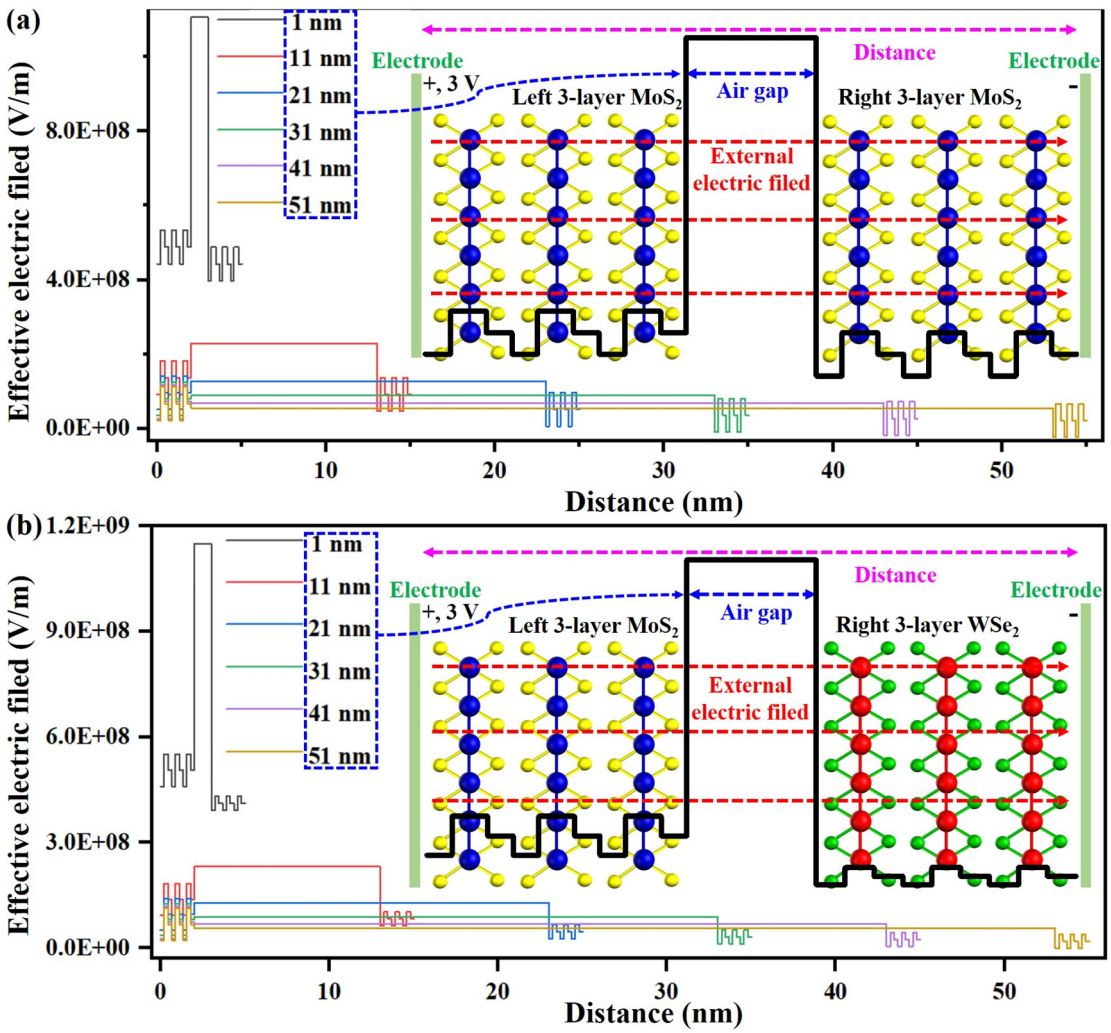

Fig. 4 Effective electric field distribution at vdW 2D material interfaces. (a) Spatial distribution of the effective electric field in a MoS_2/MoS_2 homostructure under an externally applied vertical electric field, for air gap thicknesses ranging from 1 to 51 nm (discrete preset values). The inset illustrates the localization of charges within the S–Mo–S atomic layers. The electric field inside MoS_2 exhibits periodic oscillations, while the field in the air gap shows a non-monotonic evolution with increasing gap thickness. (b) Spatial distribution of the effective electric field in a WSe_2/MoS_2 heterostructure under an externally applied vertical electric field, for air gap thicknesses from 1 to 51 nm. The inset illustrates the localization of charges within the Se–W–Se atomic layers. Both MoS_2 and WSe_2 display periodic field oscillations internally, while the electric field in the air gap again exhibits a non-monotonic dependence on the gap size.

whereas air has a much lower one ($\varepsilon_r \approx 1$), so the entire structure can be viewed as a series capacitor network composed of high-ε_r (MoS_2) and low-ε_r (air) layers. According to basic electrostatics, under fixed free-charge conditions, the electric field E is inversely proportional to the dielectric constant ε, but also depends on the layer thickness d ($E = \Delta V/d$). When the air gap is ultrathin, its small thickness dominates over its low permittivity, resulting in an exceptionally high potential gradient, that is, a strong electric field, across the gap. As the gap widens, the air layer accommodates most of the applied voltage drop; however, because its thickness simultaneously increases, the electric field intensity actually diminishes. Once the gap exceeds approximately 41 nm, the air layer becomes the dominant voltage divider, and its electric field becomes significantly diluted. Meanwhile, the internal effective field in the MoS_2 layers is further suppressed by their intrinsic polarization screening. Consequently, the field in the air gap eventually falls below that inside the MoS_2 layers. This entire process is driven purely by geometric dimensions and dielectric contrast, without involving built-in fields or band engineering, clearly illustrating the fundamental physical picture in vdW materials: thickness dictates screening capability.

In contrast, the WSe_2/MoS_2 heterostructure exhibits a distinctly different evolution of the electric field (Fig. 4b). Although the air-gap field is also initially high for small gaps, as the gap increases beyond approximately 21 nm, the field continues to decrease but remains higher than the field (W atom) inside the right WSe_2 layer, even as it drops below that in the left MoS_2 layer. This difference is consistent with the presence of a built-in electric field arising from band alignment mismatch between the two materials. This built-in field vectorially superposes with the externally applied field: in the WSe_2 region, the two fields oppose each other, further suppressing the effective internal field, whereas in the MoS_2 region, they align, leading to a relatively enhanced field. As a result, even as the air gap thickens and its own field weakens, the electric field in the WSe_2 region remains pinned at a low baseline level, preventing the air-gap field from ever falling below it. In realistic heterostructures containing interface bubbles, our results quantitatively reveal how band engineering, *via* the built-in field, can actively modulate the macroscopic electric field distribution. This provides a novel physical mechanism and an additional design degree of freedom for developing next-generation electric-field-sensitive devices, such as asymmetric tunneling transistors, photodetectors, and reconfigurable logic units.

While the present simulations provide valuable insights into the role of bubble height in modulating vertical electric field distribution *via* dielectric contrast and geometry, several simplifications should be acknowledged. First, the interlayer air gap is treated as vacuum ($\varepsilon_r = 1$) with no trapped residues or adsorbates. In practice, many interface bubbles contain residual transfer media, water vapor, or organic contaminants that elevate the local permittivity (potentially $\varepsilon_r = 2$–4), which would reduce the dielectric contrast with the surrounding TMD layers ($\varepsilon_r \approx 4$) and thereby weaken the pronounced field enhancement observed for small gaps and the rapid field dilution for larger gaps. In future investigations, parametric sweep analysis of the gap permittivity should be performed to demonstrate how the conclusions would be affected when the gap medium deviates from vacuum-like characteristics.

Furthermore, although the model effectively elucidates dielectric voltage division and built-in field effects, it is oversimplified and neglects key quantum aspects significant in 2D systems. For instance, quantum capacitance arising from the density of states in ultrathin layers is omitted, potentially underestimating field screening at low biases. Similarly, layer-dependent dielectric screening, where effective ε_r varies with thickness due to electronic polarization, is not considered, as our homogeneous assumption treats multilayers uniformly. These limitations stem from the simplified electrostatic model, which prioritizes macroscopic insights over *ab initio* accuracy, and could be addressed in future work with more detailed boundary conditions, adaptive meshing, and hybrid quantum-classical solvers.

4. Conclusions

This study highlights the pivotal role of interface quality in vdW 2D heterostructures as a fundamental bottleneck that constrains the performance of next-generation electronic and optoelectronic devices. To address the interface challenges impeding wafer-scale integration in the post-Moore era, the authors systematically probe the electrical responses and dynamic evolution of vdW interfaces under realistic operating conditions, including applied electric fields, thermal annealing, and AC excitation. Using peak force conductive AFM, they directly image interface bubbles and demonstrate their pronounced suppression of interlayer carrier transport. Thermal annealing experiments reveal a non-monotonic dependence of rectification behavior on annealing temperature. Moreover, by combining experimental insights with electric field distribution simulations, the study elucidates how distinct interface types differentially attenuate or screen vertical electric fields. Beyond advancing the fundamental understanding of interface physics in vdW systems, this work establishes a robust, theory-informed yet practically oriented framework for precision interface engineering, rational design of thermal–electrical processing windows, and high-yield, reliable integration of wafer-scale 2D material devices.

Author contributions

Jianwei Chen and Yajie Guo conceived the idea and initiated the present study. Yajie Guo, Yike Zhao, and Bo Tian carried out the main experiments. Wuwei Feng offered suggestion in analyzing the data. Yike Zhao and Bo Tian carried out the simulation. Jianwei Chen, Yajie Guo, and Jun Jiang wrote the manuscript.

Conflicts of interest

The authors declare no competing financial interest.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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