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EPE contribution analysis method of multiple patterning lithography by Monte Carlo and Sobol sensitivity analysis

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As critical dimensions shrink in new semiconductor technologies, process margins become tighter. With the introduction of multiple patterning schemes, the edge placement error (EPE) analysis becomes more important than ever to assess and maintain in-line process performance and yield. In this work, the EPE contribution analysis method of a multiple litho-etch (LE) patterning process is proposed. A process flow model of quadruple patterning is built to simulate the effect of each step's impact on the after-etch-inspection (AEI) contour. Under different process conditions, profiles with different critical dimensions (CDs) on the resist can be obtained. In the step of spacer deposition, the parameters of the deposition process, such as the thickness and lateral ratio, have a significant impact on the contour of AEI. For the etching process, there is usually a situation where the top and bottom dimensions are not consistent. The distribution of the AEI under these conditions is statistically analyzed by Monte Carlo and Sobol sensitivity analysis. The contribution levels of different parameters on AEI CDs and spaces are analyzed based on Sobol sensitivity analysis. The results indicate that the impact of the after-develop-inspection (ADI) contour is the greatest, and the contribution levels of the parameters in deposition and etching processes are relatively close. The impact of the overlay is mainly reflected in the distribution change of the spaces. Under the given EPE budget conditions, the error budget for each parameter can be obtained to guide the direction of improving the processes.

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1 Introduction

In the field of integrated circuit manufacturing, edge placement error (EPE) refers to the deviation between the actual edge of a pattern on the wafer and its intended position as designed.[1,2] With the development of chip manufacturing technology, the importance of EPE significantly increases, becoming a core factor that affects chip performance, yield, and reliability.[3] In advanced processes at 3 nm and below, the transistor feature size is approaching atomic levels,[4] and even small deviations in EPE can lead to quantum tunneling effects, increased leakage current, or threshold voltage fluctuations,[5,6] directly impacting transistor performance.[7] At the same time, as the pitch of metal interconnects shrinks to below 20 nm, EPE can cause critical dimensions (CDs) or alignment deviations, significantly increasing resistance and even leading to shorts or open circuits. For example, the resistivity of cobalt interconnect material is more sensitive to EPE at smaller dimensions.[8]

Advanced processes require multiple patterning techniques (MPTs) to overcome the resolution limits. Through multiple exposures and pattern transfer, finer patterns and smaller pitches can be achieved. The accuracy of the alignment system in the lithography machine directly impacts the alignment error of multi-layer patterns. Alignment errors can lead to the accumulation of inter-layer EPE.[9]

In advanced integrated circuit manufacturing, the factors influencing EPE are numerous and complex,[10] involving multiple aspects such as lithography, etching, materials, and equipment.[11] First, the characteristics of the light source and mask play a crucial role. The wavelength and intensity uniformity of the light source, as well as the accuracy of the mask pattern, directly affect the quality of the lithographic imaging. Furthermore, during the lithography process, the shape of the light source, diffraction, interference, lithography lens and mirror aberrations can cause the pattern edges to deviate from the design values. The accuracy of the photoresist model also contributes to fluctuations in the final EPE level. The mask CD control and registration will directly affect the EPE. The EPE is highly sensitive to the alignment precision, especially in multi-layer structures, where the cumulative effect of alignment errors is significant. Due to the need for unsymmetrical features and etch correction, the accuracy of optical and resist models also has a significant impact on the EPE.

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The second major factor is the impact of etching. During etching, the uniformity of the plasma, the distribution of etching gases, and the control of etching time all influence the position of the pattern edges. Non-uniform etching can lead to edge position deviations. The etching selectivity between different materials can affect the sidewall profile and edge position. Insufficient selectivity can cause sidewall tilting or indentation, increasing EPE.

The third factor is design rules and physical design layout. The reasonableness of design rules directly affects the manufacturability of the patterns. In addition, the cumulative effect of process variations during production should not be underestimated, especially in large-scale manufacturing, where even small deviations can be amplified in high volume production.

EPE has become increasingly critical as technology nodes scale toward 3 nm and beyond. In this work, we use a 7 nm process setting as a representative advanced-node case to analyze the contribution of different EPE factors. We propose an EPE analysis method for multiple exposure processes. For the V0 layer in the middle of line of 7 nm manufacturing, a Monte Carlo method was used to analyze the EPE factors and their sensitivities. By analyzing the contributions and sensitivities of these factors, important theoretical support can be provided for optimizing the manufacturing process, improving chip performance, and enhancing yield. Understanding the sensitivity of each factor helps to identify the optimal process parameters during production, reduce manufacturing errors, optimize process flows, and improve yield, which can be described quantitatively by the Sobol sensitivity analysis.[12] For smaller technology nodes such as 3 nm, the same factors may exhibit stronger sensitivities due to reduced process windows and tighter overlay budgets, and extending the analysis to a 3 nm process model is an important direction for future work.

2 Quadruple patterning process flow

The V0 layer requires four LE processes, as shown in Fig. 1. We will provide a detailed explanation of the process integration for the first litho-etch flow here. Our process simulations are also conducted based on this flow, followed by subsequent EPE analysis.

Step 1: ILD0 TEOS deposition (initial layer deposition).

TEOS is deposited as an interlayer dielectric (ILD) layer using a Low-Pressure Chemical Vapor Deposition (LPCVD) method. This layer is used for isolating different metal layers in multilayer ICs. It provides initial insulation between active devices in the process stack.

Step 2: chemical spin-on hardmask coat.

A chemical spin-on hardmask (CSOH) layer is applied. This layer is designed to withstand subsequent etching steps and define patterns for the underlying layers. It provides a protective and patterned etch mask for the etching of deeper layers.

Step 3: V0 PECVD AlOx memorization hardmask deposition.

A thin layer of aluminum oxide is deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD). This layer acts as a hardmask for the memorization step. AlOx is used to protect certain regions of the wafer during subsequent etching or ion implantation processes.

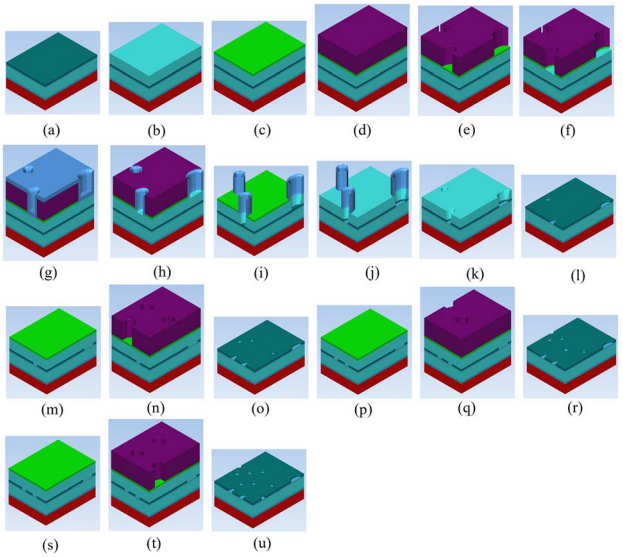

Fig. 1 The schematic diagram of quadruple patterning process flow. (a) Hardmask deposition. (b) CSOH coat. (c) SiON coat. (d) Resist coat. (e) $Mask_1$ lithography. (f) SiON etch. (g) Shrink spacer deposition. (h) Shrink spacer etch. (i) Resist and CSOH etch. (j) Hardmask etch. (k) Shrink spacer over etch. (l) CSOH ASH. (m) Coat. (n) $Mask_2$ lithography. (o) $Mask_2$ etch. (p) Coat. (q) $Mask_3$ lithography. (r) $Mask_3$ etch. (s) Coat. (t) $Mask_4$ lithography. (u) $Mask_4$ etch.

Step 4: V0 PECVD nitride memorization hardmask deposition.

PECVD is used to deposit a silicon nitride (SiN) layer that serves as a robust hardmask during various etching steps. It provides an additional hardmask for etching precision, particularly for patterns requiring better etch selectivity. It is used for memorizing each layer of the multiple patterning processes.

Step 5: 1st CSOH coat.

The role of CSOH is as a hardmask and etch-transfer layer. The photoresist-defined pattern will be transferred into the CSOH hardmask layer, which serves as an etch-transfer layer in the subsequent patterning process.

In the subsequent patterning process, the photoresist-defined pattern is transferred into the CSOH hardmask layer, which serves as an etch-transfer layer.

Step 6: SiON coat.

A layer of SiON is deposited, often through PECVD, to protect underlying layers and improve etching selectivity, as shown in Fig. 1(c). This layer provides better etch control and additional protection for the underlying material during patterning.

Step 7: 1st lithography.

The wafer undergoes a photolithographic process where UV light is projected onto the SiON-coated wafer through a photomask, as shown in Fig. 1(e). This defines the transistor gate or contact pattern on the wafer. It defines the CDs of the device.

Step 8: SiON etch.

A reactive ion etching (RIE) process is used to etch the SiON layer based on the photomask pattern, as shown in Fig. 1(f).

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This step transfers the pattern from the resist or hardmask to the SiON layer. It enables selective pattern transfer to the SiON layer, which acts as a hardmask for subsequent etching processes.

Step 9: spacer deposition.

A conformal spacer material, such as silicon oxide (SiO), is deposited over the patterned wafer, as shown in Fig. 1(g). The spacer material will form sidewalls that help define smaller transistor features by preventing overlay errors during subsequent lithography steps.

Step 10: spacer SiO etch.

The spacer material is etched to form narrow sidewall spacers, as shown in Fig. 1(h). The spacer material deposited at the bottom of the holes is removed by the etching process, leaving only the uniform sidewalls composed of spacer material. This etch step is typically highly selective to ensure that the underlying materials are not etched. The spacer formation helps in improving resolution during CD control.

Step 11: tone inversion.

This step involves etching the spacer to achieve an inverted tone (opposite polarity) to facilitate smaller CDs in the final structure. It is used to enhance etch patterning and improve the resolution of the required critical features.

In the traditional process, the line edge roughness (LER) of the photoresist layer will be transferred to the underlying material (such as spin on carbon, SOC) through the etching process and ultimately affect the pattern morphology.[13] By converting the original trench pattern to a line pattern, tone inversion avoids the rough morphology that directly depends on photoresist lines, thus interrupting the transmission path of LER. Tone inversion reduces the dependence of the etching process on line morphology by changing the path of pattern transfer. The significant advantages of the tone inversion process in LER control, defect rate suppression and other aspects make it a key patterned solution for advanced integrated circuit manufacturing.

Step 12: SiN hardmask etch.

The SiN hardmask layer is etched using a precise etching technique to transfer the spacer pattern into the underlying material layers, as shown in Fig. 1(j). The SiN hardmask helps to protect underlying layers during etching and enables finer feature sizes.

Step 13: spacer SiO over etch.

Over etching is performed to ensure complete removal of unwanted spacer material and to fully define the pattern in the underlying layers, as shown in Fig. 1(k). This ensures that the etching of the spacers is completed without leaving residues, ensuring high-definition features at the 7 nm scale.

Step 14: CSOH ashing.

Ashing is performed using an oxygen plasma to remove the organic CSOH mask layer, leaving the defined pattern behind, as shown in Fig. 1(l). CSOH ashing is essential for cleaning the wafer surface and ensuring the removal of the photoresist or hardmask layer after the etching is completed. The above is the complete lithography-etch flow cycle. In the quadruple patterning process, the integration flow for the last three cycles is the same as the first one.

We establish the above quadruple patterning process model based on the SEMulator3D software. The model can output three-dimensional graphics of the etch process results on the wafer, on which CD_{AEI} can be measured.

3 Multiple patterning process and EPE contribution analysis

The industry has adopted MPT and negative tone development (NTD) lithography, which have significantly expanded the process window for immersion lithography. These advancements have allowed ArF immersion lithography to continue serving in advanced integrated circuit manufacturing.

However, MPT still faces limitations in enhancing the process window. It is necessary to examine a solution for these limited patterns by employing a mask split strategy and simulating the NTD lithography process using source mask co-optimization (SMO), which includes factors such as illumination conditions and lithography friendly splitting conditions for MPT.

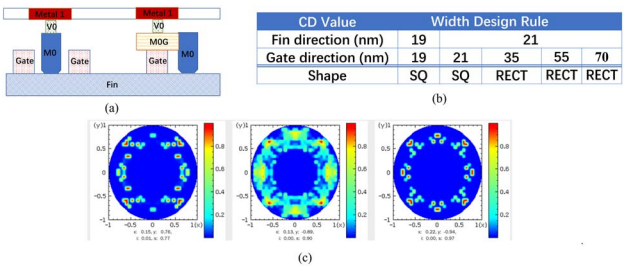
3.1 Lithography simulation and process conditions

The 7 nm process requires the introduction of a freeform source by SMO, aiming to address the issues of insufficient resolution and a narrow process window in current lithography technology through the joint optimization of the light source and mask. The specific experimental procedure includes four steps.

Step 1: design of the test pattern set. Based on the design rules of the key V0 layers for the 7 nm process, a set of test patterns suitable for this layer is designed to analyze optical challenges and select key patterns for light source optimization.

Step 2: layout retargeting study. During the light source mask optimization process, limitations of patterns are analyzed, and the impact of different layout biasing methods on the lithography process window is explored to establish pre-bias rules suitable for the 7 nm process key layers.

Step 3: sub-resolution assist features (SRAF) study. Based on the SRAF seed positions extracted using inverse lithography technology, the optimal SRAF addition scheme is researched to reduce diffraction effects and improve pattern resolution and accuracy.



CD Value	Width Design Rule				
Fin direction (nm)	19	21			
Gate direction (nm)	19	21	35	55	70
Shape	SQ	SQ	RECT	RECT	RECT

Fig. 2 The simulation conditions for the V0 layer of the 7 nm process. (a) The cross section. (b) The basic design rule. (c) The source results of SMO.

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Step 4: freeform light source and iterative mask optimization study. By optimizing the light source matrix and adjusting the light source configuration, the collaboration between the light source and mask is ensured to achieve a light source that meets lithography performance requirements.

The cross section is shown in Fig. 2(a), and the basic design rule is listed in Fig. 2(b). The minimum space between polygons in the V0 layer is 42 nm. According to the lithography limit of process ability with an ArF immersion scanner, three freeform sources have been optimized with various test patterns. As shown in Fig. 2(c), three light sources are obtained by the SMO process. During the tuning of source 1 and source 2, we used the D2 symmetry method, with a pupil fill ratio of no more than 7% for source 1 and an upper limit of no more than 20% for source 2. For source 3, we used the D4 symmetry method, with a pupil fill ratio of no more than 7%. And the first source was adopted because it provided the largest PW and maximum exposure latitude.

3.2 Large scale test pattern generation for multiple patterning development

Large-scale random test patterns that closely mimic real physical designs are crucial for developing robust multi-patterning processes, models, and recipes.[14–16] Unlike simplistic design rule checks, these patterns expose complex interactions found in actual layouts, such as the co-occurrence of rectangular vias on power rails and square vias on signal tracks. An excellent multiple patterning algorithm needs to be able to work stably under different layouts and design rules. By generating large-scale random layouts, various design scenarios can be simulated, including complex and varying polygon densities, and different circuit topologies, ensuring that the algorithm can work stably under various conditions. Randomly generated layouts reflect different design requirements and manufacturing constraints, testing whether the algorithm can flexibly handle various lithography challenges. We set each row of polygons as a fixed type, and set a polygon position at a fixed distance. The presence of polygons at each polygon position is random. This generates layouts with different polygon densities and different circuit topologies. Large-scale random layouts help assess the algorithm's performance in complex, non-ideal environments, avoiding overly idealized test scenarios.

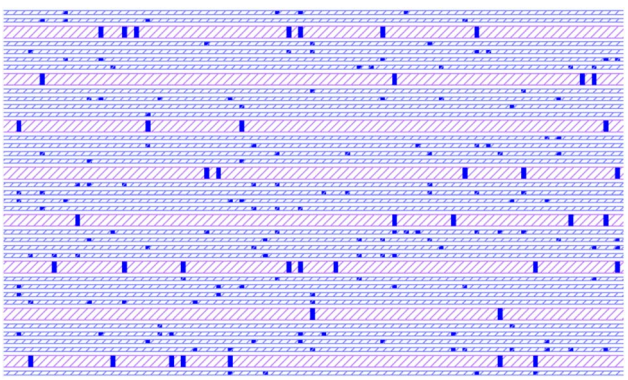

Fig. 3 The large-scale random test layout.

Hence, we generated a density-aware V0-M1 random DRC-clean random test pattern layout to develop a robust quadruple patterning algorithm. First, we generated the M1 power rail and M1 tracks to form the layout grid. Then, we only generated rectangular vias of design rule size on the M1 power rail. At the same time, based on the density level of rectangular vias on the power rail, we performed random number generation while maintaining a similar density level to generate rectangular vias. There are two types of square via sizes for the metal track, and we performed random seed placement and generation according to the proportions and density. The final large-scale test layout is shown in Fig. 3. Based on this random layout, we performed the algorithm development and splitting for quadruple patterning and adjusted the high-level splitting constraints and process-friendly splitting constraints according to the limitations of the process window. Efforts were made to minimize the occurrence of forbidden pitches on the split mask.

3.3 The quadruple patterning decomposition

In the multi-exposure decomposition algorithm, short-range constraints, long-range constraints, and density are three crucial factors that directly affect the image decomposition quality and the performance of the algorithm. Short-range constraints are mandatory decomposition guidelines. We use a hard constraint; that is, two patterns whose space or corner-to-corner (C2C) space is less than 110 nm must be separated in layout decomposition. Long-range constraints in our decomposition algorithm define the forbidden pitch range, which is approximately 1.3 to 1.7 times the minimum pitch, acting as a soft constraint. Whenever possible, we aim to minimize the presence of forbidden pitches in the layout as long as this does not violate the hard constraints, because they can significantly reduce the process window. Finally, we also conduct a further scan for density, ensuring that the four decomposed masks have roughly consistent density. In the algorithm, we limit the density difference between adjacent scan windows to no more than 5%. In the final layout coloring decomposition, we introduced the above three constraints in order of priority from high to low. The specific constraints are shown in Fig. 4. Fig. 4(a) shows short-range hard constraints, Fig. 4(b) shows long-range hard constraints, and Fig. 4(c) shows the final density regulation.

We selected a typical and important test layout for EPE analysis, performing decomposition and mask optimization corrections. This layout not only includes the minimum CD and space, but also covers a wide range of pattern types, with high density, making it reasonable for monitoring and analyzing EPE. After basic corrections using the lithography model and etching bias, the contours were fed into the model of the multiple patterning process.

3.4 The Sobol sensitivity analysis

In the step of spacer deposition, the thickness of the sidewall of the pillars is a key parameter that affects the CD difference

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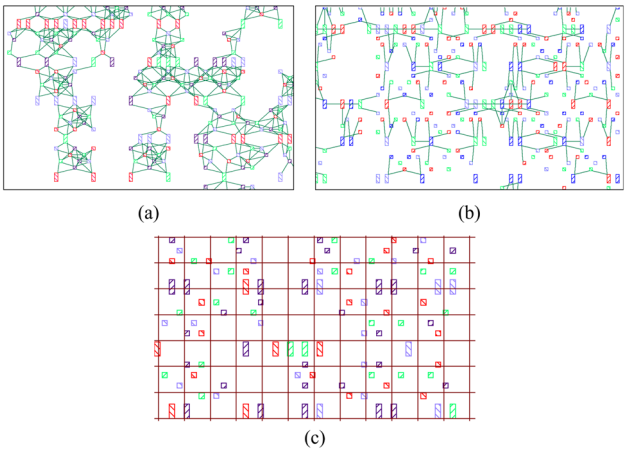

Fig. 4 The constraints of the layout coloring decomposition. (a) The short-range hard constraints. (b) The long-range hard constraints. (c) The final density regulation.

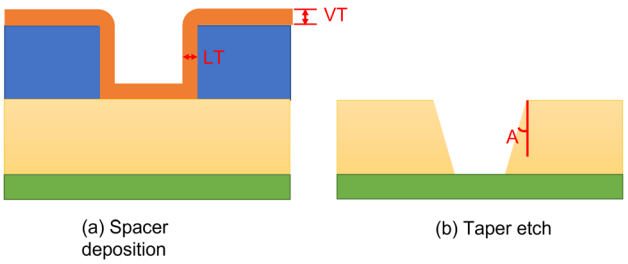

Fig. 5 The schematic diagram of the parameter definition. (a) The spacer deposition process. The thickness parameter (T) is defined as the vertical thickness (VT). The lateral ratio (R) is defined as the ratio between the lateral deposition amount (LT) and the vertical deposition amount (VT). (b) The taper etch process. The sidewall angle (A) is the angle between the sidewall generated during the etch process and the normal direction of the wafer.

between the after-etch-inspection (AEI) and the after-develop-inspection (ADI), and it is determined by the thickness and lateral ratio of the deposition process. As shown in Fig. 5(a), the thickness parameter (T) is defined as the vertical thickness (VT), and the lateral ratio (R) is defined as the ratio between the lateral deposition amount (LT) and the vertical deposition amount (VT). A conformal deposit is a thin film that uniformly covers all contours of the substrate surface. The thickness of the deposited layer is determined by the R, which compares material growth in the lateral direction (X–Y plane) to growth in the vertical direction (Z-axis). In ideal conformal deposition, the goal is to achieve a R close to 1 : 1. This ratio is critical because it directly determines the filling effect of the deposited material within complex three-dimensional structures. Specifically, the deposition rate of the lateral thickness directly equals the reduction in the critical dimension. If the lateral deposition is too rapid, which means the ratio is significantly greater than 1, the opening of the structure, such as a via, will narrow rapidly and may even close prematurely before being completely filled.

In taper etching, the sidewall angle (A) is indeed one of the core parameters in the model, as shown in Fig. 5(b), directly influencing the etch profile and the final critical dimension. The A defines the geometric shape of the etched opening, thereby directly determining the numerical relationship between the top CD and the bottom CD. In actual production, the sidewall angle may become non-uniform due to the loading effects. For example, in areas with different pattern densities, variations in the consumption of reactants and the efficiency of byproduct removal can lead to differences in the sidewall angle and etch depth across these regions, resulting in non-uniformity of the critical dimensions. Therefore, in taper etch processes, precise control and stabilization of the sidewall angle are crucial for achieving the target critical dimensions and the desired device performance.

In this study, the density-aware layout was used to provide a realistic pattern environment for evaluating EPE variation. The possible influence of etch loading was represented in a simplified form through the variation of the sidewall angle parameter. A direct quantitative comparison of EPE between high-density and low-density regions would require a calibrated local etch-loading model that relates pattern density to local etch rate and sidewall angle. Such calibration was not included in the present simulation framework. Therefore, the current results should be interpreted as a global sensitivity evaluation of the main process parameters, while density-dependent etch loading remains an important topic for future experimental calibration and model refinement.

For each of the four LE processes, the aforementioned parameters may be different, and therefore, these parameters are individually designated as T_i, R_i and A_i, where the value of i ranges from 1–4. Taking the measurement point of CDs as an example, the CD value of the ADI is an important factor that affects the CD of the pattern on the hardmask, denoted as CD_{ADI}. The CD value of the AEI can be expressed as a function of the above parameters.

$$CD_{AEI} = f(T_1, \ldots, T_4, R_1, \ldots, R_4, A_1, \ldots, A_4, CD_{ADI}). \quad (1)$$

For the function $Y = f(X_i)$, its variance can be decomposed into:

$$\mathrm{Var}(Y) = \sum_{i=1}^{k} V_i + \sum_{i<j} V_{ij} + \ldots, \quad (2)$$

where V_i represents the independent contribution of variable X_i, and V_{ij} represents the interaction contribution of variables X_i and X_j. Sobol analysis is a global sensitivity analysis method based on variance decomposition. The variance Var(Y) of output Y is decomposed into the sum of independent and interactive contributions of independent variables according to the variance decomposition theorem. Therefore, the sensitivity of T_i to the $CD_{hardmask}$ can be determined by:

$$S_{T_i} = \frac{V_{T_i}}{\mathrm{Var}(CD_{AEI})}. \quad (3)$$

And the sensitivity of other parameters can be solved by a similar method.

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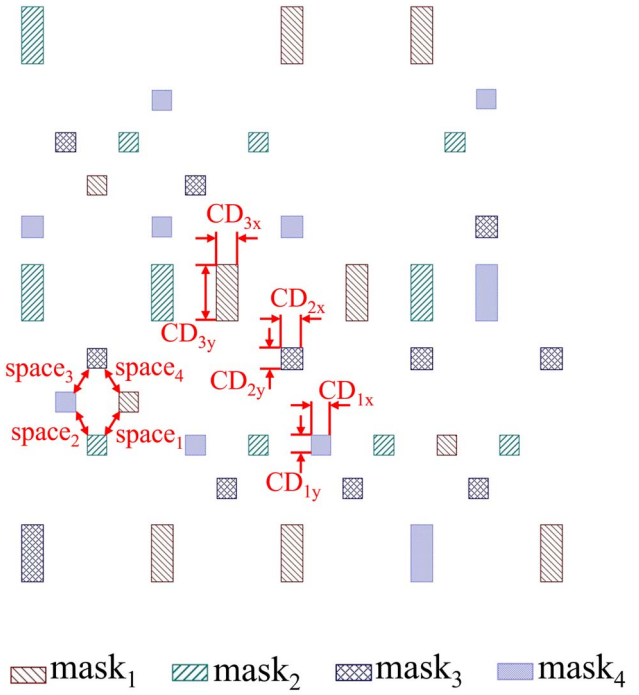

Fig. 6 The 4 masks of the quadruple patterning process and the measurement positions.

The measured CD of the AEI is compared with the target CD, and the EPE is estimated. Since EPE is usually based on a single edge, the difference in CD needs to be divided by 2. The calculation formula for EPE is:

$$\mathrm{EPE} = |\mathrm{CD_{AEI}} - \mathrm{CD_{Target}}|/2. \quad (4)$$

The ADI contours used in this work were idealized contours, and the simulated variations mainly describe process-level dimensional changes, including ADI CD variation, overlay error, deposition-induced dimensional variation, and etch profile variation. Therefore, the LER suppression associated with tone inversion is discussed here as a process-mechanism advantage, in which the direct transmission path of photoresist edge roughness is weakened, rather than as a quantitatively modeled LER term.

In the space analysis, two types of space-related parameters were distinguished. Independent space parameters denote physically defined gaps that can be directly measured at a specific process stage. ADI-affected space parameters denote final or intermediate space values that are determined by the ADI contour after subsequent deposition and etch transfer. For some ADI layouts, adjacent resist-defined features may overlap or merge before the etch-transfer step. In such cases, the nominal ADI space does not correspond to a physically meaningful final transferred gap, and direct ADI space measurement can be ambiguous. Therefore, the space parameters discussed in the EPE analysis refer to the transferred and physically measurable spaces unless otherwise specified.

4 Simulation results

4.1 The simulation experiment settings

The target pattern with the layout decomposition applied is shown in Fig. 6. The measurement positions are marked in the figure, where the target values of CD_{1x} and CD_{1y} are 19 nm, the target values of CD_{2x}, CD_{2y} and CD_{3x} are 21 nm and the target values of CD_{3y} are 55 nm. The spaces between four adjacent patterns that are not on the same mask are also measured. After basic corrections using the lithography model and etch bias, the contour diagram of this region is shown in Fig. 7. Under different process window (PW) conditions, where the dose variation range is ±5% and the defocus variation range is ±50 nm, 7 different ADI contours are obtained. In the subsequent analysis, the contour of the inner, outer and nominal conditions (NC) will be the main focus, as shown in Fig. 7(b).

4.2 The Sobol analysis for the quadruple patterning process

The parameters *T*, *R* and *A* each have random variations with a uniform distribution of ±10% in the simulation. The

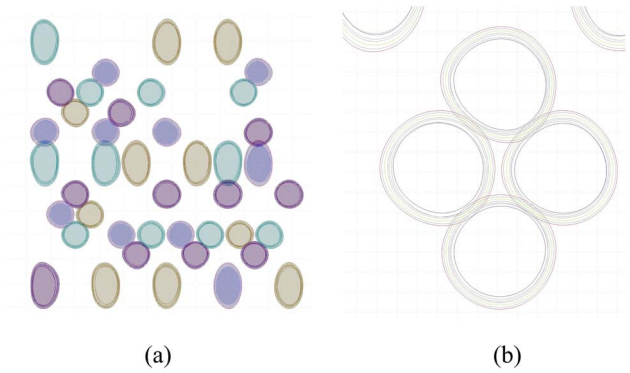

Fig. 7 The ADI contour obtained for different PW conditions. (a) The overall contour input into the model. Different colors represent different masks. (b) The partially enlarged contour. The red and blue lines represent the outer and inner circles of the contours, respectively, and the green line represents the contour under NC.

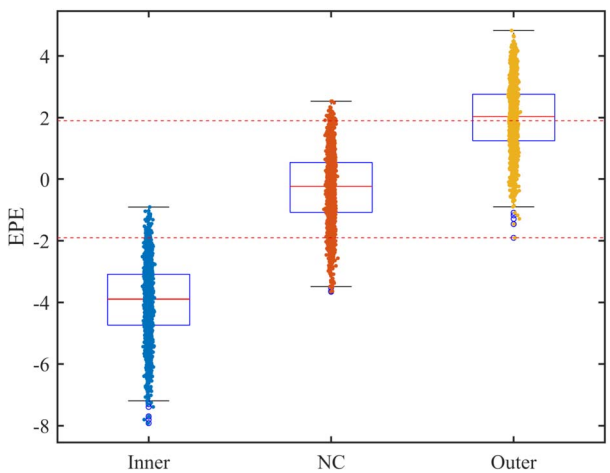

Fig. 8 The statistical results for CD_{1x} with lithography inputs of outer, inner and NC. The dotted red line represents the ±10% deviation from the target.

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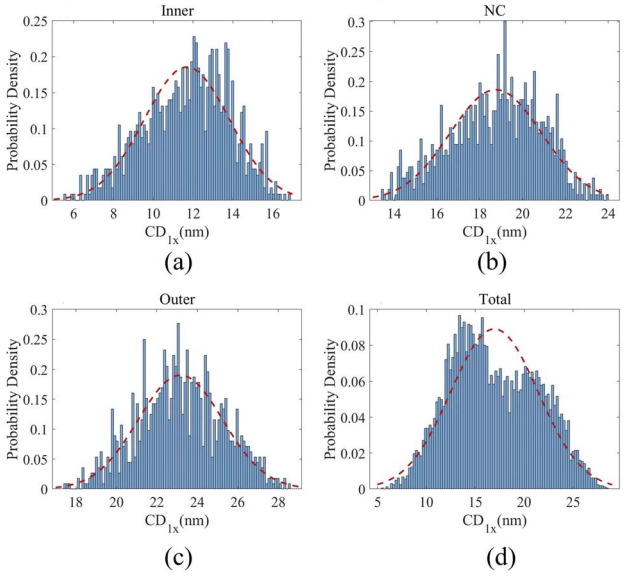

Fig. 9 The distribution of CD_{1x} measurements with lithography input of outer, inner, NC and all of the contours. (a) The CD_{1x} distribution of inner. (b) The CD_{1x} distribution of NC. (c) The CD_{1x} distribution of outer. (d) The CD_{1x} distribution of all of the contours. The red line is a Gaussian curve with the same mean and variance values.

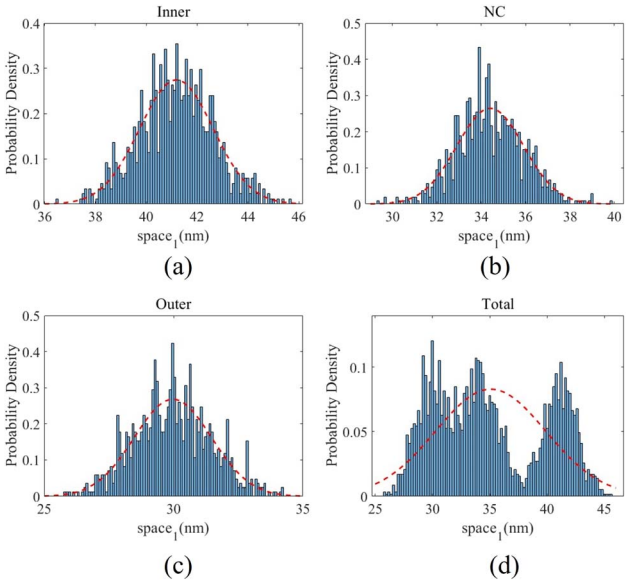

Fig. 10 The distribution of $space_1$ measurements with lithography input of outer, inner, NC and all of the contours. (a) The $space_1$ distribution of inner. (b) The $space_1$ distribution of NC. (c) The $space_1$ distribution of outer. (d) The $space_1$ distribution of all of the contours. The red line is a Gaussian curve with the same mean and variance values.

measurement results in AEI of measurement position CD_{1x} after testing 1000 sets of data are shown in Fig. 8. The comparison of the distribution of measurement results of CD_{1x} with a Gaussian curve is shown in Fig. 9. It can be seen that the distribution of CD results is a little close to Gaussian distribution, but it exhibits asymmetric behavior. The source of asymmetry is mainly the CD values of the ADI. The ADI is derived from lithography simulation results under different focus and dose conditions, and its distribution does not conform to a uniform or Gaussian distribution. It is common for the CD values of the inner and outer contours to have different deviations from the mean CD. The ADI contours have a great influence on the results, making the measurement results deviate greatly from the target, and the overall statistical results deviate from the Gaussian distribution. The statistical results of all the CD measurement positions are shown in Table 1. The 3σ values of all measurement points under all PW conditions are very close, which means that the influence of deposition and etching on EPE is relatively fixed.

The statistics results for $space_1$ are shown in Fig. 10. The four masks are modeled with overlay in MPT by adding random offsets in the x and y directions corresponding to Gaussian distribution with $3\sigma = 4$ nm. The statistics results with overlay for $space_1$ are shown in Fig. 11. It can be seen that the variation in space is more intense under the influence of overlay. The statistical results of space measurement values with and without overlay are shown in Table 2. Under the influence of overlay, the 3σ measurement value of space is about 3 nm larger than that without overlay. And the overlay has little impact on the mean of the spaces. It can be seen that compared with the distribution of CDs, the distribution of spaces is farther away from the Gaussian distribution. This is because one space value is affected by the ADI of two masks, which makes the impact of discrete ADI on the results more obvious.

The overlay error mainly broadens the space distribution rather than shifting its mean. This is because the overlay variation was introduced as a zero-mean random displacement in

Table 1 The statistical results of CD measurement values

Measurement positions	Inner		NC		Outer	
	Mean (nm)	3σ (nm)	Mean (nm)	3σ (nm)	Mean (nm)	3σ (nm)
CD_{1x}	11.69	6.45	18.75	6.43	23.17	6.29
CD_{1y}	12.25	6.69	18.71	6.55	22.94	6.32
CD_{2x}	13.63	6.60	20.83	6.07	25.13	6.78
CD_{2y}	13.23	6.44	20.68	6.18	24.96	6.81
CD_{3x}	14.32	6.36	20.91	5.95	25.23	6.06
CD_{3y}	41.42	9.72	53.07	7.57	59.48	6.90

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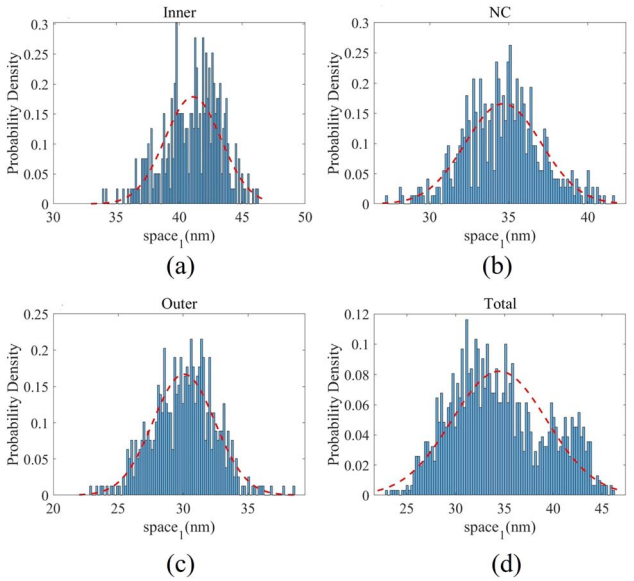

Fig. 11 The comparison of the distribution of $space_1$ measurements considering overlay. (a) The $space_{1x}$ distribution of inner. (b) The $space_{1x}$ distribution of NC. (c) The $space_{1x}$ distribution of outer. (d) The $space_{1x}$ distribution of all of the contours.

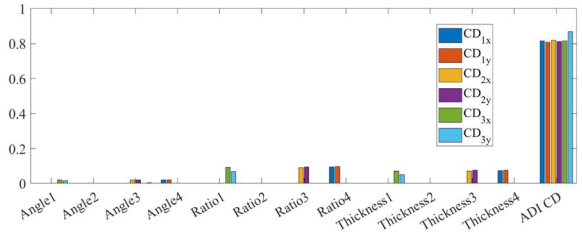

Fig. 12 The EPE contribution results of CDs with Sobol sensitivity analysis. The vertical axis represents the first-order sensitivity indexes of Sobol analysis.

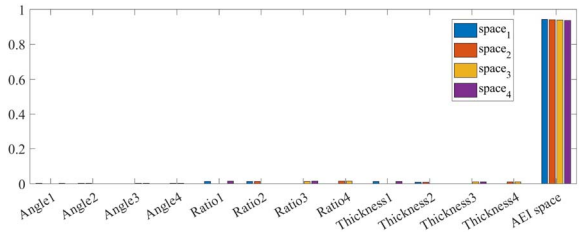

Fig. 13 The EPE contribution results of spaces with Sobol sensitivity analysis. The vertical axis represents the first-order sensitivity indexes of Sobol analysis.

the Monte Carlo simulations. Positive and negative displacement errors are statistically balanced across the sample set, so the average space remains close to the nominal value. However, in each individual realization, overlay changes the relative position between adjacent patterning levels and directly modifies the local space. Therefore, overlay increases the sample-to-sample variation and the corresponding 3σ value, while producing only a limited change in the mean. This result indicates that overlay is primarily a variability contributor rather than a systematic bias term in the present process window.

The CD and EPE distributions obtained from the Monte Carlo simulations are not strictly Gaussian and show a certain degree of asymmetry. This asymmetry mainly arises from the nonlinear propagation of ADI CD variation through the subsequent deposition and etching processes. It should be noted that the Sobol sensitivity analysis used in this work does not require the output response to be normally distributed. Since Sobol indices are based on variance decomposition, they remain applicable as long as the output has a finite variance and the input variables are sampled from the prescribed independent distributions. However, the Sobol indices should be interpreted as variance-based contribution metrics. They identify the dominant sources of EPE variance, but they do not fully describe higher-order distributional features such as skewness, tail behavior, or local extreme values.

The parameters T, R and A of each mask are taken as independent variables, respectively. The CD values of each measurement point on ADI are taken as the last parameter. The contribution of each parameter by the Sobol sensitivity analysis is shown in Fig. 12. The results of first-order sensitivity indexes are shown in Table 3.

For the spaces, the value on the ADI does not correctly reflect the result of the AEI. The adjacent patterns are located on different masks, which means they are patterns from different

Table 2 The statistical results of space measurement values

		Inner		NC		Outer	
Measurement positions		Mean (nm)	3σ (nm)	Mean (nm)	3σ (nm)	Mean (nm)	3σ (nm)
Without overlay	$space_1$	41.19	4.37	34.41	4.52	29.97	4.47
	$space_2$	41.15	4.03	33.72	4.61	29.21	4.65
	$space_3$	42.24	3.44	35.58	4.72	31.32	4.54
	$space_4$	41.07	4.56	33.86	4.62	29.43	4.58
With overlay	$space_1$	41.09	6.69	34.66	7.21	30.06	7.16
	$space_2$	41.10	6.89	33.71	7.62	29.21	7.59
	$space_3$	42.19	5.17	35.51	7.23	31.51	7.33
	$space_4$	41.22	6.60	34.16	7.82	29.64	7.65

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Table 3 The first-order sensitivity indexes of all parameters in Fig. 12 and 13

Parameter	CD_{1x}	CD_{1y}	CD_{2x}	CD_{2y}	CD_{3x}	CD_{3y}	$space_1$	$space_2$	$space_3$	$space_4$
A_1	0.0000	−0.0000	0.0000	0.0001	0.0198	0.0148	0.0032	−0.0000	−0.0001	0.0036
A_2	−0.0000	−0.0002	−0.0000	0.0000	0.0000	−0.0001	0.0028	0.0031	−0.0000	−0.0000
A_3	0.0000	0.0000	0.0197	0.0204	−0.0001	−0.0002	−0.0000	−0.0000	0.0034	0.0035
A_4	0.0196	0.0204	0.0000	−0.0000	−0.0000	0.0003	0.0001	0.0031	0.0033	−0.0000
R_1	0.0000	0.0000	0.0000	0.0001	0.0910	0.0680	0.0139	0.0000	0.0000	0.0155
R_2	−0.0000	−0.0001	−0.0001	−0.0001	0.0001	0.0000	0.0138	0.0137	−0.0001	0.0000
R_3	0.0002	0.0001	0.0901	0.0946	0.0001	0.0009	0.0001	0.0007	0.0145	0.0160
R_4	0.0931	0.0958	0.0000	0.0000	−0.0001	0.0002	0.0001	0.0155	0.0160	0.0000
T_1	−0.0000	−0.0001	0.0000	0.0000	0.0701	0.0490	0.0127	−0.0002	−0.0003	0.0127
T_2	0.0000	0.0000	0.0000	0.0000	−0.0000	−0.0001	0.0103	0.0103	0.0000	−0.0000
T_3	0.0000	−0.0000	0.0713	0.0749	0.0000	−0.0000	−0.0000	0.0000	0.0109	0.0121
T_4	0.0735	0.0749	0.0003	0.0001	0.0002	0.0009	0.0001	0.0123	0.0116	−0.0002
ADI	0.8139	0.8090	0.8187	0.8098	0.8150	0.8684	0.9445	0.9423	0.9400	0.9377

Table 4 The first-order sensitivity indexes of each parameter with respect to EPE

Parameter	A	R	T	ADI
CD_{AEI}	0.0191	0.0888	0.0690	0.8225
Space	0.0065	0.0300	0.0230	0.9411

lithography processes. If all the ADI of the masks are put together, it will be found that many adjacent patterns overlap, which means it is meaningless to measure the space. Therefore, without adding random variation to parameter T, R and A, the spaces of AEI are measured as a parameter. Since the values of T, R and A are fixed, the space of AEI output from the model does not introduce the error caused by the deposition and etch processes, and it is not a transferred and physically measurable space but an intermediate ADI-affected parameter. The results of first-order sensitivity indexes are shown in Table 3. The vertical axis represents the S factor of Sobol analysis calculated according to eqn (3). The first-order sensitivity indexes of Sobol analysis are added and merged into the contribution of each parameter, as shown in Table 4. It can be seen that the ADI is the main factor affecting CDs and spaces, accounting for over 80% and 90% of their impact, respectively.

4.3 The Sobol analysis for deposition and etch processes

Since the impact of ADI is very significant, the impact of the three parameters of deposition and etch is discussed separately.

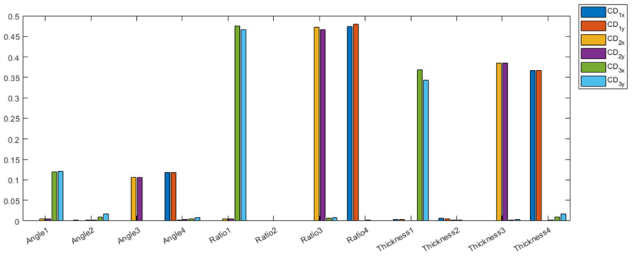

Fig. 14 The EPE contribution results of deposition and etch process parameters on CDs with Sobol sensitivity analysis. The vertical axis represents the first-order sensitivity indexes of Sobol analysis.

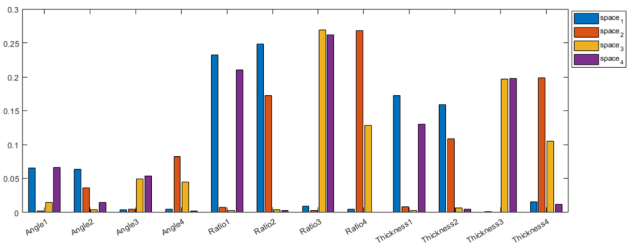

Fig. 15 The EPE contribution results of deposition and etch process parameters on spaces with Sobol sensitivity analysis. The vertical axis represents the first-order sensitivity indexes of Sobol analysis.

The Sobol analysis results of CDs are shown in Fig. 14. It can be seen that for the CD measurement point, only the parameters of the corresponding mask have a significant contribution. This is in line with expectations because a small change in the parameters of a patterning process will not affect the results of the other patterning processes. The results of spaces are shown in Fig. 15. It can be seen that the results of each space are affected by the parameters of two patterning processes. The results of first-order sensitivity indexes are shown in Table 5.

4.4 The EPE budget allocation

The first-order sensitivity indexes of Sobol analysis are added and merged into the contribution of each parameter, as shown in Table 6. If we want the EPE introduced by deposition and etch processes to meet a budget, we can use these data to derive the budget for each parameter. The EPE budget of deposition and etch processes can be assumed to be $3\sigma_{AEI}$. According to eqn (2), the variance of AEI CD can be decomposed into the individual contributions of each independent variable and the interaction contributions between independent variables. From the results, it can be seen that the sum of first-order sensitivity indexes of parameters A, R, and T, which represent their individual contributions, is close to 1. Therefore, the proportion of interaction contribution is very small and can be ignored. The sensitivity index of Sobol analysis can be used as the weight assigned to each independent variable in the equation. It is

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Table 5 The first-order sensitivity indexes of all parameters in Fig. 14 and 15

Parameter	CD_{1x}	CD_{1y}	CD_{2x}	CD_{2y}	CD_{3x}	CD_{3y}	$space_1$	$space_2$	$space_3$	$space_4$
A_1	0.0004	0.0005	0.0049	0.0055	0.1189	0.1202	0.0655	0.0026	0.0145	0.0662
A_2	0.0017	0.0012	0.0017	0.0017	0.0095	0.0173	0.0633	0.0365	0.0039	0.0145
A_3	0.0007	0.0007	0.1057	0.1066	0.0001	0.0006	0.0041	0.0050	0.0495	0.0537
A_4	0.1185	0.1183	0.0028	0.0039	−0.0054	−0.0085	−0.0051	0.0825	0.0442	−0.0027
R_1	−0.0013	−0.0013	0.0056	0.0054	0.4754	0.4658	0.2318	−0.0075	0.0036	0.2101
R_2	0.0010	0.0009	−0.0011	−0.0012	−0.0001	−0.0001	0.2481	0.1725	−0.0040	−0.0029
R_3	0.0004	0.0002	0.4730	0.4661	−0.0063	−0.0087	−0.0096	−0.0030	0.2685	0.2621
R_4	0.4739	0.4793	0.0010	0.0016	0.0005	0.0001	−0.0045	0.2679	0.1281	0.0005
T_1	0.0040	0.0040	0.0008	0.0010	0.3681	0.3433	0.1722	0.0084	0.0027	0.1304
T_2	−0.0064	−0.0058	−0.0023	−0.0026	−0.0006	0.0000	0.1592	0.1089	−0.0064	−0.0050
T_3	0.0008	0.0008	0.3849	0.3844	−0.0020	−0.0040	0.0013	0.0009	0.1970	0.1974
T_4	0.3670	0.3678	0.0015	0.0017	0.0105	0.0180	0.0156	0.1985	0.1051	0.0118

Table 6 The first-order sensitivity indexes of the parameters in deposition and etch processes with respect to EPE

Parameter	A	R	T
CD_{AEI}	0.1213	0.4717	0.3725
Space	0.1285	0.4561	0.3302

assumed that the first-order sensitivity index of the independent variable x_i is S_i, and the target variance assigned to x_i is:

$$\mathrm{Var}_i = S_i \cdot {\sigma_{\mathrm{AEI}}}^2. \tag{5}$$

Therefore, the error budget for each variable x_i can be obtained:

$$3\sigma_i \le 3\sigma_{\mathrm{AEI}} \cdot \sqrt{S_i}. \tag{6}$$

For example, the EPE budget of the deposition and etch processes is assumed to be $3\sigma_{\mathrm{AEI}} = 3$ nm. According to eqn (6) and Table 6, the error budget for parameters A, R, and T can be obtained as:

$$\begin{aligned} 3\sigma_A &\le 1.04^\circ, \\ 3\sigma_R &\le 2.06, \\ 3\sigma_T &\le 1.83 \ \text{nm}. \end{aligned} \tag{7}$$

The EPE budget is allocated to parameters T and R, which are requirements for the ability of the deposition process, and to parameter A, which is a requirement for the ability of the etch process. In this way, according to the EPE budget, this model can be used to obtain the accuracy requirements of the parameters in deposition and etch processes, and then guide the direction of improving the processes to reduce EPE.

Table 7 A budget table for 7 nm process parameters

Parameter	A	R	T
3σ	0.6966°	1.3736	1.2207 nm

According to the report by Wu *et al.*,[17] the CDU budget of the V0 layer for the 7 nm technology node is 2 nm. Based on these data, we make a budget table for 7 nm process parameters, as shown in Table 7.

SEMulator3D is effective for building three-dimensional process flows and extracting relative EPE trends, but the absolute accuracy of the simulated EPE depends on the calibration of input process parameters and model assumptions. Thus, the results should be interpreted primarily as a comparative sensitivity analysis for identifying dominant EPE contributors and evaluating process-window robustness. Further experimental calibration would be required for direct quantitative prediction on manufactured wafers.

5 Conclusions

With the introduction of multiple patterning schemes, the EPE analysis becomes more important than ever to assess and maintain in-line process performance and yield. In this work, the EPE contribution analysis method of a multiple litho-etch patterning process is proposed. A process flow model of quadruple patterning is built to simulate the effect of each step's error on the AEI contour. After basic corrections using the lithography model and etch bias, the contour diagram with different PW conditions of the region is obtained. The variations in the sidewall angle of the etch process and the thickness and lateral ratio of the spacer deposition process result in a Gaussian distribution of the measured CD values. The variation in space becomes more intense under the influence of overlay. The results of the Sobol sensitivity analysis show that the impact of the ADI contour is the greatest, and the contribution levels of the parameters in deposition and etching processes are relatively close. The setting of the parameter variation range in the simulation is relatively large, for which the variation range of the results is larger than that of the actual process. The contribution of each parameter in the patterning related processes can be obtained by this method, and then the error budget of each parameter can be estimated according to the EPE budget. This work is dedicated to proposing a method for analyzing the contribution degree of factors affecting EPE.

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Conflicts of interest

There are no conflicts to declare.

Data availability

Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

Acknowledgements

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