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Raised or recessed? Finding the optimal gate architecture for improving the static performance of graphene transistors

Tzu-Jung Huang, [ab] Andrew Spencer, [c] Luke Ingraham, [a] Anibal Pacheco-Sanchez [d] and Ivan Puchades [abc]

As silicon CMOS technology approaches its scaling limits, graphene offers a compelling alternative as the active material channel in transistors due to its high carrier mobility and atomically thin profile, which provide strong electrostatic control and promise high-performance analog applications. However, roadblocks such as device-to-device variation, high contact resistance, poor dielectric interfaces, and non-uniform graphene quality have limited the adoption of graphene field effect transistors (GFETs). Hence, further investigations are required for mitigating these issues at a material, *e.g.*, by improving graphene transfer, and device level, *e.g.*, by finding an appropriate gate architecture. In this work, we directly compare two GFET structures through a controlled, side-by-side process split to evaluate the impact of gate stack architecture: raised *vs.* recessed buried local gate, in which both structures use hBN as the gate dielectric. Benchmarking is performed in terms of device performance and device-to-device variation. While the top-performing devices remain similar across the two proposed structures, significant statistical differences are seen in terms of device performance and yield in the two populations studied. A total of 256 identical devices from each gate architecture are electrically tested and characterized for a statistically significant comparison. The most significant difference is seen in the Dirac voltage, which is reduced from 1.2 V to 0.7 V with the recessed architecture, making it more suitable for low-power analog applications. Average hole mobility increases from 3383 $cm^2\ V^{-1}\ s^{-1}$ to 4794 $cm^2\ V^{-1}\ s^{-1}$, and device yield increases from 54.4% to 65.1%. Physical analysis, which includes spectroscopy and hysteresis measurements, indicates that these improvements are due to the proposed planarized gate architecture and reduction of interface defects. This study shows that direct statistical comparison studies of process conditions can help identify favorable process conditions to improve the manufacturability of graphene-based transistors.

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1 Introduction

Since the isolation of graphene, interest in atomically thin two-dimensional (2D) materials has surged, spurring progress in the fabrication of layered materials.[1] As sub-nanometer semiconductor technology nodes approach practical implementation through ongoing advancements in manufacturing, graphene and other 2D materials present significant opportunities due to their exceptional electrical properties, whether as monolayers or integrated with silicon in heterogeneous architectures.[2] Owing to its high carrier mobility, graphene stands out as a candidate for enabling terahertz (THz) and microwave communication, promising substantial improvements in data transmission speed and efficiency.[3,4] Graphene-based devices continue to show promise for high-frequency applications, including amplifiers, modulators, and resonators. Despite these advantages, achieving wafer-scale integration of graphene material-based devices remains challenging due to substantial device-to-device variability.[5] This variability arises from factors such as transfer-induced imperfections, inconsistencies in fabrication, and process-related defects. The current research efforts aim to minimize such variability and enhance device yield, paving the way toward scalable and commercially viable graphene material-based electronics.

There are numerous fabrication methods for graphene-based devices,[6–11] with the selection of a specific approach typically depending on the intended application, targeted performance, and available fabrication resources. High-performance graphene field effect transistors (GFETs) often employ nanometer-scale channel lengths and process

[a]*Department of Microsystems Engineering, Rochester Institute of Technology, USA. E-mail: ivan.puchades@rit.edu*
[b]*Nanopower Research Laboratories, Rochester Institute of Technology, USA*
[c]*Department of Electrical and Microelectronics Engineering, Rochester Institute of Technology, USA*
[d]*Departamento de Electrónica y Tecnología de Computadores, Universidad de Granada, Spain*

techniques to minimize source/drain capacitance.[12] Gate electrodes in high-frequency graphene transistors may follow a top-gated,[13] buried,[14] or trench-filled damascene design.[15] Top or local gate materials can vary from gold or platinum to aluminum (Al), to reduce gate resistance, ease of integration, or to take advantage of the native oxide that is formed in the case of Al.[14] Dielectric materials such as ultrathin aluminum oxide (natively grown or atomic layer deposited (ALD)), transferred hexagonal boron nitride (hBN), and other high-k materials are commonly used to enhance the performance of graphene transistors.[10,16,17] For example, graphene/hBN heterostructures have been shown to achieve hole carrier mobilities up to 60 000 $cm^2\ V^{-1}\cdot s^{-1}$.[18] Large-scale (up to 6-inch) chemical vapor deposition (CVD) hBN and graphene films are available commercially and can be transferred with the same PMMA-assisted process.[19] In addition, the substrate underneath the graphene channel also plays a crucial role as it significantly affects interface quality.[5,20]

Despite promising progress, large-scale GFETs fabrication continues to face challenges with device-to-device variability.[21–25] Most of the studies dealing with the variability of performance indicators of large-scale fabrication, such as mobility and Dirac voltage, are based on GFETs using high-k bulk dielectrics. On the contrary, most published works of hBN as a dielectric for GFETs report only one device or a small number of devices.[26–33] One large-scale paper by Fukamachi *et al.*, in 2023,[34] presented an integrated electrochemical hBN transfer method to create globally back-gate graphene field-effect transistor arrays *via* a lithography process. The hBN is used as the dielectric and was grown through a chemical vapor deposition (CVD) process on an iron-nickel alloy foil and had a thickness of about 5 nm. GFETs with SiO_2 as the dielectric were simultaneously fabricated as a control group. The maximum hole mobility increased from 5384 $cm^2\ V^{-1}\ s^{-1}$ to 7074 $cm^2\ V^{-1}\ s^{-1}$, and ultimately to 10 219 $cm^2\ V^{-1}\ s^{-1}$ when another layer of optimized hBN was used to encapsulate the devices. On the other hand, significant variability can be observed in the results of 62 tested devices, with hole mobilities as low as 2000 $cm^2\ V^{-1}\ s^{-1}$ in the optimized hBN encapsulated process. A second report by Martini *et al.*, in 2023, presented a scalable process by growing a 10 nm nanocrystalline hBN film *via* an ion beam-assisted physical vapor deposition on a 1 cm × 1 cm. Transfer length method (TLM) measurements of PMMA-transferred graphene resulted in a carrier mobility of 7500 ± 850 $cm^2\ V^{-1}\ s^{-1}$.[35] A 2025 report by Zheng *et al.* shows improved top-gated GFET reliability with the use of hBN as the dielectric with minimal hysteresis shift even after >2000 sweeps.[36]

It is essential to investigate the variability of graphene-based field-effect transistors and identify the underlying sources of variation. Although fabrication approaches for graphene devices often differ, the choice of process significantly influences device performance, application scope, and resource requirements. Prior studies generally have shown improved GFET performance or reduce variability when evaluating disparate device structures, materials, or fabrication flows, but focus only on "hero" devices that do not reflect broader statistical trends. This work employs a comparative process split to study the effect of the gate architecture on device performance, yield, and variability of GFETS using hBN as a dielectric. An Al/hBN/graphene gate stack is used as it presents advantages of simple integration and lattice match between the hBN and graphene, and has been shown to result in improved device performance.[18] The choice of gate architecture (*i.e.*, global back gate, raised local bottom gate, recessed local bottom gate, or top gate) can depend on the final application of the GFET, but also on the available resources and economically driven decision. In particular, this process split looks at the effect of local-back (a) raised Al gate *versus* (b) planarized and recessed Al gate. A local-back gate architecture has been chosen as it reduces the exposure of the graphene channel to subsequent processing steps and potentially preserves its quality. In addition, the local-back gate architecture is conducive to the fabrication of sensors which can be interrogated independently or as arrays.[37] Several studies using the local-back raised gate architecture have reported high performance of representative transistors but have also indicated that this may not be the ideal architecture due to the expected sharp transition as the graphene goes over the gate, as well as the effects of the sidewall roughness, and the potential air gap of the draping graphene.[38,39] As such, a planarized recessed architecture could present some advantages in device performance and variability. Finally, although the local-back raised gate architecture is simpler to implement as it does not require chemical and mechanical planarization (CMP) equipment, the recessed architecture can be easily integrated in the back-end-of-line (BEOL) of CMOS processes, and it may be proven to be a worthy investment in large volume manufacturing if clear performance improvements can be observed.

This report starts by briefly presenting the theoretical aspects of the different materials studied, as well as a presentation of a novel methodology employed to extract individual device mobility and, for the first time, contact resistance of a large number of individual transistors. Next, the fabrication splits and measurement methodologies are presented and discussed. Then, the physical and electrical results of the fabricated devices are presented. A total of 256 identical devices from each group are electrically tested and characterized for a statistically significant comparison. Finally, a discussion of the results is carried out, comparing the results of this experiment while providing insights and recommendations to improve GFET performance and reduce variability.

2 Theory

Graphene is a two-dimensional material composed of carbon atoms arranged in a hexagonal lattice. It exhibits high theoretical carrier mobility of up to 250 000 $cm^2\ V^{-1}\ s^{-1}$,[40] making it well-suited for high-speed GFETs that use graphene as the active channel material. In contrast to conventional silicon MOSFETs, where the channel lies within the crystalline silicon substrate, GFETs leverage the atomically thin, surface-level conduction of graphene to enable superior charge transport characteristics. Previous graphene transistors have frequently utilized atomic layer deposited (ALD) aluminum oxide (Al_2O_3) as

the gate dielectric, chosen over silicon dioxide (SiO_2) for its higher dielectric constant of 9.8 *versus* 3.9, respectively,[37] as well as ALD's ability to deposit single atomic layer thick dielectric layers per cycle. Hexagonal boron nitride (hBN), by comparison, has a relative dielectric constant of approximately 4,[41] similar to that of SiO_2. Oxide dielectrics like Al_2O_3 and SiO_2 are known to introduce trapped charges and surface roughness, which increase unintentional doping in the graphene channel.[42] This leads to shifts in the Dirac point, reflecting changes in the Fermi level due to altered carrier concentrations. Such variability undermines electrostatic control and contributes to significant device-to-device variation.[41,43] In contrast, the atomically flat and chemically inert nature of hBN minimizes charge traps and dielectric-induced perturbations, thereby stabilizing the Dirac voltage and enhancing device uniformity.[44,45] As a result, the use of hBN has been correlated with improved yield and more consistent electrostatic performance in GFET fabrication.[46]

While the contact resistance between bulk metal and a two-dimensional graphene channel is often extracted using the transfer length method (TLM), this study uses an alternative approach to measure this parameter for each individual transistor. TLMs are unable to capture localized variations in contact resistance that arise from van der Waals-dominated interactions at the graphene–metal interface. These interactions can vary significantly across a wafer, and imperfections at the contact region further exacerbate this variability.[47] To address this, we extract contact resistance by analyzing the transfer characteristics (I_DV_G) of individual transistors under varying drain biases, which has been proposed and published by Pachecho-Sanchez *et al.*[48] The contact resistance extraction method used in this study is based on a unipolar drain current I_D model of GFETs considering mobility degradation effects.[48] The methodology assumes that a weak V_{DS}-dependence of μ can be considered for two transfer curves at two close values of V_{DS}. Hence, the relation between I_{D1} and I_{D2}, obtained at V_{DS1} = 50 mV and V_{DS1} = 100 mV, respectively, can be written as in eqn (1), where V_0 is a voltage related to a residual charge, $V_{GCO} = V_{GS} - V_{Dirac} - V_{DS}/2$-with $V_{Dirac} = V_{GS|min\ ID}$-, and R_C is the contact resistance. The value of Dirac voltage is extracted directly from the I_DV_G transfer plots as the value of V_{GS} when the drain current is minimum. By solving eqn (1) for R_C at $|V_{GS}| >> |V_{Dirac}|$, a straightforward expression shown in eqn (2) can be used for calculating this device parameter.[48]

$$\frac{I_{D1}}{I_{D2}} = \frac{\sqrt{{V_{01}}^2 + {V_{GCO1}}^2}(V_{DS1} - I_{D1}R_C)}{\sqrt{{V_{02}}^2 + {V_{GCO2}}^2}(V_{DS2} - I_{D2}R_C)} \quad (1)$$

$$R_C \approx \frac{V_{DS2}I_{D1}V_{GCO2} - V_{DS1}I_{D2}V_{GCO1}}{I_{D1}I_{D2}(V_{GCO2} - V_{GCO1})} \quad (2)$$

By following the same underlying transport model, eqn (3) can be used for obtaining a value for μ of a GFET without the influence of R_C, provided the oxide capacitance per unit area C_{ox} and the transconductance parameter β. The value of C_{ox} can be measured to avoid any uncertainties related to gate dielectric thickness and composition, as shown in the Methods section. The transconductance parameter β is equal to $\mu_0 C_{ox} W/L$, where μ_0 is the bias-independent low-field mobility, C_{ox} is the oxide capacitance per unit area, and W and L are the width and length of the device and is extracted experimentally from a modified *Y*-function method presented in,[49] *i.e.*, from the slope of the plot of Y^2 *versus* ${V_{GCO}}^2$, where $Y = I_D/{g_m}^{1/2}$, and $g_m = \delta I_D/\delta V_{GS}$. An example of the use of this methodology to extract mobility is shown in the SI.

$$\mu = \frac{\beta}{C_{ox}\left(\frac{W}{L}\right)} \quad (3)$$

3 Materials and methods

3.1 Device fabrication

Two 4-inch silicon (100) wafers are used as the substrates for the fabrication of the different GFET structures analyzed. As shown in Fig. 1 and 2, device fabrication starts with an RCA clean prior to thermally growing 300 nm of SiO_2 at 1000 °C in an oxygen atmosphere. Then, the wafer with the recessed gate (b in Fig. 1 and 2) undergoes a partial 100 nm dry etch into the SiO_2 to define the gate electrode patterns and other dense rectangular CMP tiles. Then, 150 nm of aluminum is sputtered onto both wafers. A chemical-mechanical-planarization (CMP) process is then carried out on the recessed gate wafer to remove the excessive aluminum in the field area, leaving only aluminum in the previously etched trench region, forming the recessed gate. The gate electrode for the raised gate structure (a in Fig. 1 and 2) is then patterned and etched through a wet Al etch. The wafers are then processed together through the remainder of the steps. Next, hBN is transferred onto the raised and the recessed aluminum electrodes, respectively, using CVD-grown hBN on copper foil (6-inch × 6-inch), commercially purchased from

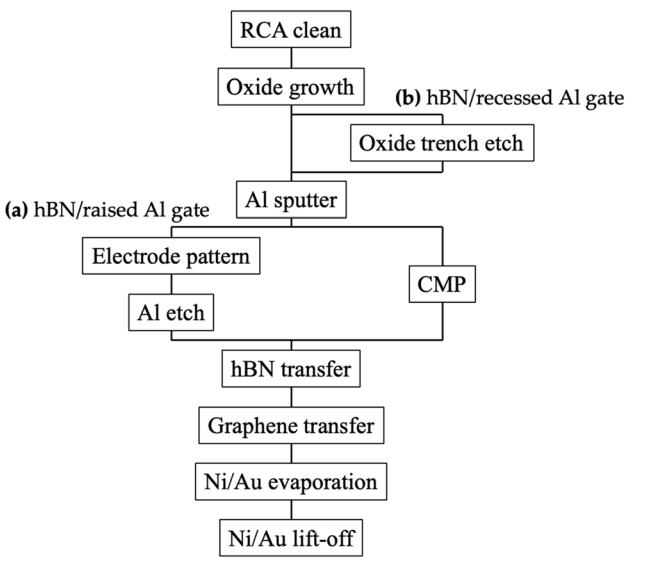

Fig. 1 Side-by-side process split for graphene on (a) hBN/raised Al gate, and (b) hBN/recessed Al gate.

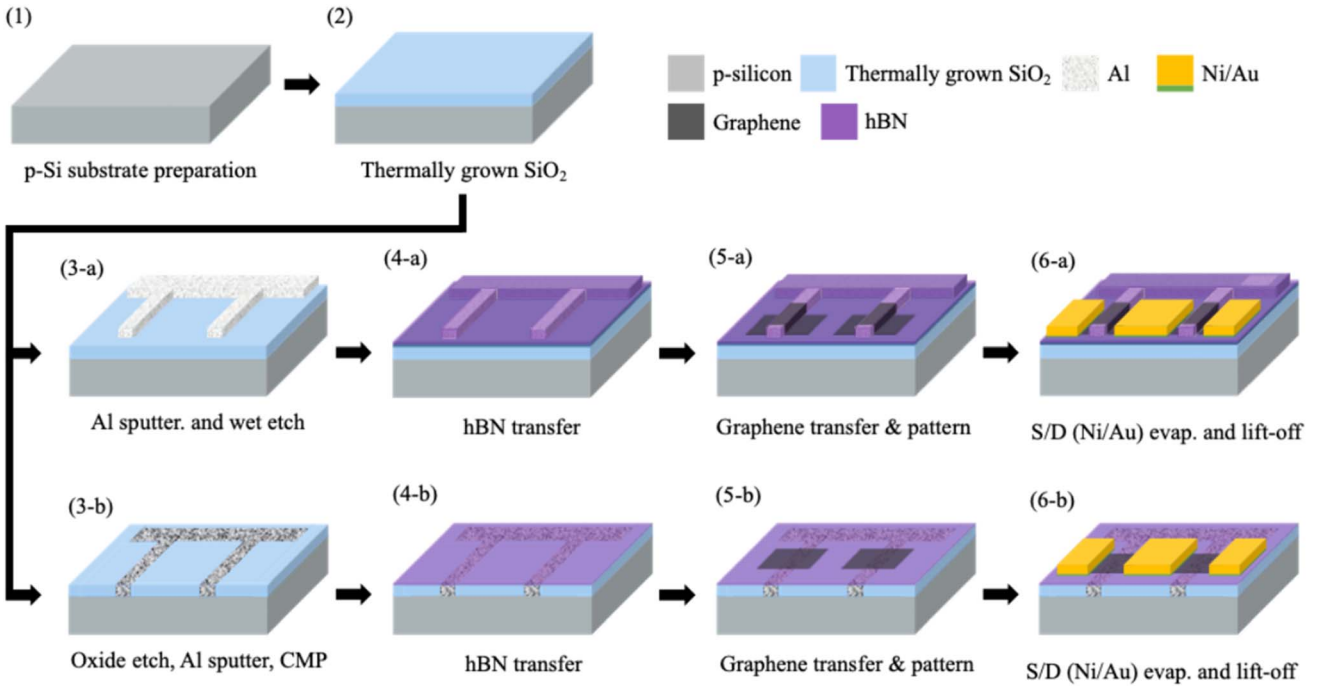

Fig. 2 Process flow schematic for the proposed process split of (a) raised and (b) recessed Al gate with monolayer hBN dielectric.

Grolltex, Inc. in 2023. An area of 2″ by 2″ was cut out and transferred onto the surface of the wafer *via* a PMMA-assisted process that was identical to our graphene transfer technique detailed in prior work.[37] The graphene transfer process follows a previously reported PMMA-assisted technique with CVD grown material from Graphenea, Inc.[37] Graphene is then patterned through standard photolithography and etched by oxygen plasma for 45 seconds. The resist was removed by an overnight acetone soak and rinsed with DI water. Lastly, source drain electrodes of Ni/Au (5/95 nm) were thermally evaporated and patterned with a lift-off approach.

3.2 Characterization and test methods

A scanning electron microscope (SEM) was used to inspect the fabricated graphene channels for any discontinuities and voids. The Tescan Mira3 Scanning Electron Microscope with a field-emission electron gun was utilized at the RIT Nanoimaging Laboratory to obtain all the shown SEM images at different tilt angles.

White light interferometry was used to observe the surface of the fabricated structures. The samples were coated with a 5 nm layer of Au in order to provide a reflective surface for accurate measurements. A Veeco Wyko NT110 was used to obtain 3D and 2D profiles at a 20× magnification. Phase shift mode was used to measure the expected dimensions accurately.

A Veeco Dimension 3000 AFM Atomic force microscope was used to inspect the active area of the Al gate electrode for surface roughness and topography while providing comparative results demonstrating that a CMP process reduces the topography of Al electrodes.

Raman spectroscopy was carried out with a JY Horiba Labram-HR Raman Spectroscope for further analysis on the quality of post-processing transferred graphene at multiple points of interest within the device's active area. A red 633 nm laser was used for the spectroscopy measurement with a measurement accumulation time of 30 seconds per measured data point.

Electrical testing was done with a semi-automated RK probe card station with an HP-4156 semiconductor parameter analyzer. Transfer characteristics curves were used to extract individual device Key Performance Metrics (KPMs) of Dirac voltage, mobility, and contact resistance as described in the Theory section.[48,49] A total of 256 devices, located within a rectangular area of 50 mm × 25 mm in the center of each 4-inch wafer, were tested. All these devices have a gate size of $W = 20$ μm and $L = 10$ μm.

The capacitor structures formed by the channel-to-gate overlap of larger GFETs were used for capacitance–voltage (C–V) measurements. A Keithley 4200A-SCS Parameter Analyzer at 100 kHz, 30 V-rms, as shown in the SI, was used to measure the value of C_{ox} for the extraction of mobility. Dielectric breakdown voltage to validate the C_{ox} values obtained was measured by increasing V_{GS} in steps of 20 mV, while keeping V_D and V_S at 0 V (see SI). Hysteresis sweeps, including 0 V-pulsed and 1 V-pulsed hysteresis sweeps (where V_{GS} is set to 0 V or 1 V prior to each measurement data collection), were used to evaluate interface traps of representative devices. More information on the hysteresis sweep method is presented in the SI.[50]

Following the electrical testing, statistical analysis was conducted using JMP 19™ (JMP Statistical Discovery LLC, SAS Institute Inc) on Dirac voltage, mobility, and contact resistance.

For each metric, the two groupings of data (raised Al gate and recessed Al gate) were compared utilizing an independent two-sample *t*-test. The *t*-test compares the average for each individual group as well as a pooled standard deviation between two normally distributed groups. The resultant *p*-value is then compared to an assumed alpha risk of 0.05 for a 95% confidence in the results.

4 Results

A schematic cross-section of the different structures under study in this work is shown in Fig. 3, showing a representation of local-back (a) raised and (b) recessed Al/hBN/graphene devices. The hBN dielectric is represented as purple and orange, while the graphene is represented as black. The gate electrode is designed as not to overlap the source and drain electrodes with a symmetrical ungated graphene access area with a length and width of 1 μm by 20 μm per side, respectively. The schematic representations are not to scale, as one would expect the raised aluminum gate not to be entirely vertical and have some isotropy, as well as the possibility that the hBN and graphene would drape over the raised gate and create an air gap.[39]

Fig. 4 shows a side-by-side scanning electron microscope (SEM) image of a raised aluminum gate device (Fig. 4(a)) with a gate length of 10 μm as defined by the aluminum and a gate width of 20 μm as defined by the graphene, and a recessed aluminum gate device (Fig. 4(b)) of similar dimensions. As seen in the close-up SEM of Fig. 4(c), the step created by the raised Al gate is clearly visible as the graphene drapes over the 100 nm edge. Conversely, this step is not as visible in the recessed Al gate device shown in Fig. 4(d), but a transition region can still be seen as the graphene goes over the Al gate. Fig. S1 shows three-dimensional white light interferometry scans of the surface of representative raised and recessed devices. As seen in the 2D profile in Fig. S2, the transition over the raised aluminum gate is measured to be about 110 nm, whereas the recessed aluminum gate step is under 3 nm. It is also observed from Fig. S2 that the CMP tiles provide a uniform surface within the features of matched dimensions and show the effectiveness of the CMP process. In contrast, dishing is observed in larger structures; subsequently, additional optimization of the CMP process may be necessary to reduce the observed variation further.

Atomic force microscopy (AFM) analysis was carried out to understand (1) the surface roughness near the step/transition

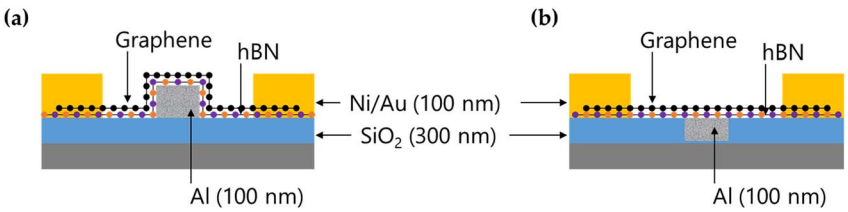

Fig. 3 Device cross-section for (a) raised and (b) recessed Al gate with hBN gate dielectric.

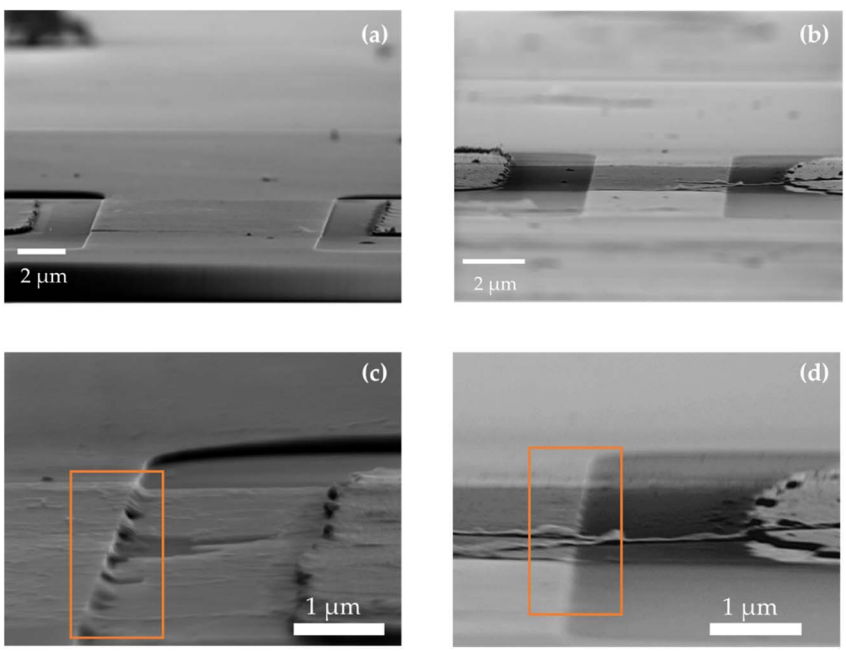

Fig. 4 SEMs of raised (a and c) and recessed (b and d) Al gate devices with monolayer hBN gate dielectric.

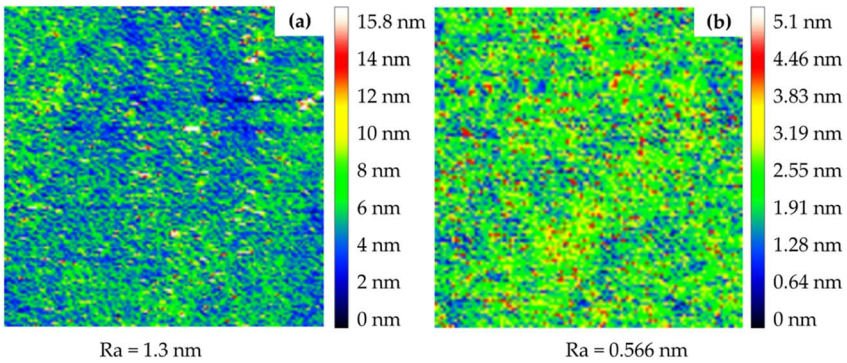

Fig. 5 AFM scan of (a) graphene on active area gate electrode hBN/raised Al gate with Ra of 1.3 nm, (b) graphene on active area gate electrode with hBN/recessed Al gate with Ra of 0.566 nm.

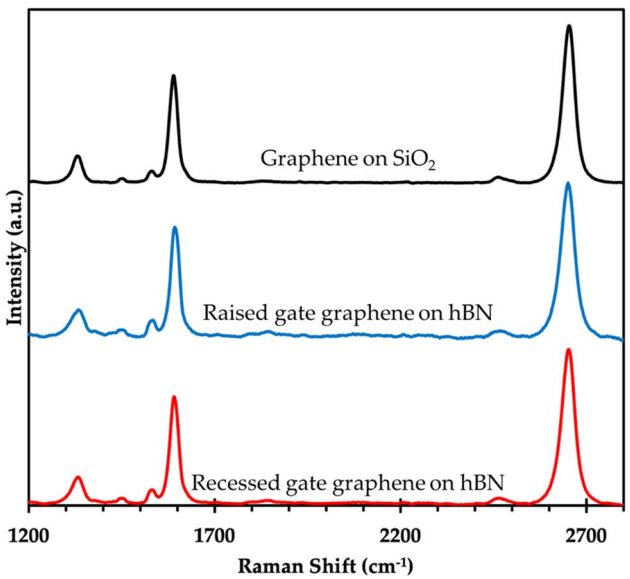

Fig. 6 Raman spectra of graphene on SiO_2, and on hBN on a raised and recessed aluminum gate, as indicated in the labels.

onto the gate electrode and (2) the roughness on top of the gate electrode itself. The average surface roughness (R_a) on the top of the electrode for the raised Al gate shown in Fig. 5(a) was 1.3 nm, while in Fig. 5(b), the recessed Al gate R_a was 0.566 nm, approximately half of its raised Al gate counterpart.

Raman spectroscopy was collected from the graphene film on top of SiO_2, and on top of the hBN dielectric on a raised and a recessed aluminum gate. As shown in Fig. 6, the qualitative spectra of the three structures are similar, which indicates that the quality of the graphene is not significantly different between the groups and does not seem to be influenced in great measure by the observed substrate smoothness.

Fig. 7(a) and (b) illustrate the I_DV_G transfer characteristics overlay of GFETs with a gate length of 10 μm and a gate width of 20 μm at V_{DS} = 0.1 V for raised Al gate and recessed Al gate devices, respectively. The transfer curves shown in the plots are normalized to the device gate width. Non-working devices, as well as the top and bottom 5% have been removed for all device structures in this investigation. Raw data, including all devices, is presented in Fig. S3 in the SI. The overlaid I_DV_G plots include both red and green transfer curves to illustrate the average and hero device performance of each group, respectively.

As seen in the green curves of Fig. 7 and the values on the insets, the performance of the hero devices is similar between the two groups in terms of maximum current drive and extracted hole mobility. In contrast, there is a clear difference in the variability of the transfer curves between the raised Al gate and the recessed Al gate. When looking only at current drive and the mobility of the hero devices, one may infer that they behave similarly with similar current drive at $V_{GS} = -1$ V, $V_{DS} = 0.1$ V of 7 μA μm^{-1} and 7.6 μA μm^{-1}. However, the average value increased significantly from 4.8 μA μm^{-1} to 6.6 μA μm^{-1}, while the variation is also reduced in the recessed Al gate structures. In addition, the Dirac voltage of the recessed Al gate process is significantly lower in magnitude, from an average of 1.2 V to 0.7 V, and shows much less variability.

5 Discussion

Fig. 8 shows a statistical analysis of the KPMs in box plots of the working devices of each group. Out of 256 tested devices in each group, only 137 and 175 devices work properly for (a) raised and (b) recessed Al gate structures, respectively. These numbers represented a yield of 53.5% for the raised process and of 68.5% for the recessed gate structure, which represents an improvement over the 18% yield that was previously presented for a raised Al gate process with a 15 nm Al_2O_3 gate dielectric.[37] Fig. S3 presents the distribution of working devices in 7 mm × 7 mm dies of raised and recessed hBN devices. The distribution of working devices does not present a clear pattern, but the overall yield numbers are similar to those observed over the larger tested area of 50 mm × 25 mm. The improvement in yield between the processes with Al_2O_3 to hBN dielectric is related to the inherently better matching properties between hBN and graphene, which favor the adhesion on the substrate during fabrication.[35,51] On the other hand, the adhesion properties of Al_2O_3 and graphene need to be carefully designed for optimal results.[52]

Recessed	V_{Dirac} (V)	μ_p ($cm^2V^{-1}s^{-1}$)	R_C (kΩ)
Hero	1.64	6980.54	0.65

Raised	V_{Dirac} (V)	μ_p ($cm^2V^{-1}s^{-1}$)	R_C (kΩ)
Hero	0.74	8358.73	0.43

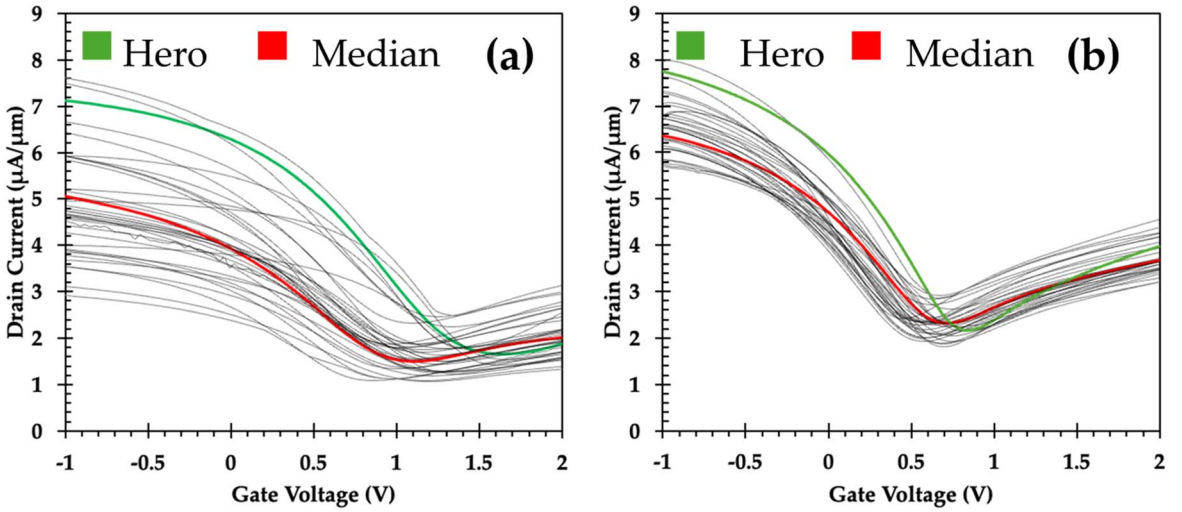

Fig. 7 Transfer characteristics overlay at $V_{DS} = 0.1$ V of fabricated graphene FETs with a gate length of 10 μm. Drain current is normalized to its width of 20 μm for (a) raised and (b) recessed Al gate with monolayer hBN gate dielectric.

5.1 Dirac voltage

As seen in Fig. 8(a), the recessed Al gate structure significantly reduces the Dirac voltage to an average of 0.7 V as opposed to 1.2 V for the raised Al gate. A *t*-test comparison of the two normal distributions showed a *p*-value of <0.0001. This indicates that there is a significant difference in the Dirac voltage between a raised and recessed Al gate structure. This significant reduction in Dirac voltage of the recessed Al gate structures is related to both the smoother transition step from the field to the gate structure, as seen in the SEM pictures, and the smoother surface of the gate area, measured *via* AFM. As shown in the results section, the transition step is reduced from 100 nm to just a few nanometer, and the surface roughness Ra of the gate region of the raised Al gate process is 1.3 nm, while the recessed Al gate R_a is 0.566 nm. The draped area of the raised Al gate structures and its rougher surface, which shows ripples and other derivations from a perfectly flat structure, can lead to electron–hole puddles,[53] strain-induced defects,[54] and adsorption of molecules and impurities, all of which led to Dirac point shifts.[55]

When integrating atomically thin gate dielectrics such as hBN, aggressive scaling without compromising device performance may be achieved with its superior electrostatic control in graphene FETs, which is attributed to its high breakdown strength, lattice matching, and minimal interface traps.[35] Both the dielectric material and its thickness affect shifts in the Dirac voltage. Monolayer hBN provides an atomically flat and inert surface that reduces charge inhomogeneity and results in a more consistent Dirac voltage when compared to other dielectric materials; in addition, the thickness of the dielectric layer affects the electrostatics in the gated channel region, and thus, the electrical conditions to set a charge neutrality point (Dirac voltage).[35] The consistent standard deviation of 13-16% suggests that the improvement is mainly driven by material and structural changes, not outlier behavior. Achieving a Dirac point near 0 V is crucial for low-power non-linear analog applications, and this trend confirms the effectiveness of the hBN dielectric and recessed gate architecture.[56]

5.2 Mobility

The mobility for each device can be calculated as described in eqn (3). The value used for $C_{ox} = 5.5 \times 10^{-3}$ F m^{-2} was measured on large capacitor test structures as opposed to individual devices to avoid parasitic capacitances or other parameters already factored with the proposed extraction methods. An extended discussion of the C_{ox} measurement and calculation is presented in the SI, with *C*–*V* measurements of large area Al-dielectric-graphene capacitors shown in Fig. S1, dielectric breakdown voltage measurements in Fig. S4, and an estimation of the dielectric film composition in Fig. S5. The fact that the capacitance per unit area (F m^{-2}) is consistent across each of the large area capacitors tested and the breakdown voltage is >3 V, indicates that a native AlO_x dielectric is present between the monolayer hBN and the gate aluminum electrode.[39]

As seen in Fig. 8(b), the value of hole carrier mobility shows an improvement in the recessed Al gate structures. Although the Raman spectra shown in Fig. 6 did not indicate much differences in the graphene quality, the observable improvement in hole carrier mobility is both in terms of magnitude, which increases by 42% from 3383 V s cm^{-2} to 4794 V s cm^{-2}, and variability, which is reduced by nearly 50%, from 36% to 18% standard deviation for the normally distributed populations of

data. Performing the statistical analysis detailed in Section 3.2, a *p*-value of <0.0001 was produced, supporting that there is a statistically significant change in mobility with the recessed gate architecture. These improvements are supported by the smoother transition over the gate structure and the smoother surface roughness of the recessed Al gate process. In comparison, a much smoother surface provides a more pristine graphene film, especially when in contact with hBN in both the field and channel area, serving as the gate oxide, providing improved lattice-matching qualities. These improvements in surface topology lead to less scattering of the carriers and improved mobility.[57]

5.3 Contact resistance

Fig. 8(c) shows the box plots of the contact resistance values of both groups. The contact resistance mean and percent standard deviation remain comparable between the two device structures, as contact materials and processes are identical between the two groups. The size of the measured contact area between the Ti/Au and graphene over hBN is 12 μm long by 20 μm wide. As mentioned before, the role of the hBN as an underlayer in this contact structure is to provide a matched lattice layer for the graphene as opposed to Al_2O_3 or SiO_2, which may introduce trapped charges and surface roughness.[42] The mean contact resistance of the raised Al gate is 0.75 kΩ, which is only slightly higher than 0.67 kΩ for recessed Al gates. The relatively large percent standard deviation values are similar at 42% and 37%, respectively. Upon comparing the groups, however, a *t*-test *p*-value of 0.025 is observed, indicating there is a significant difference between the two device structures, albeit less so than for the Dirac voltage or mobility. This difference could be attributed to the presence of random defects rather than process or materials differences, and further investigation is necessary. In contrast, the contact resistance drops significantly when moving from Al_2O_3 to hBN as the contact underlayer dielectric, as shown in Fig. S11 in the SI. When compared to data presented previously by our group in,[37] substituting hBN in an identical Al_2O_3/raised gate process improves the contact resistance compared to an average of 2.59 kΩ measured in 37 devices. In addition, the standard deviation of the Al_2O_3/raised gate was 78%, likely due to poor interfacial quality, and increased roughness.[37]

5.4 Hysteresis

Hysteresis sweeps of GFETs with non-pulsed and pulsed (based 0 V) bias are shown in Fig. 9(a) and (b) for a raised Al gate device, and in Fig. 9(c) and (d) for a recessed Al gate device. The purpose of the pulsed testing is to reduce the impact of traps, while under the assumption that the time constant associated with trap charging is greater than the pulse width.[58] A hysteresis window is reported next as the difference between V_{Dirac} at forward and backward V_{GS} sweeps. As seen in Fig. 9(a) and (b), the hysteresis window is 240 mV for GFET with a raised Al gate structure without pulsing, while a 30 mV hysteresis window is seen when pulse testing is applied. Additionally, when applying a 1 V pulse, the hysteresis window is further reduced to 15 mV as seen in Fig. S8 in the SI. These results indicate the presence of interface traps, which would lead to device variation during test.[50] As seen in Fig. 9(c) and (d), the hysteresis window is about 90 mV for GFET with the recessed Al gate structure without pulsing, while a 50 mV hysteresis window is seen when pulse testing is applied. The smaller 40 mV difference between the pulse and no-pulse method indicates that although interface traps exist, these are much less than with the raised Al topology. Although these results indicate that the step architecture and surface roughness of the raised aluminum gate topology lead to interface traps and increased variation, the effect of the different channel electrostatics cannot be ignored, and further studies are necessary.

In summary, the planarization process presented in this paper provides a statistical improvement in the performance and variability of graphene transistors in terms of the Dirac point and mobility when compared to a raised gate architecture. The reason for these improvements is related to the planarization process and the smoother transition and gate surface. Hysteresis measurements indicate that the level of traps in the hBN/graphene interface is much lower in the recessed process, which accounts for the reduced device-to-device variation. In

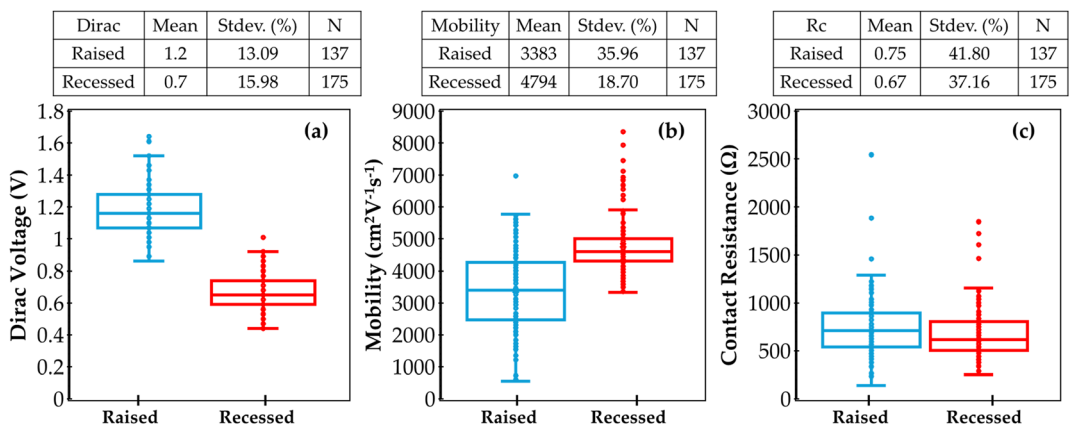

Fig. 8 Box and whisker illustration of device performance and variation of working raised and recessed Al gate devices determined by (a) Dirac voltage, (b) mobility, and (c) contact resistance.

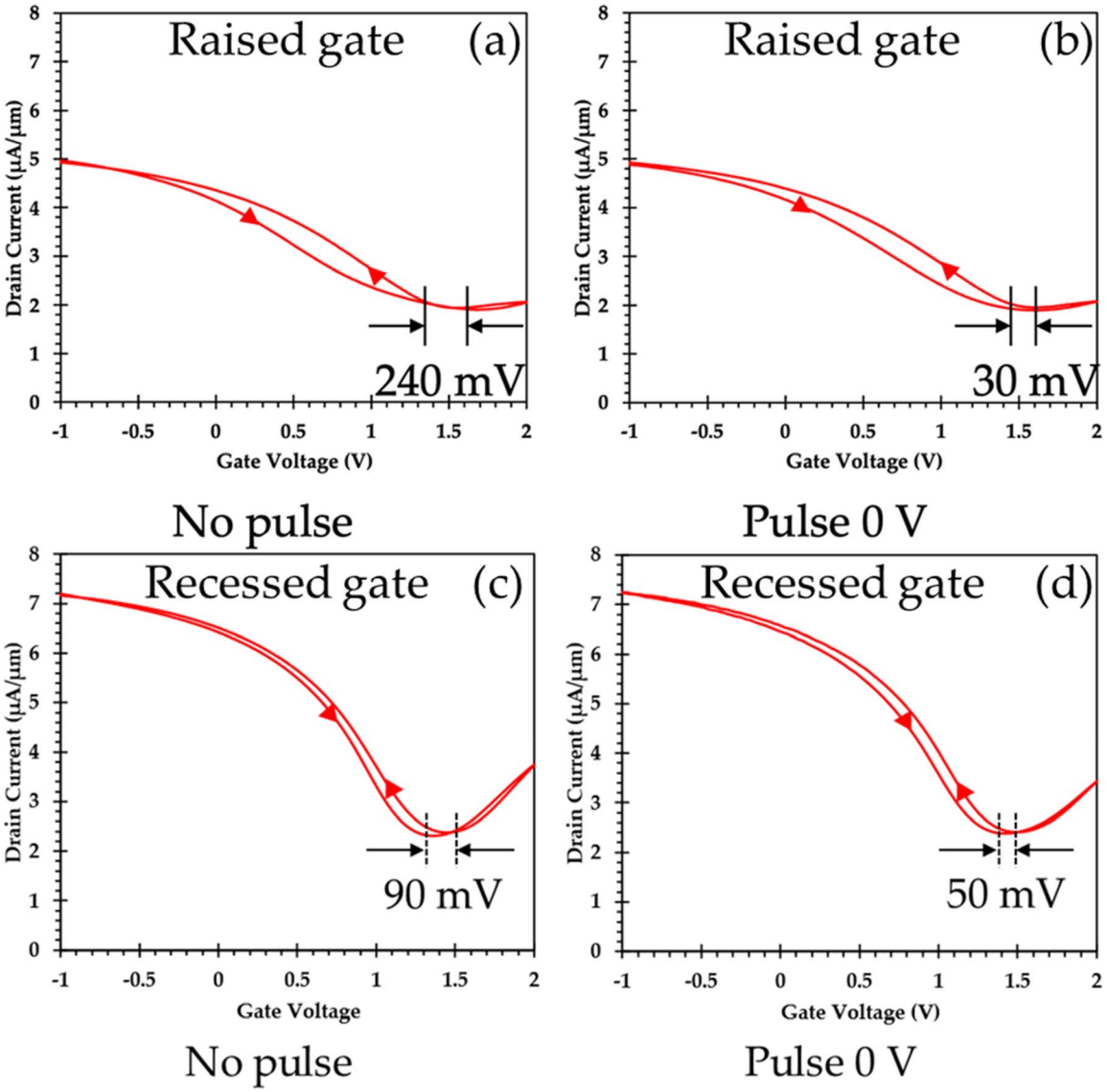

Fig. 9 Hysteresis curves for raised (a) and (b), and recessed (c) and (d) Al gate GFETs with a no-pulse method (a) and (c), and a 0 V-pulse method (b) and (d).

addition, the non-homogeneous features of the raised gate architecture (*i.e.*, unpolished aluminum, graphene draping) play a significant role in the mobility degradation and in the minimum carrier density affecting both the drain current and Dirac voltage.[38] When compared to other dielectrics, such as Al_2O_3,[37] hBN also offers advantages in terms of yield and contact resistance when used in a local-back gate process. In addition, the observed parameter variability is much reduced with the use of hBN as a dielectric due to better material compatibility during processing, which, along with other process improvement and considerations, could lead to the needed improvement in yield and reliability.[34,36,59]

Finally, the presented results are compared to other published work that includes similar statistical data. Martini *et al.*, 2023,[35] presented a scatter plot distribution of hole mobility *versus* V_{Dirac} measured on >100 TLM-like structures of graphene on hBN continuous films grown *via* ion beam-assisted physical vapor deposition directly on 300 nm-SiO_2 on Si substrates. The V_{Dirac} measurements have been transformed into the vertical electric field (E_{field}) by normalizing to the reported dielectric thickness in all cases. Martini *et al.* used a back-gate configuration so that the graphene channel had no topology. As such, this flat structure serves as a best-case scenario for our intended recessed Al gate architecture. As seen in Fig. 10, the hole mobility numbers reported by Martini *et al.* are slightly higher than ours in the recessed architecture, which corroborates the fact that our channels are not entirely flat and would benefit from improvements in the transition step between the field and gate regions. In addition, the E_{field} at V_{Dirac} is comparable between the flat and the recessed architecture. Moreover, this

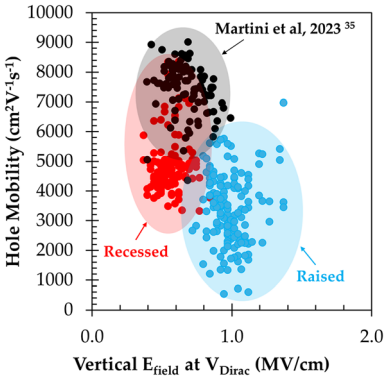

Fig. 10 Scatter plot of mobility *vs.* E_{field} at V_{Dirac} comparing our study to Martini *et al.*, 2023.[35] Shaded color areas are added to guide the eye and do not represent any statistical measurements.

data corroborates that both the flat and recessed architecture improves the performance in terms of hole mobility and the E_{field} at V_{Dirac} when compared to the raised architecture.

6 Conclusion

While prior studies have aimed to improve GFET performance or reduce variability, most work has typically been done in evaluating disparate device structures, materials, or fabrication flows, and focusing only on "hero" devices that do not reflect broader statistical trends. In contrast, our work systematically integrates monolayer hBN as a gate dielectric and directly compares a raised *versus* a CMP-recessed aluminum gate within a unified fabrication platform, enabling direct, controlled comparisons across design variations. By analyzing complete device distributions rather than peak values alone, this study offers critical insights into how gate topology influences reproducibility. This work statistically demonstrates that the recessed Al gate topology not only enhances key performance metrics, including Dirac voltage and hole mobility, but also reduces device-to-device variation and increases yield. Due to the smoother surface, channel to gate transition, and lower number of interface traps, the recessed Al gate topology, as opposed to a raised gate, decreases the standard deviation of the extracted graphene hole mobility from 36% to 18%, while improving device yield from 54.4% to 65.1%. In addition, the Dirac point shifted closer to 0 V (from ~1.2 V to 0.7 V), and the contact resistance was reduced from 0.75 kΩ to 0.67 kΩ. Ultimately, our findings establish practical design and process guidelines for realizing scalable, high-performance graphene electronics to bridge gaps between isolated breakthroughs and manufacturable, wafer-level technologies. The observed consistency suggests that a recessed Al gate structure with a hBN dielectric is a strong candidate for an optimal platform of scalable and high-performance GFET fabrication.

Author contributions

Conceptualization: T-J. Huang, I. Puchades. Data curation: T-J. Huang, A. Spencer, L. Ingraham. Formal analysis: T-J. Huang, A. Spencer, L. Ingraham, A. Pacheco, I. Puchades. Funding acquisition: A. Pacheco, I. Puchades. Investigation: T-J. Huang, L. Ingraham, A. Pacheco, I. Puchades. Methodology: T-J. Huang, A. Spencer, Project administration: I. Puchades. Resources: I. Puchades. Software: T-J. Huang, A. Spencer, L. Ingraham. Supervision: T-J. Huang, I. Puchades. Validation: L. Ingraham, A. Pacheco, I. Puchades. Visualization: T-J. Huang, A. Spencer, L. Ingraham, A. Pacheco, I. Puchades. Writing – original draft: T-J. Huang, A. Spencer. Writing – review & editing: L. Ingraham, A. Pacheco, I. Puchades.

Conflicts of interest

There are no conflicts of interest to declare.

Data availability

Data for this article are available at the Rochester Institute of Technology repository https://repository.rit.edu/data/3/ at [https://doi.org/10.58044/kgcoe-hy06]. The following data files are available.

IDVG of fabricated raised and recessed graphene transistors sorted by gate length: IDVG_Raised_GFETs.csv; IDVG_Recessed_GFETs.csv.

Calculated mobility sorted by gate type: GFET_Rsd_Rec_Mobility.csv.

Calculated contact resistance by gate type: GFET_Rsd_Rec_Contact Resistance.csv.

Measured VDirac by gate type: GFET_Rsd_Rec_Dirac.csv.

Mobility *vs.* Efield at VDirac sorted by gate type and compared to Martini *et al.* 2023: GFET_Rsd_Rec_u *vs.* Vdirac.csv.

Supplementary information (SI): 3D and 2D white-light interferometry of typical fabricated devices. ID–VG plots of all tested devices. Mobility extraction example. CV measurements of test structues. Gate dielectric breakdown voltage measurements. C_{ox} discussion. Hysteresis pulse test description and measurements. Heatmaps of key performance parameters and yield. Contact resistance comparison between hBN and Al_2O_3 as underlaying films. See DOI: https://doi.org/10.1039/d5na01086a.

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References

1 M. C. Lemme, D. Akinwande, C. Huyghebaert and C. Stampfer, *Nat. Commun.*, 2022, **13**, 1392.
2 A. Splendiani, L. Sun, Y. Zhang, T. Li, J. Kim, C.-Y. Chim, G. Galli and F. Wang, *Nano Lett.*, 2010, **10**, 1271–1275.
3 G. C. Ghivela and J. Sengupta, *IEEE Microw. Mag.*, 2020, **21**, 48–65.
4 M. Saeed, P. Palacios, M. Wei, E. Baskent, C. Fan, B. Uzlu, K. Wang, A. Hemmetter, Z. Wang, D. Neumaier, M. C. Lemme and R. Negra, Graphene-based microwave circuits: a review, *Adv. Mater.*, 2022, **34**(48), 2108473–2108473, DOI: 10.1002/adma.202108473.
5 P. Bøggild, *Nat. Commun.*, 2023, **14**, 1126.
6 Z. Gao, H. Kang, C. H. Naylor, F. Streller, P. Ducos, M. D. Serrano, J. Ping, J. Zauberman, Rajesh, R. W. Carpick, Y.-J. Wang, Y. W. Park, Z. Luo, L. Ren and A. T. C. Johnson, Scalable production of sensor arrays based on high-mobility hybrid graphene field effect transistors, *ACS Appl. Mater. Interfaces*, 2016, **8**, 27546–27552, DOI: 10.1021/acsami.6b09238.
7 M. Tian, B. Hu, H. Yang, C. Tang, M. Wang, Q. Gao, X. Xiong, Z. Zhang, T. Li, X. Li, C. Gu and Y. Wu, Wafer scale mapping and statistical analysis of radio frequency characteristics in highly uniform CVD graphene transistors, *Adv. Electron. Mater.*, 2019, **5**(4), 1800711, DOI: 10.1002/aelm.201800711.
8 A. Quellmalz, X. Wang, S. Sawallich, B. Uzlu, M. Otto, S. Wagner, Z. Wang, M. Prechtl, O. Hartwig, S. Luo, G. S. Duesberg, M. C. Lemme, K. B. Gylfason, N. Roxhed, G. Stemme and F. Niklaus, *Nat. Commun.*, 2021, **12**, 917.
9 N. Hong, D. Kireev, Q. Zhao, D. Chen, D. Akinwande and W. Li, Roll-to-roll dry transfer of large-scale graphene, *Adv. Mater.*, 2021, **34**(3), 2106615, DOI: 10.1002/adma.202106615.
10 M. B. Lerner, D. Pan, Y. Gao, L. E. Locascio, K.-Y. Lee, J. Nokes, S. Afsahi, J. D. Lerner, A. Walker, P. G. Collins, K. Oegema, F. Barron and B. R. Goldsmith, *Sens. Actuators B Chem.*, 2017, **239**, 1261–1267.
11 A. D. Smith, S. Wagner, S. Kataria, B. Gunnar Malm, M. C. Lemme and M. Ostling, *IEEE Trans. Electron Devices*, 2017, **64**, 3919–3926.
12 M. Bonmann, M. Asad, X. Yang, A. Generalov, A. Vorobiev, L. Banszerus, C. Stampfer, M. Otto, D. Neumaier and J. Stake, *IEEE Electron Device Lett.*, 2019, **40**, 131–134.
13 H. Xu, Z. Zhang, H. Xu, Z. Wang, S. Wang and L.-M. Peng, *ACS Nano*, 2011, **5**, 5031–5037.
14 W. Wei, X. Zhou, G. Deokar, H. Kim, M. M. Belhaj, E. Galopin, E. Pallecchi, D. Vignaud and H. Happy, *IEEE Trans. Electron Devices*, 2015, **62**, 2769–2773.
15 H. Lyu, Q. Lu, J. Liu, X. Wu, J. Zhang, J. Li, J. Niu, Z. Yu, H. Wu and H. Qian, *Sci. Rep.*, 2016, **6**, 35717.
16 L. Zakrajsek, E. Einarsson, N. Thawdar, M. Medley and J. M. Jornet, *IEEE Antennas Wirel. Propag. Lett.*, 2016, **15**, 1553–1556.
17 J. Crabb, X. C. Roman, J. M. Jornet and G. R. Aizin, *Appl. Phys. Lett.*, 2022, **121**, 143502.
18 S. Karak, S. Paul, D. Negi, B. Poojitha, S. K. Srivastav, A. Das and S. Saha, *ACS Appl. Nano Mater.*, 2021, **4**, 1951–1958.
19 K. Y. Ma, M. Kim and H. S. Shin, *Acc. Mater. Res.*, 2022, **3**, 748–760.
20 D. Y. Jung, S. Y. Yang, H. Park, W. C. Shin, J. G. Oh, B. J. Cho and S.-Y. Choi, *Nano Converg.*, 2015, **2**, 11.
21 C. J. McClellan, E. Yalon, K. K. H. Smithe, S. V Suryavanshi and E. Pop, *ACS Nano*, 2021, **15**, 1587–1596.
22 H. Wang, A. Hsu, J. Wu, J. Kong and T. Palacios, *IEEE Electron Device Lett.*, 2010, **31**, 906–908.
23 C.-W. Chen, W.-H. Cho, C.-Y. Chang, C.-Y. Su, N.-N. Chu, C.-C. Kei and B.-R. Li, *J. Vac. Sci. Technol. A*, 2023, **41**, 012602.
24 N. C. S. Vieira, J. Borme, G. Machado Jr., F. Cerqueira, P. P. Freitas, V. Zucolotto, N. M. R. Peres and P. Alpuim, *J. Phys.: Condens. Matter*, 2016, **28**, 085302.
25 W. G. M. Van Den Hoek, *MRS Online Proc. Libr.*, 1986, **68**, 71.
26 C. J. Estrada, Z. Ma and M. Chan, *IEEE Electron Device Lett.*, 2021, **42**, 1890–1893.
27 M. Šiškins, C. Mullan, S. K. Son, J. Yin, K. Watanabe, T. Taniguchi, D. Ghazaryan, K. S. Novoselov and A. Mishchenko, *Appl. Phys. Lett.*, 2019, **114**, 123104.
28 N. Petrone, T. Chari, I. Meric, L. Wang, K. L. Shepard and J. Hone, *ACS Nano*, 2015, **9**, 8953–8959.
29 Y. Shimazu, R. Ishikawa and H. Akaishi, *Phys. Lett. A*, 2025, **554**, 130724.
30 T. Knobloch, B. Uzlu, Y. Y. Illarionov, Z. Wang, M. Otto, L. Filipovic, M. Waltl, D. Neumaier, M. C. Lemme and T. Grasser, *Nat. Electron.*, 2022, **5**, 356–366.
31 W. B. Choi, Y. Son, H. Park, Y. Jeong, J. Oh, K. Watanabe, T. Taniguchi and J. Jang, Characterization of a graphene-hBN superlattice field effect transistor, *Appl. Phys. Lett.*, 2024, **125**, 0335303, DOI: 10.1063/5.0216377.
32 A. K. Behera, C. T. Harris, D. V. Pete, C. M. Smyth, M. B. Muniz, O. Koybasi, T. Taniguchi, K. Watanabe, B. D. Belle and S. R. Das, *ACS Appl. Nano Mater.*, 2024, **7**, 12366–12375.
33 Z. Zhang, B. Zhang, Y. Zhang, Y. Wang, P. Hays, S. A. Tongay, M. Wang, H. Han, H. Li, J. Zhang and A. Song, *Nat. Commun.*, 2025, **16**, 1–10.
34 S. Fukamachi, P. Solís-Fernández, K. Kawahara, D. Tanaka, T. Otake, Y. C. Lin, K. Suenaga and H. Ago, *Nat. Electron.*, 2023, (6), 126–136.
35 L. Martini, V. Mišeikis, D. Esteban, J. Azpeitia, S. Pezzini, P. Paletti, M. W. Ochapski, D. Convertino, M. G. Hernandez, I. Jimenez and C. Coletti, *ACS Appl. Mater. Interfaces*, 2023, **15**, 37794–37801.
36 W. Zheng, S. Pazos, Y. Yuan, K. Zhu, Y. Shen, Y. Ping, O. Alharbi, S. Krotkus, S. Pasko, J. Mischke, E. Yengel, A. Henning, S. ElKazzi and M. Lanza, *Adv. Mater.*, 2025, e10501.
37 T.-J. Huang, A. Ankolekar, A. Pacheco-Sanchez and I. Puchades, *Appl. Sci.*, 2023, **13**(12), 7201, DOI: 10.3390/app13127201.
38 W. Wei, E. Pallecchi, M. Belhaj, A. Centeno, Z. Amaia, D. Vignaud and H. Happy, in *EuMIC 2016 - 11th European Microwave Integrated Circuits Conference*, Institute of Electrical and Electronics Engineers Inc., 2016, pp. 165–168.

39 W. Wei, X. Zhou, G. Deokar, H. Kim, M. M. Belhaj, E. Galopin, E. Pallecchi, D. Vignaud and H. Happy, *IEEE Trans. Electron Devices*, 2015, **62**, 2769–2773.
40 M.-Q. Long, L. Tang, D. Wang, L. Wang and Z. Shuai, *J. Am. Chem. Soc.*, 2009, **131**, 17728–17729.
41 J. E. Padilha, R. B. Pontes and A. Fazzio, *J. Phys.: Condens. Matter*, 2012, **24**, 075301.
42 I. Meric, C. R. Dean, N. Petrone, L. Wang, J. Hone, P. Kim and K. L. Shepard, *Proc. IEEE*, 2013, **101**, 1609–1619.
43 M. Chhikara, G. Bratina and E. Pavlica, *ACS Omega*, 2023, **8**, 27534–27542.
44 H. Agarwal, B. Terrés, L. Orsini, A. Montanaro, V. Sorianello, M. Pantouvaki, K. Watanabe, T. Taniguchi, D. Van Thourhout, M. Romagnoli and F. H. L. Koppens, *Nat. Commun.*, 2021, **12**, 1070.
45 A. R. Cadore, E. Mania, K. Watanabe, T. Taniguchi, R. G. Lacerda and L. C. Campos, Thermally activated hysteresis in high quality graphene/h-BN devices, *Appl. Phys. Lett.*, 2016, **108**, 233101, DOI: 10.1063/1.4953162.
46 A. Laturia, M. L. Van de Put and W. G. Vandenberghe, *npj 2D Mater. Appl.*, 2018, **2**, 6.
47 A. D. Smith, S. Wagner, S. Kataria, B. Gunnar Malm, M. C. Lemme and M. Ostling, *IEEE Trans. Electron Devices*, 2017, **64**, 3927–3933.
48 A. Pacheco-Sanchez, N. Mavredakis, D. Jiménez and F. Pasadas, *15th Spanish Conference on Electron Devices, CDE 2025*, 2025, 1–4.
49 A. Pacheco-Sanchez, N. Mavredakis, P. C. Feijoo and D. Jimenez, *IEEE Trans. Electron Devices*, 2022, **69**, 4037–4041.
50 A. Pacheco-Sanchez, N. Mavredakis, P. C. Feijoo, W. Wei, E. Pallecchi, H. Happy and D. Jimenez, *IEEE Trans. Electron Devices*, 2020, **67**, 5790–5796.
51 M. Szyniszewski, E. Mostaani, A. Knothe, V. Enaldiev, A. C. Ferrari, V. I. Fal'ko and N. D. Drummond, *ACS Nano*, 2025, **19**, 6014–6020.
52 D. W. Park, S. Mikael, T. H. Chang, S. Gong and Z. Ma, *Appl. Phys. Lett.*, 2015, **106**, 10.
53 J. Martin, N. Akerman, G. Ulbricht, T. Lohmann, J. H. Smet, K. Von Klitzing and A. Yacoby, *Nat. Phys.*, 2008, **4**, 144–148.
54 D. Das, S. Bhattacharyya, E. Muñoz and A. K. Singh, *Phys. Rev. B*, 2016, **94**, 115438.
55 X. Zhu, K. Liu, Z. Lu, Y. Xu, S. Qi, G. Zhang and P. E. L. Dimens, *Syst. Nanostruct.*, 2020, **117**, 113827.
56 A. Pacheco-Sanchez, J. N. Ramos-Silva, N. Mavredakis, E. Ramírez-García and D. Jiménez, *Electronics*, 2024, **13**, 4022.
57 A. Tyagi, V. Mišeikis, L. Martini, S. Forti, N. Mishra, Z. M. Gebeyehu, M. A. Giambra, J. Zribi, M. Frégnaux, D. Aureau, M. Romagnoli, F. Beltram and C. Coletti, *Nanoscale*, 2022, **14**, 2167–2176.
58 M. Haferlach, M. Claus, T. Nardmann, A. Pacheco-Sanchez, P. Sakalas and M. Schröter, in *NSTI-Nanotech*, 2014, pp. 512–517.
59 IRDSTM, Beyond CMOS and Emerging Materials Integration - IEEE IRDSTM, 2023, https://irds.ieee.org/editions/2023/20-roadmap-2023-edition/126-irds%E2%84%A2-2023-beyond-cmos-and-emerging-materials-integration, accessed 24 July 2025.