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A tellurium-free GeSbSe thin film for reliable selector-only memory operation

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Selector-only memory (SOM) devices are promising candidates for non-volatile memory units with high-density crossbar array architectures due to their simple two-terminal configuration, compatibility with two-terminal architectures, and the elimination of the need for separate selector-storage layers. These advantages reduce fabrication complexity, minimize cell footprint, and enable low-power operation. To date, most SOM devices have been based on tellurium (Te)-containing chalcogenide materials, in which Te atoms act as essential trigger elements, enabling field-driven switching due to their highly polarizable p-orbitals. However, the intrinsic properties of Te also introduce critical limitations, including poor thermal stability, high leakage current, and a narrow read window margin (RWM), which constrain device reliability and scalability. To overcome these challenges, a Te-free amorphous material, GeSbSe (GSS), has been developed to preserve desirable threshold switching behavior. The GSS-based SOM device exhibits a wide RWM (2 V), reliable operation at fast operation speeds (50 ns), and ultra-low write-pulse current (10 μA), indicating its potential for high-speed and low-power operation. Furthermore, a Te-containing counterpart, GeSbSeTe (GSST), was fabricated and systematically characterized to investigate the detrimental impact of Te incorporation on the electrical characteristics. By evaluating various electrical performance metrics, the electrical degradation of SOM devices induced by Te incorporation was systematically evaluated. A comparative analysis with the Te-free GSS counterpart highlights the adverse effects of Te on device stability and switching uniformity, offering insights into the design of more reliable SOM devices.

New concepts

Selector-only memory (SOM) devices have widely employed Te-containing chalcogenides. However, the specific impact of Te in governing SOM characteristics has not been systematically clarified from a materials perspective and the performance has largely been discussed in terms of compositional optimization rather than a mechanism linking composition, bonding structure, and electronic transport. Here we show that the governing factor of SOM operation is not the presence of Te itself but the defect and bonding landscape controlling trap energetics. In contrast to prior studies where Te-containing chalcogenides were predominantly used for SOM operation, our results indicate that Te incorporation can limit stability and integration compatibility. By directly comparing Te-containing GeSbSeTe and Te-free GeSbSe, we find that Te deepens trap states and introduces bonding instability, leading to degraded threshold stability, reduced read-window margin (RWM), slower operation speed, and reliability loss. Furthermore, the low crystallization temperature and high leakage characteristics of Te-containing chalcogenides are unfavorable for chip-level integration under back end of line (BEOL) thermal constraints. Implementing a Te-free ternary Ge–Sb–Se system enables BEOL-compatible SOM operation with improved performance. These results establish a materials design principle that links trap-controlled electronic switching, bonding stability, and device reliability in amorphous chalcogenides.

1. Introduction

The rapid growth of artificial intelligence and cloud-based data storage markets is driving an unprecedented surge in memory demand. However, the conventional von Neumann architecture inherently suffers from the so-called "memory wall," a fundamental latency bottleneck arising from frequent data transfers between the processor and memory units. This bottleneck induces significant slowdowns in communication between memory and computational devices, ultimately degrading overall information processing performance. Recently, emerging memory architectures such as high bandwidth memory (HBM) and Compute Express Link (CXL) have been actively investigated to address these limitations. CXL is a next-generation memory interface that enables flexible, byte-addressable, and

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coherent memory expansion across CPUs, GPUs, and accelerators.[1–3] Unlike conventional architectures centered on a single processing unit, CXL allows multiple processing devices to share a large, unified memory pool, thereby enabling high-speed data processing. In CXL-based memory architectures, there is an increasing demand for next-generation memory that consumes less power than dynamic random-access memory (DRAM) and offers faster access speeds than NAND flash memory, serving as a bridge between memory and storage for efficient computation.[4–7] In particular, next-generation non-volatile memories (NVMs) with two-terminal crossbar array (CA) structures are considered compatible with high integration density and back-end of line (BEOL) processes.[5] However, the practical implementation of CA structures is often constrained by parasitic sneak-path currents, which not only degrade signal fidelity but also complicate large-scale array integration. To mitigate this issue, conventional architectures have employed a one-selector–one-memory (1S1M) configuration; however, this approach suffers from increased fabrication complexity and elevated operating voltages due to interfacial resistance.

To overcome these limitations, there has been increasing demand for a material and device concept capable of simultaneously providing selector functionality *via* threshold switching (TS) and enabling information storage within a compact two-terminal cell. To elaborate further on this concept, TS is generally described as an abrupt transition of an amorphous insulating material from a high-resistance state to a highly conductive state when the applied bias reaches a threshold voltage (V_{th}).[8] TS has been realized through multiple physical mechanisms depending on the targeted hardware functionality, most notably electronic ovonic threshold switching (OTS) selectors or diffusion-driven threshold memristors explored for neuromorphic computing. In diffusion-driven threshold memristors, switching originates from field-induced migration and aggregation of mobile ions (*e.g.*, Ag or Cu), forming a transient conductive pathway that spontaneously dissolves through diffusion after stimulus removal. This intrinsic relaxation behavior provides built-in temporal dynamics, enabling spike generation, short-term plasticity, and probabilistic response characteristics suitable for emulating neuromorphic neurons and synapses. In this context, diffusion-driven threshold memristors naturally exhibit stochastic activation and history-dependent responses, operate at low energy, and support biologically relevant time constants, which are advantageous for adaptive and learning-oriented neuromorphic systems. Their ion-mediated dynamics also enable gradual conductance evolution and flexible switching behavior, allowing functional diversity in neuromorphic implementations across variability and temporal-response regimes.[9–11] In contrast, electronic OTS switching arises primarily from electronic excitation and trap-assisted transport within an amorphous chalcogenide network without requiring ionic filament formation. Consequently, OTS devices typically exhibit steep nonlinearity, fast response latency, improved cycle-to-cycle uniformity, and moderate endurance, desirable for crossbar arrays.[8] From a system perspective, diffusion-driven threshold memristors are well-suited to neuron- or synapse-oriented hardware where stochasticity and adaptive temporal dynamics are desirable. OTS selectors, on the other hand, have been widely utilized in dense memory arrays owing to their low leakage, reproducibility, and reliable switching margins. At the same time, recent studies suggest that OTS-based and selector-only memory (SOM)-type devices may also be adaptable for neuromorphic functionalities; for example, a chalcogenide SOM demonstrated in a 4k crossbar array exhibited multilevel programmable threshold states under different write conditions, implying the possibility of representing multiple conductance levels.[12,13] However, such applications remain at an early stage of development and require further investigation. Building upon this selector-grade OTS behavior, polarity-dependent threshold–voltage modulation can be further exploited to encode information in the threshold state itself, motivating the SOM concept that integrates selection and storage within a single device and alleviates the density penalty of conventional 1S1M architectures.

SOM, an emerging solution, integrates both memory and selector functionalities within a single chalcogenide active layer, enabling a compact, low-power two-terminal device architecture favorable for scaling.[14–17] Owing to its advantages in low-power consumption and high operating speed, SOM has attracted significant interest as a potential candidate for storage-class memory (SCM) in advanced CXL architectures. Its simplified device architecture holds promise for meeting the durability and performance requirements of future high-bandwidth memory ecosystems.[18–20] In SOM devices, memory operation is realized through the intrinsic, polarity-dependent TS behavior of Group VI chalcogenide materials. This property enables compact two-terminal designs, improved scalability, reduced power consumption, and lower process complexity. SOM operation is governed by a TS mechanism in which two distinct V_{th} are induced depending on whether the polarity of the write pulse matches that of the read pulse, corresponding to the binary states "0" and "1," respectively. Among chalcogenide materials that exhibit TS, tellurium (Te)-based compounds have been extensively studied for selector applications due to their favorable switching characteristics associated with the relatively high defect density in Te-rich amorphous networks.[21–24] Considerable efforts have been devoted to understanding Te-containing chalcogenides in OTS selector systems, where the electronic and structural roles of Te have been actively discussed. Nevertheless, the specific influence of Te on SOM operation has not yet been fully clarified. Although Te has been examined in relation to threshold formation, crystallization behavior, and leakage characteristics in OTS devices, its role in SOM-specific operational metrics – such as polarity-dependent dual-threshold behavior, memory margin, fast pulse programmability, and long-term reliability – remains comparatively less explored. Previous SOM studies have often employed Te-containing chalcogenides as practical platforms, while direct attempts to isolate the elemental contribution of Te under otherwise identical device conditions have been relatively limited, leaving the relationship between bonding configuration, trap energetics, and SOM switching behavior to be investigated further.

In addition, when considering the feasibility of chip-level integration, Te-based chalcogenides – widely adopted in prior SOM studies – have been reported to exhibit several practical limitations. Their low crystallization temperature (~210–260 °C) compromises thermal stability and poses challenges for compatibility with BEOL metallization processes.[21,25,26] Furthermore, numerous studies have indicated that Te-containing materials tend to show increased leakage currents.[8,27] These factors can complicate reliable operation in densely integrated memory arrays, particularly under prolonged electrical stress or elevated temperature conditions. To address both the remaining mechanistic questions and the integration-related concerns, we adopt a paired-material design in which a Te-containing GeSbSeTe (GSST) device and a Te-free GeSbSe (GSS) SOM device are fabricated with the same device architecture and operating scheme. This strategy enables a more direct assessment of how Te incorporation correlates with bonding configuration, trap energetics, and electrical switching behavior. Building upon this framework, we further explore a Te-free SOM platform based on the GSS material system to pursue improved operational stability and BEOL compatibility. The Ge–Sb–Se ternary system leverages the complementary properties of its constituent elements. Germanium (Ge) forms strong covalent bonds that enhance network rigidity and thermal stability.[28–30] Selenium (Se) suppresses off-state leakage current and improves field responsiveness.[31] Antimony (Sb) stabilizes the amorphous structure at elevated temperatures and modulates TS behavior.[32] Importantly, the proposed design avoids the use of toxic arsenic (As), commonly employed in conventional SOM thin films, thereby contributing to safer and more sustainable materials engineering.

To further improve SOM stability, a carbon (C) interlayer was introduced between the top electrode (TE) and the active GSS layer, serving as a physical diffusion barrier to suppress interfacial resistance and atomic interdiffusion, while enhancing thermal stability.[33] As a result, the GSS-based system demonstrates a wide RWM of approximately 2 V, stable and repeatable switching at low write-pulse currents of ~10 μA, and ultrafast operation speeds of ~50 ns. These findings demonstrate the device-level feasibility of Te-free SOM devices under the evaluated operating conditions and suggest their potential compatibility with SCM architectures, enabling fast operation at low write-pulse currents. We anticipate that this approach will drive the expansion of next-generation memory technologies across a wide range of application domains.

2. Experimental section

2.1. Device fabrication

Two types of SOM devices were fabricated using a two-terminal structure on Si/SiO_2 substrates. The fabrication process was identical for both devices, except for the active layer composition. A 30 nm-thick tungsten (W) bottom electrode (BE) was deposited *via* physical vapor deposition (PVD) and patterned using standard photolithography and inductively coupled plasma reactive-ion etching (ICP-RIE). The etching process employed 4 sccm of Ar and 30 sccm of Cl_2 under a process pressure of 5 mTorr, with an etching rate of approximately 1 nm min^{-1}. Following BE formation, the chalcogenide layer was deposited by radio frequency (RF) co-sputtering. For the GSS SOM device, a GSS composite target and a separate Sb target were co-sputtered with RF powers of 35 W and 10 W, respectively. For the GSST SOM device, the same targets were used along with an additional co-sputtering with a Te target at 10 W RF power. All sputtering was conducted under a base pressure of 7×10^{-7} Torr and a working pressure of 3.3 mTorr, with an Ar flow rate of 20 sccm. To suppress interfacial diffusion between the chalcogenide layer and TE, a 15 nm-thick C barrier layer was deposited *via* direct current (DC) magnetron sputtering at 200 W, using 50 sccm of Ar gas. The base and working pressures were 8×10^{-7} Torr and 2.3 mTorr, respectively. A W TE layer (80 nm-thick) was subsequently deposited using DC magnetron sputtering (140 W, base pressure 9×10^{-7} Torr, working pressure 2.1 mTorr, Ar flow rate 15 sccm). The TE pattern was defined *via* photolithography followed by lift-off. The final stack structure for both devices was thus W/C/GSS (or GSST)/W/SiO_2/Si. In the split experiment examining the effect of the C layer position, as presented in Fig. S1, the fabrication process was identical to that described above, with the following exception for the C layer on the BE side: after depositing the W BE by PVD, the C layer was deposited under the previously mentioned process conditions before performing the ICP-RIE etching step. The etching time was then extended to ensure that the C layer was properly formed between the BE and the active layer.

2.2. Materials and characterization

High-resolution transmission electron microscopy (HR-TEM; JEM-ARM200F NEOARM, JEOL) was conducted to examine the cross-sectional morphology of the SOM devices, with sample preparation performed using focused ion beam milling (FIB; Crossbeam 350, ZEISS). Energy-dispersive spectroscopy (EDS) mapping was carried out during HR-TEM analysis to confirm the elemental distribution and verify the successful deposition of Ge, Sb, and Se in the GSS device and of Ge, Sb, Se, and Te in the GSST device. Rutherford backscattering spectroscopy (RBS) was employed to quantify the atomic composition of each chalcogenide layer. X-ray photoelectron spectroscopy (XPS; Thermo K-Alpha) was used to investigate the chemical bonding states within the active layers, with particular focus on distinguishing homopolar and heteropolar bonds in both the GSS and GSST compositions. Ultraviolet photoelectron spectroscopy (UPS; NEXSA G2, Thermo Scientific) was utilized to determine the work function and valence band maximum (VBM) information for constructing energy band diagrams. Additionally, optical properties of the thin films were characterized using UV-vis-NIR spectroscopy (V-650, JASCO). Transmittance and reflectance spectra were analyzed to calculate the optical bandgap (E_g).

2.3. Electrical characterizations

DC current–voltage (I–V) measurement of the SOM devices was performed using an HP4155B semiconductor parameter analyzer in sweep mode to characterize the TS behavior. Electrical pulse

measurements were also carried out using an HP4155B, an arbitrary function generator (AFG, Agilent 81150A), an oscilloscope (OSC, MSOX3024T, Tektronix), and an RF electrical circuit switch box. In all pulse measurements conducted in this study, shown in Fig. S2, the write pulse scheme used a ±5 V amplitude, 50 ns pulse width, and rise/fall times of 6 ns/50 ns. For speed testing, the write pulse width varied from 50 ns to 1 μs. V_{th} drift was analyzed by varying time intervals (10^{-6} to 10^{2} s) between the write and read pulses. Endurance testing was conducted using repetitive write pulses at +5 V and −5 V, with periodic verification of V_{th} using read pulses. Temperature-dependent DC measurements were carried out using a hot stage equipped with a precision temperature controller. A complementary analysis was performed to verify Poole–Frenkel (PF) conduction by examining the electric-field dependence of current at different temperatures. DC *I–V* measurements for both the GSS and GSST SOM devices were obtained at 25, 45, 65, and 85 °C. For each temperature, the data were reformulated as ln(*J*/*E*) as the *y*-axis and $E^{1/2}$ as the *x*-axis, where *E* and *J* represent the applied electric field and current density, and linear fitting of these plots verified whether the devices operate based on the PF-type conduction mechanism. Furthermore, the correlation between ln(*J*/*E*) and 1/*T*, where *T* is the temperature, under a fixed applied voltage was used to extract the trap depth of the active layer.

3. Results and discussion

3.1. Fundamental characteristics of GSS and GSST SOM devices

In general, SOM devices adopt a two-terminal sandwich structure, in which the desired active layer is inserted between the TE and BE. During operation, write or read pulses are applied to the TE, while the BE is grounded. Fig. 1 presents the characteristics of the materials of the SOM devices based on GSS and GSST active layers. HR-TEM images reveal that both devices exhibit structurally well-defined stacks with comparable film thicknesses and interface configurations. A distinct 15 nm C interlayer is clearly visible between the TE and the chalcogenide layer in both the GSS and GSST samples. As reported in previous studies, a C interlayer can serve as a diffusion-blocking layer, preventing elemental migration from the active layer, and is typically placed between the TE and the active layer.[33] In this work, the same approach was applied to both the GSS and GSST devices. The experimental reason for depositing the C layer only between the TE and the active layer will be briefly explained after introducing a pulse measurement scheme. The active layers for both the GSS and GSST devices were uniformly deposited to a thickness of approximately 65 nm under identical fabrication conditions. The selected area diffraction patterns, shown as insets in Fig. 1(a) and (b), confirm that the chalcogenide layers in both devices are amorphous. Elemental mapping *via* EDS, conducted concurrently with HR-TEM and described in the lower insets of Fig. 1(a) and (b), further confirms the homogenous elemental distribution across the active layer.

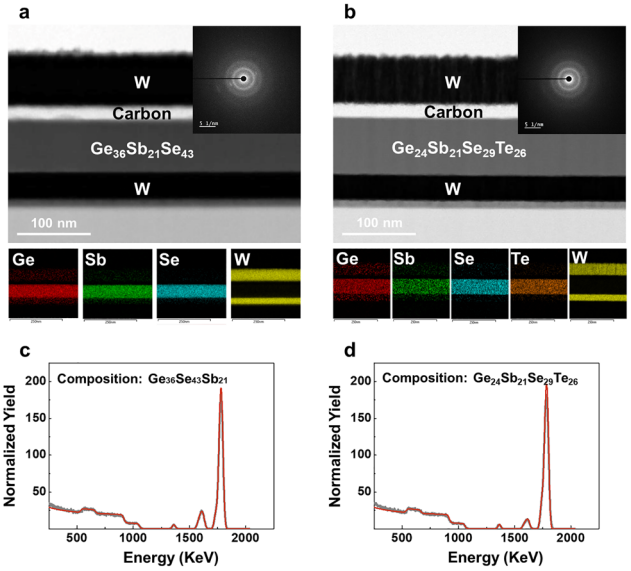

Fig. 1 Cross-sectional HR-TEM image of (a) the GSS and (b) GSST SOM devices. A symmetric structure with an approximately 65 nm GSS or GSST layer with a C interlayer were stacked between the W BE and TE. The insets represent the FFT images, confirming the amorphous nature of the GSS and GSST layers. The lower insets show the EDS results for both GSS and GSST, confirming that each element is well-deposited in the active layer without serious diffusion due to the 15 nm thickness of the C layer. (c) RBS results of the GSS thin film indicating a film density of 2.00 × 10^{17} atoms per cm^2 and an elemental composition ratio of Ge : Sb : Se = 85 : 50 : 100. (d) RBS results of the GSST thin film indicating a film density of 1.60 × 10^{17} atoms per cm^2 and an elemental composition ratio of Ge : Sb : Se : Te = 40 : 35 : 50 : 45.

RBS analysis, shown in Fig. 1(c) and (d), was employed to determine the quantitative elemental composition of the active layers. Prior to discussing the RBS results, it should be emphasized that the RF powers for all constituent materials except the Te target, were kept identical during co-sputtering for both the GSS and GSST devices to match the thickness of the active layers between the two devices. The deposition times were then adjusted differently for GSS and GSST so that the active layer thickness was set to 65 nm in both cases, as confirmed by the HR-TEM images presented earlier. For the GSS device, as shown in Fig. 1(c), the measured atomic ratios of Ge : Sb : Se = 85 : 50 : 100 translate to an approximate composition of $Ge_{36}Sb_{21}Se_{43}$. For the GSST counterpart, as shown in Fig. 1(d), the elemental ratios of Ge : Sb : Se : Te = 40 : 35 : 50 : 45 yield a composition of $Ge_{24}Sb_{21}Se_{29}Te_{26}$. These results highlight that, aside from the addition of Te in GSST, the Ge and Se contents are reduced compared to GSS, while the Sb content is maintained.

To briefly describe the operation of the SOM device, it requires the presence of two distinct V_{th}, which depend on the polarity of the preceding write pulses. These different states serve as the basis of programming the SOM device by assigning them to logical "0" and "1" states, thereby enabling its operation as a memory device, as shown in Fig. 2(a) and (b). In this work, a lower V_{th} observed after the application of a positive write pulse is defined as V_{th1} (denoted by the blue line), whereas

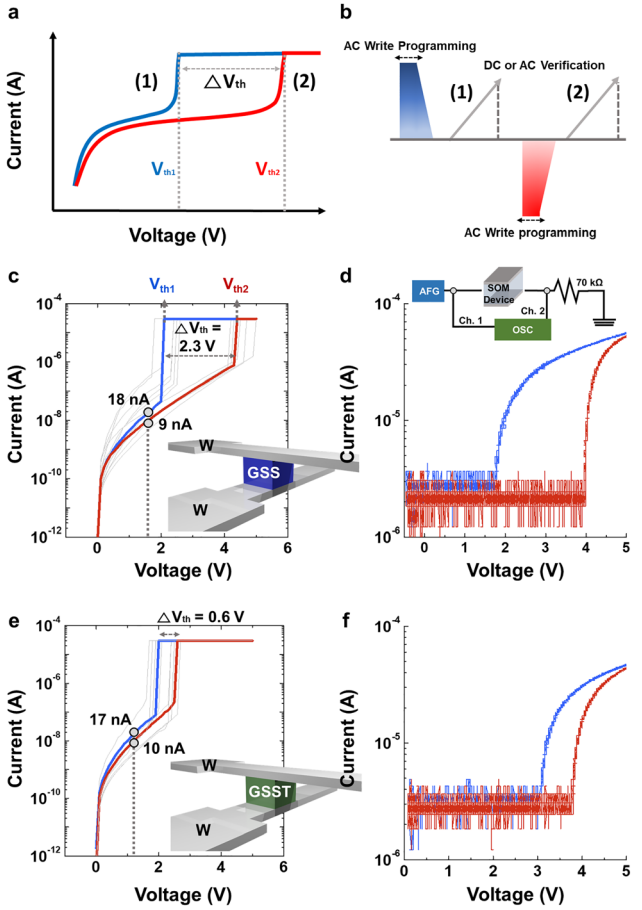

Fig. 2 Schematics of (a) the DC *I*–*V* graph of the working mechanism of the SOM devices and (b) the sequential pulse scheme of the write programming and read verification processes. V_{th} switching characteristics of (c) GSS and (e) GSST, and PIV measurement of (d) GSS and (f) GSST. The insets of (c) GSS and (e) GSST show the representative schemes for each SOM device. The inset of (d) represents the measurement circuit with an oscillator, pulse generator, and 70 kΩ external resistance.

a higher V_{th} obtained following a negative write pulse is defined as V_{th2} (denoted by the red line), as shown in Fig. 2(c). Before presenting the main results, it is necessary to outline the measurement schemes employed to distinguish and characterize these states. In contrast to nonvolatile memory devices, SOM displays a transient current response once the writing operation is completed. Therefore, the DC *I*–*V* method involves applying a write pulse of a given polarity to program the device into either the V_{th1} or V_{th2} state, followed by a continuous voltage sweep to detect the corresponding V_{th}. This approach provides a clear comparison between the two programmed states under static measurement conditions. During a DC *I*–*V* test, the applied voltage is maintained throughout the measurement, enabling real-time observation of the device's current behavior. Nevertheless, this method is not well-suited for assessing the electrical reliability characteristics that rely on electrical pulse operation. For this reason, the pulsed *I*–*V* (PIV) measurement was employed by applying the same write pulses used in the DC *I*–*V* method, while the read operation was performed with a pulse instead of a DC sweep. The PIV technique was utilized to evaluate the TS characteristics under dynamic read conditions. The measurement circuit, illustrated in the inset of Fig. 2(d), consists of an AFG supplying the electrical pulses, the SOM device under test, a 70 kΩ external load resistor connected in series, and an OSC. The OSC, with high input impedance, simultaneously monitors the pulse generated by the AFG and the voltage drop across the load resistor through two separate channels, Ch. 1 and Ch. 2. When TS occurs, the voltage distribution between the SOM device and the load resistor changes abruptly; the monitored voltage across the load resistor is then converted to current by dividing it by the known resistance value. This configuration allows precise extraction of the transient current response during the switching event, complementing the information obtained from the DC *I*–*V* measurements.

Before discussing the DC *I*–*V* and PIV results in detail, a brief overview of the split experiment conducted on the C layer deposition is presented. As mentioned earlier, the C interlayer was introduced with reference to previous studies to block factors that could impair device reliability, such as the diffusion of elements from the active layer.[33] For the purpose of preventing factors that can degrade device reliability, the experiment was conducted to determine the optimal position for placing the C interlayer, as shown in Fig. S1. Assuming the alternating positive and negative write pulses as one cycle, based on the aforementioned write pulse conditions, 10^4 cycles of pulses are applied sequentially to each GSS SOM device. After that, the V_{th1} and V_{th2} states of each device were examined using PIV measurements to determine whether repeated electrical stimulation induced reliability degradation issues. As a result, the GSS device with the C layer deposited only between the TE and the active layer exhibited the most stable maintenance of both the V_{th1} and V_{th2} states, as well as sustained RWM. Therefore, as previously described, this study was conducted using GSS and GSST devices in which the C layer was placed exclusively between the TE and the active layer.

Fig. 2(c) and (e) show the DC *I*–*V* characteristics of the GSS and GSST SOM devices, respectively. The write pulse width was fixed at 50 ns with 6 ns rising and 50 ns falling times, followed by a DC read sweep up to 5 V. A compliance current of 30 μA was set to prevent irreversible damage during TS. To assess the V_{th} memory states of the SOM devices, the read voltage (V_{read}) was configured at the midpoint between V_{th1} and V_{th2}. The rationale for this way of setting V_{read} is as follows: when V_{read} is applied to the SOM device in the V_{th1} state, the V_{th} is lower than V_{read}, thereby inducing TS and detecting the V_{th1} state. Conversely, in the V_{th2} state, the V_{th} exceeds V_{read} and the V_{th2} is not observed. This configuration thus provides a clear voltage difference for distinguishing the V_{th1} and V_{th2} states.

As a result in GSS, V_{th1} and V_{th2} were observed at 2.1 V and 4.4 V, respectively, yielding a RWM of 2.3 V. In contrast, the GSST device exhibited V_{th1} and V_{th2} values of 2.0 V and 2.6 V, respectively, resulting in a significantly narrower RWM of 0.6 V. This suggests that Te incorporation substantially reduces the

distinctiveness of the switching states. Additionally, in SOM devices, the leakage current is a critical evaluation parameter, as it can act as a sneak current in the CA configuration, leading to significant operational errors. To mimic realistic CA operation scenarios, a 1/2 V_{read} scheme has been adopted for evaluating the leakage current at a voltage equal to half of V_{read}. For GSS, the leakage currents at 1/2 V_{read} were 18 nA and 9 nA for the V_{th1} and V_{th2} states, measured at around (2.1 + 4.4)/4 = 1.625 V. In the GSST device, the corresponding leakage currents were 17 nA and 10 nA, measured at around (2.0 + 2.6)/4 = 1.15 V. These findings indicate that, although both devices exhibit similar leakage currents in terms of the 1/2 V_{read} scheme, the RWM in GSS is notably larger. This is a favorable deviation from the typically inverse relationship between leakage current and RWM reported in prior studies, since the level of V_{th} tends to decrease as the leakage current increases.[20,21,34–36] The ability to maintain low leakage currents while achieving a broader RWM in the GSS device underscores the benefits of Te-free compositions for SOM applications. Further confirmation of the SOM behavior was obtained *via* PIV measurements using a triangular read pulse following the identical write pulse condition with DC *I–V* measurement. As shown in Fig. S2, the triangular read pulse had a width of 20 μs with a 6 V amplitude, a 16 μs rising time, and a 16 μs falling time. Fig. 2(d) and (f) show the PIV characteristics of the GSS and GSST SOM devices. The corresponding RWM values extracted from Fig. 2(d) and (f) were 2.1 V for GSS and 0.8 V for GSST, reinforcing the observations of the V_{th} switching characteristics from the DC *I–V* results. In addition, comprehensive statistical data further supporting the reliability of these results are provided in Fig. S3.

The DC *I–V* and PIV results collectively highlight that Te-free GSS devices not only preserve low leakage characteristics but also achieve significantly enhanced V_{th} modulation with a wider RWM compared to Te-containing GSST counterparts. Similar to previous studies on OTS and SOM devices, we propose that the variations in TS behavior induced by Te incorporation, as well as the separation between V_{th1} and V_{th2}, are associated with distinct electronic trap states in each device.[34,37]

3.2. Influence of Te insertion on the bonding network in amorphous GSS thin films

To analyze the DC *I–V* and PIV results of the GSS and GSST SOM devices presented earlier, this section investigates the conduction mechanisms governing each device. The PF mechanism describes electric-field-assisted emission of charge carriers from localized trap states within the E_g of a semiconductor or insulator. Such traps arise from structural defects, chemical inhomogeneities, or the incorporation of impurities, and can immobilize carriers until sufficient energy is supplied.[8,32,38,39] However, when a sufficient external electric field is applied, the potential barrier experienced by the trapped carriers is reduced through field-induced lowering, effectively decreasing the activation energy required for emission. As a result, carriers can be released with lower energy input, enhancing the current flow. Prior studies have reported that the conduction behavior of SOM devices is predominantly governed by trap-assisted transport mechanisms, particularly in chalcogenide-based systems.[37,40] In particular, the GSST composition has frequently been described as utilizing the PF current conduction mechanism.[34] Motivated by these findings, this work also applies PF analysis to both the GSS and GSST devices to examine whether both devices follow a trap-based PF conduction mechanism and how the trap depth levels may be correlated with the emergence of distinct V_{th} values during their SOM operation.

In this framework, the PF effect is inherently temperature dependent, which means the higher temperatures increase the thermal energy available to carriers, thereby amplifying the field-assisted emission process and accelerating charge transport.[37–39] This temperature-field interplay makes PF analysis a powerful diagnostic tool for identifying trap-controlled conduction in amorphous or defect-rich materials, such as the chalcogenide active layers used in SOM devices. The PF equation is described as an equation in eqn (1), where a constant C is the proportionality factor, ϕ is the trap depth, k_B is the Boltzmann constant, β is the PF constant, T is the temperature, and q is the carrier charge.[21]

$$\ln\left(\frac{J}{E}\right) = \ln C - \frac{q\phi - \beta\sqrt{E}}{k_B T} \quad (1)$$

The current density (J) exhibits a nonlinear dependence on the applied field, typically expressed as an exponential function of the square root of the electric field. This relationship and PF equation can subsequently be interpreted as an expression describing the correlation between $\ln(J/E)$ and $E^{1/2}$, as well as between $\ln(J/E)$ and $1/(k_BT)$, which are essential for verifying the consistency of the PF conduction mechanism and for analyzing the trap depth. Fig. 3(a), (c), (e) and (g) present the DC *I–V* characteristics measured at temperatures ranging from 25 °C to 85 °C in increments of 20 °C. The results reveal that the current increases with temperature, suggesting that the probability of carrier emission rises as thermal energy becomes greater. Fig. S4(a)–(d) shows the $\ln(J/E)$ *versus* $E^{1/2}$ plots for all states of the two devices, where a clear linear trend is observed in every case. The $\ln(J/E)$ *versus* $1/(k_BT)$ plots for each V_{th} state, shown in Fig. S4(e)–(h), also exhibit linearity, enabling a comparative analysis of the trap depth values. These findings provide strong evidence that the PF conduction mechanism is the dominant factor governing the electrical characteristics in the subthreshold region following the write pulse programming in the GSS and GSST SOM devices.

After verifying the consistency of the PF conduction mechanism, the trap depths corresponding to each V_{th} state of the GSS and GSST SOM devices were examined. Fig. 3(b), (d), (f) and (h) depict the relationship between $E^{1/2}$ and the reduced trap depth (ϕ_r). The term reduced trap depth refers to the degree to which the trap potential barrier decreases under an applied electric field and was quantified through analysis of the logarithmic dependence on the reciprocal electric field.[21] For both the V_{th1} and V_{th2} states in the GSS and GSST SOM devices, the

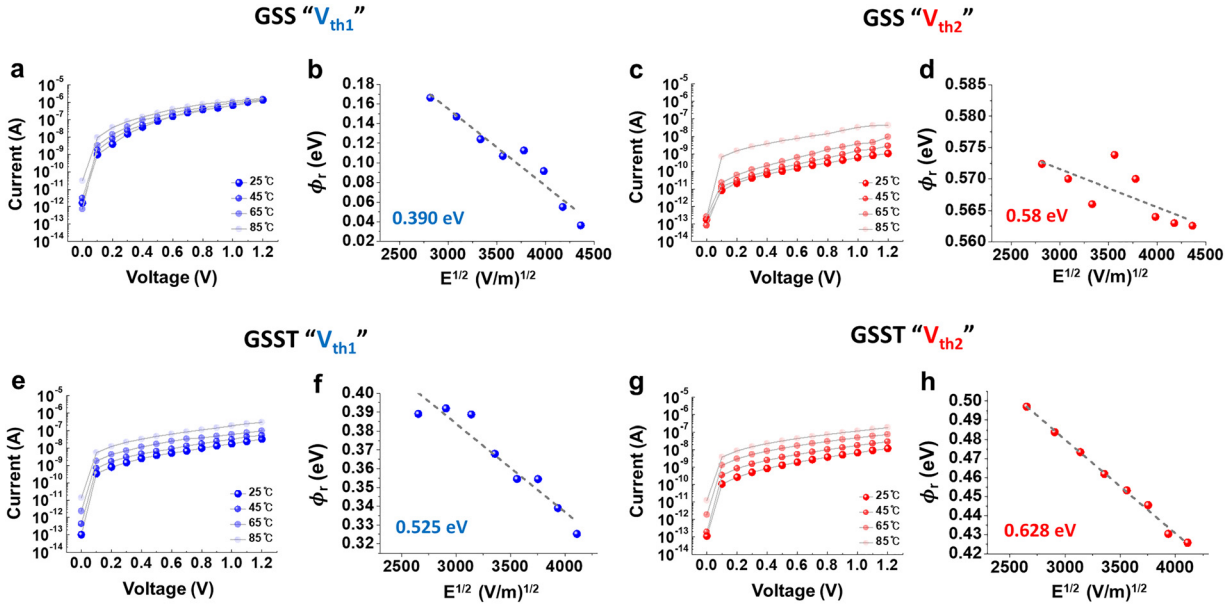

Fig. 3 Temperature-dependent DC I–V plots and plots of the relationship between ϕ_r and $E^{1/2}$ for (a) and (b) the V_{th1} state and (c) and (d) the V_{th2} state of the GSS SOM device, while (e) and (f) represent the same plots of the V_{th1} state and (g) and (h) the V_{th2} state of the GSST SOM device. The DC I–V plots were obtained at various temperatures of 25, 45, 65, and 85 °C. The plots representing the relationship between ϕ_r and $E^{1/2}$ give the trap depth, the value when there is no electric field applied on SOM devices, from a linear fit of the ϕ_r *versus* $E^{1/2}$ plot.

evaluation was carried out in the vicinity of each V_{th}, followed by the extraction of the slopes from the fitted linear trends. This procedure yielded the electron trap depths associated with each V_{th} state, revealing a proportional decrease in ϕ_r with increasing electric field. The zero-field trap depths were finally obtained from the corresponding y-intercepts of these linear fits.

As shown in Fig. 3(b) and (d), the electronic trap depths of the V_{th1} and V_{th2} states in the GSS device were determined to be 0.390 eV and 0.580 eV, respectively. In contrast, the corresponding values for the GSST device were 0.525 eV and 0.628 eV, respectively, as shown in Fig. 3(f) and (h). Based on the energy band diagram depicted in Fig. S5, Fig. 4 provides a schematic representation of the trap depth values obtained from PF fitting for the V_{th1} and V_{th2} states of both the GSS and GSST devices, enabling a straightforward visual comparison of their respective trap energy levels. The definition of trap depth can be summarized as follows: the energy difference between the transport states, where electrons or carriers can move freely, and the localized trap states arising from defects or structural disorder. A smaller energy difference implies that carriers can be emitted more easily, whereas a larger difference indicates that carriers, once trapped, require higher energy to be thermally or field-assisted detrapped. Consequently, shallow traps generally allow carriers to be trapped and detrapped more readily, thereby contributing to carrier motion such as TS, while deep traps tend to hinder detrapping and act as obstacles to carrier transport.[41] From this perspective, it was observed that the trap depth corresponding to V_{th1}, where TS occurs in lower voltages, is shallower than that of V_{th2}, in which switching occurs at higher voltage in both the GSS and GSST devices.

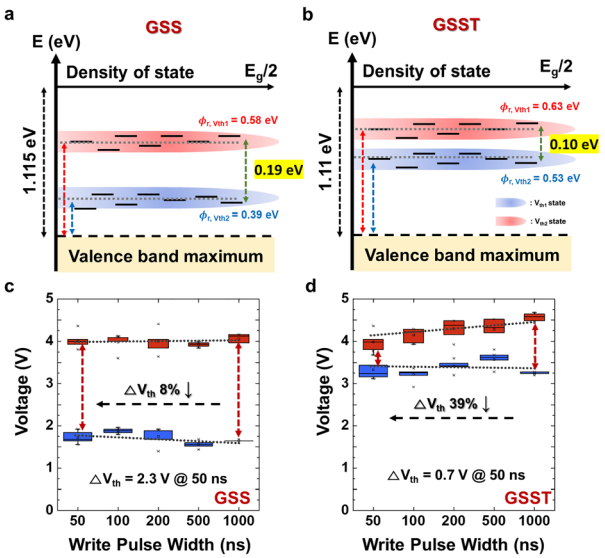

Fig. 4 Schematics of the trap depth states in (a) the GSS and (b) the GSST SOM devices. The trap depths of both the V_{th1} and V_{th2} states in GSS are lower than those in GSST. GSS demonstrates roughly twice the trap-depth variation of GSST, in accordance with its significantly larger RWM, indicating that enhanced trap-energy differentiation supports more distinct polarity-dependent switching. Speed characteristics of (c) the GSS and (d) the GSST SOM devices when the write pulse width was varied from 50 ns to 1 μs for both the V_{th1} and V_{th2} states.

This indicates that the trap states in the V_{th1} state are relatively shallower than those in the V_{th2} state, allowing electron trapping and detrapping to occur more readily, even at lower voltages. These findings corroborate the consistency between

the trap depths obtained from PF fitting and the experimental results from the DC *I–V* and PIV measurements. In addition, a notable observation is that the trap depth difference between the two V_{th} states is approximately 0.19 eV for GSS, whereas the difference is reduced to about 0.10 eV, nearly half, upon Te incorporation in GSST, as depicted in Fig. 4(a) and (b). This reduction indicates that the trap depth states defining V_{th1} and V_{th2} become more similar due to the Te addition. Such behavior aligns with the earlier DC *I–V* and PIV results, which revealed that Te incorporation significantly narrows the RWM and diminishes the distinction between the two threshold states. Therefore, assuming that all other variables are controlled except for the presence of Te, the PF fitting results and DC *I–V*, and PIV measurements provide strong evidence that Te incorporation reduces the trap depth difference between V_{th1} and V_{th2}, thereby lowering the memory RWM.

Additionally, many previous studies have analyzed the conduction mechanism of disordered selector materials using the thermally assisted hopping (TAH) model in conjunction with PF fitting.[34,37,42] In the TAH model, carriers move through a spatially distributed network of localized trap states. Under a sufficiently strong electric field, carriers acquire additional energy and can hop or tunnel to neighboring trap sites, resulting in an enhanced charge-transport rate and a nonlinear increase in current above the threshold. The transport current can be described by eqn (2),

$$I = 2qAN_t\frac{\Delta z}{\tau_0}\exp\left(\frac{E_c - E_F}{kT}\right)\sinh\left(\frac{qV_A\Delta z}{2kTd}\right) \quad (2)$$

where q is the electronic charge, A is the device area, N_t is the density of localized states, Δz denotes the average spacing between traps, τ_0 is the carrier escape time, E_c and E_F are the conduction-band edge and Fermi level, respectively, k is the Boltzmann constant, V_A is the applied voltage, and d is the film thickness.[43] This formula reflects the cooperative influence of thermal excitation and electric field on trap-mediated transport.

At a fixed bias condition, the temperature dependence of the current follows an Arrhenius-type behavior, described by eqn (3),

$$J = J_0\exp\left(-\frac{E_a}{kT}\right) \quad (3)$$

where J_0 is a prefactor, and E_a represents the activation energy for carrier emission from the trap states. Therefore, a linear relationship in a $\ln(J)$ and $1/kT$ plot indicates thermally activated hopping conduction through localized states.[43] Because PF conduction corresponds to field-assisted emission from traps, whereas TAH describes thermally activated hopping between traps, employing PF fitting together with Arrhenius/TAH analysis provides a reliable approach to determine whether transport is governed by trap-controlled electronic processes rather than purely ohmic or filamentary conduction.

For the GSS and GSST devices, Arrhenius analyses were performed separately for the V_{th1} and V_{th2} states. For the GSS device, the extracted activation energies were approximately 0.394 eV for V_{th1} and 0.537 eV for V_{th2}. For the GSST device, the corresponding values were 0.521 eV for V_{th1} and 0.617 eV for V_{th2}. The activation energies extracted from the temperature-dependent measurements showed close agreement with the trap depths obtained from PF fitting. This consistency between two independent analyses further supports that carrier transport in both threshold states is dominated by trap-assisted electronic conduction. Accordingly, the TS observed in the GSS and GSST SOM devices can be attributed to a trap-governed conduction mechanism. The detailed Arrhenius analysis is presented in Fig. S6. In addition, as shown in Fig. S7, we further examined the temperature dependence of the switching speed by measuring the transient current responses associated with TS at 25, 45, 65, and 85 °C. The results confirm that both the GSS and GSST devices exhibit delay times below 50 ns regardless of temperature, demonstrating temperature-independent fast switching behavior.

Based on the measurement method shown in Fig. S2(c), the speed measurement results of the GSS and GSST devices are summarized in Fig. 4(c) and (d). To clarify the use of the term ''speed measurement'' in this study, we define ''speed'' as the temporal parameter of the write pulse applied during device programming. A shorter write pulse duration allows evaluation of whether the device can still be programmed under such brief signals and whether it can distinctly separate the V_{th1} and V_{th2} states. Also, the short write pulse enables programming to be performed more efficiently in terms of both time and energy, which constitutes a substantial advantage for memory devices. Therefore, the ability of the SOM device to maintain reliable RWM operation even under such short write-pulse conditions is considered a major strength of the device. In our experiments, the pulse width of the write signal was progressively reduced, followed by read operations to assess the extent to which the GSS and GSST devices could sustain reliable RWM operation and maintain clear separation of V_{th1} and V_{th2} even under minimal programming times. Furthermore, PIV measurements were selected for this analysis to evaluate the speed measurement under electrical pulse operating conditions similar to those of actual memory devices.

The write pulse conditions are a fixed pulse amplitude of 5 V, rising time of 6 ns, and falling time of 50 ns. By decreasing the pulse width from 1 μs to 50 ns, each device's ability to sustain a distinguishable RWM under increasingly fast switching conditions was assessed. As depicted in Fig. 4(c), the GSS device shows an average RWM (10 cycles) of 2.5 V at a write pulse width of 1 μs, which decreased to 2.3 V at 50 ns, a reduction of roughly 8%. Conversely, for the GSST device, as shown in Fig. 4(d), the average RWM (10 cycles) was 1.15 V at 1 μs, which dropped to approximately 0.7 V at 50 ns, corresponding to a reduction of around 39%, particularly due to a significant drop in V_{th2} under negative write pulse conditions. This indicates that the RWM characteristics in the GSST device containing Te decrease sharply as the write pulse width is shortened to the 50 ns range, significantly reducing the device's ability as an SOM to distinguish between the V_{th1} and V_{th2} states.

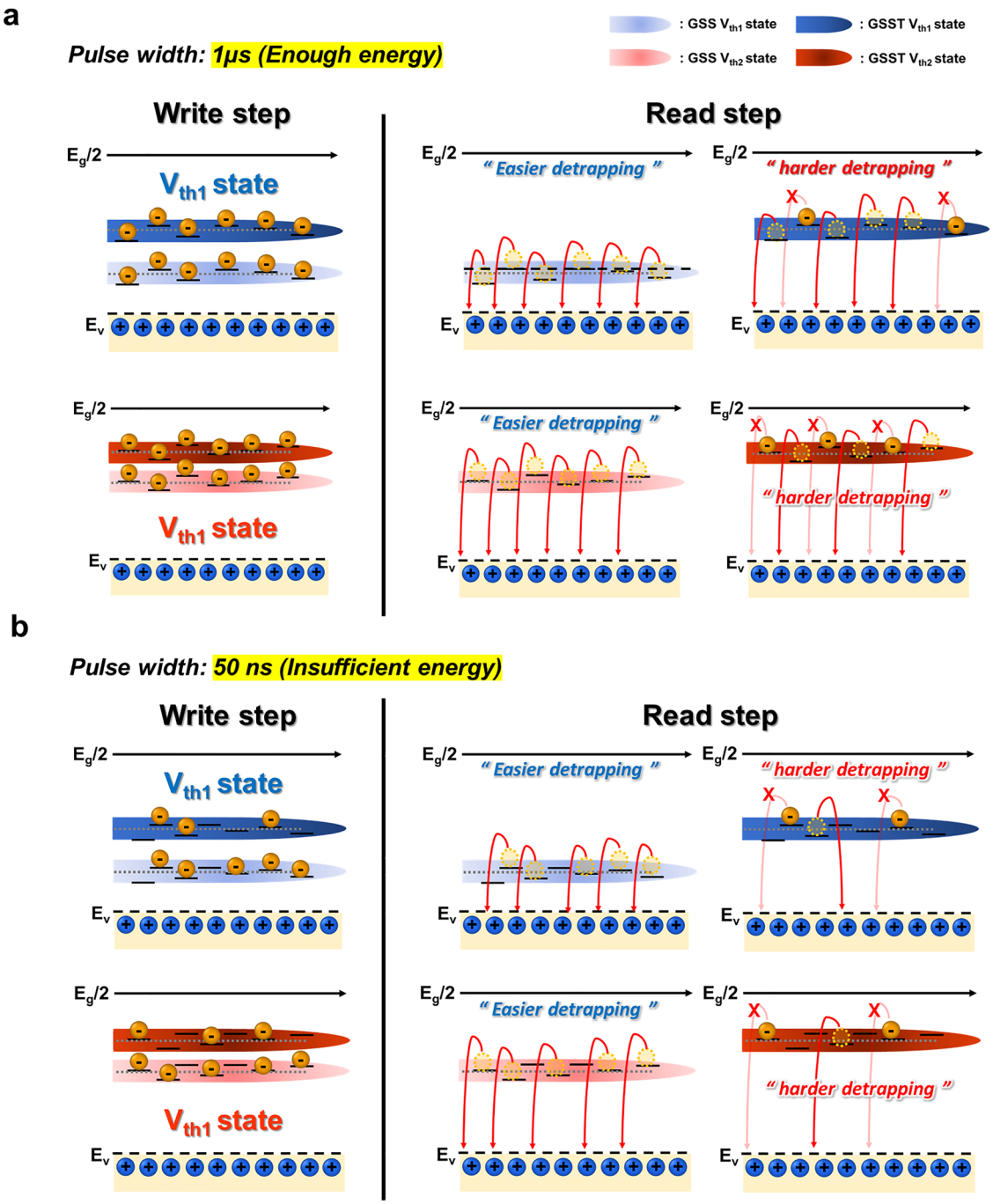

Fig. 5 Mechanistic schematics depicting the speed-dependent switching process for the GSS and GSST devices under (a) a 1 μs write pulse width, providing sufficient excitation energy for carrier trapping and detrapping in both devices, and (b) a 50 ns pulse, where the reduced energy is still adequate for enabling trap modulation in GSS but insufficient for GSST, thereby suppressing its TS response. In the GSST device, electrons experience relatively deeper trap states than in the GSS counterpart, such that even when transitioning from a 1 μs to a 50 ns write-pulse condition – thereby reducing the supplied electrical energy – the probability of carrier trapping or detrapping remains low. Consequently, GSST exhibits limited responsiveness to fast, low-energy pulses compared to the GSS device.

To contextualize the trap depth values extracted from the PF fitting and the experimentally observed speed characteristics, Fig. 5 provides schematic illustrations depicting the device's behavior under varying pulse width conditions. As shown in Fig. 5(a) and (b), the switching scenarios for the GSS and GSST devices are conceptualized for two representative write pulse widths: 1 μs, corresponding to a sufficiently high energy input that allows electrons to readily undergo trapping and detrapping events, and 50 ns, representing a significantly lower energy stimulus. These schematics qualitatively illustrate how the probability and ease of electron trapping and detrapping differ across the V_{th1} and V_{th2} states for each material system,

thereby aiding the interpretation of the observed programming and read behavior in both SOM devices. Based on the aforementioned definition and meaning of trap depth, the magnitude and variation of trap depth are critical factors in determining the formation of distinct trap states such as V_{th1} and V_{th2} in the SOM devices, and they strongly influence the rate at which carriers are released from traps. As depicted in Fig. 5, it is evident that both the V_{th1} and V_{th2} states in the GSS device exhibit relatively shallower trap depths compared with those in GSST, indicating that electrons trapped in these states in GSS can be detrapped more easily. This is consistent with the speed measurements, where the GSS device exhibited minimal variation relative to the GSST device in its V_{th1}, V_{th2}, and RWM values as the write pulse width decreased, indicating a strong tendency to preserve its threshold states. As the write pulse width is shortened, the reduced electrical energy inherently lowers the probability of electron trapping and detrapping events in both devices. Under such low-energy conditions (50 ns pulses), the separation between V_{th1} and V_{th2} becomes less pronounced for both systems, challenging reliable polarity-dependent switching. However, the impact is markedly different between the two materials. In GSS, the relatively shallow trap depths facilitate efficient trap and detrapping processes even under fast-pulse operation, allowing the device to retain a clear distinction between V_{th1} and V_{th2}. In contrast, Te incorporation in GSST deepens the trap-state energy levels and simultaneously narrows the trap-depth difference between V_{th1} and V_{th2} to roughly half that of GSS. As a result, the GSST device experiences a rapid loss of V_{th} separation as the programming energy decreases, making the two V_{th} states increasingly indistinguishable and degrading the RWM under short-pulse conditions. This behavior highlights the intrinsic difficulty of maintaining robust polarity-dependent switching in Te-containing systems under conditions where high-speed programming operation is required.

One significant thing to consider about speed measurement results is that a wide range of electronic devices, including SOM, utilize carrier trapping and detrapping as a fundamental transport mechanism. For example, both bistable resistive memories and OTS-based SOM devices involve defect-mediated carrier capture and release processes; however, the resulting switching event and electrical manifestation are fundamentally different. In bistable resistive random access memory (RRAM) devices, the SET operation fills relatively deep trap states, and these trapped charges remain stable until an external RESET bias is applied. The low-resistance state (LRS) is therefore maintained by the presence of filled deep traps, while carrier transport occurs through shallower traps *via* trap-assisted hopping conduction, commonly described by PF type transport.[44,45] Because carrier motion proceeds continuously through these localized states, the device current reflects a persistent conductive transport path and exhibits nonvolatile resistance behavior. In contrast, SOM devices exhibit OTS behavior. The write pulse does not directly create a conductive path but instead modifies the effective trap depth configuration within the amorphous chalcogenide film. When an external voltage is subsequently applied and reaches a critical V_{th}, strong electric field-induced band bending occurs, which dramatically increases carrier excitation from the trap states into the conduction band. This trap-to-conduction band transition produces the abrupt current increase characteristic of TS.[8] Therefore, unlike bistable RRAM, where trapping enables carrier hopping conduction, the conductive state in SOM originates from a field-induced electronic excitation process and cannot be sustained once the bias is removed. Furthermore, because the write polarity establishes different trap-depth configurations, the voltage required to trigger this excitation differs, leading to multiple distinguishable V_{th} (V_{th1} and V_{th2}). In this manner, SOM stores information not as a persistent low-resistance conduction state but as a programmed trap-depth condition that determines the external voltage necessary to induce TS.[34] Consequently, although both mechanisms involve carrier trapping and detrapping, bistable switching defines a stored resistance state, whereas SOM utilizes trap-depth modulation to control a field-driven threshold transition. From the perspective of carrier trapping/detrapping–based switching events, the write speed of SOM devices can be theoretically interpreted as being closely governed by the trap-depth configuration established during the write programming process.

Another noteworthy observation in the speed measurement results is that the V_{th2} value in the GSST device decreases much more sharply as the write pulse width is reduced, compared to the corresponding change observed for the V_{th2} state in the GSS device, which can be interpreted by its trap depth being approximately 0.048 eV deeper than that of GSS. As conceptually depicted in Fig. 5, when the write pulse width is reduced, thereby lowering the supplied energy, the deeper trap state of V_{th2} for GSST exhibits a far more pronounced reduction in the probability of electron trapping or detrapping relative to that for GSS, resulting in the V_{th2} state rapidly converging toward the V_{th1} level and diminishing the distinguishability between the two threshold states. Therefore, Te incorporation results in deeper trap depths across all states, making SOM devices less responsive to short-pulse operation. Previous studies have also reported that increasing Te content tends to form deeper traps, supporting the assertion that Te-induced deep trap formation is a plausible cause of the reduced RWM and degraded speed performance observed here.[21,46] The next section will address the electrical reliability measurements and examine the structural and bonding changes induced by Te incorporation in the active layer to establish the causal relationship between these effects.

3.3. Experimental proof of the reliability of GSS and GSST SOM devices

To experimentally investigate the differences in electrical reliability characteristics depending on the presence or absence of Te, measurements for the electrical reliability of the GSS and GSST devices were conducted. V_{th} drift behavior was investigated to further assess the long-term stability of the switching characteristics. V_{th} drift, defined as the gradual change in V_{th} over time following a programming event, is a critical reliability metric in selector devices. It is known to reflect the structural

stabilization and charge redistribution processes that occur after the application of a write pulse, and excessive V_{th} drift can compromise readout accuracy and data retention in high-density memory arrays.[20,47] Fig. 6(a) and (b) show the V_{th} drift results for the GSS and GSST devices, based on the measurement scheme in Fig. S2(d). The pulse conditions used for both the write and read operations were identical to those employed in the previous PIV and speed measurements. The only difference in the measurement scheme was the time interval between the write and read pulses, which was varied from 1 μs to 100 s to monitor the evolution of the V_{th} drift characteristics over time. For the GSS device, the extracted drift rates were 31.0 mV dec^{-1} for V_{th1} and 36.3 mV dec^{-1} for V_{th2}, with variations (σ) of approximately 33 mV and 105 mV, respectively. In contrast, the GSST device exhibited elevated drift values of 37.2 mV dec^{-1} (σ = 33 mV) for V_{th1} and 60.4 mV dec^{-1} (σ = 114 mV) for V_{th2}, indicating a pronounced degradation in drift stability due to the insertion of Te.

To assess long-term operational reliability, endurance measurements were also conducted. Endurance characterizes the device's tolerance to repeated switching cycles. It was evaluated using write and read pulse conditions identical to those employed in the previous reliability measurements. One cycle is defined as the application of both a positive and negative write pulse (Fig. S2(e)), and device endurance was evaluated by repeatedly applying multiple cycles. After multiple cycles, write pulses of both positive and negative polarities were applied, followed by corresponding read operations, to evaluate whether the device could sustain repeated pulse stress without degradation, while maintaining proper write and read functionality. As with the V_{th} drift measurements, the pulse conditions and PIV measurement procedures were identical to those used in the previous experiments. As shown in Fig. 6(c), the GSS device sustained its TS behavior up to 10^6 cycles. In contrast, the GSST device, shown in Fig. 6(d), began to fail after 10^4 cycles, showing that the incorporation of Te experimentally resulted in degraded endurance characteristics. In addition, potential read-disturb behavior, which may be associated with endurance-related reliability issues, was also experimentally evaluated, as presented in Fig. S8.

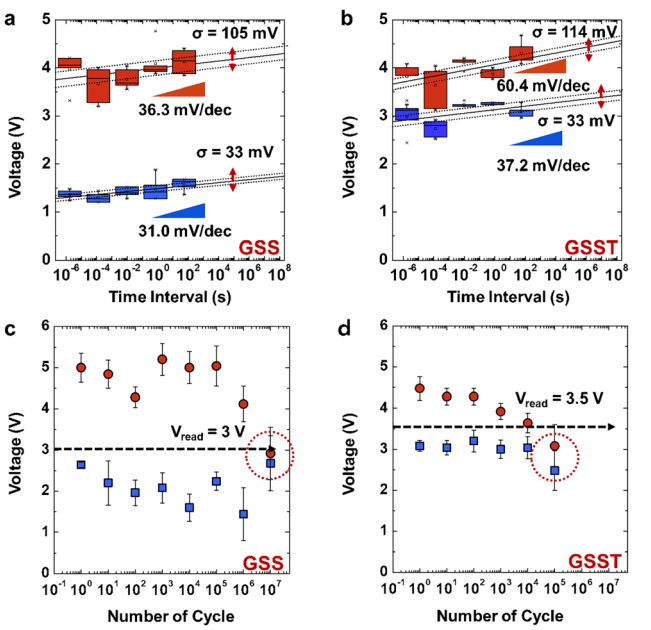

Fig. 6 V_{th} drift characteristics of the (a) GSS and (b) GSST SOM devices were evaluated at V_{th1} and V_{th2} over time intervals ranging from 10^{-6} to 10^2 seconds. Endurance characteristics shown in voltage-scale of (c) GSS and (d) GSST used to evaluate the V_{th1} and V_{th2} state separation as the number of write pulse cycles was increased, demonstrating that GSS endures more write pulse cycles than GSST in terms of V_{read}. V_{read} values are 3 V for the GSS SOM device and 3.5 V for the GSST SOM device.

To analyze the implications of Te incorporation on the amorphous chalcogenide film, considering the preceding electrical reliability results, we conducted a comparative XPS analysis of the GSS and GSST thin films, as shown in Fig. 7(a) and (b). The binding energy peaks were assigned to specific chemical bonds based on detailed deconvolution, with attention to the spin–orbit splitting of the $3d_{3/2}$ and $3d_{5/2}$ levels. In the GSS sample, the Ge 3d spectrum reveals a Ge–Se peak at 32.0 eV, and Ge–Ge peak at 30.2 eV.[48,49] The Se 3d region includes Se–Ge peaks at 54.4 eV ($3d_{3/2}$) and 53.5 eV ($3d_{5/2}$), Se–Sb peaks at 54.6 eV ($3d_{3/2}$) and 53.8 eV ($3d_{5/2}$), and Se–Se peaks at 54.8 eV ($3d_{3/2}$) and 54.0 eV ($3d_{5/2}$), indicating rich heteropolar bonding.[50–53] For Sb 3d, Sb–Se peaks are observed at 540.1 eV ($3d_{3/2}$) and 530.7 eV ($3d_{5/2}$), and Sb–Sb peaks at 538.1 eV ($3d_{3/2}$) and 528.8 eV ($3d_{5/2}$).[32,34,54]

Upon Te incorporation in GSST, notable spectral changes are observed. The Ge 3d spectrum exhibits a minimal shift in the Ge–Se peak to 31.9 eV and reduced intensity, suggesting a substantial decrease in the number of Ge–Se bonds. The Ge–Ge peak at 30.8 eV also diminishes, while a new peak for Ge–Te at 30.3 eV emerges, indicating the formation of Te-related bonds.[48,49] In the Se 3d region, Se–Ge peaks at 54.4 ($3d_{3/2}$) and 53.5 eV ($3d_{5/2}$), and Se–Se peaks at 54.7 ($3d_{3/2}$) and 53.9 eV ($3d_{5/2}$) show reduced intensities, reinforcing the suppression of the Se-centered heteropolar bonding.[50–53] Meanwhile, in the Sb 3d spectrum, the Sb–Se peaks at 540.5 ($3d_{3/2}$) and 531.5 eV ($3d_{5/2}$) show decreased intensities, while prominent new peaks at 530.4 eV ($3d_{3/2}$) and 528.9 eV ($3d_{5/2}$) corresponding to Sb–Te bonds appear.[32,34,54,55] Further confirmation comes from the Te 3d spectrum, which exclusively appears in GSST, with Sb–Te peaks at 584.3 eV ($3d_{3/2}$) and 573.5 eV ($3d_{5/2}$), Te–Te peaks at 583.2 eV ($3d_{3/2}$) and 572.8 eV ($3d_{5/2}$), and Ge–Te peaks at 582.5 eV ($3d_{3/2}$) and 572.2 eV ($3d_{5/2}$).[34,48,55] These peaks confirm the formation of multiple Te-related bonding configurations in GSST. To aid interpretation of the XPS data, schematic representations of both the GSS and GSST SOM devices are included in Fig. 7(c). The XPS spectra show that the GSST device demonstrates the emergence of Te-related bonds and a corresponding decrease in Ge-, Sb-, and Se-centered bonds relative to the GSS device. This suggests that, compared to the original GSS structure, a large portion of the Ge, Sb, and Se-based bonds were substituted by Te-centered bonds upon Te incorporation.

These XPS results and changes in bonding types are closely related to the information presented in Table S1. This table

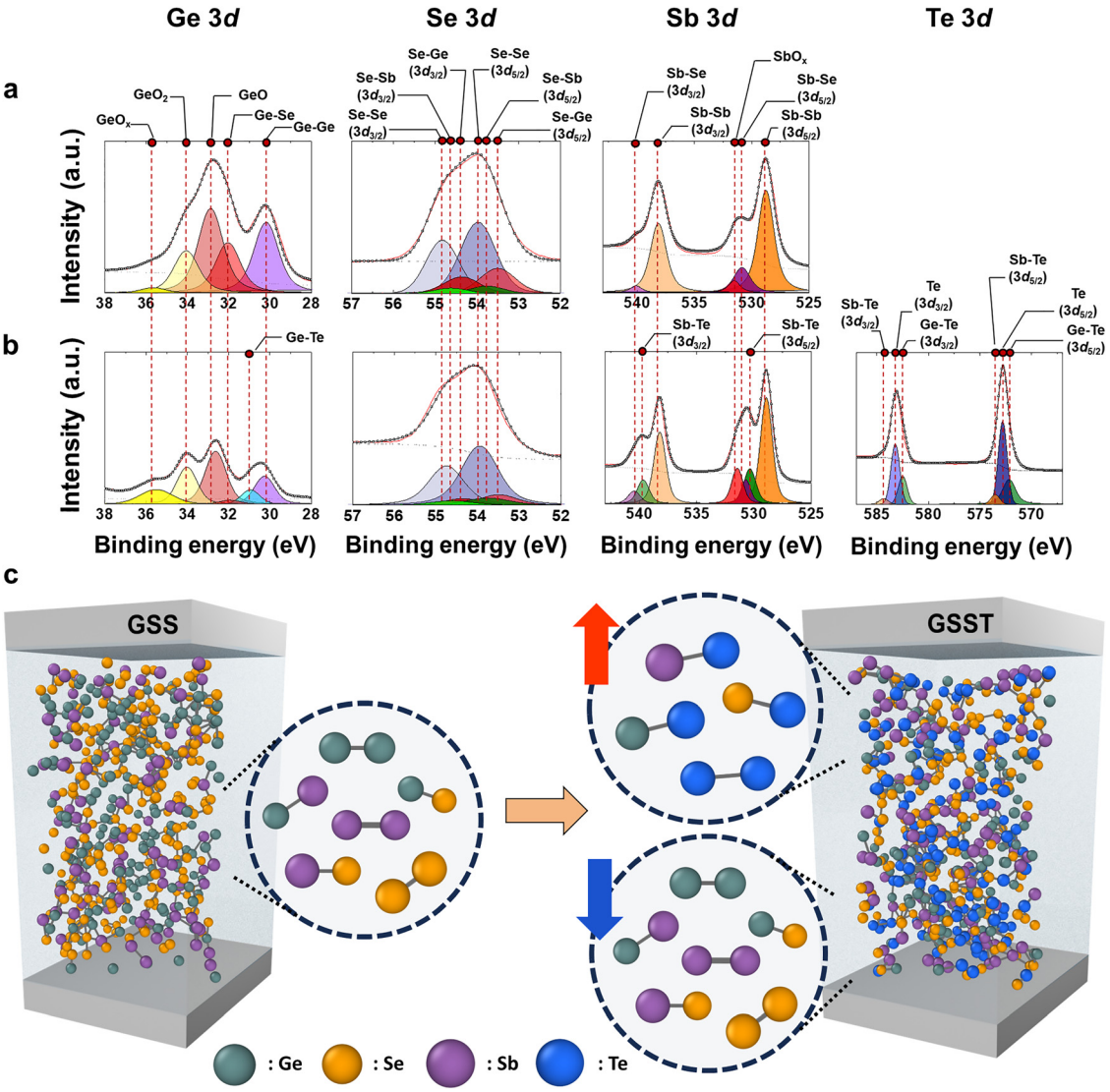

Fig. 7 Ge 3d, Se 3d and Sb 3d XPS spectra of (a) GSS and Ge 3d, Se 3d, Sb 3d and Te 3d XPS spectra of (b) GSST. (c) Schematic illustration of GSS and GSST SOM devices reflecting the XPS data.

systematically summarizes the bond energy (kcal mol^{-1}), bond length (Å), and electronegativity difference (Pauling scale) based on the electronegativities of each element (Ge (2.01), Se (2.55), Sb (2.05), and Te (2.1)) for both homopolar and heteropolar bonds between Ge, Sb, Se, and Te atoms, which are the principal constituents of both the GSS and GSST devices.[56–64] The data presented in the table highlight distinct differences in bonding characteristics between the Se-based and Te-based bonds. The heteropolar bonds involving Se – particularly the Ge–Se and Sb–Se bonds – demonstrate considerably stronger bonding interactions, with higher bond energies (*e.g.*, Ge–Se: 49.1 kcal mol^{-1}), shorter bond lengths (*e.g.*, Ge–Se: 2.37 Å), and greater electronegativity differences ($\Delta\chi \approx 0.5$), which together confer a highly polar and favorable character to these bonds. Such strong bonds can enhance structural stability even under external stress, thereby positively contributing to the electrical reliability of the device.[15,65] By contrast, Te-containing bonds, including Ge–Te and Te–Te, exhibit relatively lower bonding energies and longer bond lengths – for example, 35.5 kcal mol^{-1} and 2.64 Å for Ge–Te, and 33.0 kcal mol^{-1} and 2.76 Å for Te–Te. These values are indicative of structurally weaker and more spatially extended bonding interactions. Such weak bonds are more susceptible to structural disorder under external stress, which can adversely affect the electrical reliability of the device.

The increased presence of weak Te-related bonds is expected to contribute to variations in reliability characteristics, including V_{th} drift and endurance, as evidenced by the preceding measurements. Previous reports have identified such post-programming structural stabilization as a dominant source of V_{th} drift in amorphous chalcogenide-based selector devices, particularly when the bonding network lacks sufficient rigidity. The mechanism associated with structural stabilization in V_{th} drift is related to the thermodynamically driven transformation

of unstable bonds into more stable configurations as elapsed time increases, accompanied by an increase in the E_g and a reduction in the total energy of the chalcogenide thin film.[47,65] Accordingly, the increased V_{th} drift observed in GSST can be attributed to the presence of a larger proportion of weakly bound and structurally unstable Te-centered bonds, such as Ge–Te and Sb–Te. These bonds with relatively low bonding energy are more susceptible to rupture or reconfiguration during the structural stabilization phase following the write pulse excitation. In contrast, the Te-free GSS device, which is predominantly composed of stronger and more robust Ge–Se and Sb–Se bonds, resists such bond breakage and reformation, even under extended time intervals. Therefore, XPS analysis and V_{th} drift measurement revealed that GSST contained a higher proportion of weak and unstable Te-related bonds compared to GSS, which indicates a greater number of bonds prone to structural rearrangement over time, thereby accelerating rapid bond reconfiguration and leading to degradation in the V_{th} drift characteristic.

4. Conclusions

In this study, the electrical characteristics and underlying mechanisms of GSS and GSST SOM devices were comparatively analyzed. The results demonstrate that both the difference and the absolute magnitude of trap depths in the V_{th1} and V_{th2} states are closely related to the RWM and the write pulse operation speed of the SOM devices. Experimental observations revealed that the introduction of Te significantly reduced the trap depth difference between the two states while also deepening the trap levels. These changes were found to negatively impact RWM and degrade the speed of write pulse operations. Furthermore, from a bonding perspective, the incorporation of Te increased the number of structurally weak bonds, which in turn contributed to the deterioration of electrical reliability parameters such as V_{th} drift and endurance.

Such degradation in electrical performance and reliability caused by Te may limit device-level characteristics relevant to advanced memory architectures, including CA and CXL-type systems. As summarized in Table S2, a comparative analysis of key electrical metrics – firing voltage (V_F), RWM, write operation speed, write pulse amplitude, write current, V_{th} drift, retention, and endurance – drawn from representative SOM studies is presented.[40,66–69] This comparative analysis highlights the advantages of the Te-free GSS SOM device. The GSS device exhibited an exceptionally wide RWM of 2.1 V, an ultrafast operation speed down to a 50 ns pulse width, and a remarkably low write current of 10 μA, demonstrating competitive performance compared to previously reported SOM devices under similar conditions. These attributes indicate the potential for fast operation, wide memory margins, and energy-efficient, low-power performance in SOM applications. Accordingly, we propose that research on Te-free SOM devices, particularly GSS, could provide valuable guidelines for future SOM development.

Author contributions

Inchan Oh: data curation, formal analysis, investigation, and writing – original draft. Won Hee Jeong: data curation, formal analysis, and investigation. Jaeho Jung: methodology. Min Kyu Yang: conceptualization and methodology. Gun Hwan Kim: conceptualization, funding acquisition, project administration, resources, supervision, and validation.

Conflicts of interest

The authors have no competing interests to declare that are relevant to the content of this article.

Data availability

The data supporting the findings of this study are available from the corresponding author (Gun Hwan Kim). Further experimental details and additional figures associated with the main text are presented in the supplementary information (SI). Supplementary information (SI) is available. See DOI: https://doi.org/10.1039/d6mh00158k.

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