Materials Advances

ROYAL SOCIETY OF CHEMISTRY

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Cite this: *Mater. Adv.*, 2026, 7, 3923

AI enabled lead-free halide perovskite memristor crossbar arrays for energy efficient in-memory computing

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Received 3rd August 2025,
Accepted 29th March 2026

DOI: 10.1039/d5ma00844a

rsc.li/materials-advances

The rapid growth of edge computing is progressively requiring memories that provide rapid access, low energy consumption, and smooth integration with adaptable thin-film electronics. Halide perovskites meet these requirements because ion migration in their soft lattice enables field-tunable conductance. Importantly, this mechanism operates without conventional charge storage. The focus of research has thus transitioned to benign, lead-free compositions that inhibit parasitic ion drift, extend data retention, and enhance moisture tolerance. This review examines the latest developments in halide perovskite crossbar arrays. Uniform polycrystalline layers created *via* solution or vacuum methods demonstrate wide resistance ranges, remarkably low leakage, and consistent multilevel conductance throughout prolonged cycling. Selector-integrated cells effectively reduce sneak paths, ensuring signal integrity throughout closely linked planar meshes and vertically arranged networks. Additionally, their inherent rectifying properties allow for completely passive nodes ideally suited for analog inference. The density, switching speed, and adaptive behavior already achieved confirm that lead-free halide perovskite memristors represent a promising platform for energy-efficient data storage and on-device intelligence.

1. Introduction

Cutting-edge data applications such as edge inference engines, autonomous vehicles, and wearable health monitors continue to elevate the standards for on-chip memory.[1–6] Every platform requires quick bit access, low energy loss, and effortless interaction with complementary electronics.[7–12] Thin-film photovoltaic cells, light-emitting diodes, thin-film transistors, chemical sensors, and, notably, resistive switching memories can meet specific criteria.[13–22] Among various non-volatile approaches, conductance-tunable cells retain information without depending on charge accumulation.[23–28] Halide perovskites are particularly notable in this context because their soft lattice structures facilitate ion migration under moderate electric fields.[29–32] Initial investigations focused on lead-based perovskites.[33–37] However, environmental regulations and health issues restrict the commercial potential of Pb chemistry. Studies have consequently shifted focus to lead-free formulations that incorporate copper, bismuth, tin, antimony, or silver while maintaining the perovskite structure. The selection of B-site cations in these lead-free compositions directly impacts defect formation energy and ion migration pathways, thereby influencing the switching voltage, resistance window, and stability of individual memristive devices. Thus, the unintentional drift of ions is reduced, thereby enhancing endurance and extending data retention.[38] The mixed-cation approach adjusts the A-site ionic radius more precisely, which reduces lattice strain and improves moisture tolerance.[39] Crossbar arrays using these lead-free films exhibit distinct benefits.

Selector-free one-resistor nodes use inherent rectification to prevent half-selected leakage. In contrast, one-selector-one-resistor stacks integrate the perovskite layer with a threshold switch to significantly reduce sneak currents by multiple orders of magnitude. Sneak currents in crossbar arrays indicate the unintended leakage currents that pass through unselected neighboring cells, potentially distorting the readout signal and compromising memory reliability. A selector-free one-resistor (1R) node is a setup in which a single memristive element operates independently, using the material's inherent rectifying properties to reduce leakage paths without an extra selector device. Structures created using these methods provide uniformly distributed conductance states ideal for analog weight storage, pixel retention, and vector-matrix multiplication. The interaction between ions and electrons is analogous to synaptic plasticity, as demonstrated by spike-timing-dependent learning, which makes the material suitable for neuromorphic applications.

This paper examines the latest advancements in crossbar arrays using lead-free halide perovskite films as the active layer for resistive switching. Recent research on crossbar arrays

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based on Cu, Bi, Sn, and Ag as B-site components in halide perovskites has emphasized their stability, endurance, and low operating voltage. Array-level performance is closely tied to the underlying device physics, which include wide resistance windows, low leakage currents, and multilevel conductance suitable for in-memory computing. The discussion covers scalable fabrication compatible with standard silicon processing, as well as reliable data obtained under realistic environmental stress conditions. The results presented here will guide future developments toward high-density, energy-efficient, and non-volatile memories based on environmentally friendly materials.

2. Basic principles of crossbar arrays

Each array consists of four essential components: an activated word line, a fixed bit line, a nonlinear selector to suppress sneak currents, and a memristive switching element. At the intersection between a word line and a bit line, the selector (S) is integrated with the switching element (R), forming a fully functional 1S1R memory cell within the lattice architecture.[40,41] Programming initiates when a voltage pulse is sent along the designated word line to activate the targeted memory cell. When the applied bias exceeds the selector threshold, carriers move through the selected memristor, thus altering its conductance. The electrical properties of each memristor, such as the switching threshold, resistance ratio, and leakage current, play a crucial role in defining the reliability and scalability of the complete crossbar array. Unlike transistor-based memories, there is no need for a secondary gate; activating the relevant word and bit lines is sufficient to access any specific cell within the array. During readout, a differential voltage is produced by comparing the resistance of the selected memory cell to that of a reference device, thereby accurately determining the encoded logical state.

In practical circuits, perfect isolation is difficult to achieve. Unintended sneak paths can bypass the targeted junction and disrupt the addressing scheme.[42,43] Parallel metal traces create leakage paths extending across inactive regions that remain connected to the same lines as the addressed node. These unintended pathways introduce additional bias at the selected cross-point and form unpredictable shunts through neighboring inactive cells. This diverted current interferes with the passive behavior of the crossbar, modifying the effective voltage delivered to the resistive divider network.

However, the advantages memristors provide in terms of speed and energy efficiency continue to drive efforts to develop innovative strategies for minimizing unintended leakage paths. In situations where non-volatile bits are arranged in densely packed planar lattices or integrated vertically into 3D stacks, each device maintains a clearly defined conductance value exactly at its designated operating condition level.[44,45] A common approach involves adjusting the width, length, or composition of the localized conductive filament. An alternative method is to modify the electron tunneling gap, enabling incremental changes in overall conductance. The tunneling current exhibits an exponential relationship with the gap dimension, frequently resulting in distinctly nonlinear current–voltage (*I–V*) characteristics in practical applications.[46,47] Customizing the composition within the conductive path is another approach that is considered promising for achieving durability.

In three-terminal ionic architectures, the ability to regulate doping distributions through gate control allows for real-time adjustments of channel conductance during successive program/erase cycles, ensuring that both reliability and efficiency are maintained.[48–50] Ion migration that shapes filament geometry resembles biological learning processes. As a result, memristive devices can function as physical analogs of synapses in neural circuits. A significant number of memristive devices exhibit a characteristic where their conductance changes due to ion displacement, similar to the charge-transfer processes that promote adaptability in living neural tissue during the cycles of learning and memory formation. This biologically inspired strategy enhances the role of memristors within hardware neural networks. It is necessary to properly balance transistor-augmented crossbars with smaller, entirely passive meshes in order to realize these benefits. A dominant configuration connects each memristive element in series with a MOSFET, ensuring that large-scale arrays remain compatible with conventional processing methods.[51,52] This transistor effectively reduces stray currents in inactive cells, ensuring precise read and write functions are maintained. The gate provides an additional node, facilitating highly linear and symmetrical weight updates in a semi-parallel programming environment, significantly accelerating instruction cycles.

Recent investigations have focused on material platforms that maintain crossbar scalability while removing the toxicity associated with traditional lead-based compounds. Inorganic and double perovskites that are free of lead present inherent chemical stability, reduced ion migration, and suitability for low-power operation, making them attractive alternatives. The following section examines notable devices that utilize lead-free halide perovskite films in high-density crossbar arrays, demonstrating their reliable neuromorphic performance under ambient conditions. While these device demonstrations show the potential of crossbar integration, the varying testing conditions of many reported results complicate direct comparisons between materials. Consequently, comprehensive investigations of the material composition, defect chemistry, and array-level performance are still necessary to formulate definitive design guidelines for scalable perovskite memristor systems.

Kwak *et al.* presented highly stable, uniform, vertically stacked $CsCu_2I_3$ perovskite films, characterized by their non-toxic nature, serving as the active layer.[53] The evaluation of the device's analog and pulsed potentiation and depression behaviors was conducted under ambient conditions, with results confirming the remarkable structural integrity of $CsCu_2I_3$ after 160 days. The $CsCu_2I_3$ platform exhibited multiple conductance states as consecutive voltage spikes caused iodine vacancies. During prolonged pulse sequences, the devices demonstrated remarkable cyclability and extended endurance. Furthermore, they successfully emulated biologically plausible synaptic

phenomena, including paired-pulse facilitation (PPF) and spike-timing-dependent plasticity (STDP). To assess their viability for neuromorphic computing, these $CsCu_2I_3$ artificial synapses were subsequently simulated within a crossbar array architecture. During the MNIST training, the device-centered model achieved an accuracy of 95.2%, falling short of the theoretical optimum by only 0.3%. Meanwhile, fashion-MNIST reached an accuracy of 84.5%, just 1.7% below the ideal result. The neuromorphic responses arise from ion migration mediated by iodine vacancies in the $CsCu_2I_3$ lattice, demonstrating the influence of the material's intrinsic defect chemistry on the memristor's dynamic modulation of conductance.

Double perovskites may serve as viable alternatives to lead-free halide perovskites in crossbar array applications. Ye *et al.* reported two-terminal optoelectronic resistive random-access memory devices made from lead-free $Cs_2AgBiBr_6$ perovskite, exhibiting unique optoelectronic resistive characteristics that can be reset using UV illumination.[54] The lead-free $Cs_2AgBiBr_6$ memristor is arranged in an Ag/PMMA/$Cs_2AgBiBr_6$/ITO configuration. It exhibits a SET voltage of 1 V, an ON/OFF ratio of 10^3, and a data retention capability of 10^3 s. An experimental artificial self-storage visual architecture developed on this optoelectronic resistive memory demonstrates reinforcement learning and memory-decay traits similar to those of the human visual system, achieving integrated image-sensing and memory capabilities with an extended retention period (>6000 s). A 3×4 crossbar array has been constructed to verify neuromorphic pattern reinforcement. Theoretical analysis indicates that UV exposure eliminates Br defects and disrupts conductive filaments, thus elucidating the optical RESET effect. Furthermore, the integration with perovskite solar cells has enabled the implementation of a universally applicable optical logic gate.

Additionally, Lyu *et al.* presented resistive memory devices that employ environmentally friendly and air-stable lead-free double perovskite $Cs_2AgBiBr_6$ thin films, which were selectively adjusted by incorporating rare-earth La^{3+} dopants.[55] This study involved the synthesis of $Cs_2AgBiBr_6$ crystals and their corresponding thin films using both vacuum sublimation and solution-based processing techniques, incorporating varying concentrations of La^{3+} ions. X-ray diffraction analysis revealed that the La-doped $Cs_2AgBiBr_6$ demonstrated enhanced crystallinity. Elemental mapping *via* EDS demonstrated a uniform distribution of Ag, Br, La, Cs, and Bi throughout the doped perovskite films. A streamlined ITO/La-doped $Cs_2AgBiBr_6$/Ag structure was designed in a crossbar array that allows high-density integration with ease of operation. The engineered La-doped $Cs_2AgBiBr_6$-based memory devices exhibited clear write-once-read-many-times (WORM) characteristics, functioning at a low threshold voltage of 1 V and ensuring data retention for 12 000 s. The ON/OFF current ratio achieved an impressive value of 10^4, indicating a 100-fold improvement over the undoped $Cs_2AgBiBr_6$ devices. This innovative doping strategy presents a compelling opportunity to adjust material properties and improve device performance in lead-free, air-stable double perovskite systems.

3. Recent studies of lead-free halide perovskite-based crossbar arrays

This text provides an overview of recently documented cutting-edge demonstrations, focusing on material engineering, device architecture, and neuromorphic devices. Recent advancements have significantly broadened the performance capabilities of lead-free halide perovskite crossbar arrays. These studies demonstrate that environmentally friendly chemistries currently equal or exceed the performance of lead-based alternatives in terms of memory density and bio-inspired computing capabilities. Nevertheless, most reports focus on demonstrations of single devices or limited-scale arrays. A thorough understanding of how material composition affects switching uniformity, endurance, and array-level functionality is still developing.

Wang *et al.* reported the construction of a dynamic memristor utilizing lead-free copper-based perovskite, $CsCu_2I_3$, to develop a reservoir computing hardware system.[56] The thermal evaporation process for $CsCu_2I_3$ results in the fabrication of high-quality films that are dense, uniform, and stable. As shown in Fig. 1a, synapses function as essential connections within the biological nervous system, enabling the transmission of information between neurons. Upon neuronal excitation, neurotransmitters are released into the synaptic cleft, activating neighboring neurons and initiating the propagation of electrochemical signals. Fig. 1b illustrates the *I–V* response of the $CsCu_2I_3$ memristor following 20 cycles of positive ($0 \rightarrow +0.2 \rightarrow 0$ V) and negative ($0 \rightarrow -0.2 \rightarrow 0$ V) bias sweeps. The element displays distinct pinched hysteresis loops when subjected to bipolar periodic stimuli, which is a characteristic feature of analog memristive behavior. Fig. 1c illustrates the recorded current of the device across various pulse amplitudes (0.3, 0.6, 1.0, and 1.5 V), with the duration consistently maintained at 10 ms. With increasing amplitude, the current experiences a surge upon pulse delivery, followed by a rapid decay to its baseline once the excitation stops, reflecting the characteristics of short-term potentiation (STP). The shift from STP to LTP in perovskite memristors is closely linked to the timescale of ion migration and the intensity of the applied programming current. When low-amplitude or short-duration pulses are applied, ion migration is constrained, and the conductive filament partially relaxes following the stimulus, leading to volatile conductance changes typical of STP. Conversely, increased pulse amplitudes or elevated compliance current (CC) facilitate the accumulation of more mobile ions, thereby stabilizing the conductive channel and yielding enduring conductance states that align with LTP. As a result, the plasticity of perovskite memristors can be quantitatively adjusted by controlling the pulse width, pulse interval, and CC throughout the programming process.

The system consists of an input layer, a reservoir layer, and an output layer, as illustrated in Fig. 1d. The training complexity is reduced because only the linear readout layer requires adjustment, while the reservoir remains unchanged. To clarify operational details, the letter 'N' has been utilized as an illustrative sample, as shown in Fig. 1e. The input template utilizes a 5×5-pixel matrix, with each pixel being either active,

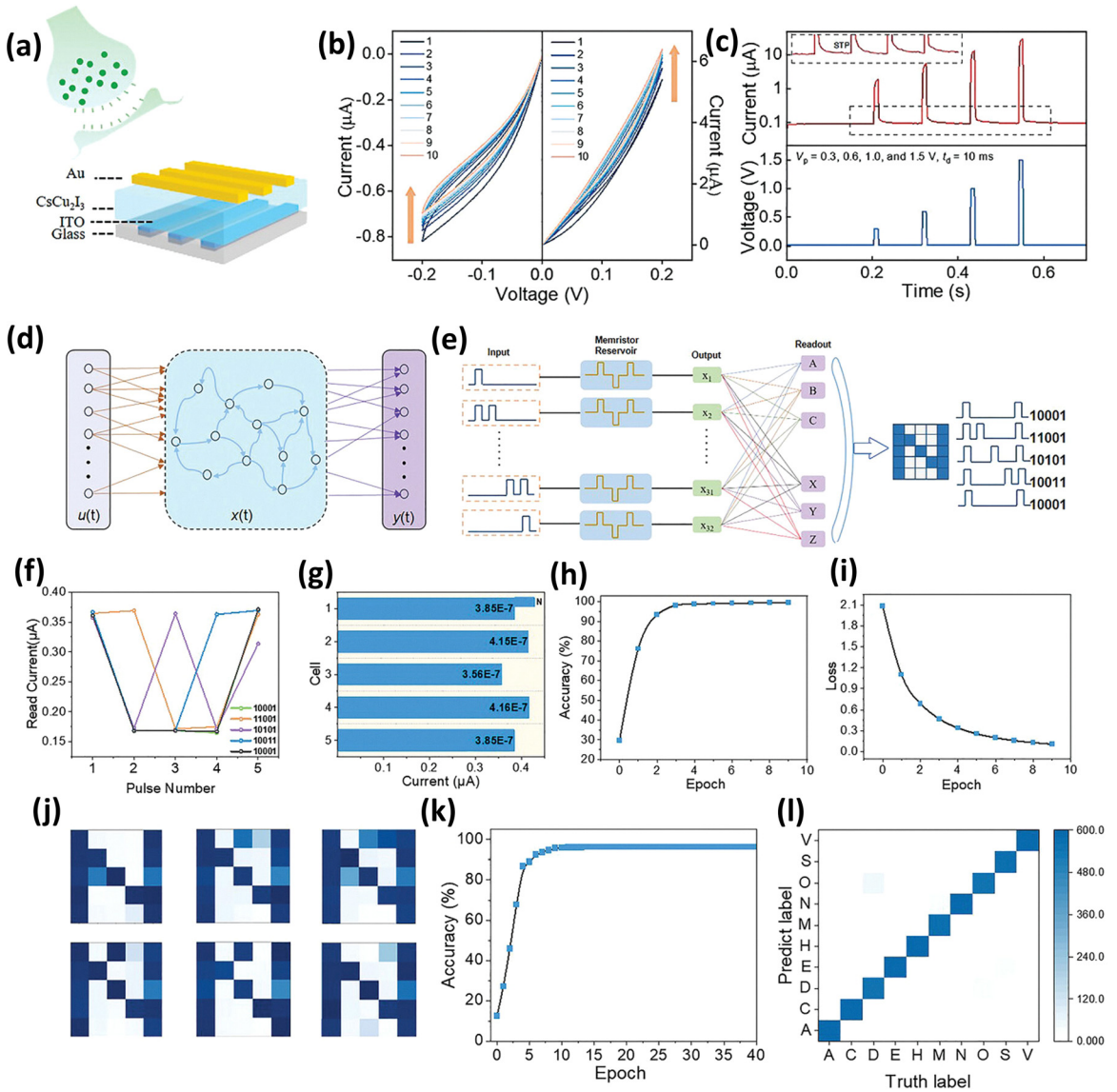

Fig. 1 (a) Diagram illustrating the electrical synapse alongside the memristor model derived from $CsCu_2I_3$. (b) *I*–*V* sweep characteristics of the $CsCu_2I_3$ memristor. (c) Varying amplitudes of electrical pulses influence the STP effect. (d) Schematic representation of the RC system, comprising three distinct layers. (e) A schematic illustration of the memristor-based RC system designed for letter recognition, exemplified by the digit "N." (f) Current responses of the device were recorded about five fundamental pulse trains. (g) Conclusively documented resistance states for the input character "N". (h) The accuracy of the letter recognition and (i) the RC system determines the associated loss function. (j) Noise introduced at various pixel locations within the image of the letter "N". (k) Recognition accuracy of the letter following the addition of noise. (l) The confusion matrix for the test images indicates that the majority of letters continue to be accurately classified. Reproduced with permission.[56] Copyright 2024, Wiley-VCH.

indicated by a pulse, or inactive, represented by the absence of a pulse. The binary matrix is transmitted to the reservoir filled with memristors, which dynamically alter their resistance states based on the sequence of pulses. Five pulse trains produce 32 permutations, allowing for the creation of various letter patterns. The responses of the device to the five fundamental pulse trains corresponding to the letter 'N' are recorded to evaluate behavior under various input conditions, as shown in Fig. 1f. A dataset comprising ten letters ('A', 'C', 'D', 'E', 'H', 'M', 'N', 'O', 'S', 'V') is utilized for recognition and forecasting, with the resistance states of the memristors associated with the letter 'N' illustrated in Fig. 1g. The resistance profiles provide insight into the internal processing and are instrumental in determining recognition precision. After the training phase, the reservoir computing system achieved a recognition accuracy of 98.2% across all samples, as demonstrated in Fig. 1h. Further assessment of the related loss function indicates a significant reduction in classification errors, as illustrated in Fig. 1i. The examination of system durability against noise involved the introduction of perturbations at different pixel locations within the input image of the letter 'N', as shown in Fig. 1j. Even with the introduction of noise, the recognition accuracy continues to be impressive at 96%, as demonstrated in Fig. 1k. Furthermore, the confusion matrix for test images with noise in Fig. 1l

indicates that most digits are still accurately recognized despite the distorted conditions, highlighting the robustness of the reservoir computing system.

The addition of Sn to the precursor solution enhances the formation energy of Sn vacancies, which effectively reduces the oxidation of Sn^{2+} by addressing vacancy-mediated pathways. Moreover, the presence of metallic Sn promotes a reaction between Sn^{2+} and Sn^{4+} during the oxidation procedure, which results in a reductive chemical environment. The reductive environment notably hinders the oxidation of Sn^{2+}, which plays a crucial role in enhancing the chemical stability of the perovskite material.

Kim *et al.* introduce a memory device that employs a Sn halide perovskite as the switching layer.[57] The constructed device featuring a Pt/formamidinium tin iodide ($FASnI_3$)/Ag configuration, illustrated in Fig. 2a, demonstrates reconfigurability by displaying both volatile and nonvolatile characteristics within a unified system, accomplished through the selective modulation of the primary switching mechanisms. The $FASnI_3$ thin film was derived from a precursor solution with a concentration of 1.2 M, comprising formamidinium iodide (FAI) and tin iodide (SnI_2), which were dissolved in a DMF/DMSO mixture at a volume ratio of 4 : 1. During the spin-casting process, chlorobenzene was used as the antisolvent. Furthermore, SnF_2 and metallic Sn were incorporated to reduce the oxidation of Sn^{2+}. Optical microscopy confirmed the presence of an 8 × 8 array of square devices, with each device spanning an area of 100 × 100 μm^2, as illustrated in Fig. 2b. The electrical characterization demonstrated non-volatile behavior driven by the reversible formation of metallic filaments within the Sn-halide perovskite. Upon applying a positive potential to the Ag electrode, the transition from the high-resistance state (HRS) to the low-resistance state (LRS) occurred at 0.41 V (SET). Reversing the polarity restored the device to the HRS at −0.57 V (RESET), as illustrated in Fig. 2c. A CC of 10 mA, applied solely during the SET transition, constrained filament growth, whereas the RESET operation occurred without current limitations to guarantee the complete rupture of the conductive path. The examination of reliability was conducted *via* endurance and retention trials. Fig. 2d and e demonstrate consistent

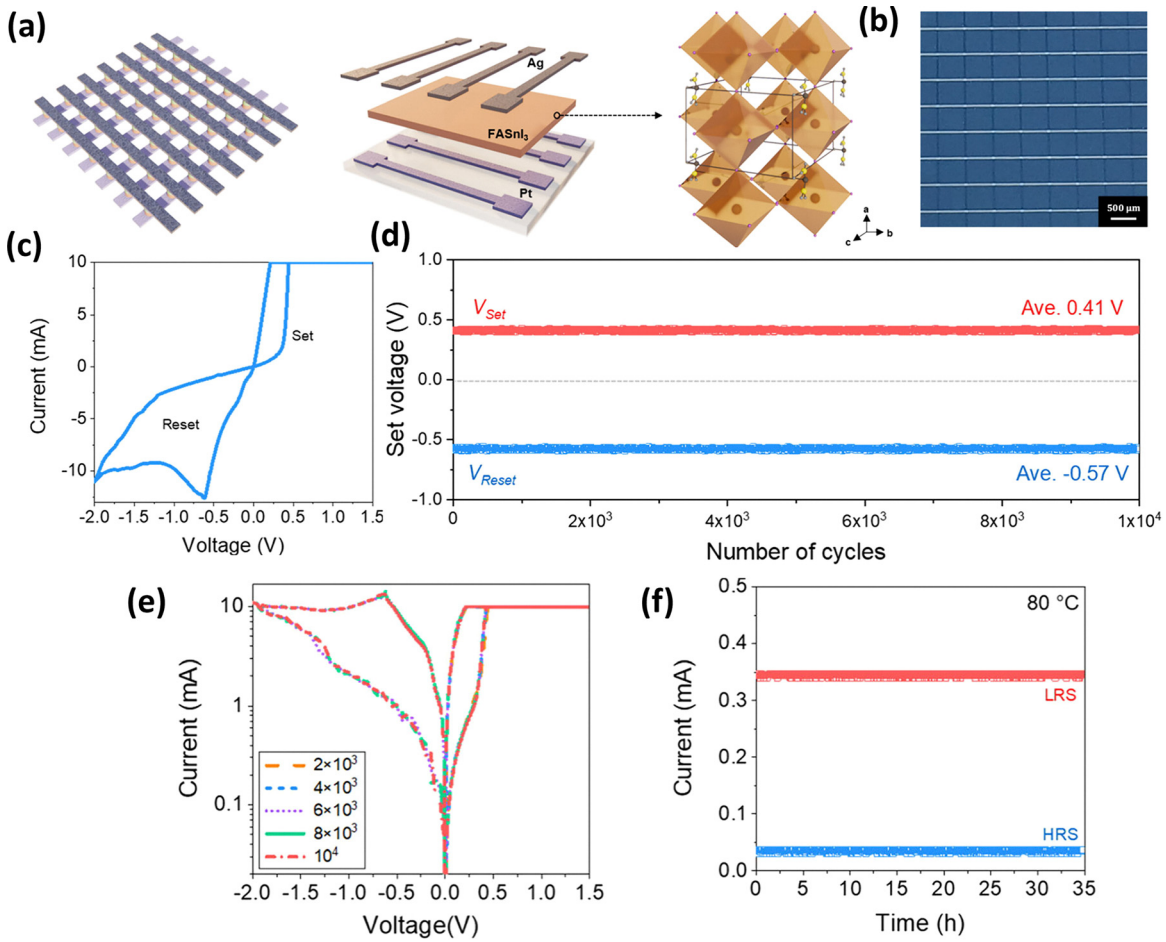

Fig. 2 (a) Schematic representations of the crossbar array (left), distinct layers of the reconfigurable memory device featuring a Pt/$FASnI_3$/Ag configuration (middle), and the crystal structure of $FASnI_3$ (right). (b) Optical microscope image showcasing 8 × 8 crossbar arrays, with each device measuring 100 × 100 μm^2. (c) Representative *I*–*V* characteristics with a positive voltage sweep applied to the Ag electrode. (d) Cycle-to-cycle variation. (e) *I*–*V* curves at 2 × 10^3, 4 × 10^3, 6 × 10^3, 8 × 10^3, and 10^4 cycles. (f) Retention time was assessed at 80 °C for both HRS and LRS with a read voltage of 0.01 V. Reproduced with permission.[57] Copyright 2025, American Chemical Society.

bipolar switching over 10^4 consecutive cycles measured in ambient air, underscoring remarkable repeatability. Furthermore, Fig. 2d illustrates thermal stability: both resistance states maintained distinctly separated conductance distributions for over 34 hours at 80 °C. The results validate long-lasting data retention and underscore the appropriateness of tin-halide perovskites for applications in non-volatile memory.

Bi^{3+}, characterized by its lone pair of $6s^2$ electrons, contributes to enhanced stability and facilitates the formation of low-dimensional perovskites that exhibit low leakage currents, a high ON/OFF ratio, and multilevel resistive states. Vishwanath *et al.* reported flexible lead-free $Cs_3Bi_2I_9$ 8 × 8 crossbar memristors.[58] Fig. 3a illustrates a flexible $Cs_3Bi_2I_9$ perovskite memristor constructed on transparent PET substrates. A straightforward yet reliable single-step spin-coating approach is used to realize an 8 × 8 Au/PMMA/$Cs_3Bi_2I_9$/PMMA/Au crossbar array. The diagram provided depicts around 250 nm of $Cs_3Bi_2I_9$ positioned between ultrathin PMMA layers, which are approximately 20 nm thick, and sputtered Au electrodes that measure about 50 nm. During a thorough *I–V* assessment of the 8 × 8 lead-free crossbar array, a regulated positive bias was applied to the upper Au electrode with a CC of 1 mA. In contrast, the lower Au electrode was securely grounded. The direct current (DC) cycling was systematically extended to 50 cycles, during which the device consistently exhibited characteristic bipolar resistive switching, achieving an impressive ON/OFF ratio that exceeded 10^6. The exceptional ratio is mainly due to the significantly reduced leakage current in the HRS of the $Cs_3Bi_2I_9$ element. This phenomenon can be linked to the restricted charge transport that takes place among the isolated $[Bi_2I_9]^{3+}$ octahedral structure. The reduced dimensionality of this crystal structure not only reduces leakage currents but also stabilizes filament formation, enabling reliable multilevel switching at the device level and enhancing signal integrity in crossbar arrays. All 50 DC sweeps consistently stayed within an HRS of approximately 0.13 nA and an LRS of about 0.6 mA at 0.08 V, clearly illustrating remarkable operational stability, as shown in Fig. 3b. The data retention exceeded 10^5 s for both LRS and HRS at a modest 0.05 V read voltage, showing no noticeable deterioration, as illustrated in Fig. 3c. Endurance testing extending to 10^4 cycles also maintained stable switching with an ON/OFF ratio significantly exceeding 10^4, as shown in Fig. 3d. In addition to its resistive properties, the device demonstrated dependable multilevel switching, which significantly enhanced memory density beyond two bits per element. The emergence of such multilevel behavior was consistently observed by modifying the current from 50 μA to 1 mA during the SET process, as demonstrated in Fig. 3e. The HRS was

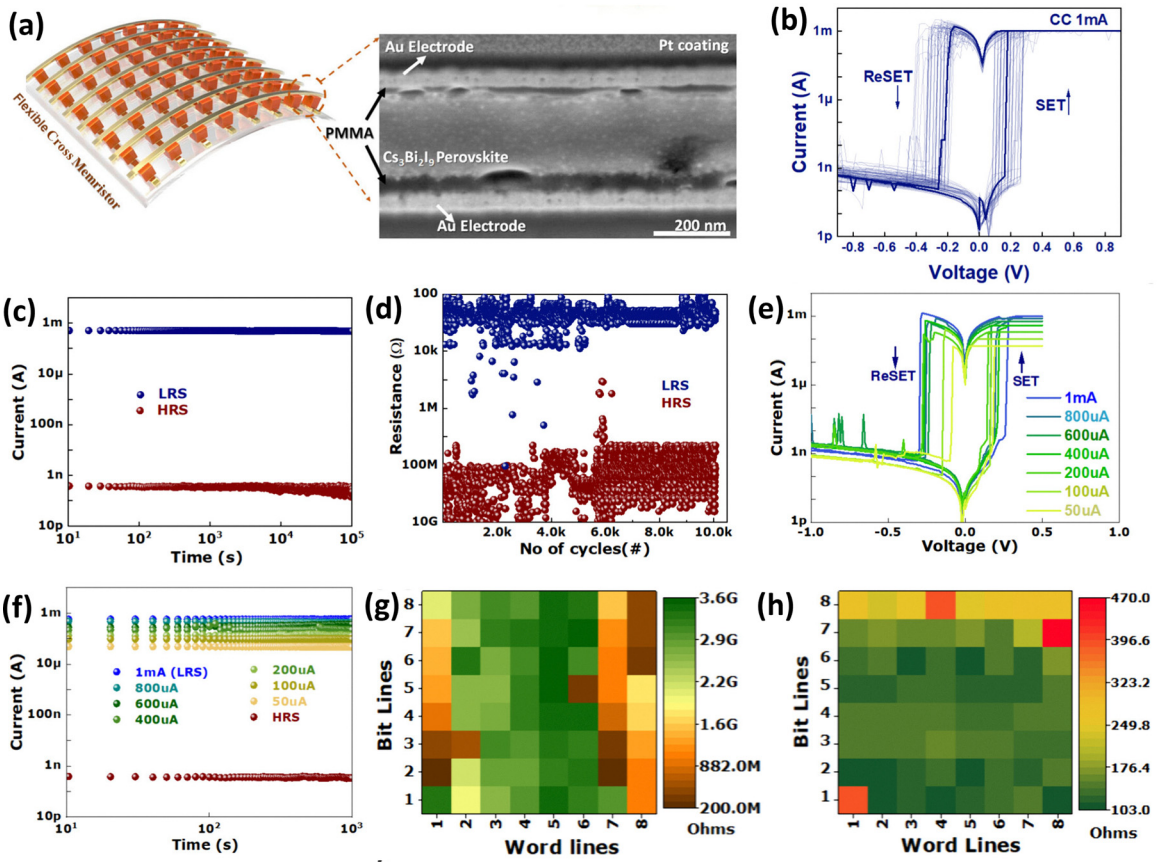

Fig. 3 (a) Diagram illustrating the flexible crossbar perovskite memristor with an SEM cross-section of the device. (b) 50 consecutive *I–V* characteristics were recorded. (c) Retention. (d) Endurance. (e) Multilevel resistive switching. (f) Multilevel retention analysis. The color map illustrates the resistance distribution of the 64 $Cs_3Bi_2I_9$ memristors in HRS (g) and LRS (h). Reproduced with permission.[58] Copyright 2025, American Chemical Society.

unaffected by CC, while seven distinct LRS values were accurately determined based on the selected CC. A lower CC (50 μA) resulted in a significant decrease in reset voltage and reset current compared to higher settings, likely due to the formation of a thinner conductive filament under the moderate SET condition. In total, eight resistance levels exhibiting retention beyond 10^3 s are clearly illustrated in Fig. 3f. Fig. 3g and h present color maps that illustrate the distributions of LRS and HRS across the 8 × 8 array, which consists of 64 individual cells. The challenge of reducing sneak-path leakage currents in passive memristor crossbar networks persists in the absence of an auxiliary switch matrix. The differences observed among the produced cells were minimal, and importantly, a significant portion (90%) demonstrated enhanced performance. The notable resistive switching characteristics of the $Cs_3Bi_2I_9$-based device makes it a strong candidate for non-volatile memory technology.

Li *et al.* presented a memristor constructed from vacancy-ordered double perovskite, specifically Cs_2TiBr_6 nanocrystals, that features rapid switching capabilities, achieving switching times in the tens of nanoseconds range.[59] The performance characteristics and conduction mechanism of the memristor were investigated using the Al/Cs_2TiBr_6/FTO architecture in Fig. 4a. Fig. 4b presents the resistive switching curves of the memristor, demonstrating standard bipolar switching between HRS and LRS, with an electrode area of approximately 50 × 50 μm^2. The study of programmable conductance levels utilized sequences of positive and negative pulses (±0.8 V, 200 ns) produced under controlled testing conditions, which led to successive potentiation and depression within the memristive synapse, as illustrated in Fig. 4c. The electronic synapses based on Cs_2TiBr_6 exhibit notable PPF characteristics when subjected to twin pulses with an amplitude of 0.8 V and a width of 200 ns, as illustrated in Fig. 4d, where the ratio decreases with extended intervals. Fig. 4e and f illustrate the observed alterations in synaptic weight (conductance change) in response to different programmed pulse stimuli across various conditions. The results demonstrate that their electronic synaptic devices successfully replicated the STDP learning rule.

An 8 × 8 memristive crossbar was constructed through high-precision fabrication and patterning processes to emulate image denoising and assess uniformity, as shown in Fig. 4g. Bit lines and word lines are linked to the STM32 microcontroller processing unit *via* two specific digital-to-analog converters (DACs) and two analog-to-digital converters (ADCs), as illustrated in Fig. 4h. Prior to the denoising process, the symmetric Gaussian filter was pre-configured on the crossbar. Following this, the STM32 delivered input pulses to the bit lines, with pulse amplitudes reflecting the pixel intensities in the noisy image in real time. The pixels of the filtered image were generated *via* the dot product of the 64D voltage vector (mapped from the 8 × 8 input sub-image) and the 64D conductance vector (stored within the 8 × 8 memristor array). The sub-image was scanned with a stride of one, resulting in filtered outputs measuring 8 × 8. The resulting current was concurrently gathered and analyzed as the pixel value in the denoised output. The Gaussian distribution employed in the denoising process is depicted in Fig. 4i and is distinctly observable. The evaluation of recognition accuracy was conducted utilizing the original, noisy, and denoised image datasets, as demonstrated in Fig. 4j–l. The denoised image achieved recognition accuracy of 92%, closely approaching the original image's accuracy of 94% and significantly exceeding the noisy version's 82%, emphasizing the effectiveness of the denoising process. The recognition confusion matrix, obtained from testing 173 images, is illustrated in Fig. 4m–o.

Additionally, Huang *et al.* investigated the inorganic double perovskite $Cs_2AgBiBr_6$, exploring its potential as an intermediate layer for the preparation of artificial synapses, using +40 V spikes to induce breakdown in the synapse.[60] Through this approach, the $Cs_2AgBiBr_6$ synapse can establish self-generated Ag^+ conductive channels. Applying a voltage allows for the adjustment of self-conducting Ag^+ conduction, thus enabling changes in the device's conductivity.

A continuous sequence of 12 triangular waveforms was established to evaluate the current characteristics of the inorganic double perovskite $Cs_2AgBiBr_6$ synaptic element depicted in Fig. 5a. From 0 to 25 s, a triangular voltage of +1 V was applied to the device, while from 25 to 50 s, a triangular voltage of −1 V was introduced to the same element. The synaptic conductance exhibited a gradual increase from 0 to 25 s, followed by a decline from 25 to 50 s. The maximum current obtained from each measurement shown in Fig. 5b was subsequently organized for further analysis. Cycles 1 through 6 showed a consistent increase in peak current, while cycles 7 through 12 demonstrated a declining trend. Additional evaluation used spike voltages of +2 V and −2 V, as illustrated in Fig. 5c. With stimulation at +2 V, conductance consistently increased, while stimulation at −2 V led to a continuous decrease, confirming the behaviors of potentiation and depression. The conductance states exhibited stability over spike sequences lasting more than 1000 s.

To evaluate the device's capacity for image learning and pattern storage, a 5 × 5 array of Au electrodes was deposited on the active surface (Fig. 5d). A 5 × 5 pixel pattern of the letter 'X' was then programmed into the array. The learning process unfolded in three distinct stages: the acquisition of short-term memory (STM), the consolidation of long-term memory (LTM), and the subsequent erasure of letters followed by a phase of relearning. Initially, the lack of spike excitation resulted in the device generating no electrical response, which manifested as red pixels, as illustrated in Fig. 5e. Following this, a single +2 V spike was applied to the electrodes corresponding to the letter X geometry, and the excitatory postsynaptic current for each measurement was recorded. The excitatory postsynaptic currents were organized in a matrix format according to the input sequence, enabling the extraction of the X image under +2 V stimulation. Following a duration of 15 minutes, the device was probed with a voltage reading of +0.5 V. At that moment, the pattern associated with the letter was undetectable, suggesting a lapse in memory within a 15-minute timeframe. The device was subsequently allowed to rest for thirty minutes to ensure full recovery, as illustrated in Fig. 5f. A sequence of ten or more

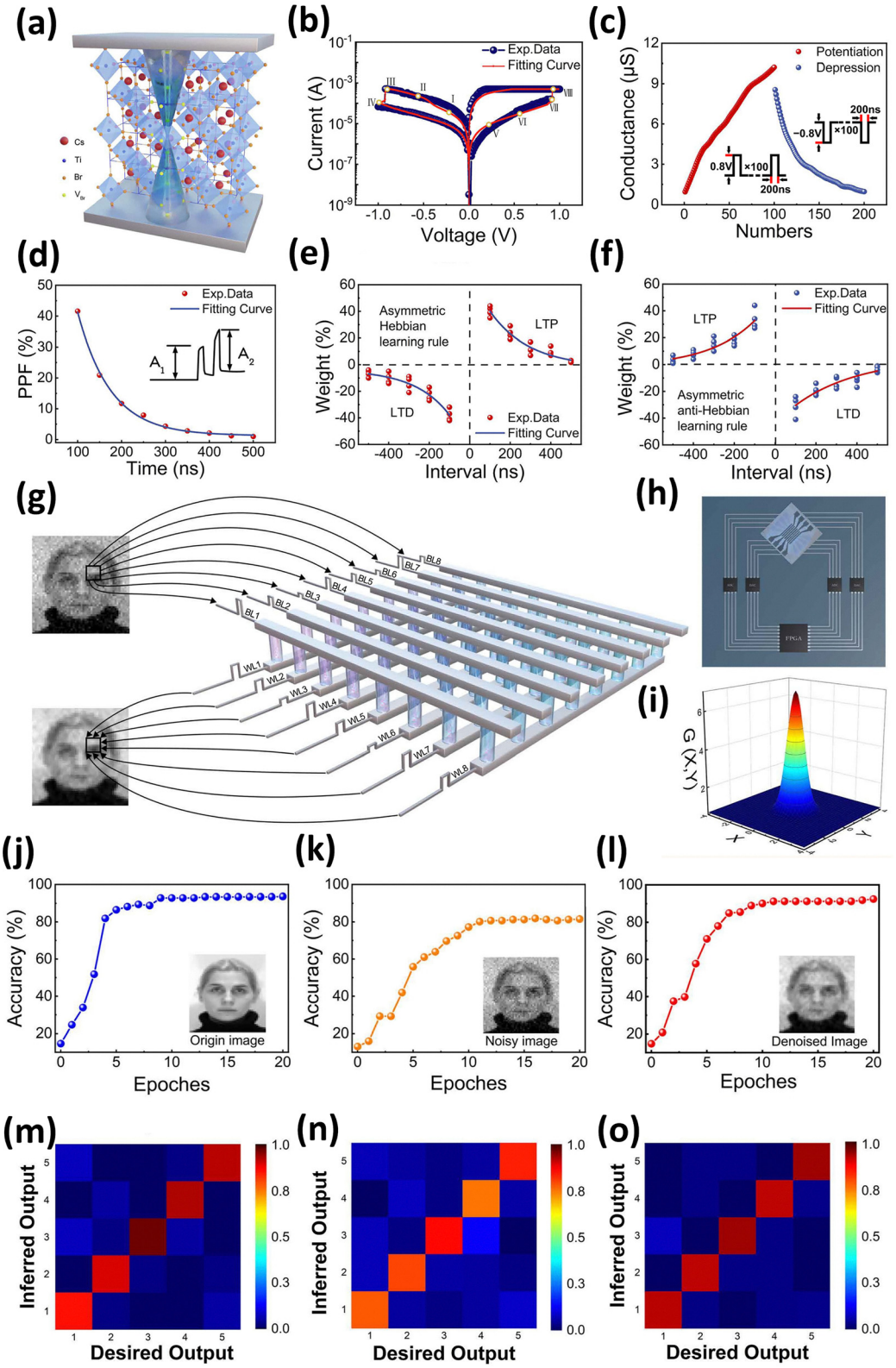

Fig. 4 (a) Schematic representation illustrating the formation of conductive filaments in the Al/Cs_2TiBr_6/FTO system. (b) The experimentally obtained *I*–*V* curve (blue) exhibits typical resistive switching behavior, and matches with the curve obtained from the COSMOL simulation. (c) The conductance obtained from the stimulation with multiple positive and negative pulses, demonstrating potentiation and depression, respectively. (d) The pulse-interval-dependent PPF index, representing the STP characteristic of the synapse. The inset illustrates the alteration in postsynaptic current induced by a pair of input sequences. (e) and (f) The measured changes in synaptic weight (conductance change) under different programmed pulse stimuli with varied relative timing (Δt) of the presynaptic and postsynaptic pulses, demonstrating the STDP characteristics of the memristor. (g) Diagram of the crossbar array

for the image denoising system, with eight input bit lines (BL1–8) and eight output word lines (WL1–8). (h) A diagrammatic representation of the circuit block. (i) The Gaussian distribution employed during the denoising procedure. (j)–(l) Recognition accuracies for the (j) original, (k) noisy, and (l) denoised images during the training phase of the artificial neural network, respectively. (m)–(o) Confusion matrices illustrate recognition outcomes for the (m) original, (n) noisy, and (o) denoised images, respectively. Reproduced with permission.[59] Copyright 2025, Cell Press.

+2 V spikes, following the X pattern, was subsequently applied, resulting in the regeneration of the image under the same stimulation conditions. Fifteen minutes later, excitatory postsynaptic currents measured at 0.5 V continued to exhibit the letter-shaped profile. In Fig. 5g, when N is set to 20, and in Fig. 5h with N at 30, there is a noticeable absence of yellow pixels and a reduction in orange pixels. This observation suggests a more pronounced differentiation between the excitatory postsynaptic currents in feature and non-feature regions. In Fig. 5i, with N set at 40, and in Fig. 5j, with N at 50, the synapse ultimately revealed a distinct X feature map corresponding to the target symbol.

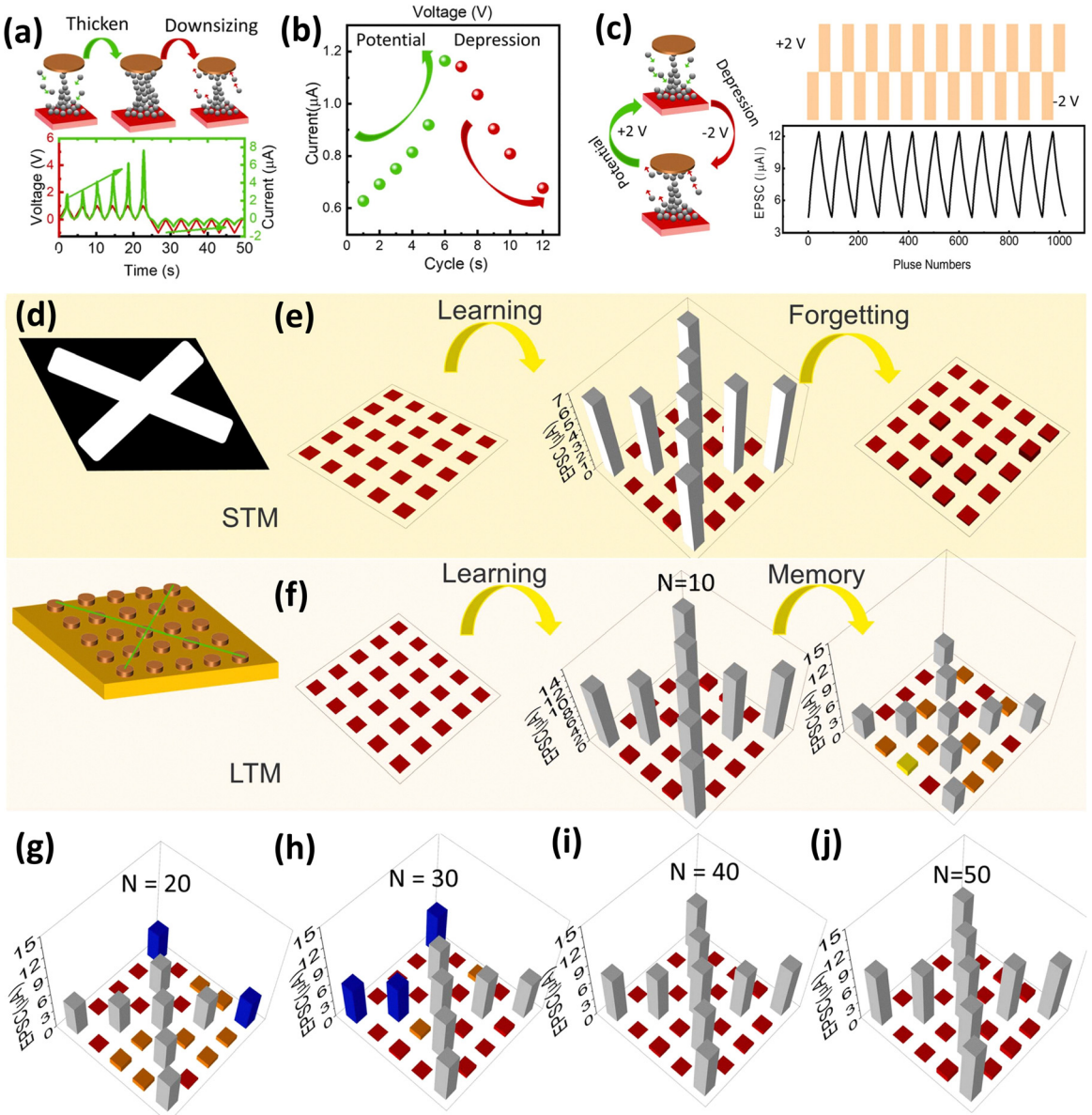

Fig. 5 (a) Schematic representation of the initial 25-second-long series of excitatory signals (0 V → +1 V → 0 V), followed by a 25-second-long series of inhibitory signals (0 V → −1 V → 0 V). (b) The peak response current illustrates the potentiation and depression pattern of the synapse. (c) Potentiation and depression pattern of the synapse over alternating trains of +2 V spikes and −2 V spikes, which remained stable over 1000 stimulations. (d) Schematic representation of the letter X to be represented in a 5 × 5 array of synapses. (e) The array of synapses acquired short term memory of the letter X (2 V, N = 1), and then lost the memory spontaneously after 15 minutes. (f)–(j) The array of synapses acquiring more durable memory of the letter X with increasing number of spikes (2 V). (f) N = 10, (g) N = 20, (h) N = 30, (i) N = 40, and (j) N = 50. Reproduced with permission.[60] Copyright 2024, Elsevier.

Overall, the devices illustrated in Fig. 1–5 exhibit unique functional features based on the perovskite composition and switching mechanism. The $CsCu_2I_3$ memristor depicted in Fig. 1 has volatile short-term dynamics, making it particularly suitable for reservoir computing systems, where transient conductance responses enhance temporal signal processing. Conversely, the $Cs_3Bi_2I_9$ device shown in Fig. 3 demonstrates robust multilevel resistive switching with an ON/OFF ratio exceeding 10^6, making it more suitable for high-density non-volatile memory applications. Additionally, the $FASnI_3$ device (Fig. 2) employs filamentary switching to attain dependable bipolar resistive memory characteristics. In contrast, the Cs_2TiBr_6 and $Cs_2AgBiBr_6$ systems (Fig. 4 and 5) focus on synaptic plasticity and conductance modulation that mimic biological learning mechanisms. These contrasts highlight how compositional engineering in lead-free perovskites facilitates a variety of device capabilities, from short-term neuromorphic computing components to stable multilevel memory storage. As a result, modifying the composition and defect landscape of lead-free perovskites offers a clear approach to enhancing the electrical performance of individual memristors and the overall functionality of extensive crossbar computing architectures. While performance metrics like ON/OFF ratios are well-documented, the underlying physical mechanisms remain relatively poorly understood. Future efforts must bridge this gap by establishing robust connections between material defect chemistry, ion migration dynamics, and large-scale array operations.

Nevertheless, ensuring long-term reliability remains a significant challenge for large-scale perovskite crossbar arrays. The degradation pathways are mainly linked to the continuous formation and breaking of filaments during switching cycles, leading to the accumulation of structural defects and a gradual destabilization of the conductive paths. Furthermore, ion migration, particularly involving halide vacancies or mobile metal cations, can result in localized compositional changes, leading to fluctuations in switching voltage and resistance states during long-term operation. Environmental factors such as increased temperature and humidity can enhance ionic diffusion and initiate partial chemical decomposition of the perovskite lattice.

4. Conclusion

Crossbar arrays constructed from halide-perovskite memristors are advancing into practical platforms for efficient storage and on-chip learning. Each cell incorporates a perovskite switching layer featuring either an intrinsic rectifying junction or an external selector, effectively blocking stray paths that previously constrained array size. Selector thresholds currently exceed half-select voltages by multiple orders of magnitude, effectively reducing leakage and maintaining signal integrity throughout thousands of interconnected nodes. Optimizing materials has been fundamental to achieving these improvements. Lead-free halide perovskites, stabilized through lattice doping or compositional adjustments, demonstrate consistent filament growth and regulated tunneling gaps. CC engineering generates uniform conductance levels, providing the multistate weights necessary for analog inference. The ionic dynamics present in perovskites inherently mimic synaptic responses, allowing for the hardware implementation of temporally correlated learning without the need for algorithmic complexity. Nonetheless, there are remaining challenges. Residual sneak currents constrain the maximum dimensions of arrays, and the endurance of selectors under billions of switching cycles warrants further investigation. Variability between devices requires the development of compact models that accurately represent filament statistics and ion kinetics, enabling efficient allocation of circuit margins. Long-term operation under electrical, thermal, and environmental stress must be systematically investigated. In particular, the evolution of microscopic defects should be correlated with device failure limits. When examined through the perspective of the crossbar array, halide-perovskite memristors exhibit the density, speed, and adaptive plasticity required for advanced memory and edge intelligence. Interdisciplinary collaboration across chemistry, device engineering, and circuit design will transition these laboratory prototypes into commercial, non-volatile neuromorphic hardware. Future investigations should focus on scalable fabrication techniques that enable consistent switching characteristics across large crossbar arrays, while ensuring complete control over filament formation and conductance states. Furthermore, implementing advanced defect passivation and interface engineering techniques will be crucial for reducing uncontrolled ion migration and enhancing long-term endurance and environmental stability. Moreover, advances in dependable compact models and circuit-level design approaches will enable the effective integration of perovskite crossbar arrays into extensive neuromorphic and in-memory computing systems.

Conflicts of interest

The authors declare that there is no conflict of interest regarding the publication of this paper.

Data availability

No primary research results, software or code have been included and no new data were generated or analysed as part of this review.

Acknowledgements

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korean government (MSIT) (RS-2025-00554803).

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