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Broader Context

Solar energy is central to global efforts to mitigate climate change and secure affordable, low-carbon electricity at the scale required for a sustainable energy transition. Perovskite solar cells have emerged as a promising next-generation photovoltaic technology due to their high efficiency and low manufacturing costs. However, a critical barrier to their real-world deployment is that devices performing exceptionally well at laboratory scale often lose efficiency when fabricated over larger areas, limiting their industrial relevance. This study addresses this scalability challenge by identifying how interfacial quality and electrical uniformity govern performance losses in larger-area devices. By applying a vapour-phase deposition technique to form ultrathin, uniform charge-transport layers, we demonstrate a practical pathway to significantly reduce efficiency losses during upscaling. Our findings provide fundamental insight into why scaling losses occur and show how they can be mitigated without relying on complex chemical additives or fragile interfacial treatments. This work highlights the importance of scalable interface engineering for translating laboratory advances into commercially viable solar technologies, supporting the broader goal of accelerating the global adoption of renewable energy.



ARTICLE

Scalable Inverted Perovskite Solar Cells Enabled by Atomic Layer Deposition (ALD)

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Perovskite solar cells (PSCs) have managed to achieve certified power conversion efficiencies (PCEs) of 27.3%, yet losses during device upscaling remain a major roadblock in the path to commercialization. Compared with mature photovoltaic technologies such as crystalline Si and thin-film CdTe or CIGS, PSCs show a more pronounced performance loss when transitioning from small lab-scale cells to larger modules. These losses are commonly attributed to increasing series resistance (R_s) in transparent conducting oxide (TCO) substrates and challenges in maintaining film uniformity over larger areas. Here, inverted PSCs were systematically fabricated and evaluated across active areas of 0.06, 0.25, and 1 cm² without altering the device architecture, enabling isolation of intrinsic scaling losses. Atomic layer deposition (ALD) was employed to deposit an ultrathin nickel oxide (NiO) hole transport layer (HTL), allowing precise thickness control and highly conformal coverage compared to solution-processed nanoparticle (NP) and sol-gel NiO films. Thin film and interfacial characterization demonstrate superior coverage, electrical homogeneity, and surface wettability for ALD-NiO, resulting in an improved platform for perovskite growth. Devices incorporating ALD-NiO exhibit the smallest efficiency loss upon scaling, with PCE depreciation minimized to approximately 2% when increasing the active area from 0.06 to 1 cm² (19.8% to 17.6%). While the open-circuit voltage (V_{oc}) and short-circuit current density (J_{sc}) remained stable, the PCE loss was primarily driven by a decrease in fill factor (FF). This work identifies ALD-deposited NiO as an effective, dopant-free HTL for mitigating scaling-induced losses in inverted PSCs and provides mechanistic insight into the interplay between interfacial conformity, perovskite microstructure, and scale-related resistive limitations. Overall, this work advances understanding of scaling-induced performance losses in PSCs and underscores the potential of ALD-enabled interface control for future large-area and tandem photovoltaic applications.

Broader Context

Solar energy is central to global efforts to mitigate climate change and secure affordable, low-carbon electricity at the scale required for a sustainable energy transition. Perovskite solar cells have emerged as a promising next-generation photovoltaic technology due to their high efficiency and low manufacturing costs. However, a critical barrier to their real-world deployment is that devices performing exceptionally well at laboratory scale often lose efficiency when fabricated over larger areas, limiting their industrial relevance. This study addresses this scalability challenge by identifying how interfacial quality and electrical uniformity govern performance losses in larger-area devices. By applying a vapour-phase deposition technique to form ultrathin, uniform charge-transport layers, we demonstrate a practical pathway to significantly reduce efficiency losses during upscaling. Our findings provide fundamental insight into why scaling losses occur and show how they can be mitigated without relying on complex chemical additives or fragile interfacial treatments. This work highlights the importance of scalable interface engineering for translating laboratory advances into commercially viable solar technologies, supporting the broader goal of accelerating the global adoption of renewable energy.

Introduction

Perovskite solar cells (PSCs) are emerging as a leading next-generation photovoltaic (PV) technology. Their tunable bandgap,^{1,2} long charge-carrier diffusion lengths,^{3,4} high defect tolerance,⁵⁻⁷ and

strong absorption,⁸ have enabled power conversion efficiencies (PCEs) of 27.3%,⁹ rivalling the performance of crystalline silicon (c-Si) solar cells. The combination of high-efficiency, low-temperature processing, and compatibility with flexible and tandem architectures positions PSCs as promising candidates for low-cost, high-performance PVs.¹⁰⁻¹³

Despite rapid progress, commercialization remains constrained by three persistent challenges: long-term stability, lead (Pb) toxicity, and large-area upscaling. While considerable research has focused

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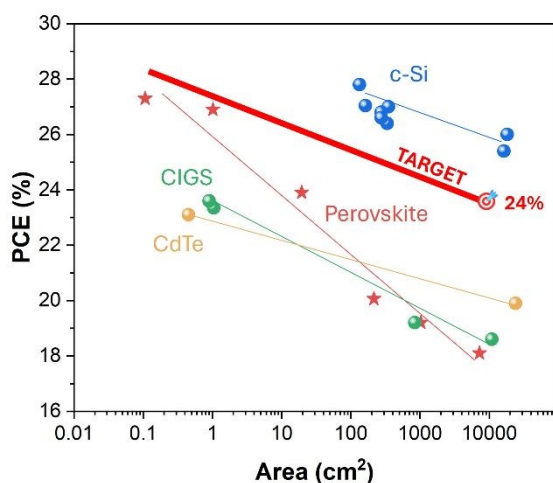


Figure 1. Comparative power conversion efficiency (PCE) decline of c-Si (blue), perovskite (red stars), CIGS (green), and CdTe (orange) devices with increasing area. The 'TARGET' line uses the more favourable c-Si scaling trend to project performance that commercially viable perovskite modules should ideally achieve. Data from Solar Cell Efficiency Tables (Version 66).¹⁸

on mitigating stability and toxicity concerns, the issue of scalability remains comparatively underexplored. All PV technologies experience decreased PCE when transitioning from small-area cells to large-area modules.^{14–17} However, PSCs suffer a particularly pronounced drop, historically showing $\approx 10\%$ reductions in PCE from champion small devices to modules greater than 10 cm^2 in area.^{9,15,18}

As illustrated in Figure 1, this decline is far steeper than in mature c-Si, CIGS, or CdTe devices. This discrepancy clearly indicates that scalability remains one of the most significant obstacles to the commercial adoption of PSCs. The sources of these losses are multifaceted. A major contributor is the linear increase in series resistance (R_s) with increasing device area, stemming from the sheet resistance of the transparent conducting oxide (TCO) substrate.^{19,20}

Equally important are non-uniformities and morphological defects that arise when producing large-area thin-films; including pinholes/cracks, increased grain boundary (GB) density and reduced film homogeneity. These issues collectively diminish the short-circuit current density (J_{sc}) and, more notably, the fill factor (FF).^{21,22} Since

FF is typically the most sensitive parameter to resistive and interfacial losses in PSCs, mitigating FF decline is essential for achieving favourable scaling behaviour.

In this context, inverted (p-i-n) PSCs (iPSCs) have gained significant attention. They exhibit improved operational stability, low hysteresis, compatibility with flexible substrates, and integration potential for tandem devices.^{11–13,23–27} In iPSCs, the hole-transport layer (HTL) plays a defining role in determining perovskite film formation, interface quality, and charge extraction efficiency due to its location directly beneath the absorber layer. Nickel oxide (NiO) has emerged as a widely adopted HTL due to its suitable energy alignment with perovskite, strong chemical, thermal and light stability, and compatibility with low-temperature, large-area processing.^{28–32} Nonetheless, solution-processed NiO films often exhibit low conductivity, interfacial defects, and non-uniform coverage—limitations that become markedly more severe during device upscaling.^{14,33,34} To overcome these challenges, this work employs atomic layer deposition (ALD) to fabricate the NiO HTL. ALD is a vapour-phase deposition technique that enables atomic-scale thickness control and exceptional conformality through sequential, self-limiting surface-reaction chemistry (Figure 2). These characteristics are advantageous for PSC fabrication, as HTL thickness and uniformity strongly influence FF and overall device performance.^{22,35} In particular, ALD's ability to conformally coat high-aspect ratio features is critical for ensuring a uniform NiO layer across FTO substrates, mitigating shunting paths and local non-uniformities that can significantly hinder device performance during upscaling. Prior studies have demonstrated high small-area efficiencies using ALD-NiO iPSCs,^{30,36–39} yet the implications of ALD-NiO for device upscaling have not been systematically examined.

Here, we present a controlled study investigating the upscaling behaviour of ALD-NiO iPSCs compared to more traditional solution processed sol-gel and nanoparticle (NP)-NiO iPSCs across active areas ranging from 0.06 to 1 cm^2 . The device architecture and processing conditions are intentionally kept constant, enabling a direct evaluation of scaling effects. The HTL deposition method is the sole variable factor in the fabrication process, which allows for a clear

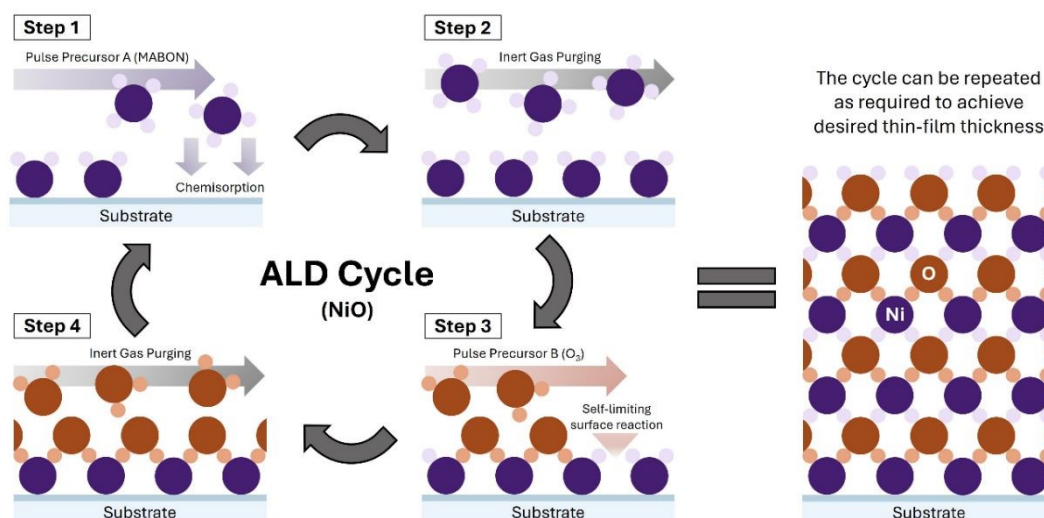


Figure 2. Schematic of the atomic layer deposition (ALD) cycle. The process involves alternating pulses of chemical precursors and inert gas purges, enabling conformal, self-limiting, layer-by-layer growth of thin films. In this work, MABON ((1-dimethylamino-2-methyl-2-butoxide)Nickel(II)) and ozone (O_3) precursors are used for NiO deposition.



analysis and comparison of ALD, sol-gel, and NP-deposited NiO layer suitability for upscaling iPSCs. Furthermore, unlike many reports that incorporate interlayers, dopants, surface passivation layers, or self-assembled monolayers (SAMs), this work isolates the intrinsic benefits and drawbacks of each HTL deposition method without additional performance-enhancing modifications. As such, the devices fabricated here are not intended to challenge current state-of-the-art PSCs but rather serve as a foundation for understanding the potential for ALD as a HTL deposition strategy to translate the high performance of today's champion iPSCs to larger areas more suitable for commercialization. The focus is intentionally placed on relative performance losses, identifying practical strategies for scalable fabrication rather than pursuing record efficiencies.

Our results demonstrate that ALD-NiO acts as a superior platform for triple-cation perovskite growth compared to solution-processed NiO-HTLs, resulting in improved film uniformity and reduced defect density. Device performance analysis reveals that FF remains the dominant loss mechanism upon increasing device area. To elucidate the underlying cause, we introduce a 3D model that quantifies the total internal GB area within the perovskite absorber. A simplified void-free and perfectly packed cubic geometry is utilised for mathematical clarity and to establish a direct quantitative relationship between GB density and FF deterioration, offering mechanistic insight into scaling-induced performance losses. Although real-world films deviate from this idealised symmetry, the model effectively aids relative trend analysis. Further details on model constraints are available in the SI. Leveraging ALD's conformality and thickness precision, scaling-induced PCE loss was minimized to approximately -2%, with efficiencies of 19.8% and 17.6% for active areas of 0.06 and 1 cm², respectively. To the best of our knowledge, these values represent some of the highest reported efficiencies for dopant-free inverted PSCs employing ALD-NiO HTLs, underscoring the potential of ALD as a robust strategy for overcoming scalability limitations in PSCs.

Results and discussion

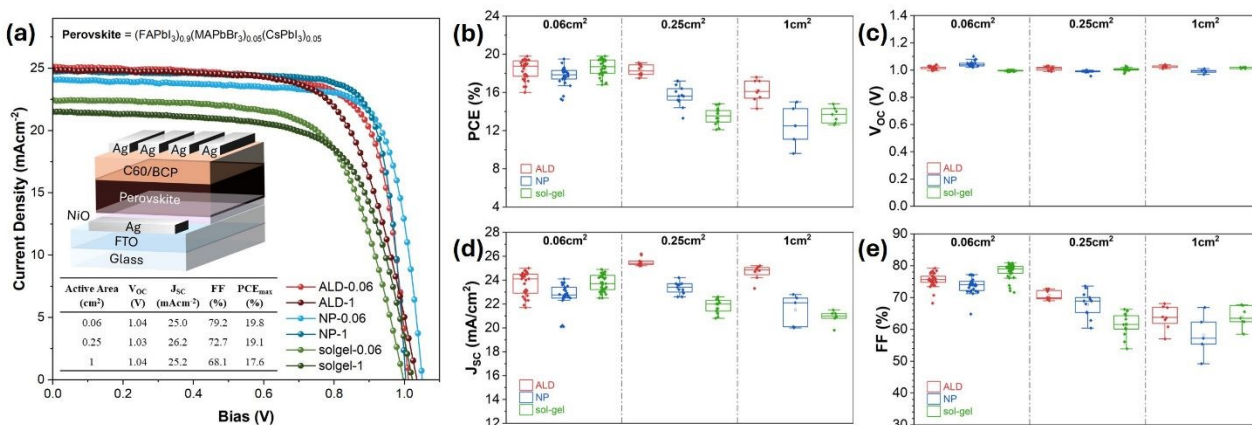


Figure 3. (a) J-V curves of iPSCs incorporating ALD-, NP-, and sol-gel-NiO HTLs at 0.06 and 1 cm². Champion cells at each area size for ALD-NiO HTL-based iPSCs are shown in the table as inset. The triple-cation perovskite composition and 3D device architecture schematic are also shown inset. (b-e) Statistical photovoltaic parameters: (b) power conversion efficiency (PCE), (c) open-circuit voltage (V_{oc}), (d) short-circuit current density (J_{sc}), and (e) fill factor (FF) for devices fabricated using the three NiO deposition methods at active areas of 0.06, 0.25, and 1 cm². V_{oc} remains largely unchanged across all conditions, while J_{sc} and FF exhibit the strongest area-dependent losses. The total number of data points decreases with increasing active area because the fixed substrate dimensions limit the number of large-area devices per fabrication batch; all functional devices from a single representative batch for each area are presented here to ensure statistical transparency. Full device statistics are provided in Table S1.

PSC Device Performance

iPSC devices were fabricated with solution-processed sol-gel-NiO, NP-NiO (control), and vapour-processed ALD-NiO (target) HTLs, while keeping all other device layers unchanged. As presented in Figure 3, all three devices with different HTLs were fabricated at active areas of 0.06, 0.25, and 1 cm² to observe how their performance changes when subject to upscaling. Detailed J-V data for best-performing devices at each active area is listed in Table S1. Maximum PCEs of 19.5-19.8% are consistent with other published work on iPSCs with pure-NiO HTLs (see, Figure 3a). Figure 3b shows a clear drop in PCE for all device types when upscaling. Increasing the active area from 0.06 to 1 cm² induces PCE drops of -5% for solgel NiO, -4.5% for NP NiO, and -2.2% for ALD NiO devices. Despite all device types having comparable PCE at the lab-scale, performance degradation as the device active area varies with the HTL deposition method. The observed stability of V_{oc} across all devices and measurement areas (Figure 3c) is a strong experimental indicator of well-controlled, reproducible fabrication and suppressed non-radiative recombination.⁴⁰ Although current state-of-the-art PSCs can achieve higher V_{oc} values, consistency across increasing active areas is of more importance than the absolute value for identifying upscaling loss mechanisms.

As shown in Figure 3d, J_{sc} remains consistent across all ALD-NiO devices, with a modest improvement of approximately +4% when scaling from 0.06 cm² to 1 cm². In contrast, NP and sol-gel devices exhibit clear area-dependent losses of -5.3% and -12%, respectively. Although the HTL compositions are nominally identical, the ALD process produces NiO films with markedly different morphological and structural characteristics compared to NP or sol-gel counterparts, which directly influence charge transport and collection during device operation. The excellent conformality of ALD-NiO films—despite the underlying rough FTO substrate—likely facilitates more homogeneous deposition of the subsequent perovskite absorber. Variability in spin-coating is well-documented, and



the technique is widely considered unsuitable for large-area fabrication.^{16,41–44} While solution processed perovskite films can appear uniform over small lab-scales, gradient spreading inevitably introduces thickness and compositional variations over larger areas, contributing to the observed J_{SC} decline in sol-gel and NP devices. Alternative scalable deposition techniques, such as thermal evaporation or blade coating, have been shown to mitigate these losses while maintaining high performance.^{16,41–44} Overall, these results indicate that the fabrication method of the active layers—both the HTL and perovskite absorber—plays a decisive role in J_{SC} retention during area scaling, and consequently the PCE of iPSCs.

Lastly, fill factor (FF) data for devices is shown in Figure 3e. Unlike J_{SC} , which showed varying trends between devices with solution and vapour processed NiO HTLs, the trend of FF decreasing with increased active area is consistent across all devices. The maximum FF (absolute) values of all devices decrease by more than 10% when scaling from 0.06 cm² to 1 cm², while the average FF falls by -11.9% for ALD, -14.3% for sol-gel, and -15.6% for NP devices. Although ALD-based devices exhibit a less pronounced decrease compared to sol-gel and NP devices, the absolute reduction in FF remains significant and represents the largest performance loss among all J–V parameters. At 1 cm², all device sets contain some devices with FF values below 60%, a sharp decline from the maximum values of around 80% in small-area devices. These results signify that FF is the critical limiting factor in upscaled devices, offering the greatest opportunity for improvement through interface and transport layer engineering. This observation motivates a

deeper examination of the physical origins of FF loss, and the reasoning behind why ALD-based NiO HTLs mitigate these losses more effectively than NP and sol-gel NiO films.

Impact of Resistive Losses on Upscaling

Resistive losses are a well-established source of FF drop in PSCs.^{19,45} Galagan et al., used direct-current (DC) simulations to show that scaling PSCs from 0.09 to 1 cm² can reduce FF from 76% to 69% for devices with a TCO sheet resistance of 10 Ωcm^{-1} .²⁰ Subsequent experimental work confirmed a corresponding 10% drop in PCE, with even larger efficiency losses observed for high-resistance substrates. In this study, both the active-area range (0.06 - 1 cm²) and the sheet resistance of the FTO substrates (6 - 9 Ωcm^{-1}) are comparable to those used by Galagan et al., indicating that the TCO resistivity is a substantial contributor to FF degradation in our devices.

Consistent with this expectation, ALD-NiO devices show stable shunt resistance (R_{SH}) with increasing active area (Figure 4b), whereas the series resistance (R_S) increases notably (Figure 4c). Figure 4a compares the J–V characteristics of devices with different active areas. (The dependence of resistive parameters and FF on device area for sol-gel and NP NiO devices is shown in Figure S1.) While all devices exhibit nearly identical current densities at low bias, a pronounced roll-off in the high-bias region becomes increasingly severe as the active area increases. This roll-off occurs when voltage losses across the series resistance become comparable to the applied bias. At high current-densities near V_{OC} , a growing fraction of the voltage is dissipated in resistive elements of the device, which weakens

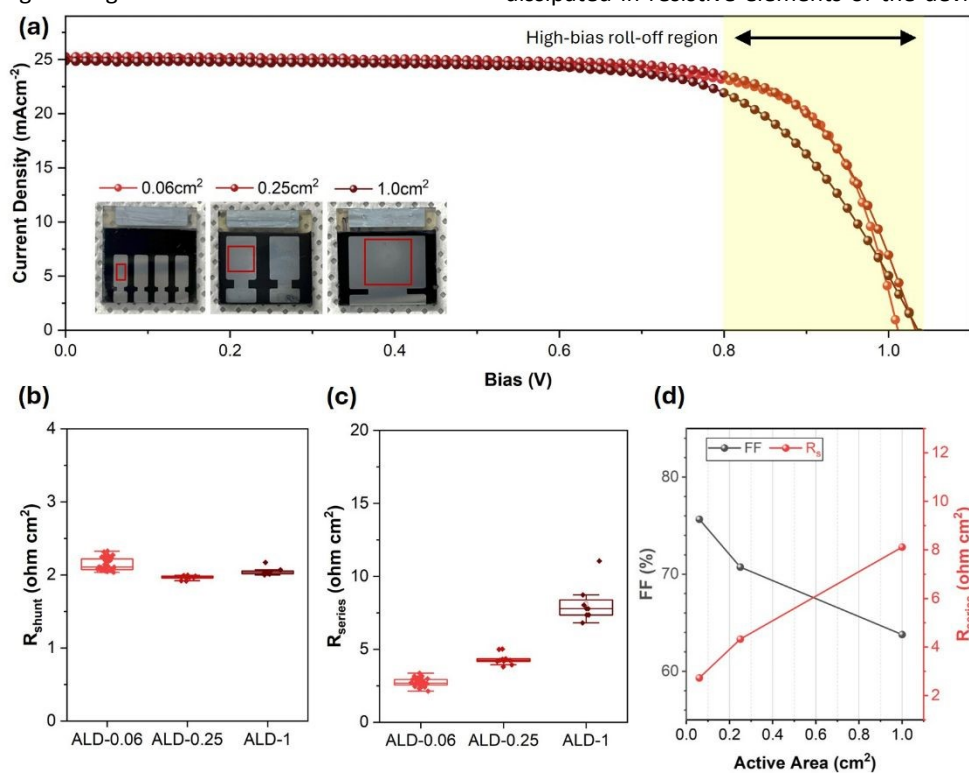


Figure 4. (a) J–V curves for each device, highlighting the high-bias roll-off region (yellow box), where R_S dominates; inset images show top-view photographs of representative devices with the active areas indicated by red boxes. Dependence of resistive parameters and FF on device area in ALD-NiO HTL-based iPSCs. Box plots showing the evolution of (b) shunt resistance (R_{SH}) and (c) series resistance (R_S) for device areas of 0.06, 0.25, and 1 cm². (d) Relationship between FF and R_S with increasing active area, identifying series resistance as the dominant loss mechanism in larger-area devices. Corresponding plots for sol-gel and NP-NiO-based iPSCs are shown in Figure S1.



the internal field and limits charge extraction, producing the observed flattening of the J-V curve and corresponding reduction in FF.^{46,47} The behaviour is characteristic of R_s -limited charge extraction and directly explains the observed reduction in FF for larger-area devices. The trend is summarized in Figure 4d, where increasing active area leads to increased R_s and decreased FF. The strong inverse correlation between FF and R_s confirms that R_s is the dominant factor governing FF loss, and therefore PCE decrease, upon device upscaling.

Resistive losses, however, originate from multiple aspects of device architecture, including geometry and charge transport layer (CTL) & electrode design. Several strategies have been shown to mitigate scaling-induced resistive limitations, such as implementing strip-like geometries, using modules composed of narrow interconnected sub-cells, and optimizing CTL layer thickness.^{48–53} Together, these findings emphasize that managing both intrinsic TCO resistance and device design is another essential consideration when trying to fabricate large-area devices near their performance limits.

Comparison of ALD and solution-processed NiO films

To investigate the effect of NiO deposition method, solution processed sol-gel and NP NiO films (control) alongside ALD NiO (target) were comprehensively characterized, focusing on their impact on the morphology and optoelectronic properties of the overlying perovskite absorber layer. NiO layer thickness varied between approximately 6 and 15 nm (Table S2). The ALD process demonstrated linear growth, yielding a growth-per-cycle (GPC) of 0.22 Å/cycle on 4-inch Si wafers (Figure S2). This precise thickness control and large-area uniformity offer a significant advantage over solution-based sol-gel or NP methods.

Grazing-incidence X-ray diffraction (GIXRD) was used to probe the crystallinity of NiO layers. As shown in Figure 5, diffraction features are observed at $2\theta \approx 37^\circ$, 43° , 62° , 75° , corresponding to the (111), (200), (220) and (311) planes of cubic NiO. The signal is weak for thinner films (sol-gel, NP, and ALD 200 cycles) while a clear and higher-intensity pattern is observed for the thicker ALD film (500 cycles). This behaviour is attributed to the limited diffracting volume of the thinner films rather than to amorphous NiO. The increased diffraction

intensity from 200 to 500 ALD cycles further reflects controlled thickness scaling in the ALD-grown NiO layers.

Field-Emission Scanning Electron Microscopy (FE-SEM) imaging of the bare NiO films on Glass/FTO substrates (Figure 6a-c) reveals distinct differences in the morphology formed by ALD, NP, and sol-gel methods. The ALD-NiO film (Figure 6a), being the thinnest at just ~ 6.4 nm, forms a highly conformal layer morphologically indistinguishable from the surface of the FTO grains. Unlike other methods, ALD ensures uniform coverage over the rough FTO crystallites without significantly altering the surface texture. In contrast, the NP-NiO film (Figure 6b) exhibits a rougher, granular texture composed of grain clusters approximately 20nm in diameter, which appear to fully cover the underlying FTO. The sol-gel NiO (Figure 6c), however, provides only partial coverage. As highlighted in the inset (red box), protruding FTO crystallites are clearly exposed, while the NiO appears to have preferentially accumulated in the valleys. Achieving full coverage with the sol-gel method would likely require a significantly thicker layer, which could be detrimental to device performance by increasing series resistance (R_s) and causing subsequent FF losses. Simultaneous comparison with Conductive-Atomic Force Microscopy (C-AFM) imaging provides a more comprehensive understanding of the effect of morphology differences on electrical homogeneity. C-AFM topography maps (Figure 6d-f) confirm the high-aspect nature of the underlying FTO. Bright areas indicate high peaks, and valleys appear dark. Corresponding conductivity maps (Figure 6g-i) reveal a stark contrast in film quality. The ALD-NiO film reveals the most spatially uniform conductive response with a low occurrence of high-current hotspots. Conversely, NP-NiO and sol-gel NiO films display frequent high-current features and significant heterogeneity in local current, indicative of local shunt pathways or non-uniform contact. The overlay of conductivity and topography (Figure 6j-l) conclusively shows that current hotspots in sol-gel and NP-NiO films are

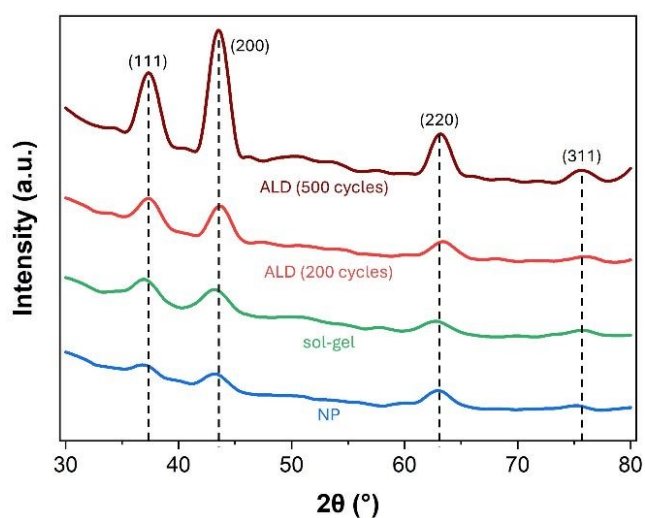


Figure 5. Grazing incidence X-ray diffraction (GIXRD) patterns of NiO films prepared by NP (blue), sol-gel (green), and ALD (200 cycles, red), and ALD (500 cycles, dark red). Diffraction peaks consistent with cubic NiO are observed, with stronger intensity for the 500-cycle ALD film primarily due to its increased thickness.



concentrated around FTO peaks that were identified in the FE-SEM analysis. The superior coverage of the ALD-NiO layer, despite the roughness of FTO beneath, results in a much more qualitatively uniform conductivity map. Given that FF is highly sensitive to leakage and local shunts³⁵—particularly in large-area devices—such conductivity inhomogeneities help explain why NP and sol-gel devices struggle to maintain FF during upscaling.

To elucidate the effect of the NiO deposition method on hole transport, current-voltage (I-V) curves for FTO/NiO(ALD)/Ag, FTO/NiO(NP)/Ag, and FTO/NiO(sol-gel)/Ag were measured (Figure S3). All three NiO films exhibit a linear current-voltage relationship, indicating ohmic behaviour. Small slope differences likely reflect variations in leakage and contact resistance rather than the operating-condition series resistance, which is quantified separately in Figures 4 and S1.

Contact-angle measurements (Figure 7a-c) reveal that ALD-NiO is the most wettable (smallest contact angle = 13.6°), followed by sol-gel ($\approx 16.2^\circ$) and NP-NiO ($\approx 26.2^\circ$). The lower contact angle on the surface of ALD films promotes more uniform precursor wetting during spin-coating of perovskite and hence improved nucleation and larger, more continuous grains. This trend in wettability correlates with the perovskite morphologies observed in SEM (Figure S4). Each method produces distinct microstructures and grain sizes. ALD-NiO yields compact, well-covered perovskite films while NP and especially sol-gel films show poorer coverage, numerous voids, and smaller, more irregular grains that can facilitate shunts or non-uniform current pathways—factors that reduce FF as area increases. Histograms of perovskite grain size depending on the NiO deposition method are shown in Figure S6. To provide qualitative insight into how grain size influences the effective

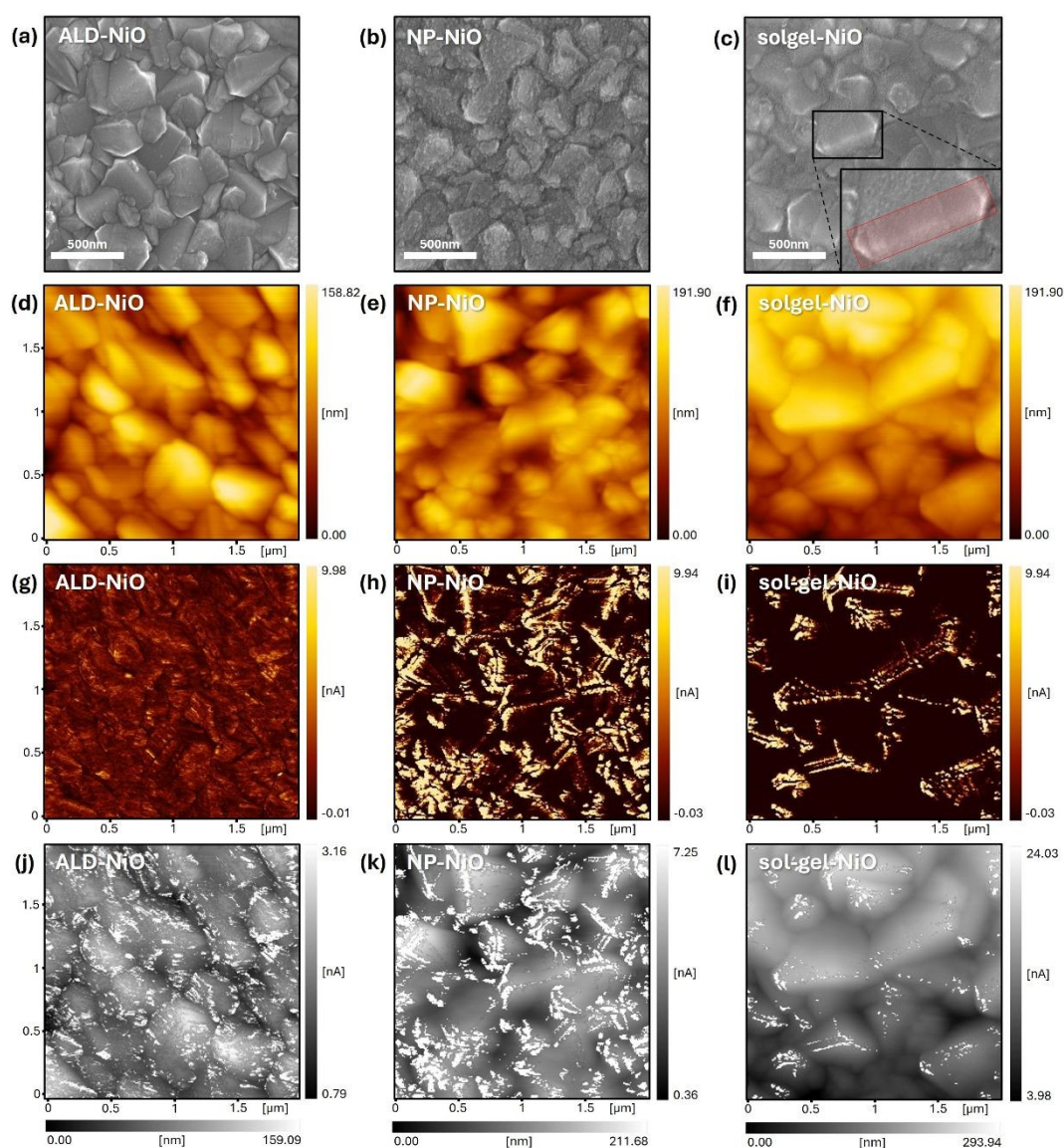


Figure 6. Surface characterization of NiO thin films deposited by ALD, NP, and sol-gel methods. *First row (a-c):* SEM topography of NiO films on Glass/FTO substrates. *Second row (d-f):* Topographical C-AFM images showing surface morphology. *Third row (g-i):* C-AFM current maps indicating local conductivity variations. *Fourth row (j-l):* Overlay of topography and current images in rows two and three, highlighting differences in how each NiO deposition method deposits over high-aspect ratio FTO. Note: The current scales in conductivity (g-i) and topography-current (j-l) overlays are individually optimized for each deposition method to clearly resolve local current variations and avoid signal saturation or loss of detail caused by the differing current ranges inherent to each film.



internal grain boundary area, a simple geometric model was employed (Figures S7–8). The model assumes idealized grain packing and is intended to illustrate scaling trends rather than provide a quantitative description of charge transport. The model parameters and equations are summarized in the supplementary information (Tables S3-S4 and following text).

Steady-state photoluminescence (PL) measurements of Glass/FTO/(HTL)/perovskite stacks were carried out using a 455 nm excitation laser source. Figure 7d compares the PL response of perovskite films deposited on ALD-, NP-, and sol-gel-NiO HTLs with a Glass/FTO/perovskite control and FTO-free Glass/NiO/perovskite reference structure. It should be noted that the FTO-free reference employs the same ALD-NiO layer as the corresponding Glass/FTO/NiO/perovskite stack, with the omission of underlying FTO being the only difference. In contrast to the Glass/NiO/perovskite reference, which exhibits clear PL quenching, all Glass/FTO/NiO/perovskite stacks show enhanced PL intensity relative to the Glass/FTO/perovskite control. Among the NiO HTLs, the ALD-NiO sample exhibits the highest PL intensity, followed by sol-gel and NP-NiO samples. The maximum PL peak positions for the FTO-containing samples remained largely unchanged, with emission maxima at 797 nm on FTO, 797 nm on NP-NiO, 794 nm on sol-gel NiO, and 798 nm on ALD-NiO, whereas the Glass/NiO/perovskite reference shows a modest blue-shift to 787 nm, which may be associated with changes in the dominant radiative recombination pathway under strong interfacial charge transfer conditions.^{54,55} PL quenching observed in the FTO-free reference is consistent with either efficient interfacial hole transfer or enhanced non-radiative recombination at the interface.⁵⁶ In the present case, the FTO-free reference is included to demonstrate that ALD-NiO

can induce strong quenching in a simplified structure. By comparison, the increased PL intensity observed in device-relevant Glass/FTO/ALD-NiO/perovskite stacks is consistent with reduced interfacial recombination while maintaining effective charge extraction, as support by the high performance of the corresponding devices. Similar behaviour, where NiO HTLs exhibit enhanced PL intensity despite efficient charge extraction and superior device performance have been observed in prior reports.^{36,38} Yang et al., observed that PL intensity decreased as the NiO HTL thickness increased. Despite a PEDOT:PSS sample showing PL quenching, and a NiO (ALD, 200 cycles) sample showing increased PL intensity, the NiO devices

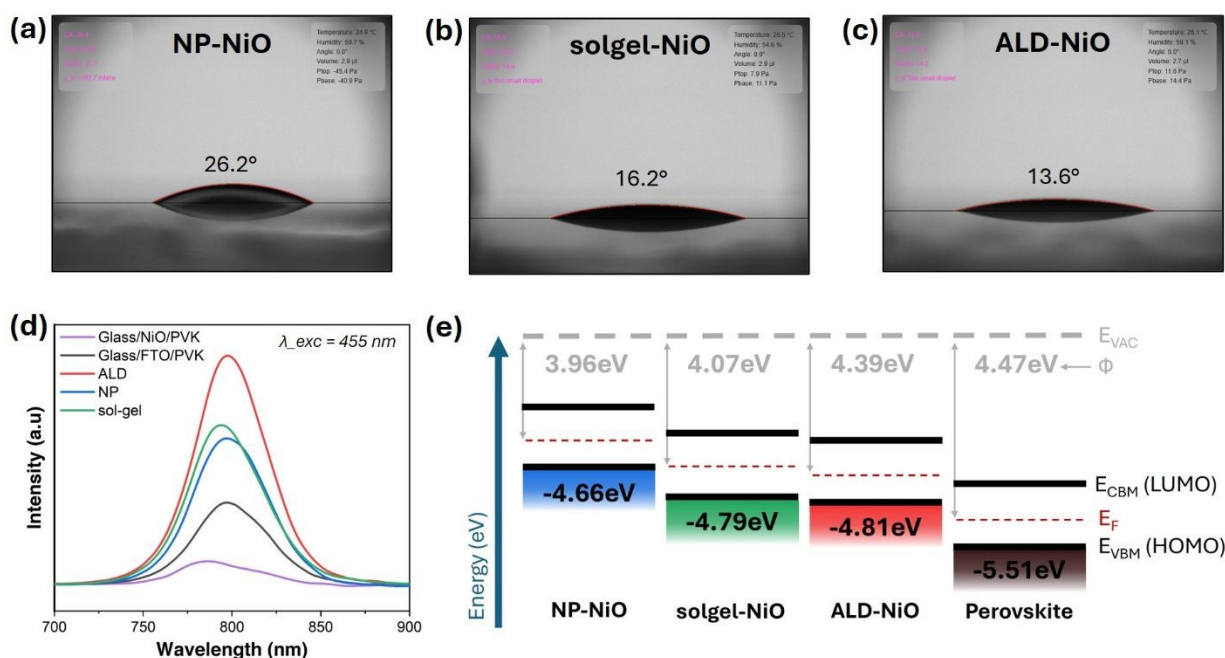


Figure 7. Water contact angle on the surface of (a) NP-NiO, (b) solgel-NiO, and (c) ALD-NiO films. (d) Steady-state photoluminescence (PL) spectra of perovskite films deposited on Glass/FTO/HTL substrates with ALD-NiO (red), NP-NiO (blue), and solgel-NiO (green), with respect to Glass/FTO/perovskite (black), and Glass/(ALD-NiO)/perovskite (purple) references. (e) Energy level diagram of ALD-, NP-, and solgel-NiO HTLs with respect to perovskite. Work function (Φ) and E_{VBM} were calculated by finding the secondary electron cutoff and fermi edge regions from UPS measurements, as shown in Figure S5.



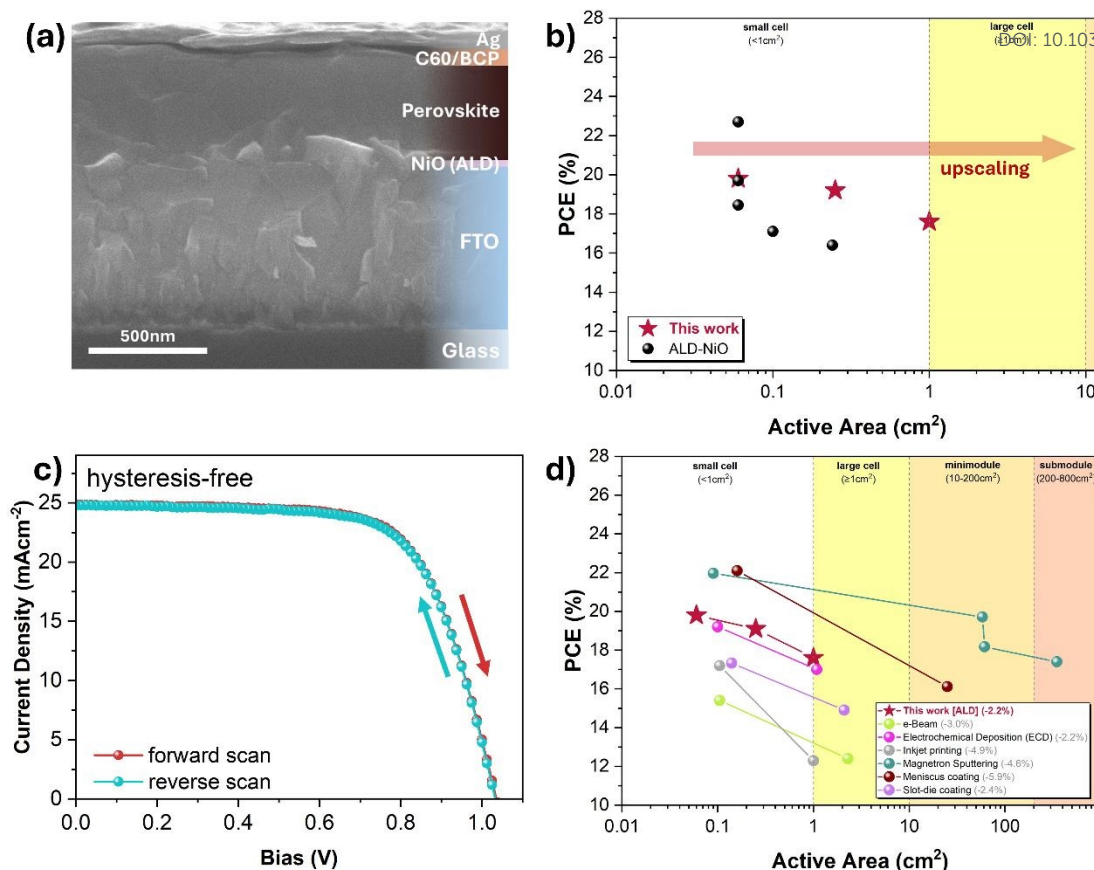


Figure 8. (a) Cross-sectional SEM image of iPSC full-device stack. (b) Power conversion efficiency (PCE) as a function of active area for perovskite solar cells employing pure ALD-NiO hole transport layers, comparing the present work with reported literature devices employing ALD-NiO HTLs.^{31,37–40} The yellow shaded region highlights the large-area regime (≥ 1 cm²). Red stars indicate devices fabricated in this work. (c) J-V curves of champion 1cm² ALD-NiO device showing hysteresis behaviour. Measurements were conducted at a scan speed of 187 mV/s (12.5 mV step size, 50 ms voltage settling time). The device exhibited negligible hysteresis, yielding an average PCE of 17.5% (reverse-scan PCE = 17.6%, forward-scan PCE = 17.4%). (d) Comparison of PCE retention across different scalable NiO-HTL deposition methods. Values in parentheses represent the total absolute PCE loss between champion devices across the area range. Full numerical data are detailed in Table S5 of the SI.

outperformed PEDOT:PSS devices in terms of the PCE and J_{sc} .³⁶ Taken together, the PL results and device metrics indicate that ALD-NiO forms a high-quality interface that mitigates recombination while maintaining effective hole extraction in device-relevant architectures.

Ultraviolet photoelectron spectroscopy (UPS) measurements of perovskite and NiO films (UPS Spectra shown in Figure S5) were used to produce an energy level diagram, as shown in Figure 7e. All three NiO deposition methods yield valence-band onsets close to the perovskite valence band maximum (VBM), but with subtle differences in work function and valence level. The measured valence energies for NP, sol-gel and ALD-NiO were approximately -4.66 eV, -4.79 eV and -4.81 eV, respectively, compared to the perovskite valence energy at -5.51 eV. The slightly deeper valence position of ALD-NiO compared to sol-gel and NP-NiO suggests marginally improved hole extraction, which could be a contributing factor to improved JSC and FF retention upon scaling in ALD-based devices.

The comparison in Figure 8b places the present results within the broader context of ALD-NiO based PSCs and highlights the role of a controlled, systematic scaling approach. Furthermore, the 1 cm² ALD-NiO devices exhibit negligible J-V

hysteresis (Figure 8c), confirming a high-quality interface between the HTL and absorber layer. ALD-NiO forms a seamless, low-loss contact with the perovskite, allowing for efficient hole collection even over larger areas. Unlike many literature reports where device area varies across unrelated architectures and processing conditions, this work examines performance evolution from small- to large-area devices within a consistent materials system and fabrication framework. The observed retention of PCE upon increasing active area therefore reflects intrinsic scalability of the ALD-NiO HTL and device design, enabling a more meaningful assessment of upscaling behaviour in PSCs.

Lastly, the performance retention observed in this work was benchmarked against various scalable NiO deposition techniques reported in the literature (Figure 8d and Table S5). While techniques such as magnetron sputtering and meniscus coating have achieved higher absolute PCEs, those results were contingent upon the use of multi-layer (sputtered-NiO/NP-NiO/SAM) HTL stacks and perovskite passivation. Despite these additional layers, those systems show scaling losses (-4.6% and -5.9%) more than double those of our baseline ALD-NiO devices (-2.2%). These results indicate that the superior uniformity of ALD-NiO provides a more robust morphological foundation for



suppressing the interfacial defects that typically compromise performance in large-area PSCs that incorporate NiO-HTLs. Furthermore, by focusing on the 1 cm² scale, we enable a precise evaluation of intrinsic HTL scaling losses without introducing further complexities of laser-patterning and interconnection required for perovskite solar modules (PSMs).

Conclusion

In this work, we systematically investigated the scalability of iPSCs by isolating the impact of the HTL deposition method across active areas of 0.06, 0.25, and 1 cm² while maintaining an identical device architecture. By employing ALD to fabricate ultrathin, conformal NiO HTLs, scaling-induced efficiency losses were significantly mitigated compared to solution-processed NP and sol-gel NiO counterparts.

ALD-NiO films exhibited superior conformality, electrical homogeneity, and surface wettability on rough FTO substrates, yielding a favourable platform for subsequent perovskite growth. As a result, ALD-based devices demonstrated enhanced J_{SC} retention and the smallest PCE loss upon upscaling, with efficiencies decreasing by only around 2% when increasing the active area from 0.06 to 1 cm². Importantly, V_{OC} remained stable across all device sizes, confirming reproducible fabrication and suppressed non-radiative recombination. FF emerged as the dominant limiting parameter for large-area devices, driven primarily by increasing series resistance and amplified by microstructural non-uniformities. While upscaling losses can also be influenced by factors such as perovskite crystallization kinetics, the concentration of trap-states, and electrode design; our results highlight that interfacial conformality is a critical prerequisite for maintaining performance as area is increased. This underscores the need for simultaneous management of both charge-transport interfaces and large-area film uniformity to bridge the cell-to-module efficiency gap.

To elucidate the physical origins of this behaviour, a 3D model was introduced to quantify the total internal grain boundary area within the perovskite absorber. The model establishes a direct connection between perovskite microstructure and FF deterioration, providing mechanistic insight into how conformal HTLs can suppress scaling-induced losses by promoting larger, more continuous grains. By minimizing internal grain boundary density, ALD-NiO enables devices to more closely approach resistive performance limits imposed by the TCO substrate.

These results demonstrate that ALD-NiO serves as an effective, dopant-free HTL for inverted PSCs, offering precise thickness control, excellent uniformity, and improved upscaling behaviour without the need for additional interlayers or chemical modification. While the absolute efficiencies reported here were intentionally achieved without the use of chemical doping, surface passivation layers, SAMs, or other high-performance interfacial strategies, such approaches are expected to be largely complementary to ALD-based HTL engineering and offer clear pathways to further enhance PCE while retaining favourable scaling behaviour. It is important to note that the NiO/perovskite interface is a recognized site of

potential long-term degradation. Consequently, addressing interfacial chemical stability remains a vital consideration for future studies aimed at improving the operational lifetime of similar device architectures. In addition, the perovskite deposition method itself is known to play a critical role in determining large-area film uniformity and device performance; integration of scalable coating or vapour-based deposition techniques represents an important direction for future work beyond the scope of this study. More broadly, this work provides a mechanistic framework for understanding and mitigating efficiency losses during PSC upscaling, and highlights ALD as a promising route toward robust, scalable perovskite photovoltaics and future tandem solar cell integration.

Experimental section

Substrate preparation

Fluorine-doped tin oxide (FTO) coated glass substrates (Pilkington, TEC8, sheet resistance = 6~9 Ω□⁻¹) were cut into 21 mm x 21 mm pieces and subsequently patterned by wet etching using Zn powder (Aldrich) and 4 M HCl (Duksan Chemical, Republic of Korea). The etched substrates were cleaned sequentially in a four-step ultrasonic bath process for 15 min each, using the following solutions: Hellmanex (2% v/v solution in water), deionized water, acetone, and ethanol. After cleaning, the substrates were dried with nitrogen gas (N₂) and UV-ozone treated for 10 min to remove residual organic contaminants and improve surface wettability.

Nickel Oxide (NiO) Deposition

ALD NiO: NiO was deposited by ALD using a LUCIDA D-100 ALD system (NCD, Republic of Korea). Bis(1-dimethylamino-2-methyl-2-butoxy)nickel (MABON) was used as the Ni precursor, while ozone (O₃), generated from an external ozone generator (Ozone Tech LAB-II, Republic of Korea; generating power = 49%) was used as the oxidizing agent. Carrier gas flow rates were set to 50 sccm for N₂ (purging gas), and 500 sccm for oxygen (O₂). The chamber temperature was kept at 200 °C for the entire duration of deposition. Each ALD cycle consisted of the following sequence: injection of the nickel precursor with a 0.2 s assist pulse, followed by a 2 s main pulse, 1.5 s exposure, and a 10 s N₂ purge. This was followed by oxidizer exposure, consisting of a 2.5 s O₃ pulse, 2.5 s exposure, and a 7 s N₂ purge. Repetition of these cycles yielded a NiO film with an approximate thickness of 6.4 nm. After removal from the ALD chamber, substrates were annealed in a box furnace at 300 °C for 1 h.

Sol-gel NiO: Nickel(II) nitrate hexahydrate (Ni(NO₃)₂ · 6H₂O, 99.999%, Sigma-Aldrich) was dissolved in acetonitrile (ACN, Sigma-Aldrich) at a concentration of 0.1 M, and stirred for 90 min. In a dry box, 100 μL of filtered solution was spin coated at 3000 rpm for 30 s. The spin-coated substrates were soft-baked at 100 °C for 10 min, and then annealed in a box furnace at 300 °C for 1 h, resulting in ~15nm thick NiO film.

NP NiO: NiO NP powder (particle size: ~5nm, 99.999%, Advanced Election Technology Co., Ltd) was dispersed in a mixed solvent



of deionized water (DIW) and isopropyl alcohol (IPA) in a 3:1 volume ratio. The suspension was sonicated to ensure uniform dispersion and prevent nanoparticle aggregation. Following sonication, the solution was filtered to remove any impurities or large aggregates. 100 μL of the filtered solution was spin coated at 5000 rpm for 30 s under ambient conditions. The resulting $\sim 9\text{nm}$ thick film was annealed on a hot plate at 150 $^{\circ}\text{C}$ for 20 min.

Synthesis of Formamidinium Lead Triiodide (FAPbI₃)

Formamidinium lead triiodide (FAPbI₃) powder was synthesized by dissolving 688 mg of formamidinium iodide (FAI, Greatcell Solar) and 1844 mg of PbI₂ (ultradry, 99.999%, Alfa Aesar) in 5 mL of 2-methoxyethanol (anhydrous, 99.8%, Aldrich) under stirring for 90 min. The resulting precursor solution was injected into 50 mL of anisole (anhydrous, 99.7%, Aldrich) preheated to 150 $^{\circ}\text{C}$ to induce retrograde precipitation. The suspension was stirred for 20 min, after which the solid product was collected by vacuum filtration with a Büchner funnel and paper filter. The powder was vacuum-dried to remove residual solvents and subsequently annealed at 150 $^{\circ}\text{C}$ for 30 min to yield black FAPbI₃ powder.

Synthesis of Triple-Cation Perovskite Solution

A 1.45 M perovskite precursor solution with the composition was prepared. The as-prepared FAPbI₃ powder described above (861.1 mg) was mixed with MABr (8.1 mg), PbBr₂ (26.6 mg), PbI₂ (33.4 mg + 33.4 mg excess), CsI (18.8 mg), and MAI (10 mol%, Merck). The precursors were dissolved in 1 mL of a DMF:DMSO (4:1 v/v) solvent mixture (DMF: 99.8% anhydrous, Aldrich; DMSO: $\geq 99.9\%$ anhydrous, Aldrich). The solution was stirred at room temperature for 4 h and filtered through a polytetrafluoroethylene (PTFE, pore size $\approx 0.2\ \mu\text{m}$) membrane before use.

Perovskite Film Deposition

Perovskite films were deposited inside a dry box under controlled humidity and temperature. The prepared perovskite precursor solution was dispensed onto freshly prepared FTO/NiO substrates and spin coated at 5000 rpm for 30 s, with a ramp of 10 s at 1000 rpm/s. During spin coating, 300 μL of chlorobenzene (CB) was dynamically dropped onto the spinning substrate as an antisolvent 20 s after the start of the spin cycle. The resulting films were annealed on a hot plate at 110 $^{\circ}\text{C}$ for 15 min.

C60, BCP & Ag Film Deposition

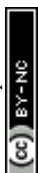
After perovskite deposition, substrates were transferred to a thermal evaporation chamber for sequential deposition of electron transport and buffer layers. C60 (25 nm, Nano-C) and bathocuproine (BCP, 5 nm, Sigma-Aldrich) were deposited under high vacuum ($< 3.0 \times 10^{-6}$ Torr) at a deposition rate of 0.1–0.3 $\text{\AA}/\text{sec}$. Following organic layer deposition, the substrates were moved to a second thermal evaporator chamber where a 100 nm-thick Ag electrode was deposited under high vacuum ($< 3.0 \times 10^{-6}$ Torr), using patterned masks to define active areas of 0.06, 0.25, and 1.0 cm^2 .

Device Characterization

Current-voltage (J–V) measurements were carried out in ambient conditions using a Keithley 2400 source meter under simulated AM 1.5G sunlight at an illumination intensity of one sun (100 mW/cm^2). Solar illumination was provided by an Oriel Sol 3A class AAA solar simulator equipped with a 1600 W xenon lamp (Newport 94083A). The simulator intensity was calibrated using a National Renewable Energy Laboratory (NREL)-calibrated silicon (Si) reference cell with a KG-5 filter. During measurements, the active area was defined by metal shadow masks corresponding to device active areas of 0.06, 0.25, or 1.0 cm^2 . Series (R_s) and shunt resistance (R_{sh}) was simultaneously output with J–V measurements. The thickness of NiO-films was measured by ellipsometry (J.A. Woollam M-2000). Grazing-incidence X-ray diffraction (GIXRD) of NiO was performed at Korea Institute of Science and Technology (KIST) on a D/MAX-2500V (Rigaku) using Cu K α radiation ($\lambda = 1.5406\ \text{\AA}$) at an incidence angle $\alpha = 0.5^{\circ}$. Scans were collected from $2\theta = 30\text{--}80^{\circ}$ with a step size of 0.1° and a counting time of 1 s/step. Steady-state photoluminescence (PL) spectra were measured via FLS-1000 (Edinburgh Instruments). Ultraviolet X-ray photoemission spectroscopy (UPS) was measured via ESCA2 (AXIS SUPRA, KRATOS Analytical Ltd.) with an unfiltered He I (21.22 eV) gas discharge lamp, and Fermi edge calibration was performed with an Ag standard to ensure that all energies were referenced to a common Fermi level (0 eV). Contact angle measurements were performed using a Femtobiomed SmartDrop system. A 3 μL droplet of deionized water was dispensed from a height of 4 μm onto each Glass/FTO/NiO substrate. The droplet profile was recorded by the system's integrated camera, and the contact angle was calculated using the instrument's analysis software. Conductive atomic force microscopy (C-AFM) was employed to obtain simultaneous topographical and current distribution images of the NiO films deposited on Glass/FTO substrates, using an environment-controlled, variable-temperature scanning probe microscopy system (SPA-300HV, Seiko Instruments). Topographical and cross-sectional microstructures of the device layers were captured using field-emission scanning electron microscopy (FESEM, JSM-7600F, JEOL).

Author contributions

A.G. conceived the idea, designed the experiments, fabricated perovskite devices, measured device performance, and characterized thin films. C.W. and U.A. assisted with the fabrication and characterization of devices. C.W. conducted PL measurements. Y.I. conducted SEM measurements. S.H. conducted ellipsometry and C-AFM measurements. C.W., U.A., H.J.J., H.S.J. and H.S. participated in the data analysis and result discussions. A.G. wrote the manuscript with input from H.S. and H.S.J. All authors contributed to the discussion, commented, reviewed and approved of the paper. H.S. provided direction and supervision.



Conflicts of interest

There are no conflicts to declare.

Data availability

All data supporting this article are included in the main article and the supplementary information (SI). Reference 50 is cited in the SI. Additional data can be provided upon request to author(s).

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Data availability

All data supporting this article are included in the main article and the supplementary information (SI). Reference 50 is cited in the SI. Additional data can be provided upon request to author(s).

