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From solar cells to memristors: halide perovskites as a platform for neuromorphic electronics

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Halide perovskites are widely recognized for optoelectronic devices such as photodetectors, photovoltaics, and light emitting diodes. Crucially, their unique characteristic as a mixed ionic-electronic semiconductor has recently positioned them as a highly promising material for neuromorphic computing, which necessitates a dedicated review of this rapidly emerging field. This comprehensive review first correlates the relationship between the perovskite's crystal structure and its resulting optoelectronic and ionic properties, which underpins memristor functionality. We then systematically discuss the figure of merit, operating mechanisms, and characterization techniques for halide perovskite memristors. After critically reviewing the state-of-the-art devices, we analyze the critical gap between lab-scale systems and real-world applications, specifically tackling the challenges of crossbar array implementation and discussing various neuromorphic applications. Finally, we detail an outlook, highlighting persistent hurdles like endurance and stability as well as identifying key research directions, such as high-throughput experimentation and customizing devices based on the necessary trade-off between response time, energy, and retention to realize practical, next-generation neuromorphic hardware.

1. Introduction

Halide perovskites were first synthesized the late 1970s,[1,2] but their incorporation in optoelectronic devices started in 2009 with methylammonium lead iodide ($MAPbI_3$) as photosensitizer in a solar cell.[3] Over the past years, perovskites have come to dominate research in optoelectronic devices such as photovoltaics and light-emitting diodes (LEDs), largely due to their remarkable breakthroughs in efficiency. Their extraordinary optoelectronic properties—such as long carrier diffusion lengths, high optical absorption coefficients, and excellent defect tolerance—along with the ability to easily tune these properties, have made perovskites highly attractive materials.[4] Coupled with the ability to form high-quality films through low-temperature and low-cost solution-based fabrication,[5] these advantages have paved the way for rapidly increasing solar cell efficiencies,[6,7] and facilitated their integration into a wide range of devices, including LEDs,[8] photodetectors,[9] thin film transistors,[10] and memristors be it in flexible or rigid substrates. As with all

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perovskite structures, they adopt the molecular formula of ABX_3. The A-site cation is 12-fold coordinated, while the B-site cation is 6-fold coordinated by X-site anions.[11] In lead–halide perovskites, since the halide forms the anion at the X-site, the A-site has an oxidation state of +1, and the B-site that of +2.

The optoelectronic properties of perovskites can be precisely engineered through strategic compositional modifications, be it on the A-site, B-site, or X-site ions. As the size of the ions need to abide by the Goldschmidt tolerance factor,[12] substituting or partially replacing standard 3D A-site ammonium cations (*i.e.* methylammonium – MA^+, formamidinium – FA^+, cesium – Cs^+) with bulky alkylammonium species like phenyl ammonium (PEA), 1,3-propanediammonium (PDA), *etc.* enables controlled dimensionality reduction. These bulky cations disrupt the 3D BX_6 octahedral network, forming 2D layered structures (*i.e.* $(PEA)_2PbX_4$, $PDAPbX_4$) or quasi-2D phases where isolated 3D regions alternate with organic layers (Fig. 1). Further increasing the bulky cation size triggers the collapse of the 3D perovskite framework into lower-dimensional 1D chain-like assemblies or 0D isolated octahedra (Fig. 1). Following the octahedral factor that govern the ratio between the B-site cation and the X-site cation, replacing or partially substituting the common I^- with other halide ions such as Br^-, and Cl^-, can also be done to further modulate their optoelectronic properties. In addition, B-site metal substitution further expands functionality beyond lead-based systems, such as Sn^{2+}, Sb^{3+}, Ag^+, or Bi^{3+} based perovskite. Thus, this wide range of tunable parameters offers unparalleled opportunities for tailoring perovskite optoelectronic properties to specific applications.

Despite these advantages, halide perovskites are known to suffer from issues related to ionic migration which contributes to the reduced performance of photovoltaic and LED devices. However, this coupling between ionic and electronic transport can be effectively harnessed in memristors, where it enables

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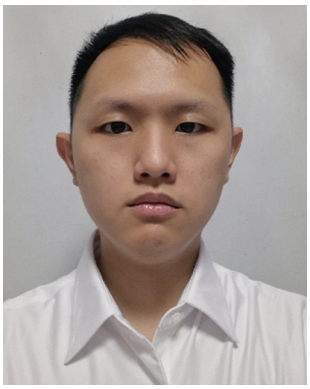

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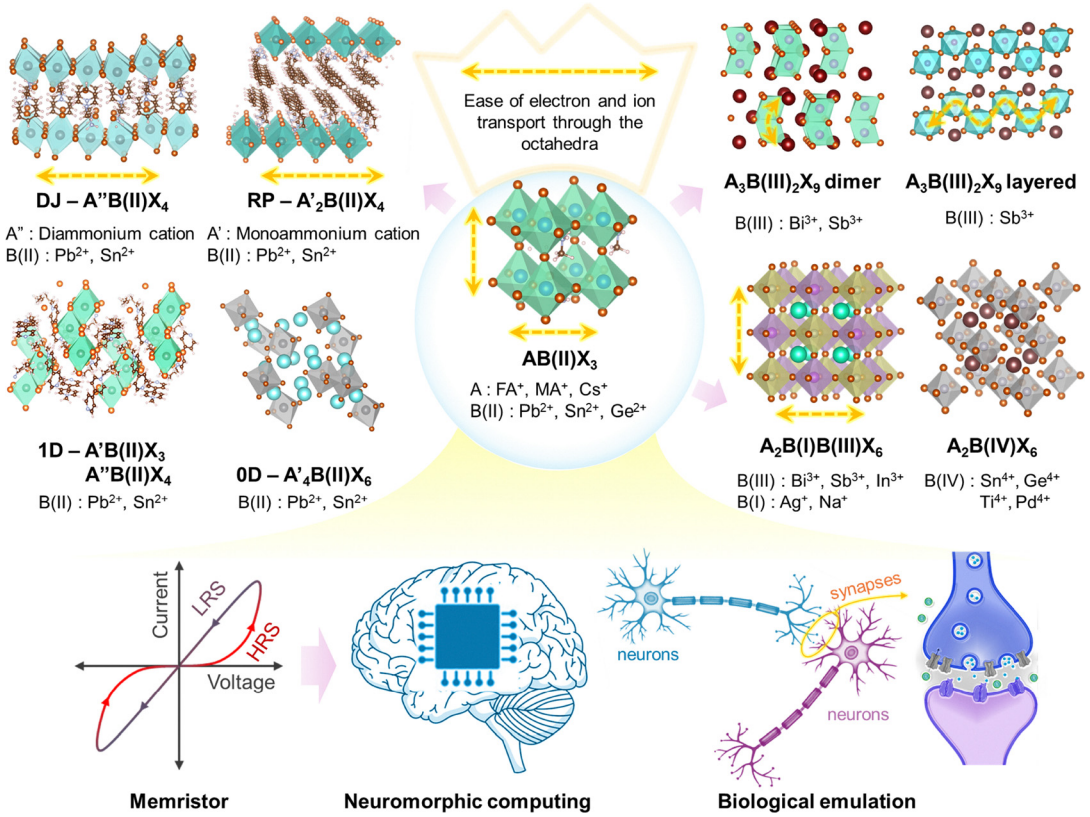

Fig. 1 The various crystal structures of possible perovskite inspired families depending on the choice of A-site, B-site cation, and halide anion (X) together with the implication of its ionic and electronic transport and application in memristor for neuromorphic computing and biological emulation.

unique functionalities. Memristors are resistive memory devices capable of altering their conductance in response to external stimuli such as voltage, current, or light pulses. They can be classified based on their conductance states into digital and analog types. A digital memristor typically switches between two distinct states: a high-resistance state (HRS) and a low-resistance state (LRS), with switching triggered by specific external stimuli. In contrast, an analog memristor operates with a continuous range of conductance states, allowing for gradual changes in response to varying stimuli. This property enables analog memristors to store and process information in a more nuanced manner, making them particularly suitable for neuromorphic computing, where they can mimic synaptic behavior to facilitate complex and efficient information processing. Memristors can also be categorized based on retention time into volatile and non-volatile types. While volatile memristors lose their states when external stimuli is removed, non-volatile memristors, on the other hand, retain their memory state even after external stimuli is removed. The terms "volatile memristor" and "diffusive memristor," as well as "non-volatile" and "drift memristor," are often used interchangeably in scientific literature, but it is important to note they are not entirely equivalent concepts. The terms "volatile" or "non-volatile" describe the device's behavior (the stability of its conductivity state) making them a classification of performance whose underlying physical origins can be diverse. In contrast, "diffusive" or "drift" denotes a specific physical mechanism involving ion migration. Diffusion describes the spontaneous redistribution of mobile species down a concentration gradient (typically results in volatile behavior), while drift describes movement due to an electric field (which generally leads to non-volatility). These mechanisms are merely one possible physical pathways that lead to the observable performance behavior. Regardless of the type, memristor operation relies on changes in conductance caused by the movement of ions or electrical charges within the material, which alters the device's electrical properties.

While reviews of mechanisms and the nature of ion migration in lead–halide perovskites[13,14] and perovskite based memristors have been published,[15–17] this work adopts a novel perspective by aiming to correlate perovskite structural variation (such as cation arrangements, octahedral connectivity, and defect landscapes) to their electronic-ionic coupling and memristor performance metrics (*e.g.*, switching speed, endurance, retention). The effect of deposition techniques, passivation strategy, buffer layer, as well as various device's structure (such as 2 terminals – 2T or 3 terminals – 3T, lateral or vertical) will also be discussed in detail. Building on this foundation, we extend the discussion beyond single-device operation to address the critical challenges of scaling perovskite memristors into functional arrays, including fabrication hurdles (*e.g.*, uniformity, lithography constraints) and system-level limitations (*e.g.* reading or writing errors associated with difficulties in isolating

a single device from the arrays). Additionally, we map these advancements to targeted applications, such as neuromorphic edge computing, reservoir computing, and logic circuits, providing a roadmap to bridge fundamental material insights with real-world technological integration.[14]

In the first section, we review the diverse families of perovskites, focusing on their structural characteristics, as well as their electronic and ionic conductivity. Understanding the interplay between ionic and electronic properties is essential, as this coupling forms the foundation of memristor operation. Following this, we delve into the key performance metrics and the current state-of-the-art in perovskite memristor technology. The next section explores the various mechanisms underlying perovskite memristors, be it in 2T or 3T configurations, along with the characterization methods—such as electrical, other spectroscopic, and simulation techniques—used to investigate and validate these mechanisms. This discussion provides the fundamental knowledge necessary for improving the performance of perovskite memristors. We also discuss a range of processing parameters that influenced memristor behavior such as type of substrates, device configurations, or deposition techniques as well as strategies for optimizing device performance at the single-device level, including compositional engineering, defect management, and interface design. The subsequent section addresses the challenges associated with scaling up to memristor arrays, considering both fabrication issues—such as achieving device uniformity and lithography steps—and system-level integration challenges, including minimizing IR drops, crosstalk, and sneak path issue. Finally, we provide an in-depth review of the various applications of perovskite memristors, covering both volatile and non-volatile devices. This includes their use in neuromorphic computing, reservoir computing, and edge sensing for volatile devices, as well as analog in-memory computing and programmable logic for non-volatile devices. Through this comprehensive overview, we aim to equip readers with a solid understanding of the fundamental principles, challenges, and opportunities in the field of halide perovskite memristors.

2. Correlating crystal structure to ionic and electronic properties

Aside from being a good optoelectronically active semiconductor for photovoltaics and LEDs, halide perovskites exhibit exceptional memristive behavior due to their unique mixed ionic-electronic conductivity and tunable ion migration dynamics. The inherent defects in perovskite crystals, such as halide vacancies (*e.g.*, iodine vacancies V_I^+), facilitate rapid ion migration under applied electric fields, allowing precise modulation of resistance states through the formation and rupture of conductive filaments or self-doping which will described further in Section 3. While being labelled as a perpetrator for performance degradation in perovskite photovoltaics, and light emitting diodes, the defect-mediated ion mobility can contribute to low operating voltages and ultrahigh switching speeds in memristors, critical for energy-efficient neuromorphic computing and artificial synapses.

This section will explore the diverse structural configurations of perovskite materials that can be tailored for memristor applications, emphasizing their design principles and functional advantages. The analysis begins with an examination of 3D perovskite lattices, focusing on their intrinsic hysteresis behavior and ion migration dynamics—key mechanisms underpinning resistive switching phenomena. Building on this foundation, the discussion transitions to low-dimensional perovskite variants (*e.g.*, 2D layered or quasi-2D structures, 1D, and 0D perovskite), which offer enhanced stability and tunable electronic-ionic transport properties. Finally, the section addresses lead-free perovskites and perovskite-derived materials, highlighting their potential to mitigate toxicity concerns while retaining memristive functionality. By systematically linking structural features to ionic migration properties, this section provides a comprehensive framework for advancing perovskite memristor technologies.

2.1. Three dimensional perovskites

2.1.1. Crystal structures and optoelectronic properties. To date, the most widely studied lead–halide perovskites are three-dimensional (3D) structures featuring interconnected $[PbX_6]^{4-}$ octahedra networks, which enable good charge-carrier mobility. These materials adopt a cubic or pseudocubic crystal symmetry with the general formula ABX_3 (Fig. 2a). The A-site is typically occupied by MA^+, FA^+, or Cs^+ cations, which exhibit tolerance factors of 0.90, 0.99,[18] and 0.805[19] respectively when X^- is the iodide anion. However, $FAPbI_3$ and $CsPbI_3$ lie at the edges of the perovskite stability window (tolerance factor range: 0.80 to 1.00), and as a result, they tend to form other thermodynamically favorable, non-perovskite phases under ambient conditions. $FAPbI_3$ and $CsPbI_3$ usually exists in a 1D structure,[20,21] with $[PbI_6]^{4-}$ chains surrounded by the respective A-site cations (Fig. 2a). However, by processing these materials at elevated temperatures-beyond the phase transition point to the perovskite phase-and then rapidly quenching them, it is possible to preserve the perovskite phase at room temperature. Even so, such perovskites often exhibit distortions from ideal cubic (α) symmetry, resulting in phases such as tetragonal (β), orthorhombic (γ), or the non-perovskitic δ-phase.[22] Meanwhile, the MA^+ cation, with a tolerance factor slightly below the ideal value of 1.00, stabilizes $MAPbI_3$ in a tetragonal structure at room temperature. This tetragonal phase can be viewed as a cubic lattice that is distorted along the *c*-axis.

The electronic properties of these materials are mainly dictated by the orbitals from the B-site and X-site ions – the $[PbX_6]^{4-}$ lattice that surrounds the A-site cations. Density Functional Theory (DFT) calculations indicated that the highest occupied molecular orbital – HOMO (valence band minimum – VBM) has contributions by the B-site s orbitals and X-site p orbitals, whereas the lowest occupied molecular orbital – LUMO (conduction band maximum – CBM) mainly has contributions from the p orbitals of the B-site cation and X-site p orbitals (Fig. 2b).[23,24] This may suggest that the choice of A-site cation does not affect the resulting bandgap of the perovskite.

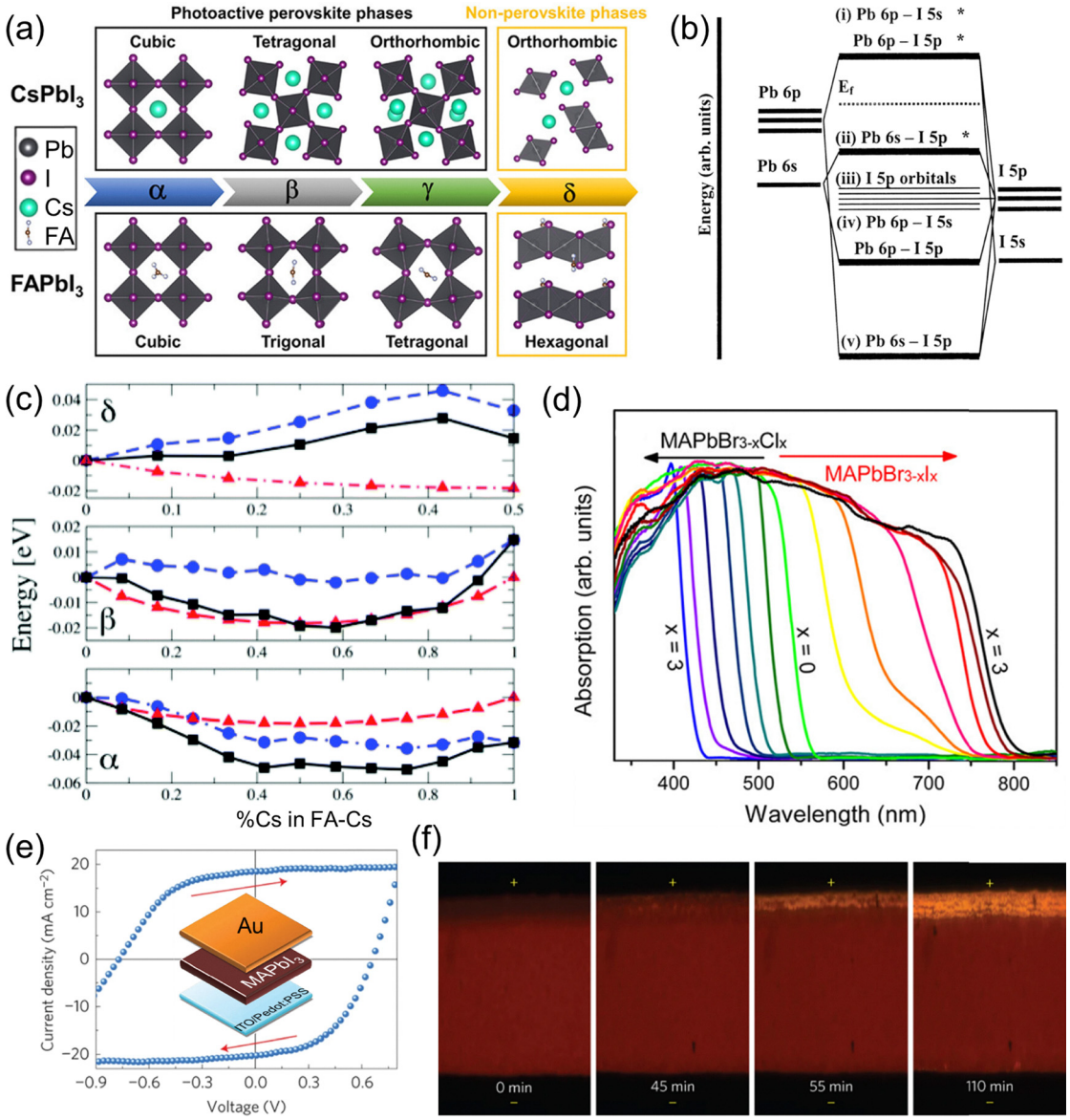

Fig. 2 (a) Structure of α-phase, β-phase, γ-phase, and δ-phase for $FAPbI_3$ and $CsPbI_3$. Reprinted with permission from ref. 33. Copyright 2021 American Chemical Society. (b) The molecular orbitals from the Pb–I lattice. Note that the HOMO is a filled antibonding orbital, which gives rise to its unique defect tolerant properties, although this weakens the Pb–I bond as well, leading to ease of formation of defects. Reproduced from ref. 24 with permission from AIP Publishing, Copyright 2016. (c) Internal energy (blue, ΔE), entropic contributions ($-T\Delta S$), free energy ($\Delta E - T\Delta S$) calculations for the mixed $Cs_xFA_{1-x}PbI_3$ perovskite. Reproduced from ref. 25 with permission from Royal Society of Chemistry, Copyright 2016. (d) The change of absorption spectra of $MAPbBr_{3-x}Cl_x$ and $MAPbBr_{3-x}I_x$ films. Reprinted with permission from ref. 30. Copyright 2015 American Chemical Society. (e) The observed photocurrent hysteresis from a $MAPbI_3$ device (shown in inset) under continuous current sweeping together with (f) the *in situ* video imaging of perovskite during electric field application (~1.2 V μm^{-1}), highlighting ion drift from anode with electrical poling. Reproduced from ref. 34 with permission from Springer Nature, Copyright 2015.

However, the size of the A-site cation causes distortions to the $[PbI_6]^{4-}$ lattice, which alters the degree of orbital overlaps, thereby changing the bandgap of the perovskite slightly. As a result, $CsPbI_3$ exhibits the largest theoretical bandgap of 1.71 eV, followed by $MAPbI_3$ (1.58 eV), and $FAPbI_3$ (1.48 eV).[18]

To further tailor the tolerance factor within the Goldschmidt requirement, mixed-cation strategies – such as combining the larger FA^+ cation with smaller cations like MA^+ or Cs^+-have been employed. This approach generates hybrid perovskites like FA–MA, Cs–FA, and Cs–MA–FA compositions. In solar cells, these mixed-cation systems enhance photovoltaic performance by tuning bandgaps between those of pure perovskites while retaining structural stability. The increased entropy of mixed cations acts as a stabilizing force compared to their pure counterparts.[25] This entropy-driven stabilization prevents a conversion back into undesirable non-perovskitic phases (Fig. 2c).

Beyond iodide, the X^- site in perovskites can also accommodate other halides like bromide (Br^-) or chloride (Cl^-). Bromide-based perovskites exhibit larger bandgaps (in the visible range) that are employed in LED-based applications.[26]

Unlike their iodide counterparts, $FAPbBr_3$[27] and $CsPbBr_3$[28] are stable in their perovskite phases. The A-site cations can also be mixed. Various ratios of Br/I mixing are also possible, giving rise to a much larger variation in bandgaps[29,30] that can allow for larger tunability in the wavelength for light emission in LED applications (Fig. 2d). Finally, chloride-based perovskites are also possible and have been investigated, where their bandgaps are far larger than the bromide-based ones. The larger bandgaps however cause the conductivity to be lower, and chloride-based perovskites can form deeper defects that is detrimental to device performance.[31] As a result, research on Cl^- based perovskites are fewer, with more focus on quantum dots, although it is notable that Cl^- was also used as one of the X-site ions in a recent solar cell paper.[32]

2.1.2. Ionic migration in 3D perovskites. Ionic migration is key for the viability of halide perovskites in neuromorphic applications. Ion migration in perovskite-based devices was first reported by Xiao *et al.*,[34] who demonstrated switchable photovoltaic effects in symmetrical perovskite devices through electric field poling (Fig. 2e). The hysteresis in current–voltage (*I–V*) behavior was linked to electric field induced ionic motion as observed from *in situ* video imaging (Fig. 2f). This hysteresis is dependent on both scan rate and scan speed,[35] highlighting possible ionic movement. Memristors exploit this current hysteresis, where an electrical bias or another external trigger can be used to tune the conductance state of the device.

In this section, we review current literature uncovering the origins of fast ionic motion in halide perovskites and the various types of mobile ions involved. These ionic movements are categorized into two groups: intrinsic (ions native to the perovskite lattice, such as halides or organic cations) and extrinsic (ions introduced externally, *e.g.*, metal ions from electrodes or dopants). We also examine factors influencing ion migration rates—such as light, moisture, and other external stimuli. This understanding is critical, as it provides a foundation for materials engineering strategies to tailor perovskite memristors with enhanced performance.

2.1.2.1. Intrinsic ion migration. Notably, fast ionic migration in halide perovskites arises from their exceptionally low defect formation energies (DFE) and minimal activation barriers (E_A) for ion transport, which collectively enable dynamic lattice rearrangements.[36] These ionic movements stem from the presence of defects within the perovskite structure, which includes site vacancies (V_A, V_B, V_X), interstitial occupations (A_i, B_i, X_i), and anti-sites (X_A, X_B, A_X, A_B, B_A, B_X). The DFEs for various defects in lead–halide perovskites are often low (refer to Table 1 below) leading to shallow defects – defects that are very close to the conduction/valence band edge. This may be attributed to the lower oxidation states of the A, B, and X ions in a lead–halide perovskite system, which lowers the electrostatic potential of the lattice sites, compared to standard oxide perovskites.[37] Knowledge of the DFE as well as the activation energy for defect migration is necessary in order to modulate the overall ionic migration in the perovskite film. While E_A can be obtained experimentally, DFE is rarely measured experimentally because defects are often dilute and difficult to isolate precisely. Hence, DFE is often derived from first-principle calculations. First-principles calculations use methods like density functional theory (DFT), which relies on functionals to model the exchange-correlational energy. Various functionals exist such as the Perdew–Burke–Ernzerhof (PBE)[38] and Heyd–Scuseria–Ernzerhof (HSE).[39] In addition, the large electron cloud of Pb mean that relativistic effects need to be considered – spin–orbit coupling (SOC). A wide range of DFE values have been reported even for a single perovskite, attributable to the differing functionals and relativistic effect considerations employed in DFT calculations (Table 1). A wide range of E_A have also been reported due to variations in measurement and processing conditions. A comprehensive compilation of DFEs and activation energies from different papers is summarized Table 1.

The calculated DFE of perovskite also varies depending on the synthesis condition (*i.e.* iodide-rich, moderate, or iodide-poor conditions).[40] DFT calculations indicate that all antisite defects except MA_{Pb} have high DFE, making vacancies and interstitials the primary defects of interest. However, defect formation energy differs from the activation energy required for defect migration – a critical distinction when evaluating ionic mobility.[51] For example, the DFE of V_{Pb} in $MAPbI_3$ is calculated to be low since the Pb 6s and I 5p, which forms an antibonding valence band maximum state,[24] is fully occupied (Fig. 2b), which increases the ease of breaking the Pb and I bond to form vacancies due to the unfavorable s–p coupling.[40] A differing account by Yang *et al.*[52] discussed that the filling of these antibonding VBM causes the material to have a large dielectric constant, which screens the defects from the electrostatic potential from the perovskite crystal lattice, and hence the formation energies of the defects are lower, which may result in lower diffusion barriers. Yet, Eames *et al.*[43] have calculated the E_A required for migration of the Pb^{2+} to occur to be around 2.31 eV, and therefore while V_{Pb} forms easily, these are unlikely to be responsible for the ion migration observed in the perovskite.[53] The high diffusion barriers for Pb mean that these defects are unlikely to contribute to intrinsic ion migration, which restricts the discussions to A-site and X-site defects. However, in the case of Sn-based perovskites, the presence of Sn vacancies inhibits the ionic migration of V_I and

Table 1 A list of common 3D lead–halide perovskites and their respective ranges of DFEs and E_A. Table adapted from ref. 36

Perovskite	Defect type	DFE range (eV)	E_A range (eV)
$MAPbI_3$	V_I	0.13–1.87[40,41]	0.08–0.58[41–46]
$MAPbI_3$	V_{MA}	—	0.46–1.14[41–43,45,46]
$MAPbI_3$	V_{Pb}	—	0.80–2.31[41–43]
$MAPbI_3$	I_i	0.23–1.42[40]	0.08–0.24[42,44]
$MAPbBr_3$	V_{Br}	—	0.09[42]
$MAPbBr_3$	V_{MA}	—	0.56[42]
$FAPbI_3$	I_i	0.60–1.66[47]	—
$FAPbI_3$	V_{FA}	0.14–1.09[47]	0.61[45]
$FAPbI_3$	V_I	0.15–1.69[41,47,48]	0.16–0.75[41,45,48]
$FAPbI_3$	V_{Pb}	—	>1.20[41]
$CsPbI_3$	V_I	0.69[41]	0.21–0.36[41,49]
$CsPbI_3$	V_{Pb}	—	1.40[41]
$CsPbBr_3$	V_{Br}	1.32–2.67[50]	0.35[49]
$CsPbBr_3$	V_{Cs}	0.20–1.80[50]	—
$CsPbCl_3$	V_{Cl}	—	0.35[49]

thus the B-site defects may contribute to the overall ionic migration picture.[54]

The following subsection dives into the migration of A-site and X-site ions *via* defects. While generally accepted that the X-site motion dominates the ionic migration, followed by the A-site, Table 1 above shows the large overlap in the DFEs and E_A values. However, the lowest reported values for each of the defect corroborates the observation that X-site defects dominate the ionic migration. For example, in the case of $MAPbI_3$, V_I and I_i has the lowest reported E_A (0.08 eV), as compared to defects from the V_{MA} (0.46 eV) and V_{Pb} (0.80 eV). These values, however, can be modulated by changing or alloying the perovskite with more A-site, B-site or X-site ions, and thus the next section discusses the impact of different ions on the ionic migration within the perovskite structure.

2.1.2.1.1. A-Site cation engineering. In general, the migration of A-site defects depends on two factors – the size of the A-site cation, and the interaction between the A-site and the rest of the lattice. Although the A-site cations do not largely affect the band structure, the ionic migration within the perovskite can be tuned *via* A-site cation engineering. A combination of cations (*e.g.* MA^+, FA^+, Rb^+) can potentially slow down ionic migration, a strategy used for hysteresis-free perovskite solar cells,[55] opening a way to modulate ionic conductivity to tune memristor performances.

One example of the size effect is the MA_i defect. The MA_i defect has low formation energy due to the weak coupling between the MA^+ molecule and the $[PbI_6]^{4-}$ lattice.[40] However, Eames *et al.*[43] dismissed the possibility of interstitial migrations due to the close-packed nature of the perovskite lattice, claiming that interstitial migrations have not been observed in oxide and halide perovskites. On the other hand, DFT simulations showed that MA_i moves by expelling lattice MA_{MA}, which in turn becomes a new MA_i defect (Fig. 3a).[52] Their calculation reveals that MA_i is more mobile (E_A = 0.38–0.48 eV) than V_{MA} (E_A = 0.62–0.89 eV), but the higher formation energy means that MA^+ is unlikely to contribute to ion migration. Yet, the MA^+ cation was experimentally shown to have moved under light illumination[53] using ToF-SIMS to estimate the lateral concentration of MA^+

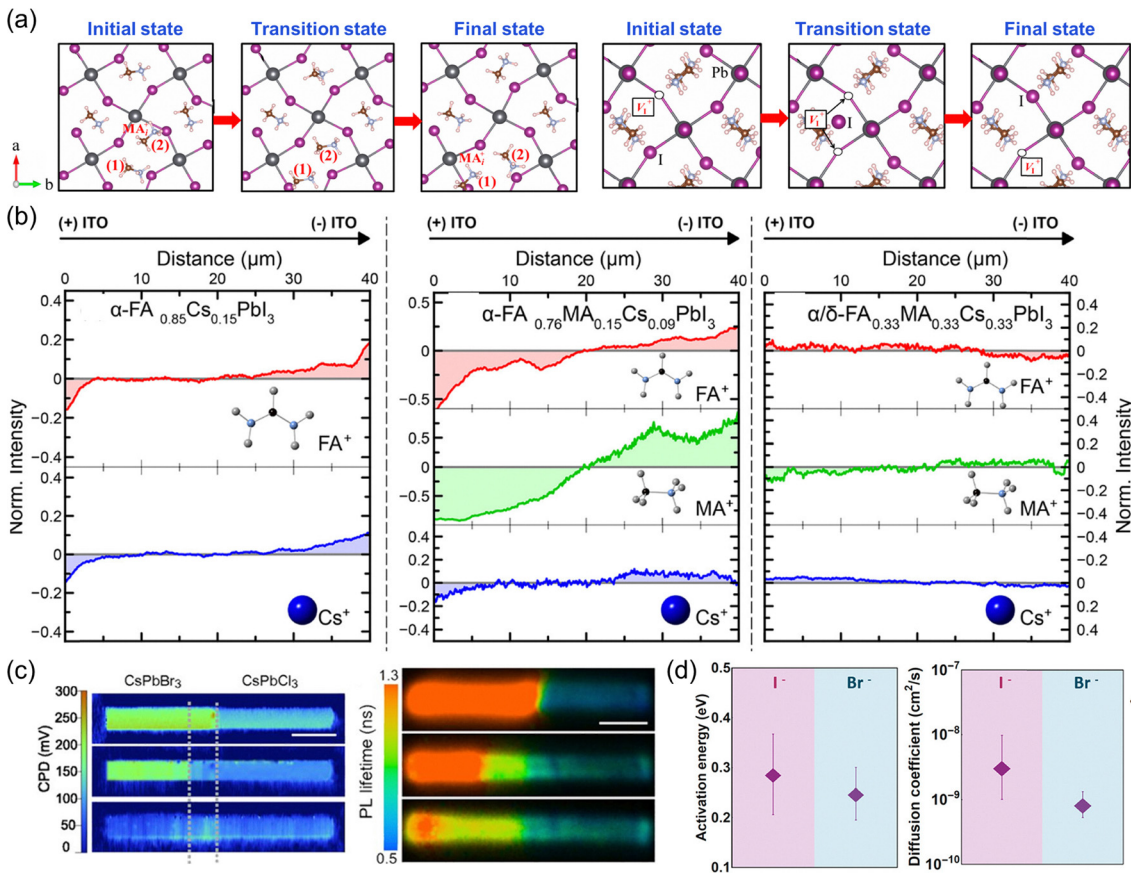

Fig. 3 (a) DFT calculations of the possible migration of MA_i (left) and V_I (right) in the perovskite lattice. Reprinted with permission from ref. 52. Copyright 2016 American Chemical Society. (b) Averaged ToF-SIMS intensity profiles for lateral devices of $FA_{0.85}Cs_{0.15}PbI_3$, $FA_{0.76}MA_{0.15}Cs_{0.09}PbI_3$, and α/δ-$FA_{0.33}MA_{0.33}Cs_{0.33}PbI_3$, shown before (gray lines) and after bias application—highlighting the migration of FA^+ (red), MA^+ (green), and Cs^+ (blue) ions. Reprinted with permission from ref. 61. Copyright 2020 American Chemical Society. (c) Contact potential difference – CPD and photoluminescence lifetime of $CsPbCl_3$–$CsPbBr_3$ nanowire at 100C for 0 h (top), 1.5 h (middle), and 5 h (bottom) – highlighting the anion interdiffusivity. Reproduced with permission from ref. 64, Copyright 2018 National Academy of Sciences. (d) TID measurements highlighting lower activation energy and diffusion coefficient in $MAPbBr_3$ as compared to $MAPbI_3$ at 300 K. Reprinted with permission from ref. 56. Copyright 2016 American Chemical Society.

cation in the film. This was the case for both $MAPbI_3$ and $MAPbBr_3$ samples. However, transient-ion drift revealed that MA^+ does not migrate for $MAPbBr_3$, which stands in direct contrast with the previous report.[56] This suggests that the movement of the A-site ions is not well understood and varies depending on the perovskite structure as well as fabrication process and measurement. Yet they can play a crucial role in determining the amount of hysteresis (or resistance switching) in the material. The possibility of other external factors, such as photodegradation, which may potentially cause MA^+ to move and leave the perovskite film, will also need to be considered.[57]

The FA^+ cation is much larger, and the increased steric hindrance drastically slows down FA^+ migration in pure FA-based perovskites as well as FA-MA mixed perovskites, as indicated *via* the open-circuit voltage buildup method.[58] A third commonly-used A-site cation is Cs^+, which was calculated to require an activation energy of ~0.5 eV in the equatorial direction of the unit cell, and ~1.16 eV in the axial direction of the unit cell.[59] Cs^+ has a lower Goldschmidt tolerance factor, and its radius is smaller than MA^+, and thus it has a higher probability of migration. John *et al.*[60] have calculated the activation energies for V_{FA}^- to be 0.61 eV, V_{Cs}^- to be 0.32 eV, and V_{MA}^- at 0.56 eV in accordance with the trend of the sizes of the A-site cations. This trend was also observed in memristors built from $MAPbBr_3$, $FAPbBr_3$, and $CsPbBr_3$, showing a one-to-one correspondence between the activation energy for migration and the memristor device performance (*i.e.* retention time, which will be elaborated further in subsequent section). In a mixed cation perovskite system, ToF-SIMS data indicated that while all cations are mobile, cation ionic migration could be modulated by varying the α/δ phase ratio on the film (Fig. 3b).[61]

2.1.2.1.2. X-site defects. In the case of X-site defects, the halide vacancy (V_x^+; *e.g.* V_I^+) is often implicated in many papers as the defect most responsible for ionic migration, rather than the halide interstitial (X_i^-, *e.g.* Br_i^-). For iodide-based perovskites, V_I has low DFE since CBM mainly has contributions from the Pb 6p orbitals rather than the iodide,[62] suggesting a weak covalent bond and easing the formation of V_I.[40] However, the E_A for V_I^+ migration is low as well, with calculated E_A to be around 0.58 eV.[43] The movement of iodide vacancies is due to a rotation of the Pb–I bond (Fig. 3a).[52] Other reports showed that E_A of $MAPbI_3$ is only 0.3 eV, which is similar to fast-ion conductors.[45] The calculated E_A values tend to vary depending on the calculation methods.[43,45] Experimentally, activation energy for iodide migration was measured to be around 0.16–0.39 eV, based on several different devices.[63] Using transient-ion drift, both iodide and MA^+ migration can be distinguished as well. For the other halide vacancies, Cl^- and Br^- migration were assumed to be faster due to their smaller sizes, but these activation energies were not calculated.

Another study unveiled vacancy-hopping of X-sites in a $CsPbCl_3$–$CsPbBr_3$ nanowire, where $CsPbCl_3$ was observed to have higher diffusivity due to larger vacancy concentrations (Fig. 3c).[64] Thus, the soft $[PbI_6]^{4-}$ lattice allows for defects to form easily, and these defects then play a role in memristors. However, the trends that govern the mobility of these X-site defects are not trivial. For example, in comparing $MAPbBr_3$ with $MAPbI_3$, although Br^- is more likely to bind to the Pb^{2+}-strongly, experimental results show that the activation energy for migration of Br^- is actually lower than I^-, which they attributed to reduced steric hindrance due to the smaller radius of the Br^- ion as compared to the I^- ion in $MAPbI_3$ (Fig. 3d).[56]

In the case of iodide interstitials, Yang *et al.* showed *via* DFT simulations that the I_i^- defect is latched to a I_I lattice site, and simply moves from one I_I to another while migration.[52] However, their higher DFE meant that these interstitial defects are unlikely to contribute to the observed ion migration, and therefore the general consensus amongst most papers are that the halide vacancies are the major components migrating within the film.

These discussions on the various defects and their migration emphasize the importance of defect chemistry and physics in perovskites. These defects are not neutral and will naturally induce doping in halide perovskites. Depending on their DFE as well as E_A, these defects can migrate and ultimately modulate the electronic properties of the perovskite. This behavior forms the basis for creating resistive switching devices, which will be discussed further in Section 3.

2.1.2.2. Extrinsic ion migration. Aside from intrinsic (native) defects migrations, extrinsic ions are also mobile in the perovskite structure. The movement of extrinsic metal ions, such as Ag^+ and Au^+, triggered by an electric field from the electrode region, has also been observed in halide perovskites solar cells and perovskite FETs (Fig. 4a).[65–69] In memristors, perovskite materials are typically integrated with electrodes and optional buffer layers in between. These electrodes often interact chemically or electrically with the perovskite – a critical process that governs conductive filament formation that modulate the overall resistance of a device – which will be discussed further in Section 3.

Usually, extrinsic metal ions enter the interstitial sites in the perovskite.[70] Table 2 shows a list of DFEs and activation energies for each extrinsic metal ion defect in $MAPbI_3$.[36,70] It is notable that some of the DFEs are negative – implying that the incorporation of metal ions (*e.g.* Ag_i^+ or Au_i^+) is thermodynamically favored. The activation energies, meanwhile, are within the range of E_A of V_I^+ and V_{Br}^+, and this suggests that these metals will play a large role in determining the memristive characteristics of a device that incorporates these metals as electrodes. Other studies[52] have also shown that Au has a tendency to form Au^+ interstitials bonded to two lattice iodide ions, with E_A of ~0.3 eV (Fig. 4b). Beyond metal ions from electrode region, the perovskite structure also allows the migration of other smaller metal ions species such as Li^+. Migration of Li^+ through perovskite layer from Spiro-OMeTAD layer (which act as hole transport layer) have been observed (Fig. 4c).[71] However, most of these studies do not provide an experimental value of the activation energy of the migration, but instead provide a qualitative comparison of the overall ionic migration. These studies are complicated by the fact that the presence of these extrinsic ions affect the migration of other species (V_I^+) in the perovskite, Many studies in perovskite solar cell literature introduce metal ions (Li^+,[72–74] Na^+,[73,75] K^+,[73,76–78]

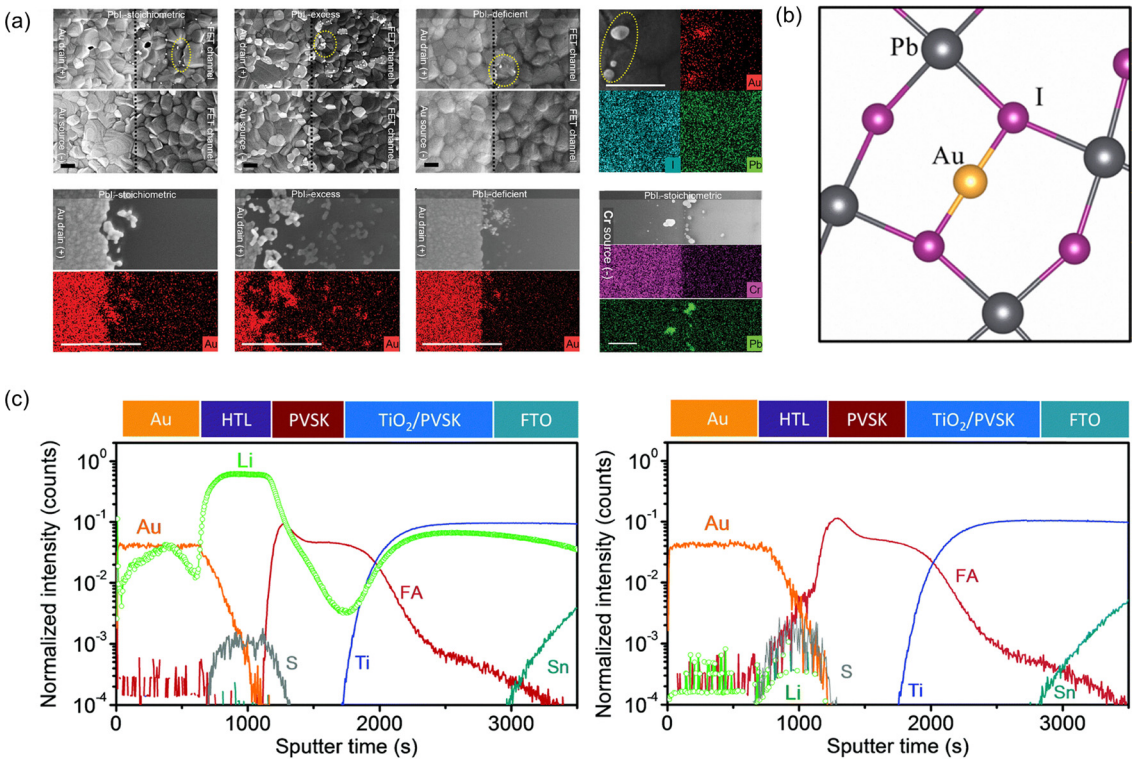

Fig. 4 (a) SEM-EDX images of the formation of gold clusters from a gold drain electrode in perovskite FETs. A comparison was made across perovskite films with varying stoichiometries to observe the effect of stoichiometry on the gold migration within perovskite. The bottom right image shows a different electrode material (chromium) which does not undergo the same migration.[69] (b) DFT simulations of the possibility of Au^+ migrating inside the perovskite layer. Reprinted with permission from ref. 52 Copyright 2016 American Chemical Society. (c) ToF-SIMS revealing the migration of Li^+ inside the perovskite layer from the Spiro-OMeTAD layer (left) and a Li-free control (right). Reproduced from ref. 71 with permission from Royal Society of Chemistry, Copyright 2017.

Table 2 List of DFEs and E_A of various extrinsic ion defects in $MAPbI_3$. Data from ref. 36 and 70

Perovskite	Defect type	DFE (eV)	E_A (eV)
$MAPbI_3$	Mo_i^{2+}	1.37	0.85
$MAPbI_3$	W_i^{2+}	2.45	0.85
$MAPbI_3$	Ag_i^+	−0.65	0.27
$MAPbI_3$	Au_i^+	−0.17	0.42
$MAPbI_3$	Co_i^+	0.51	0.37
$MAPbI_3$	Cr_i^{2+}	−0.40	0.83
$MAPbI_3$	Cu_i^+	−0.46	0.42
$MAPbI_3$	Ni_i^+	0.21	0.29
$MAPbI_3$	Pd_i^0	−0.35	0.40

Yb^{3+},[79] Nd^{3+},[80] Zn^{2+} [81] *etc.*), and they show a reduction in overall ionic migration, that led to improved stability and device efficiency.

Another complicating factor is whether these ions exist as free ions in the perovskite. Conflicting reports on where the metal ions (*e.g.* K^+) are incorporated into exist in literature –Son *et al.* employed atomistic simulations to show that the presence of K^+ in the interstitial sites prevent the formation of iodide Frenkel defect.[77] On the other hand, Kubicki *et al.* showed that potassium iodide (KI), added to introduce the metal ion, does not dissociate, and instead remains as a compound in the grain boundaries.[78] Therefore, the incorporation of extrinsic metal cations in the perovskite *via* metal salts is nontrivial. However, they appear to have a similar effect of reducing ionic migration.

2.1.2.3. Environmental effects on the ionic transport rate of perovskite. Fast ionic (defect) migration is essential for perovskite memristors, however, uncontrolled defect migration can also lead to device degradation issues. Although intrinsic defects (*e.g.* V_I^+) are said to be shallow[40] and benign, the moving ions introduce chemical and phase instability in the material. This is usually exacerbated by environmental factors, such as exposure to oxygen, light, heat, and moisture. Therefore, a clear understanding of how environmental factors and stress affect the perovskite's ion migration rate is essential.

Not limited to single halide perovskite system, ionic migration has also been observed in mixed-halide perovskites (usually I^- and Br^-). In fact, lower E_A have been reported in $MAPb(Br_xI_{1-x})_3$ system by McGovern *et al.*[82] He posit that the solubility differences between the iodide and bromide ions cause an increase in heterogeneous nucleation, leading to films with lower crystallinities and therefore inducing more anionic vacancies. Light exposure induces phase segregation in mixed halide perovskite and consequently reversible switching between two luminance states with low energy consumption in optical memristor applications (Fig. 5a).[83] The mechanism behind this effect is still not yet ascertained, and there are several theories, including surface

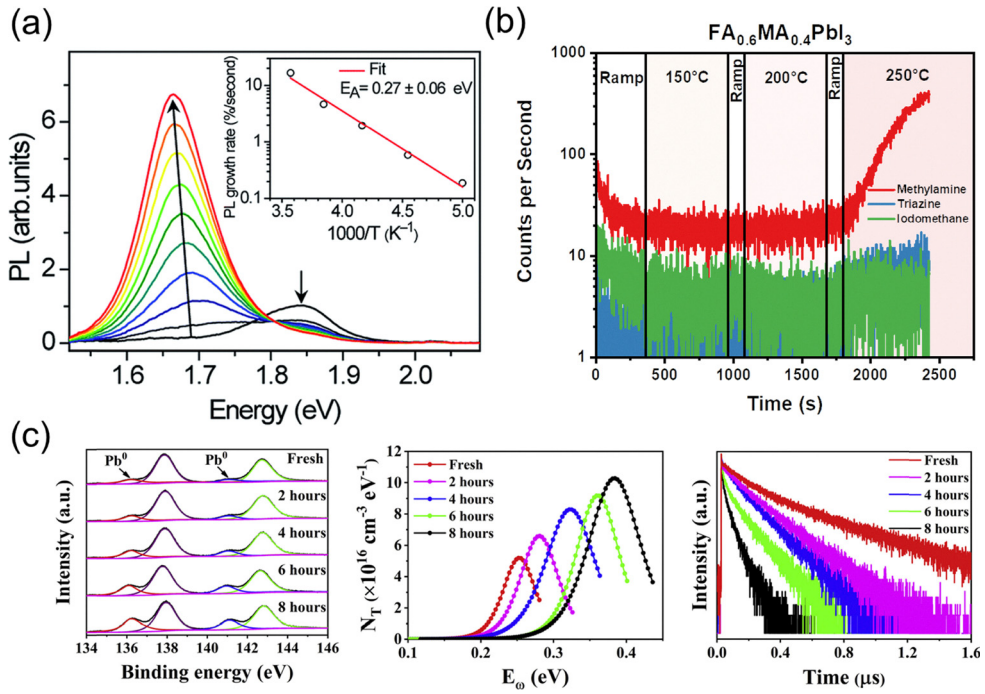

Fig. 5 (a) Change in bandgap over time for $MAPbI_xBr_{3-x}$ films, showing the eventual convergence towards lower bandgaps. This suggests phase segregation into iodide and bromide-rich regions upon light illumination. Reproduced from ref. 83 with permission from Royal Society of Chemistry. (b) Proton-transfer-reaction time-of-flight mass spectrometry measurements of the gaseous byproducts released during the thermal degradation of a mixed FA-MA cation perovskite, showing the volatility of MA^+. Reproduced from ref. 92 with permission from John Wiley and Sons, Copyright 2024. (c) The formation of Pb clusters upon light exposure as revealed by XPS, and the corresponding effects on longevity of charge carriers and defect density. Reprinted from ref. 94, Copyright 2022 with permission from Elsevier.

carrier-induced,[84] polaron-induced[85] the presence of two local wells in the excited state under light illumination,[86] or simply the fact that mixed-halide high entropy state is not stable to begin with, and light triggers spinodal decomposition.[87] What is known, however, is that the phase segregation can only occur because the halide anions are migrating. This means that, when considering using mixed-halide systems, this light-induced phase segregation phenomenon must be addressed by other means.

Aside from triggering phase segregation in mixed halide system, light illumination simultaneously modulates ionic transport. In $MAPbX_3$ system, light exposure suppresses bias-driven halide ion movement, but enhances MA^+ cation mobility, establishing MA^+ as the dominant migrating species under photoexcitation.[53] Light illumination also enhances ionic concentration in mixed halide system ($(MAPb(Br_xI_{1-x})_3)$).[82] Furthermore, light can also induce lattice softening, which weakens the bond and reduces the activation energy for ionic migration.[88] This halide ion transport modulation can be harnessed to either modulate, dissolve, or form a conductive filament, a key mechanism for resistive switching and will be discussed further in Sections 3.1.5 and 3.2.1.[89,90]

According to the Arrhenius equation, temperature plays a pivotal role in determining the ionic migration rates in halide perovskites, with higher temperatures leading to increased rates of ion migration. In addition, MA^+ cations in particular are not stable under high temperatures or when exposed to moisture. Their propensity to deprotonate and leave as methylamine gas under light and/or thermal stress (Fig. 5b) causes the eventual formation of PbI_2,[91,92] which is non-conductive in nature. This could be problematic in any optoelectronic devices, as Joule heating cannot be avoided during the device operation,[93] it triggers the escape of MA^+ ion and alters the device performance over time. The formation of PbI_2 also means that the memristor may drift overtime which is not favorable. Current strategies to mitigate this is to replace the MA^+ cation with a more thermally-stable cation such as FA^+ and Cs^+,[93] although this inevitably reduces the number of ions available for migration in the perovskite.

The Pb^{2+} site, while not directly participating in ionic migration in general, is not immune to instability issues either. X-ray photoelectron spectroscopy (XPS) studies of lead–halide films exposed to light show the photoconversion of Pb^{2+} to Pb^0 metal (Fig. 5c). The presence of the Pb metal itself can cause charge carrier recombination, which results in a drastic drop in performance.[94] The formation of Pb metal is caused by iodide lattice sites interacting with iodide interstitials, forming I_2 that leaves the perovskite, along with unpaired electrons which is then transferred to the Pb^{2+}, thereby reducing it to Pb metal.[94–96] Hence, the instability of the Pb^{2+} is tied to the instability of the iodide ion itself. Lead bromide undergoes a similar reaction,[97,98] and hence this issue is not unique to iodide-based perovskites. Unfortunately, the strategies for preventing lead formation are tied to passivation of the X-site defects. Hence, a balance between fast and slow halide ion migration rates is critical to achieving optimal memristor performance and long-term stability.

In the presence of moisture, a higher rate of MA^+ ion migration has been observed.[99] Moisture induces the formation of hydrated perovskite phases, with lower activation energies for ionic migration.[100] This reduction in energy barriers accelerates the diffusion of halide ions into adjacent metal electrodes, where their accumulation initiates electrochemical corrosion.[101] In addition, 3D lead–halide perovskites often undergo chemical changes upon exposure to ambient air. In the case of $MAPbI_3$, a hydrated phase first forms, and upon prolonged exposure, eventually converts to PbI_2. The hydrated phase is not electrically conducting,[102] and therefore this may lead to irreversible changes in the conductance of memristors that are based on $MAPbI_3$. Meanwhile, $FAPbI_3$ and $CsPbI_3$ are not phase stable, and moisture hastens the phase degradation into the 1D non-conductive delta phase. $MAPbBr_3$ is also not stable when exposed to moisture.[103] Alongside the other issues, these have spurred on further research in other perovskite-inspired structures which may offer better stabilities and optoelectronic properties.

2.2. 2D/quasi-2D lead halide perovskites

In addition to modulating A-site or X-site cations to tune halide perovskite's structure and thus the electronic, and ionic migration properties-another strategy involves the utilisation of bulky A-site cations—either alongside or in place of conventional 3D A-site cations. The size and charge of these bulky cations determine the dimensionality of the perovskite structure, enabling the formation of lower-dimensional $[PbX_6]^{4-}$ octahedral frameworks (*e.g.*, 2D, quasi-2D, 1D, or 0D configurations). The introduction of hydrophobic cations also improves the moisture stability of quasi-2D perovskites.

Quasi-2D lead–halide perovskites can be visualised as thin layers of $[PbX_6]^{4-}$ separated by bulky A-site cations (tolerance factor $\gg 1.00$). There are two classes of quasi-2D perovskites – Ruddlesden–Popper (RP) and Dion–Jacobson (DJ) perovskites, as depicted in Fig. 6a. These two differ by how the large A-site cations are arranged in the lattice. In RPs, the large A-site cation is singly charged (BA^+,[104] PEA^+,[105] TEA^+ [106]), and thus between two $[PbX_6]^{4-}$ layers, two A-site cations are required, with the formula $(A_{RP})(MA)_{n-1}PbX_{3n+1}$[107] where A_{RP} is the bulky cation and n refers to the number of layers. The MA^+ may be replaced by other small cations (*e.g.* Cs^+, FA^+) as well. Meanwhile, in DJ perovskites, doubly-charged A-site cations are required (*e.g.* 3-AMP,[108] 4-AMP,[109] BDA^{2+} [110]), and the positively-charged regions have to be geometrically correct to bridge two $[PbX_6]^4$ slabs together, so only one layer of large A-site cation separates the perovskite slabs. They therefore exhibit a structure $(A_{DJ})(MA)_{n-1}Pb_nX_{3n+1}$,[109] where A_{DJ} is the large A-site cation. Disruption of $[PbX_6]^{4-}$ octahedra connectivity due to the presence of bulky A-site cation would reduce both ionic and electronic conductivity in general. Hence, DJ perovskites may enable better charge transfer between the perovskite slabs since the distance between them is much closer than in RPs.[111]

Anisotropy in both ionic and electronic conductivity is also expected as charge carriers or ions[112] move easily through the $[PbX_6]^{4-}$ layers as opposed to across the layers (Fig. 1). This allows for greater control over ion migration and reduces current flow during writing events, resulting in lower power consumption for memristor applications. Lower-dimensional perovskites exhibit wider bandgaps than conventional 3D counterparts due to quantum confinement effects. These effects alter band alignment and modulate the Schottky barrier at the perovskite-electrode interface,[106] increasing device resistance and further widening the gap between HRS and LRS—a critical parameter for memristor performance. The intrinsic carrier densities[113] (*i.e.* in the dark) and mobilities are also reduced,[114] due to stronger exciton binding energies. In addition, anisotropic ionic migration can direct the movement of halide vacancies, resulting in the formation of more ordered conductive filaments,[104] as opposed to the random filaments in 3D perovskites, and hence affords additional control over the filament formation kinetics by tailoring the crystallisation process. Finally, it was found that any residual filament formation after the erasing process could contribute to an unstable HRS, and the odds of residual filament formation was reduced with 2D perovskites.

Ionic migration has been studied in RP perovskites. In Cho *et al.*,[115] the effect of the number of perovskite layers on halide ion migration was investigated for RP perovskite comprising MA^+ and PEA^+ cations, and I^- and Br^- halide ions. An activation energy for ion migration was calculated based on the rate of optical absorption change observed in two separate films of $(PEA)_2MA_{n-1}Pb_nBr_{3n+1}$ and $(PEA)_2MA_{n-1}Pb_nI_{3n+1}$ which were physically clamped together and exposed to heat (Fig. 6b and c). An activation energy of 57.8 kJ mol^{-1} ($\sim$0.6 eV) was calculated for n = 10 66.9 kJ mol^{-1} (0.69 eV) for n = 6 and 71.5 kJ mol^{-1} ($\sim$0.74 eV) for $-n$ = 1 (Fig. 6b). This was attributed to the large PEA^+ cation which would suppress ion migration across layers; for n = 1, the halide ions are only able to move along the 2D $[PbX_6]^4$ plane, whereas there are more paths for migration in the quasi-2D case (n = 6 and n = 10). Homogenization of the resulting film was observed within 120 minutes (Fig. 6c). Therefore, the degree of ionic migration may be modulated by controlling the number of layers in the quasi-2D RP perovskite.

Meanwhile, the bulky A-site cation appears mobile as well.[116] Sutanto *et al.*[117] investigated the thermal ageing of a 2D/3D perovskite film, where a layer of 2D perovskite is deposited atop a layer of 3D perovskite for surface passivation. 2-TMA^+ (2-thiophenemethylammonium) and PEA^+ were used to make these 2D/3D films, and they were subjected to *in situ* grazing-incidence wide-angle X-ray scattering (GIWAXS) measurement during heating (Fig. 6d). Initially, a n = 1 layer was found right at the initial scan. The 2-TMA coated film then evolved to reveal a new mixed phase that was reported by the authors to be neither 2D (n = 1) nor quasi 2D ($n > 2$). This was accompanied with a new photoluminescence (PL) peak at 700–800 nm. Meanwhile, the PEA-coated film did not show any 2D peaks after heating. This suggests a degree of mixing between the 2D and 3D perovskites, which can only be possible *via* the migration of likely, the smaller 3D A-site cations. In a different paper by the same group,[118] they show that 2-TEA-coated films do not show a reduction in the n = 1 phase *via* X-Ray Diffraction (XRD) spectroscopy. They suggested that the 2-TEA^+ layer blocks the movement of MA^+ ions, preventing its conversion to quasi-2D

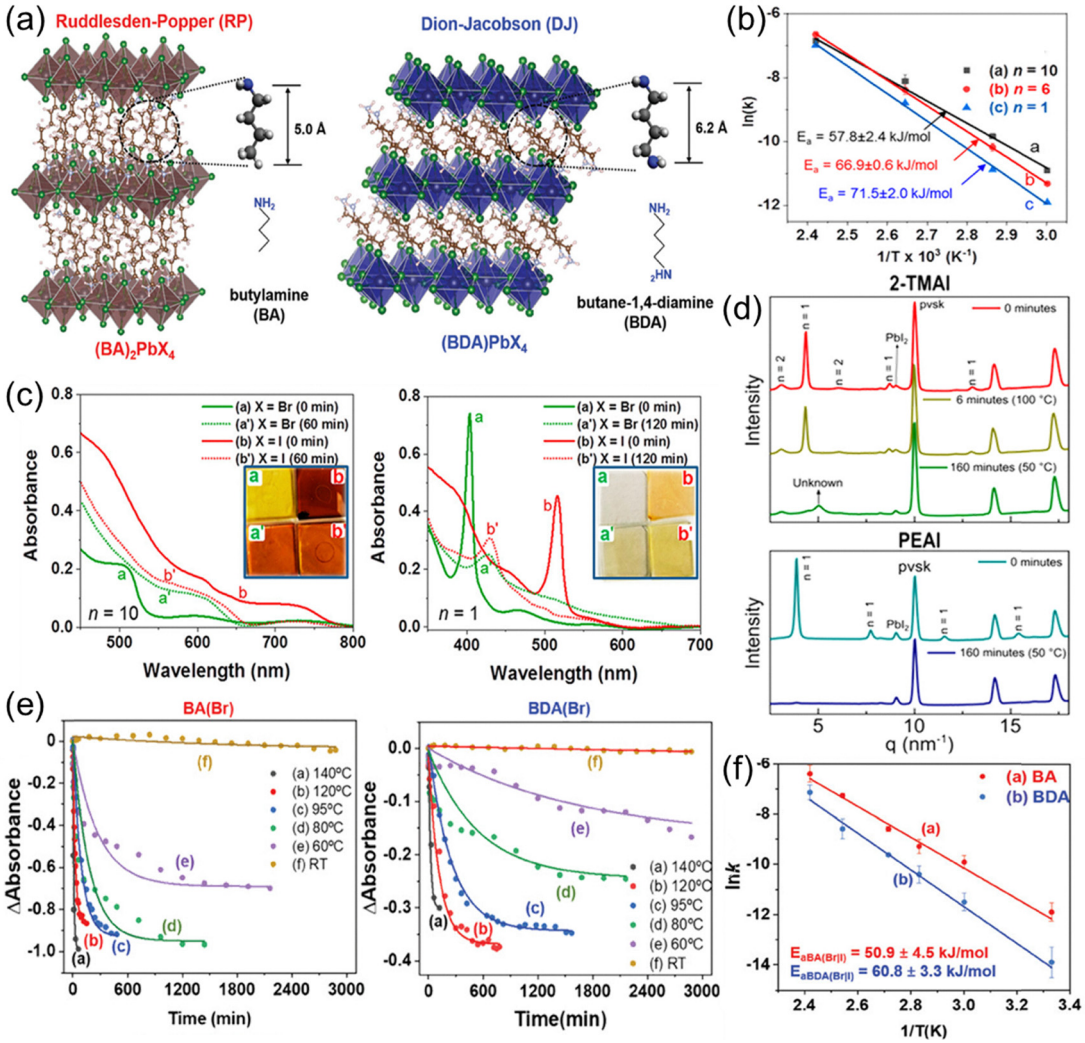

Fig. 6 (a) An example of a RP and DJ perovskite (left and right respectively). Reproduced from ref. 112 with permission from John Wiley and Sons, Copyright 2024. (b) The Arrhenius plots showing the activation energy of the migration at different n values together with (c) UV-vis absorbance spectra for n = 10 and n = 1 after heating for a prolonged period of time. Inset images show the color changes of the films, suggesting halide ion migration. Reprinted with permission from ref. 115. Copyright 2020 American Chemical Society. (d) XRD data showing the disappearance of the 2D n = 1 (2-TMA$^+$), n = 2 (2-TMA$^+$) and n = 1 (PEA$^+$) from the XRD spectra after heating. This suggests A-site cation migration. Reprinted with permission from ref. 117. Copyright 2020 American Chemical Society. (e) Halide ion migration studies at different temperatures for BA-based (RP) and BDA-based (DJ) perovskites as well as (f) the corresponding Arrhenius plots showing the activation energies of halide ion migration in BA and BDA films. Reproduced from ref. 112 with permission from John Wiley and Sons, Copyright 2024.

films. Their experiments, therefore, show that the A-site cation migration can be modulated as well.

In the case of DJ perovskites, halide ion migration has also been observed. Min and Cho[112] compared BA$^+$ and BDA^{2+} – RP and DJ A-site cations respectively. Two BA-based perovskite, iodide and bromide-based, were clamped together and heated to observe the halide ion migration. This was also done for the BDA-based DJ perovskite. In BA-perovskites, both bromide and iodide films were homogenised within 2 h of heating, whereas the BDA-based bromide and iodides retained their absorption edges (Fig. 6e). The activation energies were calculated to be 50.9 kJ mol^{-1} for BA-based perovskite and 60.8 kJ mol^{-1} for BDA-based perovskite, which shows that ion migration is hindered by the use of the BDA^{2+} spacer cation (Fig. 6f). This is although the BDA-based perovskites were more defective (based on poor PL emission). The increased rigidity of the overall 2D perovskite structure appeared to have hindered the migration of the halide ions, and they reported this to be the case for quasi-2D (n = 10) as well.

A-site cation migration in DJ perovskites has not been investigated to date. The tighter binding of the perovskite slabs may likewise prevent the MA$^+$ migration across the layers. Sutanto *et al.*[118] suggested that the packing motif of the organic cations (in the case of 2-TEA$^+$) makes the structure 'robust' and helps to prevent MA$^+$ migration into the organic spacer cation layer. The DJ perovskite is therefore expected to be similar, which would imply that DJ-perovskites are less susceptible to ionic migration as compared to RP perovskites.

Finally, it is worth noting that extrinsic ions can also migrate within the 2D perovskite layers. Reports on both RP and DJ perovskites in memristive devices can be found,[105,108,110,119] but most of them rely on the migration of extrinsic metal ions within the perovskite layer although no specific literature can be found that investigates the migration of extrinsic ions in these two 2D systems. This will be discussed in detail later in Sections 3 and 4.

2.3. Other lower dimensional perovskite: 1D, 0D, and vacancy-ordered (hollow) perovskites

The $[PbX_6]^{4-}$ octahedral connectivity can be reduced further to 1D, or completely disrupted to form 0D (isolated) structures for greater quantum confinement and anisotropic electrical conduction. There are two primary methods to achieve lower-dimensional perovskites: introducing bulky A-site cations that disrupt the $[PbX_6]^{4-}$ octahedral network and create electronic quantum well structures (Fig. 1) or forming physical nanostructures—such as nanorods or nanoparticles—stabilized by long-chain ligands. Hence, the terms appear to be blurred in this regard and 1D perovskites here refer to those where the lead–halide octahedra exists as 1D chains. While lower-dimensional perovskites exhibit higher excitonic binding energies compared to their higher-dimensional counterparts (0D > 1D > 2D > 3D) in general due to enhanced quantum confinement effects,[120] no clear trend has been observed in their ionic migration properties.

Studies on [R-α-MBA]PbI_3 crystals indicate that ionic transport is present and responsible for the trends observed in their results (Fig. 7a).[121] They also showed that upon photoexcitation, the density of mobile ions increases, but the mobility is reduced. However, they did not investigate the nature of the mobile ions. The presence of hysteresis in their results shows the suitability of 1D perovskites in memristive devices, with greater modulation potential. Meanwhile, in Vishwanath *et al.*,[122] propylpyridinium iodide ([PrPyr]PbI_3) and benzylpyridinium lead iodide ([Bnz]PbI_3) were investigated for use in memristors. DFT calculations reveal that the iodide vacancy migration barrier for [PrPyr]PbI_3 is 0.39 eV, higher than that of 3D $MAPbI_3$, which was calculated to be 0.29 eV. Meanwhile, electronic transport was improved as compared to [Bnz]PbI_3 due to the formation of edge-to-face π-stacking, which demonstrates the possibility of tuning the balance between the electrical and ionic conductivity of 1D perovskites.

0D perovskites have been utilized in memristors as well. Cai *et al.*[123] incorporated Cs_4PbBr_6, a 0D perovskite, in a memristor device stack, and observed that the films were very insulating, and required poling before they could be used. Although they attributed the memristive behavior to the migration of Br^- vacancies, they did not prove this claim in their work. Various other works have used Cs_4PbBr_6 as an active material for memristors, but investigations into the ion migration mechanisms are still lacking. Kang and Biswas[124] performed DFT calculations of the bromide vacancy, showing that it is a deep

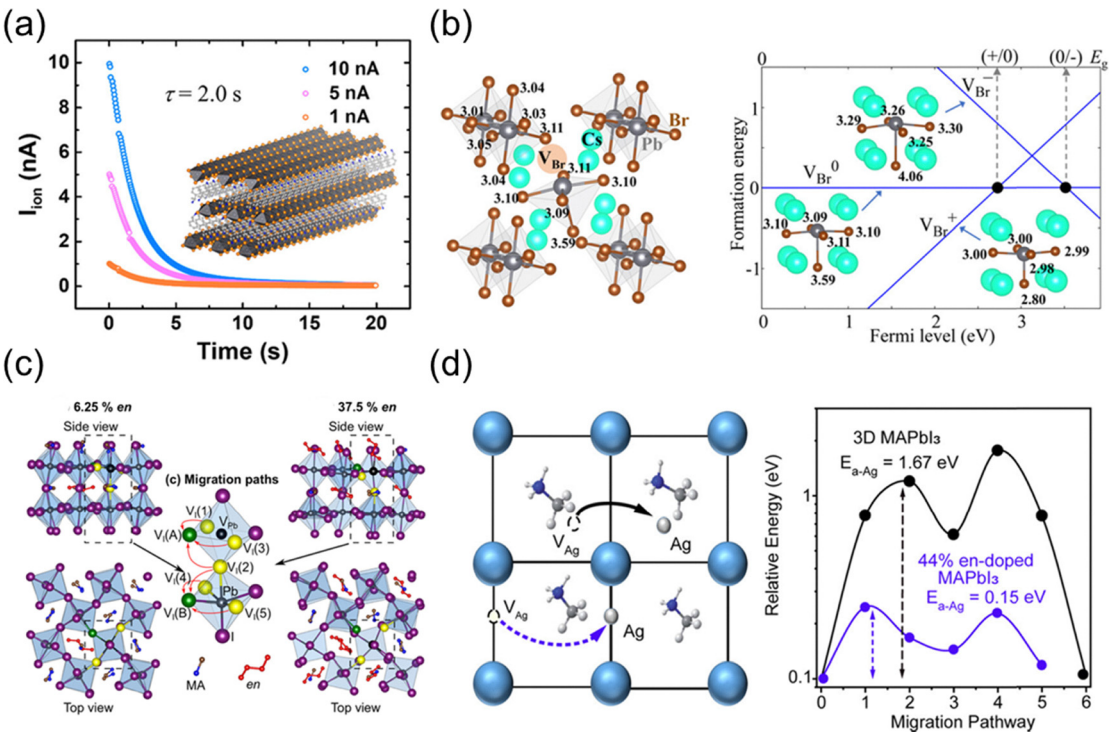

Fig. 7 (a) Ionic conductivity of [R-α-MBA]PbI_3 perovskite. Reprinted with permission from ref. 121. Copyright 2022 American Chemical Society. (b) Bromide vacancy and formation energy of the vacancy in Cs_4PbBr_6. Reprinted with permission from ref. 124. Copyright 2023 American Chemical Society. (c) Simulations of the various paths for iodide migration at two different en concentrations in en-doped $MAPbI_3$. Reprinted with permission from ref. 125. Copyright 2021 American Chemical Society. (d) Illustration of Ag^+ ion migration in en-doped perovskite, with the corresponding energy diagram showing the lower activation energy required for Ag^+ to migrate. Reproduced from ref. 126, under the terms of the Creative Commons CC BY 4.0 license (https://creativecommons.org/licenses/by/4.0).

defect which, fortunately, does not trap holes fast enough to interfere with light emission (Fig. 7b). However, their claim that the effects of the bromide vacancy on the lattice distortion is restricted to the octahedron that contains the defect. This may suggest that the 0D nature of Cs_4PbBr_6 may hinder ionic transport, although more research needs to be done to elucidate the nature of ionic migration in such systems.

For vacancy-ordered (hollow) lead–halide perovskites, the most well-studied example is the ethyladiammonium (EDA^{2+})-doped $MAPbI_3$ perovskite. These perovskites have EDA^{2+} cations dispersed within the 3D perovskite structure. As the EDA^{2+} is too large to fit the usual A-site, to make additional space,[125] some B-site vacancies will be generated, giving rise to the "hollow" nature of these perovskites. Senocrate *et al.* investigated the effect of EDA^{2+} concentration on ionic conductivity.[125] They found that iodide vacancies were responsible for the observed ionic migration, and that the EDA^{2+} doping increases ionic conductivity initially, before falling. The EDA^{2+} only partially balances the excess negative charge brought about by the missing MA^+ and Pb^{2+}, and thus positively-charged iodide vacancies are generated. At higher iodide vacancy concentrations, the excess amounts of vacancies may cause changes in migration energies due to structural distortions that are associated with the large amount of defects, and therefore despite the higher concentrations, the ionic conductivity falls (Fig. 7c). This means that the ionic conductivity can be tuned for memristor applications.

Extrinsic ionic migration has also been studied for EDA^{2+}-doped perovskites. Sakhatskyi *et al.*[126] did DFT calculations for the migration of Ag^+ ions in the perovskite, hypothesizing that the large voids in the structure can facilitate ion movement. It was revealed that the energy barrier for Ag^+ migration was greatly reduced in the 44% EDA^{2+}-doped perovskite, and thus they were able to incorporate the perovskite into a memristor (Fig. 7d). It is notable that in Senocrate *et al.*, the activation energy of migration of iodide vacancies for 47%-EDA^{2+}-doped perovskite was around 0.57 eV, higher than at lower concentrations (4%–0.34 eV). This may suggest a possibility that the dominant mechanism for hysteresis and memristive behavior can be switched between vacancy-mediated or Ag^+-mediated conditions just by controlling the EDA^{2+}-doping in the perovskite.

2.4. Lead-free perovskites and perovskite inspired architecture

Lead-free perovskites are a large subclass of halides that arose due to the search for alternative analogues that do not include toxic lead. Three general classes are currently utilised in literature[127] – those which directly replace the B-site cation with another cation with +2 charge (Sn^{2+}, Ge^{2+}, *etc.*), those which directly employ trivalent cations, and those which combine two different cations (usually +1 and +3) to replace the B-site while maintaining charge balance (Fig. 1). The main drawbacks of lead-free perovskites are the various morphological issues due to poorer solubilities of the precursors or rapid crystallization[128] and the presence of stereochemically inactive lone pairs.[129] The latter, however, is less relevant in memristors than in solar cells.[130,131]

Sn-based and Pb-based perovskites have very similar band structures and defect tolerance characteristics because the Sn^{2+} shares the same filled antibonding orbitals as Pb^{2+}. However, the shallower 5s orbitals in Sn^{2+} results in stronger s–p antibonding coupling, which raises the VBM, resulting in smaller bandgaps and higher hole mobilities.[132,133] The substitution of Pb^{2+} for Sn^{2+} is often associated with reduced ionic migration and increased electrical conductivity due to the spontaneous oxidation of Sn^{2+} to Sn^{4+} that generates a Sn vacancy (self p-doping) and two iodide vacancies (Fig. 8a).[54] From an ionic perspective, this increases the activation energy for migration for iodide vacancies near the Sn vacancy (1.45 eV in $FA[Pb_{0.5}Sn_{0.5}]PbI_3$ as compared to $FAPbI_3$ which is 0.45 eV). Thus, controlling the oxidation, which limits the self-doping of the perovskite as well, would allow of greater tunability of both electronic and ionic migration inside the mixed Pb-Sn perovskite. The activation energy for Sn^{2+} migration *via* Sn vacancies were also calculated to be high at 1.53 eV and thus do not contribute to ion migration in the Sn-perovskite.

Extrinsic ion migration has not been widely studied in Sn-based perovskites although several reports of Sn-based perovskites in memristors have been published.[134–136] Ag migration was responsible for the memristive behavior in Sn-based perovskites. In Pb-based perovskites, the migration of Au stems from the reaction between I^- and Au,[52] It is therefore expected that the Sn-perovskites with iodide as X-sites would likely undergo similar reactions as well. Hence, more studies need to be done however on the nature of extrinsic ion migration within Sn-perovskites to better control ion migration in Sn-halide perovskites for memristive applications.

2D forms of Sn-perovskites have also been studied, but to date none of these works are specific to memristors. Nevertheless, the conclusions drawn with regards to ionic migration may be extended to memristors, since ion migration is a material issue. In a study of RP and DJ Sn-based perovskites, Ji *et al.*[137] found that hysteresis persist in in-plane scans but disappear in vertical devices, suggesting that the bulky A-site cations also inhibit ion migration (Fig. 8b). Seetharaman *et al.*[138] also show A-site cation migration and the gradual formation of a quasi-2D layer in between 3D/2D heterostructures of Sn-based perovskites. These properties are similar to the 2D Pb-based perovskites, which highlights that the means for modulating ion migration in 2D Sn-based perovskites are likely similar to those for 2D Pb-based perovskites. As for extrinsic ion migration, Roh *et al.*[139] reported incorporation of Cu^+ ion into the grain boundaries of 2D Sn-halide perovskite ($PEA_2SnI_4 : FASnI_3 = 1:6$). The morphology of the perovskite film can also play a role in facilitating ion migration in the perovskite film.

The possibility for Sn^{2+} oxidation also raises the possibility of the extreme case, where Sn is fully oxidised in the +4 state – Cs_2SnX_6. This is a vacancy-ordered double perovskite.[140] Similar to Sn-perovskites,[141] the VBM has main contributions from the p orbitals of the halide anion, and the CBM has contributions from the hybridization of halide p orbitals and Sn 5s orbitals. The formation energy of the iodide vacancy in this system is 1.20 eV, similar to $CsPbI_3$. Liu *et al.*[141] performed DFT calculations of the migration barriers in Cs_2SnX_6 – 1.11 eV, 1.55 eV, and 1.69 eV for

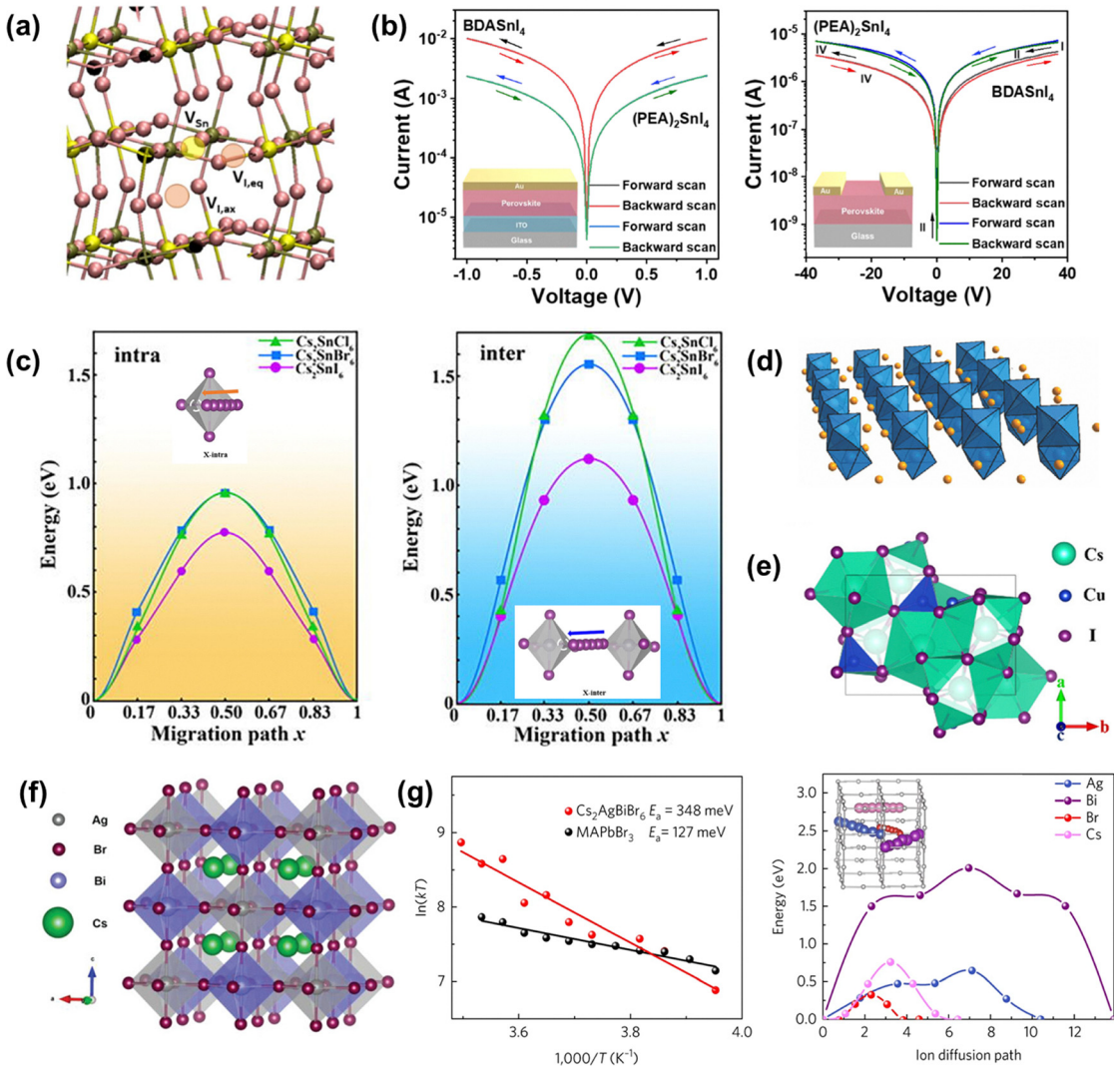

Fig. 8 (a) Simulation of the Sn vacancy with two adjacent iodide vacancies. Reproduced from ref. 54 with permission from Royal Society of Chemistry. (b) Current–voltage scans revealing a lack of hysteresis in the vertical device (shown in inset) and hysteresis in the lateral device (shown in inset), suggesting ion migration in the plane of the film but not in the vertical direction of the film for 2D Sn-halide perovskites. Reproduced from ref. 137 with permission from Royal Society of Chemistry, Copyright 2023. (c) Energy barrier calculations for iodide vacancy migration within the octahedron (intra) and across two octahedra (inter). Inset images show the movement of the iodide ion. Reproduced from ref. 141 with permission from AIP Publishing, Copyright 2021. (d) Structure of $Cs_3Bi_2I_9$. Reproduced from ref. 146 with permission from John Wiley and Sons, Copyright 2017. (e) Structure of $Cs_3Cu_2I_5$. Reprinted with permission from ref. 149. Copyright 2020 American Chemical Society. (f) The structure of a double perovskite, where alternating octahedrons with different B-site cations can be seen. Reproduced from ref. 150 with permission from John Wiley and Sons, Copyright 2019. (g) Activation energy for ionic migration in $Cs_2AgBiBr_6$, experimentally measured, by Pan *et al.*, Reprinted from ref. 151, Copyright 2017, with permission from Elsevier.

V_I, V_{Br}, and V_{Cl}, respectively, when migrating across octahedra, while energies are >0.77 eV for migration within the octahedra (Fig. 8c). In addition, they conducted temperature-dependent conductivity experiments for Cs_2SnI_6 and obtained a value of 0.91 eV. These values are higher than the iodide migration for 3D lead–halide perovskites. They attributed it to the increased covalency of the Sn–X bond. The reduced intrinsic ion migration of Cs_2SnX_6 may pose an issue for memristors relying on intrinsic ionic migration. Yet, Singh *et al.*[142] reported a Cs_2SnI_6-based memristor, though they did not discuss the mechanisms behind the observed characteristics. The presence of an Ag layer in their device may suggest that extrinsic ions (Ag^+) may be responsible for the memristive behavior. Other analogous structures (*e.g.* Cs_2TiBr_6[143]) have also been reported in literature.

Other divalent cations such as Ge^{2+}, while reported in solar cell literature,[144] have yet to be used in memristors, with only one paper that discussed the possibility of using Ge^{2+}.[145] On the other hand, substitution of the divalent cation with trivalent (*e.g.* Bi^{3+}) or monovalent (*e.g.* Cu^+) cations have been investigated.

In the case of the former, $Cs_3Bi_2I_9$ has been investigated as an active material in memristors.[146] These comprise $[Bi_2I_9]^{3-}$ bioctahedra, which share their edges rather than corners (unlike 3D perovskites), with the A-site surrounding the octahedra (Fig. 8d). Although no strict calculations and measurements

of ion migration have been done to date, the formation energy of several defects has been calculated.[147] V_I was calculated to have a formation energy of ~1 eV, with lower formation energies in I-poor conditions. The high formation energy relative to other perovskite systems may suggest that V_I may not be as dominant in contributing to ionic transport in the material. Also, as $Cs_3Bi_2I_9$ has a vacancy-ordered structure similar to the extreme case of EDA^{2+}-doping of $MAPbI_3$[125] or in Cs_2SnI_6,[141] where iodide vacancy diffusion is restricted in both, iodide vacancies in $Cs_3Bi_2I_9$ may not have low energy barriers for migration too. Nevertheless, Hu *et al.*[146] attributed the memristive behavior observed to the iodide vacancies, rather than to extrinsic ions, although they did not prove their claim.

For monovalent cations, Cu^+ was investigated as a replacement B-site cation alongside Cs^+ as the A-site cation. $Cs_3Cu_2I_5$ was studied (structure in Fig. 8e).[148] While attributing the observed memristor behavior to iodide vacancies, no experimental verification of the claim was made. An earlier paper by the same group used $Cs_3Cu_2I_5$ alongside an Ag electrode,[149] and claimed that the interaction between Ag and the iodide in the perovskite generated iodide vacancies within the perovskite film. However, they also showed that the Ag migration is responsible for the memristor performance. The lack of information in literature on the ionic and vacancy migration of $Cs_3Cu_2I_5$ therefore needs to be addressed before device performances may be improved.

Finally, in the case of double perovskites, where cations of two different oxidation states replace two B-sites, investigations in their use are aplenty. These typically have a chemical formula of $A_2B'B''X_6$; as an example, $Cs_2AgBiBr_6$, where Ag^+ and Bi^{3+} are both present in the lattice. Fig. 8f shows the structure of $Cs_2AgBiBr_6$. Cheng *et al.*[150] demonstrated its use in memristors. The migration barrier was experimentally measured in another work to be around 0.348 eV as compared to $MAPbBr_3$ at 0.127 eV (Fig. 8g).[151] DFT calculations also reveal the migration barrier for V_{Br} specifically was 0.33 eV (Fig. 8g).[151] This lower ionic migration was implicated in Cheng *et al.*,[150] where they attributed the slower switching speed to it. Another example of double perovskite is $Cs_2AgInCl_6$,[152] which has a similar structure to $Cs_2AgBiBr_6$. In this case, the memristive behavior was attributed to both the halide vacancy (V_{Cl} in this case) and Ag^+. Conducting Atomic Force Microscopy (CAFM) tests were done, and they noted that the grain boundaries have higher conductivities than the grain bulk; since grain boundaries provide a pathway for easy defect migration, they attributed this increase to the migration of Cl^-. They also acknowledged the possibility that Ag^+ participates in the memristor.

These lead-free perovskite variants, unlike the Sn-based perovskites, have not been investigated in depth, with most papers focusing more on device performance rather than the mechanisms that gave rise to the observed memristive behaviors. More research is therefore required to understand the interplay between intrinsic and extrinsic ion migration within these lead-free perovskites.

All-in-all, various lead-and lead-free halide perovskites have been investigated in literature. The unifying factors across these various classes of materials are the ionic migration and defects within them, which give rise to memristive behaviors observed in the various papers discussed in this section. The shift towards low-dimensional and alternative perovskite structures aim to exploit the increased environmental stability and the anisotropy in electrical conduction to bring forth better memristor performance.

3. Fundamental processes underlying memristive behavior in halide perovskite memristors

A memristor is an electronic device whose conductance can be modulated by external stimuli, such as electrical bias or light. This modulation arises from reversible structural or electronic changes in the active material—such as ion migration, polarization, defect redistribution, or interfacial reactions—enabling the device to ''remember'' its resistance state even after the stimulus is removed. Memristors are broadly classified into volatile and non-volatile types based on their conductance/resistance retention behavior. Volatile memristors exhibit spontaneous conductance decay once the external stimulus ceases. In contrast, non-volatile memristors retain their conductance state persistently after stimulation, emulating long-term memory. First, the performance metrics of typical perovskite based memristors will be reviewed. Next, we will delve into the fundamental operating mechanisms of both volatile and non-volatile memristors, examining how external stimuli induce changes in conductance. Then, we will review a range of characterization and simulation methods used to uncover the underlying mechanisms of memristor operation. By connecting these insights to device performance metrics—such as switching speed, energy consumption, and retention time—this section aims to provide foundational knowledge for understanding and optimizing memristors for neuromorphic applications.

3.1. Key performance metrics for memristors

Various performance indices of memristors, along with methods for their measurement and best practices, will be evaluated below. This review will cover both traditional metrics-such as on/off ratio, retention time, and endurance-as well as metrics specifically relevant to artificial synapses.

3.1.1. On/off ratio and number of states. One of the key performance metrics for memristive devices is the on/off ratio, defined as the ratio between the current in the high-resistance state and the low-resistance state. Ideally, a high on/off ratio ensures well-separated conductance states, which is essential for reliable device operation. This high ratio serves two important purposes: (A) it enables a greater number of clearly distinguishable conductance states in both analog and multi-level memory applications (Fig. 9b), and (B) it enhances the signal-to-noise ratio, allowing practical sensing circuits to more easily differentiate between resistance states. As a result, read errors are reduced and the noise margin of the system is improved. To date, halide perovskite based memristors have

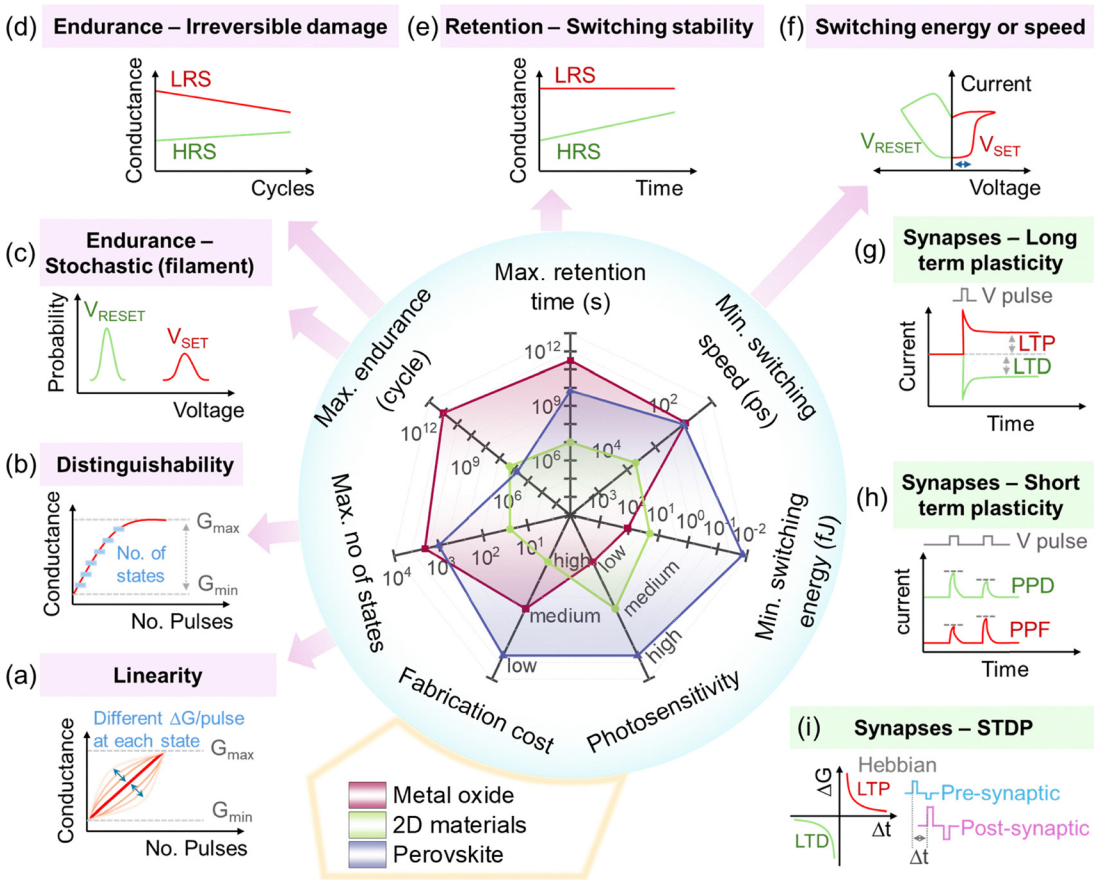

Fig. 9 The performance matrix and issues related to perovskite based memristor (such as (a) linearity and (b) distinguishability of the states, as well as (c) switching probability, (d) endurance, (e) retention, (f) and switching energy of the device) or perovskite-based synapses (*i.e.* (g) long term plasticitiy, (h) short term plasticity, and (i) spike time dependent plasticity) together with (centre) the performance metrics comparison between memristors based on perovskites, metal oxide, and 2D materials. The data of metal oxide and 2D materials were taken from ref. 160. The maximum endurance and minimum switching speed of perovskite-based devices were referenced from ref. 161, the maximum retention time from ref. 162, the maximum no of states from ref. 170, and minimum switching speed energy from ref. 163.

achieved on/off ratio as high as 1.9×10^{-9} depending on the electrode materials and buffer layer used.[153] The on/off ratio is fundamentally influenced by the off-state current (often referred to as the dark current). Reducing the dark current through strategies such as decreasing grain size,[154] or defect density (higher DFE),[155] or by utilizing lower-dimensional perovskite structures[105] can generally enhance the on/off ratio.

In memristive devices, the amount of information that can be stored depends on the number of distinct resistance states it can retain. More important than the absolute resistance values themselves is the variability between these states, especially in memristors with multilevel or analog states that exhibit long-term potentiation (LTP – increased conductivity with "writing" pulses) and long-term depression (LTD – decreased conductivity with "erasing" pulses). LTP and LTD are measured by applying sequential voltage pulses: a baseline conductance reading before "writing" action (using identical or incrementally increasing pulses), followed by intermittent read voltages to track conductance changes. The resulting LTP or LTD curve shows gradual conductance increases or decrease until saturation (Fig. 9g). However, studies often overestimate usable conductance states by conflating conduction level at various pulse counts with stable (*i.e.* retention of each state), distinguishable levels (*i.e.* gap between each state), particularly in perovskite-based devices. To address this, best practices recommend reporting variability using statistical tools such as error bars, histograms, box plots, or cumulative distribution functions across multiple devices and numerous switching cycles. This approach quantitatively determines the system's effective number of conductance levels while simultaneously assessing state separation reliability.[156]

Key metrics for LTP/LTD include ΔG (conductance change: $(G_{after} - G_{before})/G_{before}$), saturation point, linearity of modulation (Fig. 9a), and retention time. Ideal behavior features smooth, incremental conductance shifts with minimal variability, mimicking biological synaptic plasticity for neuromorphic computing. Such characteristics enable artificial neural networks to emulate brain-like learning/forgetting processes.

However, it is important to note that an excessively large on/off ratio can complicate the design of readout circuits, and increasing the current at LRS value may lead to higher energy consumption[156] and excessive parasitic voltage drops across the interconnects.[157] Additionally, in some cases, improving

the on/off ratio may compromise switching linearity-the ability to transition smoothly between resistance states-highlighting the need for balanced optimization.[158]

3.1.2. Switching endurance. Endurance in memristors is their capacity to withstand repeated switching cycles without failure. For memristors with two conductance states, one cycle involves a write-read-erase-read pulse sequence. The LRS and HRS conductance are plotted against the number of cycles, showing how many cycles the device switches through before failure (Fig. 9d). In multistate memristors, a sequence of write-read pulses is applied multiple times to induce LTP, followed by erase-read pulses to induce LTD (Fig. 9g). Repeating these cycles helps evaluate the device's ability to maintain and reproduce intermediate conductance levels.

However, many reported endurance claims are unreliable due to improper testing methods as they often rely on resistance vs cycle data from very few cycles and only a single device, which fails to capture the true cycle to cycle and device to device variability (Fig. 9c).[156,159] Especially, reports which introduce strategies to improve endurance and compare with a control composition must ensure that the improvement is statistically significant. Post-mortem characterization of the devices is also recommended to investigate the failure mechanism and make claims about the mitigation strategy more robust. To address this, a standardized method for endurance characterization has been proposed. Resistance should be measured in every cycle for both high and low resistance states across multiple devices, and endurance plots should also include one data point per cycle. This approach provides a more accurate assessment of resistive switching device reliability and is crucial for their commercial integration, as it helps avoid overestimating device performance and ensures that reported endurance truly reflects the device's operational limits and variability.[159] Halide perovskite memristors in general suffers from low endurance as compared to other established material such as metal oxides (Fig. 9).[160] To date, an endurance of up to 6×10^6 cycles has been reported for perovskite nanowires.[161] Switching endurance is generally associated with intrinsic material stability over time, which can be compromised by high electric voltage or the testing environment. Therefore, enhancing perovskite stability is a critical effort that will be covered in-depth in Section 5.1.

3.1.3. State retention time. State retention time refers to the duration a memristor can reliably preserve its programmed resistance state without any applied bias. This characteristic is typically evaluated using current–time (I–t) measurements at a constant read voltage or through periodic read pulses over time. For two-state devices (LRS and HRS), retention is assessed by tracking each state's stability over time, with the on/off ratio (HRS/LRS current ratio) serving as a key indicator of state separation (Fig. 9e). In multilevel memristors, each distinct conductance state must be individually monitored to ensure they remain well-separated and non-overlapping during testing-critical for reliable multi-bit storage.

For extrapolating long retention times beyond practical measurement periods, temperature-accelerated testing combined with Arrhenius analysis can provide more reliable lifetime estimates.[156] Based on their retention duration, memristors are broadly classified into two types: non-volatile and volatile memristor. The required retention time depends on the application, ranging from years for non-volatile memristor to fractions of a second for volatile devices used in neuromorphic computing tasks mimicking short-term synaptic plasticity. Retention in halide perovskite memristors is governed by the stability of ionic configurations enabling resistive switching. Key influencing factors include ion migration barriers, defect dynamics, electrode interface quality, and material degradation which will be discussed further in Section 4. Notably, perovskite memristors often exhibit lower retention times compared to established materials like metal oxides or 2D materials (Fig. 9).[160] Suppressing the ionic migration of Ag led to an extended retention time (up to 7×10^9 s) at the cost of higher threshold voltage and switching time in $MAPbCl_3$ nanowire based memristor.[162] Furthermore, employing perovskite with lower ionic migration rate (high E_A and high DFE) could also leads to longer retention times.[60]

3.1.4. Threshold voltage, switching time, and switching energies. Switching time refers to the duration that a device is exposed to an external stimulus, such as electrical voltage, current, or optical illumination, to induce a desired change in resistance. Threshold voltage refers to the minimum voltage needed to switch the resistance of the devices (Fig. 9f), and is dependent on the operational condition such as voltage sweep rate, pulse mode, *etc.* During this period, energy is consumed due to power dissipation caused by the applied stimulus. For electrical switching, the total energy consumption (E) is calculated by integrating the instantaneous power, which is the product of voltage and current, over the switching time. In optical switching, the total energy is determined by multiplying the intensity of the incident light with the duration of exposure. The switching time interval is defined by when the device's conductance reaches 10% and 90% of its final value, ensuring consistency in evaluating switching energy across devices. Due to the fast ionic migration in halide perovskite, fast switching time with lower switching energies are generally expected in halide perovskite as compared to other materials such as metal oxides or 2D materials (Fig. 9).[160] Switching time as fast as 0.1 ns has been reported in $MAPbI_3$ based memristor[161] while passivation treatment resulted in a low threshold voltage (15 mV) and switching energy (13.5 aJ per spike).[163] While higher ionic migration rate (low E_A and low DFE) is preferred to increase retention time, employing halide perovskites with lower E_A generally results in lower switching voltages, speed, and energy for ionic-based memristors.[162,164]

3.1.5. Photosensitivity. In photosensitive memristors, light can influence the resistance switching behavior, allowing resistance changes to be triggered not only by electrical input but also by light exposure. Perovskite materials are particularly promising candidates for photosensitive memristor due to their inherent properties, including high absorption coefficients ($>10^4$ cm^{-1}), ultrafast photo-generated carrier generation (fs–ps) and fast carrier transfer ($\sim$ns)[165] all of which enable fast photo-response in thin-film devices. The fast photo-generated carriers can be trapped in the adjacent layers, modulating the device conductivity

under illumination.[166] This phenomenon has been heavily utilized in 3T memristors and will be discussed further in Section 3.2.2C. The large photogenerated carriers can also be separated by a smaller electrical bias, increasing the carrier concentration and enhancing the trapping of these carriers. This subsequently shifts the Fermi level and lowers the Schottky barrier, thus enabling modulation in the device's switching voltage.[167]

Additionally, light illumination can also trigger phase segregation, which can be utilized for optical memristor purposes where the film's PL could be augmented depending on the light exposure given in the system.[83] Given that light controls halide ion migration, many studies detail light-induced resistance switching achieved by assisting the formation[90] or breaking[89] of conductive filaments. The enhanced ionic migration rate due to light illumination[88] has also been utilized to lower the voltage needed to change the conduction states of the devices.[168,169] Another key advantage lies in their tunable bandgap, which can be adjusted across the visible (400–700 nm), ultraviolet (350–400 nm), and near-infrared (700–1100 nm) spectra, offering spectral versatility often unmatched by other conventional solution-processed memristors.

3.1.6. Multilevel memristor to emulate biological synapses. Beyond the traditional memristor performance metrics mentioned above, various metrics exist to evaluate memristors as artificial synapses. In biological synapses, the strengthening of synaptic weights through repeated neuronal firing underlies the transition from short-term memory (STP) to long-term memory (LTP/LTD). This process can be emulated in volatile multilevel memristive devices, where the retention time can be gradually extended with repetitive stimulation. Experimentally, this transition is realized by applying a train of input electrical or optical pulses and then monitoring how long the resulting conductance state persists. Two primary testing protocols are used to study this phenomenon: amplitude modulation and interval modulation. In amplitude modulation, pulse trains with increasing amplitude or duration are applied while keeping the number and width constant. Higher amplitudes or duration enhance ion migration or charge trapping *via* stronger electric fields, leading to deeper ionic or charge redistribution, prolonged retention, and slower relaxation (longer retention time). In interval modulation, the time between pulses is varied. Shorter intervals cause cumulative ionic or charge displacement (due to incomplete relaxation between pulses), mimicking a transition toward long-term conductance states.

Excitatory postsynaptic current (EPSC) is the enhanced output current generated in the postsynaptic membrane when a synapse is stimulated. A key mechanism in this context is paired-pulse facilitation or depression (PPF or PPD), where two closely spaced stimuli (typically shorter than the device's retention time) induce a stronger or weaker ESPC response to the second pulse (Fig. 9h). In biological synapses, PPF arises from residual calcium boosting neurotransmitter release. In memristors, PPF is replicated by applying paired electrical pulses: the second pulse generates a higher conductance than the first, with facilitation magnitude depending on pulse interval, amplitude, and width. This behavior, often modelled with exponential decay, reflects rapid and slow relaxation phases akin to biological systems. Such STP-to-LTP transitions and PPF-driven plasticity provide critical insights into adaptive learning in neuromorphic computing. Higher E_A in perovskite is generally associated with a longer relaxation time and, consequently, a higher PPF value.[60]

Furthermore, the temporal spacing between pulses can emulate learning observed in biological systems. Spike-timing-dependent plasticity (STDP), a synaptic learning rule central to Hebbian mechanisms, modulates synaptic connection strength ($\sim\Delta G$) based on the relative timing of pre-synaptic and post-synaptic spikes, enabling devices to learn temporal associations. To implement STDP in memristors, paired voltage pulses simulating neuronal spikes are applied, with a pre-synaptic pulse delivered to one terminal and a post-synaptic pulse to the other. The resulting conductance change depends on the time difference (Δt) between spikes. When $\Delta t > 0$ (pre-synaptic spike precedes post-synaptic), conductance increases in Hebbian systems (Fig. 9) or decreases in anti-Hebbian systems. Conversely, when $\Delta t < 0$ (post-synaptic precedes pre-synaptic), conductance decreases in Hebbian systems (Fig. 9i) or increases in anti-Hebbian systems. The measured STDP curve exhibits an exponential or asymmetric profile, closely replicating the behavior of biological synapses.

3.2. Memristor mechanisms

Up to date, two primary mechanisms drive perovskite memristor operation (Fig. 10): filamentary and interfacial mechanisms. In the filamentary mechanism, conductive filaments form or rupture within the active material due to ion migration or defect dynamics. This mechanism can be further divided into the electrochemical metallization (ECM) and valence change mechanism (VCM). In ECM, reactive electrodes release metallic cations that migrate into the active layer, forming conductive bridges. In VCM, anion migration or vacancy reconfiguration, such as halide defects, leads to the formation or disruption of these conductive pathways, enabling resistive switching. In contrast, the interfacial mechanism involves modulating the energetic barrier at the electrode–material interface, typically through ion migration induced self-doping, reactions, charge trapping or depletion, to alter the device's resistance. Although uncommon, resistive switching driven by polarization in ferroelectric perovskites has also been demonstrated.

While various mechanisms described above may co-exist or compete, the specific device structure and thickness ultimately determine the most dominant resistive switching nature in the device. For example, studies have reported that a thin perovskite medium (<90 nm) allows for the co-existence of both ECM and VCM, while thicker perovskite results in the dominance of the VCM mechanism.[89] Increasing the perovskite thickness has also led to observed changes in the switching mechanism, shifting it from a filamentary to an interfacial type.[171] The device's switching behavior is also determined by the transport layer used, which can make it either filamentary or interfacial.[172] Consequently, the switching mechanism must be determined on a case-by-case basis for each memristive device design.

Device architecture: in general, two device configurations were widely used in perovskite based memristor: two terminals

(2T) with simple electrode/buffer (optional)/perovskite/buffer (optional)/electrode stacks and three terminals (3T) configuration mimicking transistor (Fig. 10). While 2T devices are easy to scale and allow for electrical and optical writing, they are vulnerable to short retention times as "reading" action may potentially alter the memory in the long run as well as high leakage current due to high electronic conductivity in perovskite. From mechanism point of view, memristive behavior in 2T devices could be triggered by either ion migration, charge trapping, filament formation, or polarization effects. Devices in 3T configuration, on the other hand, offer better control as they could isolate the "writing" and "reading" operation by utilising the gate-source terminals and drain-source terminals, respectively. Despite their potential, 3T-based perovskite mem-transistors have generally utilized perovskites as photosensitizers or floating gates, while employing other materials such as metal oxides, organic polymer as the active channel. When perovskites are employed as photosensitizer layers, photogenerated carriers produced during the optical "write" process are injected into the channel, thereby modulating its conductivity. In floating-gate architectures, optical excitation perturbs the gate capacitance due to photocarriers, which consequently alters the gate potential profile across the channel, yielding discrete conductance states that scale with the capacitance modulation. Mem-transistors with perovskite as the active channel have also been reported with either electrical or optical write. In electrical mem-transistors that use perovskite as the active channel, the "writing" process typically relies on the source-drain voltage rather than gate modulation. A voltage pulse applied to the drain induces ion migration, which triggers a self-doping mechanism. This self-doping enhances carrier injection at both the source–perovskite and perovskite–drain interfaces. Consequently, the device's operation closely resembles that of lateral 2T memristive devices. An additional terminal (gate) could be introduced to enable further programming of multiple conductance states and dynamic state tuning during the read process – a functionality not achievable in conventional 2T memristors.[173] In addition, gate voltage is also used to modulate retention time by regulating ion migration within the device to a certain degree.[174] To enable stronger "writing" *via* gate modulation in perovskite-based mem-transistors, a breakthrough is needed in greater control of ion transport through the gate. One promising approach involves using ferroelectric dielectric materials to modulate ionic migration within the perovskite channel[175] as well as utilizing ferroelectric-based perovskites,[176] which are sensitive to gate-induced electrical polarization.

However, it's important to recognize that switching behavior in perovskite memristors often arises from the interplay of multiple mechanisms rather than being governed by a single dominant process. These mechanisms—such as ion migration, charge trapping, filament formation, and polarization effects—can coexist and influence one another, making the overall switching behavior more complex and device-dependent. These fundamental mechanisms that govern the resistive switching behavior of memristors will be discussed further below.

3.2.1. Conductive filament formation. In resistive switching memory devices that operate *via* the conductive filament mechanism, the transition from HRS to LRS occurs when ion migration, driven by an applied electric field, leads to conductive filament formation. Conversely, reversing the field polarity causes the filament to break, restoring the HRS. Depending on the nature of ions that form the filament as well as the electrode used, it is primarily classified into two mechanisms: electrochemical metallization and valence change mechanism which will be described further on the next section.

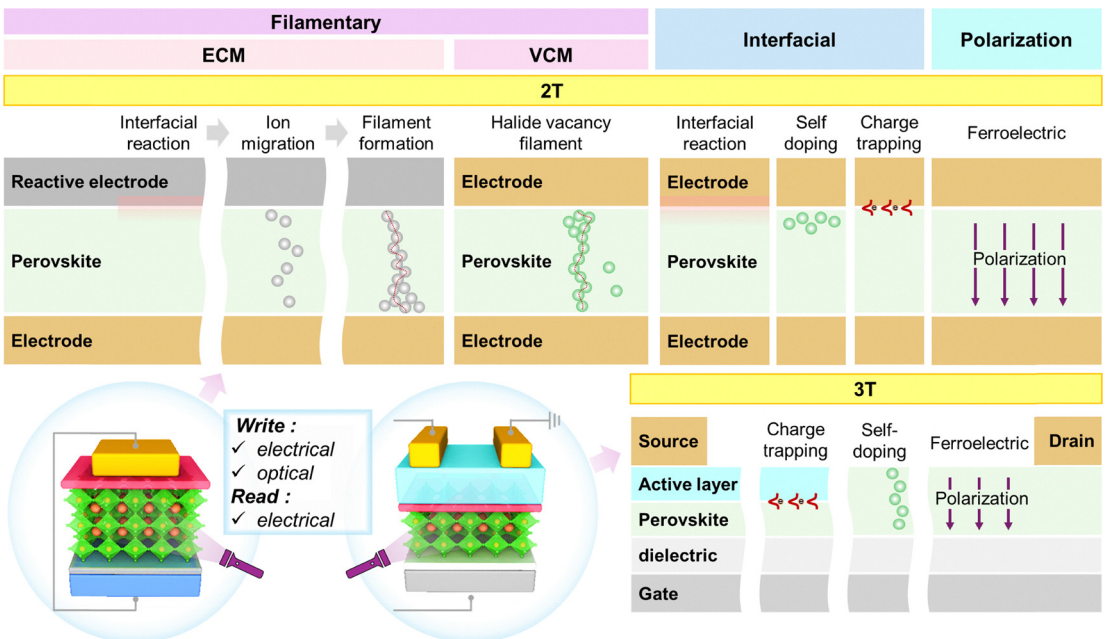

Fig. 10 Schematic diagram of various mechanisms that trigger resistive switching in halide perovskite memristors.

Regardless of the type, resistive switching *via* filament formation is inherently stochastic due to the random nature of defect generation, ion migration, and conductive filament growth within the active layer.[177] The exact location, size, and number of these filaments can vary from device to device and even from switching cycle to switching cycle, resulting in device-to-device and cycle-to-cycle variability. This stochastic behavior arises from the non-uniform distribution of defects and vacancies, which are influenced by grain boundaries, lattice strain, and unintentional dopants during film deposition. These factors create spatial variations in ion migration pathways, and when an electric field is applied, mobile ions drift toward the electrode, with their movement affected by thermal fluctuations, local electric field variations, and material inhomogeneities. This leads to filament formation at different locations across switching cycles, causing variations in switching voltage, on/off ratio, and retention time. Additionally, the dissolution and reformation of filaments during the RESET and SET processes also contribute to this randomness, as local Joule heating, electrostatic forces, and chemical interactions influence how the filament forms and breaks. Due to the nature of the process, the LRS of the filament are generally independent of device area because the conductive filament is highly localized and does not scale with electrode size.

3.2.1.1. Electrochemical metallization. When reactive metals are used as electrodes, the resistive switching of the devices is typically governed by the ECM. Metals such as silver (Ag), aluminum (Al), nickel (Ni), and copper (Cu) undergo electrochemical processes that drive the migration of metal cations, facilitating the formation or rupture of conductive filaments and modulating the device's resistance states. This metal migration is an electrochemical process initiated by oxidation at the anode, where metal atoms lose electrons and transition into ionic form. The voltage bias required to induce this migration is directly influenced by the metal's oxidation potential, which determines its tendency to oxidize under an applied electric field.[178] This phenomenon does not occur under cathodic bias,[179] as even highly reactive metals remain stable in a reducing environment.[180] When oxidation occurs at the anode, the resulting metal ions migrate toward the cathode under the influence of the electric field, driving the observed metal migration.

To change the conductivity of ECM devices from HRS to LRS (SET), three sequential processes are generally needed. (1) When sufficient positive voltage ($V = V_{th}$) is applied on the reactive electrode, oxidation of the reactive metal occurs creating metal cations in the system ($M \rightarrow M^{n+} + ne^-$). (2) The metal cations then migrate under high electric field towards the other electrode. Next, (3) reduction ($M \leftarrow M^{n+} + ne^-$) and electro-crystallization of metal cations occurs on the surface of the other inert electrode. The electro-crystallization process is boosted by the applied electric field, promoting the formation of a metal filament that extends preferentially toward the reactive electrode. Once this filament grows sufficiently to establish a metallic connection with the opposite reactive electrode (M), the device transitions to the LRS. This state remains stable until a reverse voltage of adequate magnitude is applied, triggering the electrochemical dissolution of the filament, thereby RESETting the cell back to its original HRS. During the initial stage of the RESET process, both an electronic current flows through the metallic bridge and a parallel electrochemical (faradaic) current facilitates filament dissolution. The overall switching speed of ECM memristor is primarily governed by the kinetics of these sequential SET processes.

Thus, the resistive switching mechanism induced by reactive metals is closely associated with their oxidation rate and ionic mobility. The susceptibility of a metal to corrosion is closely linked to its electrochemical stability, which is influenced by its work function. Generally, metals with lower work functions exhibit higher reactivity and are more prone to oxidation. Based on this trend, the expected reactivity ranking follows the order Cu < Ag < Al. However, while Al is highly reactive, it rapidly forms a stable Al_2O_3 layer, which can act as an insulating barrier, limiting ion migration but still enabling switching under high electric fields. Ag oxidizes moderately, forming mobile Ag^+ ions that migrate within the perovskite layer, react with halides, and create vacancies crucial for stable switching with lower voltages compared to Cu.[178]

Depending on the nature of the conductive filament (*i.e.* the diameter of the filament, the interfacial energy between the filament and active layers, heat dissipation, local temperature, *etc.*), both volatile and non-volatile memristor can be formed.[181] For example, by regulating the maximum current flow into the devices (compliance current) which govern the electrochemical reaction rate, both diffusion and drift memristor have been found in Ag based $CsPbBr_3$ memristor.[182] In addition, both analog and digital switching can also be obtained by regulating the compliance current as well as the voltage required to dissolve the filament (RESET voltage). Non-volatile multi-states memristor were observed on both Al based and Ag based memristor by modulating the compliance current.[183,184] By modulating the RESET voltage, multi-states memristor were also observed in Ag based $CsPb_{1-x}Bi_xI_3$ memristor.[185]

3.2.1.2. Valence change mechanism. Despite the use of inert metals (such as Au, carbon, Pt, Ti, or FTO) as electrodes, resistive switching due to conductive filament formation can still be formed through VCM *via* the movement of anions or its vacancies in the halide perovskite active layer. Here, applied electric field induces the movement of anions or vacancies throughout the metal halide perovskite layers, aggregating and forming conductive filaments. These conductive filaments can bridge the electrodes, leading to a significant reduction in resistance. Hence, VCM is highly dependent on the mobility of the anions and the stability of the active switching layer.

For example, lower voltages are required to change the conductance of the device from HRS to LRS (SET voltage) when more mobile Br anion (Br^-) are used instead of bulky iodide anion (I^-).[186] In general, the electric field (E) required to switch halide perovskite memristors is lower than that of oxide-based memristors, which can be explained by the lower migration barrier for halide anions or vacancies as compared to their

oxide counterparts. Devices with high anion or vacancy migration rates typically exhibit lower SET fields (V/memristor thickness), enabling faster switching and reduced power consumption. However, they also tend to have shorter retention times due to rapid anion diffusion and lower endurance or stability due to unstable switching or higher degradation rates which explain their inferior endurance and retention time as compared to oxide based memristor.[160] While the generally insulating nature and higher bandgap of oxide materials restrict their photo-memristors to UV light irradiation, halide perovskites possess characteristics that enable them to operate effectively across a broader spectral range (UV-visible-near infrared).

Similar to ECM case, both volatile and non-volatile memristor as well as analog[187] and digital[188] switching could be realized with VCM by controlling nature of conductive filament nature *via* regulating the SET and RESET voltages. In addition, any external stimuli that modulate defect migration in halide perovskite could modulate the resistive switching as well. For instance, exposure to light has been shown to reduce the ionic migration barrier in halide perovskites, facilitating the RESET process in memristors. This occurs because the lower activation energy (E_a) destabilizes iodide vacancies (V_I)-based conductive filaments, making them more prone to diffusion. Light can actively modulate V_I dynamics, leading to their redistribution in VCM based memristors.[89,188] Cooperation of photo-generated carriers and ions movement have also been shown where light could be utilized to form conductive filament instead of electrical stimuli.[90] Controlled light intensity stimuli could also be utilized to reduce both SET and RESET voltages by lowering the ionic migration barrier in the system.[168,169]

3.2.1.3. Co-existence between ECM and VCM. Although both active metal and halide vacancy conductive filaments have been independently validated as resistive switching mechanisms, their actual formation is likely a result of a complex interplay between the two. The coexistence or competition of these filament types is crucial in determining the switching behavior of halide perovskite devices. To better understand this phenomenon, switching characteristics in memristors with a Pt/$MAPbI_3$/Ag structure were examined across various film thicknesses. It was observed that the switching behavior was influenced by the relative dominance of Ag-based filaments and V_I-induced filaments.[89] Since Ag^+ migration typically requires a high electric field ($\sim 10^7$ V m^{-1}),[184] the formation of Ag-based filaments are less feasible in thicker perovskite films, where V_I filaments dominate (Fig. 11a). However, as the perovskite layer is reduced to around 90 nm, the conditions become more favorable for both filament types to coexist, leading to a more intricate mechanism that incorporates contributions from both Ag and halide vacancies. A combined presence of both ECM and VCM has been observed in $CsPbBr_3$ quantum dot-based memristors using scanning electron microscopy (SEM) along with energy-dispersive X-ray (EDX) analysis. For devices with the same perovskite thickness, ECM typically exhibits faster switching behavior, characterized by a lower SET voltage compared to VCM device with inert electrode.[189]

3.2.2. Interfacial modification. In contrast to filamentary type, interfacial modification due to doping effects or charge trapping/de-trapping could also result in resistive switching. These processes collectively influence the charge injection barrier at the interface, thereby modulating the device's electrical characteristics. This mode of resistive switching is generally classified as the interfacial modification mechanism. Due to it's nature, the HRS and LRS of devices which utilize this mechanism are generally sensitive to device area and decrease linearly with device area.[167,171,190]

3.2.2.1. Self-doping. Unlike conventional semiconductors such as silicon, where intrinsic doping is primarily governed by thermally generated charge carriers or controlled impurity doping, halide perovskites exhibit a unique self-doping behavior that allows their conductivity type to be naturally tuned between n-type and p-type. This transition is influenced by the ratio of native point defects, particularly halide vacancies and interstitials, where a halide-deficient composition favors n-type conductivity, while a halide-rich environment promotes p-type behavior.[191] The highly mobile nature of halide anions and their corresponding vacancies further amplifies this effect, allowing for dynamic modulation of the doping state. As a result, halide perovskites can undergo reversible doping and de-doping through defect redistribution. This defect-driven self-doping process becomes particularly significant at interfaces, where ionic migration can modify the carrier injection barrier by triggering either self-doping of the perovskite or doping of the adjacent transport layer, thereby altering the device resistance.

The co-existence of carrier injection barriers and ionic migration induced self-doping are two important criteria which produce resistive switching here.[60,171] Depending on the location of halide related ionic migration, two relaxation time constant can be observed in perovskite based memristor, mimicking artificial synapses. The conductivity changes are largely driven by the migration of ion vacancy defects under electrical stimulation. When low-amplitude or few voltage pulses are applied, ions migrate slightly and quickly return to their original positions once the bias is removed. This transient ion movement leads to a brief increase in conductance that rapidly decays, mimicking short-term plasticity behaviors. However, with stronger or repeated pulses, some ions migrate deeper into the device and become trapped either at the perovskite/transport layer interface or within the transport layer itself. While a portion of these ions eventually return to equilibrium, others remain immobilized-creating halide vacancies and forming conductive pathways. This results in a sustained increase in conductance, reproducing long-term potentiation (LTP) analogous to biological memory retention.[193] The energy consumption required to modulate the resistance per spike[60] and device's conductance[171] generally scales linearly with device area.

In 3T device setups, while various publications have reported perovskite-based mem-transistor with standard dielectric layer, their resistance are usually modulated through the history of source–drain voltage rather than the gate voltage.[173,174] The operation mechanism resembles "lateral" 2T devices where

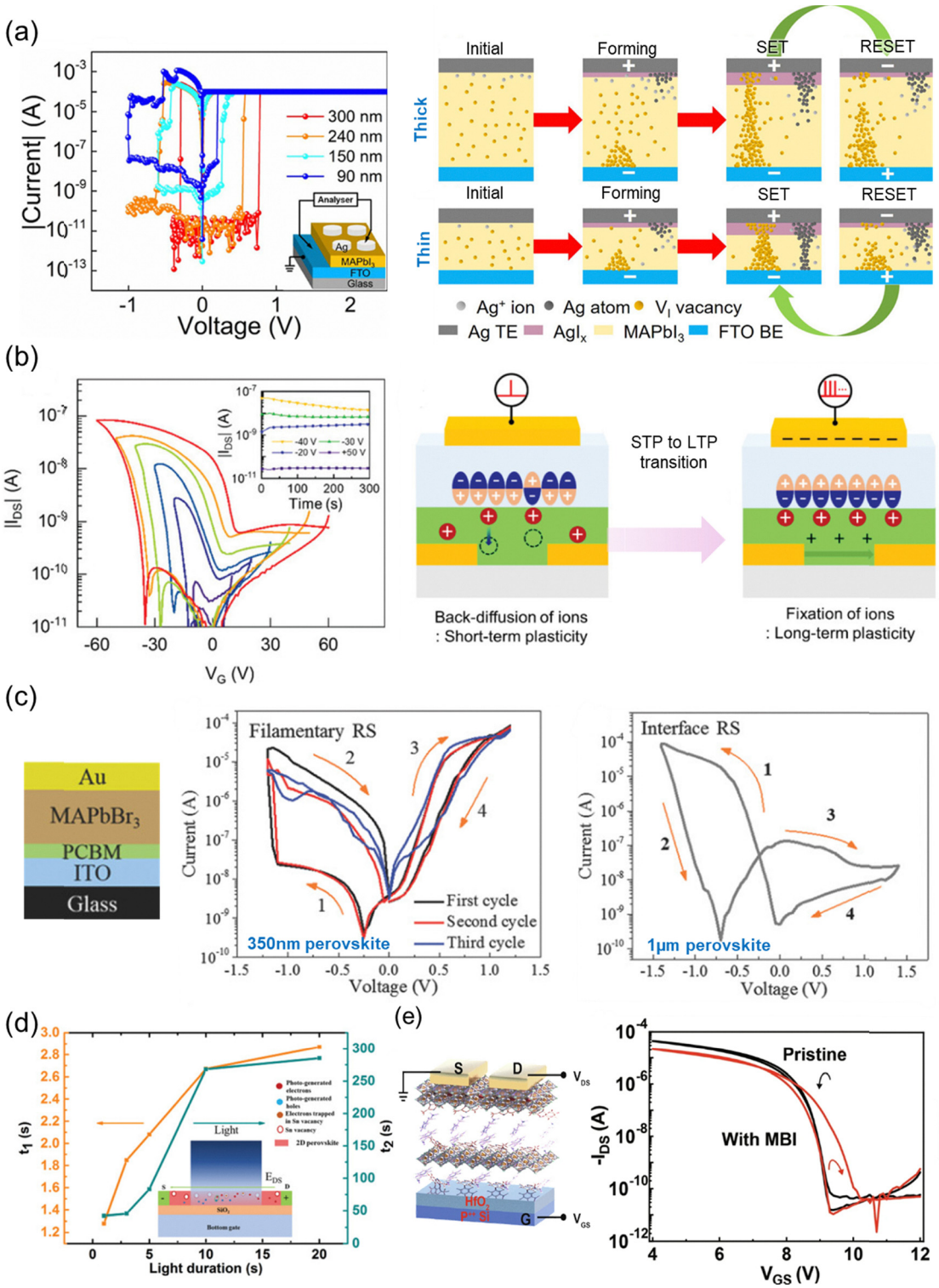

Fig. 11 (a) The current–voltage relationship for filamentary devices of different thicknesses (left) and the distinct filament formation mechanisms that occur in thick *versus* thin devices (right) reprinted with permission from ref. 89. Copyright 2018 American Chemical Society. (b) Drain current *vs.* gate voltage (transfer curve) for a ferroelectric mem-transistor with gate voltages swept from ±10 V to ±60 V (left) with the drain current retention in the inset, measured after sweeps to V_G = +50, −20, −30, and −40 V. The mechanism showing how the gate voltage modulates ion motion in the perovskite, inducing a transition from short-term to long-term plasticity with increasing pulse width (right) reproduced from ref. 175, under the terms of the Creative Commons CC BY 4.0 license (https://creativecommons.org/licenses/by/4.0). (c) The device structure (left) together with the current–voltage relationship of the devices with various perovskite thickness indicating transition from filamentary to interfacial type with increasing perovskite thickness, reproduced from ref. 171 with permission from John Wiley and Sons, Copyright 2017. (d) The time constants of photocurrent decay, fast (t1) and slow (t2), plotted against the duration of light pulses. The inset illustrates the charge-trapping process induced by Sn vacancies in Sn-based mem-transistor devices. Reproduced from ref. 192 with permission from John Wiley and Sons, Copyright 2019 (e) the device structure (left) and transfer curves (right) of a mem-transistor fabricated with and without a ferroelectric-induced dopant in the perovskite channel, reproduced from ref. 176, under the terms of the Creative Commons CC BY 4.0 license (https://creativecommons.org/licenses/by/4.0).

the injection barrier of the devices are modulated due to self-doping mechanism of the perovskite especially at the electrode/perovskite interfaces. The gate voltage was utilized to modulate the retention time of the memristor to a certain degree.[174] Short term gate modulatable ion migration have also been observed in $Cs_{0.05}MA_{0.15}FA_{0.7}PbBr_{0.5}I_{2.4}$ based mem-transistor with optical excitation.[194] To further extend the retention of the devices and/or "write" with gate voltage, a ferroelectric gate dielectric could be utilized to freeze and control the ionic distribution within the perovskite layer.[175] This enables both STP and LTP, depending on the strength and duration of the applied gate voltage (Fig. 11b). In STP, ion back-diffusion dominates, leading to temporary changes, while stronger or longer gate pulses immobilize ions, resulting in persistent conductance states (LTP). This ion redistribution alters the perovskite's doping level, thereby modulating its electrical conductivity.

3.2.2.2. Interfacial reaction. Aside from the formation of conductive filaments, interfacial reactions between migrating ions in halide perovskites and reactive electrode materials can also modulate charge transfer barriers at the electrode interfaces. For instance, reversible chemical interactions between silver (Ag) and iodide ions have been reported, leading to the formation of AgI at the $CsPbI_2Br/MoO_3/Ag$ interface.[195] The gradual development of the AgI interfacial layer improves overall device conductivity by promoting more efficient charge injection. However, its partial instability under weak electrical stimuli contributes to the short-term plasticity effects commonly observed in memristive behavior.[195]

As this mechanism is generally correlated with the early state of filament formation, it is also important to note that switching behavior in perovskite memristors is often a result of multiple coexisting mechanisms rather than a single dominant process. For instance, although ionic migration remains the underlying mechanism for resistive switching, increasing the thickness of the perovskite active layer shifts the switching behavior (Fig. 11c) from a filamentary type ($\sim$350 nm) to an interfacial type ($\sim$1 μm).[171] In addition, a reactive transport layer adjacent to the perovskite tends to promote filamentary-type memristive switching, whereas a more inert or benign transport layer favors the formation of interfacial-type memristors.[172]

3.2.2.3. Charge trapping/de-trapping. Depending on the fabrication protocols, perovskite often have a high density of defects either on their surface or in the bulk, which can trap either electrons or holes. When a forward bias is applied, these defects capture electrons or holes, creating beneficial p-type and n-type contacts either in bulk or interfaces which leads to transition from HRS to LRS states. Conversely, as the traps gradually release their charge, the device reverts to the HRS.

Generally, resistance of devices with this mechanism scales with device area in contrast to typical filament-based models.[167,190] Charge trapping/de-trapping induced resistive switching have been found in both Schottky emission or space charge limited conduction (SCLC) based devices. For example, the electrical memristive behavior in the $Au/MAPbI_3/FTO$ device have been observed due to electrons trapping and de-trapping in both bulk defects and interface states. While the initial Schottky barrier at $Au/MAPbI_3$ interfaces result in no resistive switching behavior, air exposure triggers chemical degradation (loss of iodine) at the perovskite surface, which act as donor-like interface states and reduces the Schottky barrier. Instead, the mechanism involves both SCLC and electron trapping in bulk states, where electrons fill trap states until saturation during the HRS-to-LRS transition. The LRS is maintained until a negative voltage is applied, which facilitates electron release from traps (including *via* Joule heating), thus resetting the device back to HRS. This cycle demonstrates bipolar non-volatile memory behavior.[190] Negative differential resistance (NDR) has also been observed at higher voltages as interface defects begin to trap electrons, shifting the Fermi level and suppressing current. On the other hand, modulation of Schottky barrier could also be utilized to create resistive switching in $Au/MAPbI_{3-x}Cl_x/FTO$ device.[167] Here, the HRS to LRS switching mechanism is attributed to lowering of Schottky barrier at perovskite/Au interface through hole trapping at the perovskite/Au interface to quasi ohmic interface. These trapped holes are stabilized in deep-level defects, enabling non-volatile memory. Upon applying a negative voltage, the holes are extracted, the Schottky barrier height increases, and the device resets to HRS.

Not limited to electrical excitation, light can also trigger charge trapping and de-trapping processes in halide perovskites. Photo-assisted switching have also been observed where photogenerated holes are trapped, lowering the switching voltages and energy consumption. In addition, by tuning light and voltage inputs, multiple stable resistance states can be achieved, demonstrating potential for low-power, multi-level memory applications.[167] In the $CsPbBr_3$ system, photogenerated carriers interact with defects, where electrons become trapped at defect sites, leading to an excess of free holes and creating a photodoping effect. This selective trapping enhances photoluminescence and forms the basis of the memory effect, as the trapped charges persist beyond the excitation pulse, effectively storing information about prior stimuli. This behavior is quantitatively described using an extended Shockley–Read–Hall (SRH+) model, which incorporates the time-dependent dynamics of carrier trapping, de-trapping, and recombination. The memory relaxation time spans a broad temporal range: (1) from nanoseconds to milliseconds, where trapping and recombination dominate, enabling short-term memory and signal potentiation; and (2) seconds regime, where long-term memory emerges due to slow photoinduced evolution of defect properties, such as changes in trap density, energy levels, and capture rates caused by ion migration and photochemistry.[196] The dynamics of trap filling itself depend strongly on the spatial location of the trap states. Bulk traps were filled rapidly ($\sim$10 ns) due to the immediate trapping of photogenerated carriers in close proximity to these defects. In contrast, surface trap filling was significantly slower ($\sim$100 ns), as it relied on the drift and diffusion of band-edge carriers toward the perovskite surface. The accumulation of charges in surface traps also resulted in the formation of an interfacial charge layer, which in turn screened the internal electric field

and slowed down further carrier transport to the interface, creating a feedback mechanism that further slowed trap filling.[197]

In 3T devices, light induced electrical memory behavior have been observed in 2D lead-free perovskite ($(PEA)_2SnI_4$). The dynamic photocurrent response is governed by trap-related carrier relaxation processes within the channels or at the interface. Two distinct relaxation time constants exist: (1) the faster decay component that is linked to shallow traps, which allow for quick release of trapped carriers and (2) the slower component is associated with deeper traps that retain carriers for longer durations (Fig. 11d). This dual-trap model explains the coexistence of STP and LTP, mimicking biological synapses. In STP, short light pulses predominantly filled shallow traps, allowing the channel conductance to return quickly to its baseline due to rapid de-trapping. However, with longer or more intense light exposure, deeper traps become filled, leading to a stronger photogating effect and a prolonged retention of photocarriers. In some cases, deeply trapped electrons may not fully recombine, continuously generating holes *via* the photogating effect and leading to non-volatile switching behavior.[192] In other studies, heterojunctions comprising perovskite and an active channel material (such as IGZO,[198] pentacene,[166,199] and other organic molecules[200,201]) have been employed to construct 3T based memristors. In these designs, the perovskite functions as a sensitizer, generating and injecting photo-carriers into the active channel. These photo-carriers become trapped within the channel layer, leading to a persistent increase in conductivity, which enables long-term or short-term memory behavior.

3.2.3. Polarization switching. Ferroelectricity is rarely observed in halide perovskites due to their typically centrosymmetric crystal structures, which prevent spontaneous polarization. Most 3D halide perovskites, such as $MAPbI_3$, adopt cubic or tetragonal phases at room temperature—both of which are usually centrosymmetric and thus non-ferroelectric. However, ferroelectric behavior can be introduced by breaking the structural symmetry, for example by incorporating polar molecular dopants that create local dipoles through hydrogen bonding. This approach has enabled the induction of a substantial remanent polarization, with values as high as 23.2 $\mu C\ cm^{-2}$. Utilizing this ferroelectric perovskite channel in 3T devices allows resistive switching through polarization control *via* gate voltage (Fig. 11e). For instance, in field-effect transistors (FETs) with 2-methylbenzimidazole (MBI)-doped Sn-based perovskites, applying a positive gate voltage (+10 V) aligns polarization downward, attracting holes and turning the device ON. A negative gate voltage (−10 V) reverses the polarization, repelling carriers and switching the device OFF. This switchable polarization leads to non-volatile memory behavior. As compared to non-ferroelectric channel, the memory window expands significantly (from 0.02 to 0.85 V), and both polarization states remain stable for over 1000 seconds, confirming reliable memory functionality.[176] Artificial synapses utilizing 1D ferroelectric halide perovskite, have also been reported in 2T configuration (Au/[(*R*)-(−)-1-cyclohexylethylammonium]PbI_3/Si)[202] despite the low polarization value of the 1D perovskite (0.03 $\mu C\ cm^{-2}$).[203]

3.3. Techniques for characterizing the underlying mechanisms

A structured, multi-faceted approach is crucial for unravelling the resistive switching mechanisms in memristive devices (Fig. 12). Thus, an approach that integrates experimental techniques with computational simulations, enabling a detailed investigation of the physical and chemical processes governing memristor operation is necessary. Combining experimental and computational techniques provides a comprehensive understanding of resistive switching in memristors. First, it is essential to classify the underlying switching mechanism as either filamentary or interfacial. This is done by characterizing the device's behavior, particularly its LRS and switching time, in relation to its device area. Characteristics of filamentary devices include abrupt switching and an LRS that is independent of device area variation. Following this, electrical transport studies can be employed to uncover the dominant conduction mechanisms and extract activation energy barriers. Time-resolved analyzes further provide insight into the kinetics of ion migration and defect dynamics. A range of spectroscopic and high-resolution imaging techniques can be utilized to identify the ionic species or charge carriers involved in the switching process. In addition, *in operando* imaging methods allow for real-time observation of resistive switching behavior, while computational simulations offer predictive insights for device performance optimization. This integrated approach enhances the understanding of memristor operation, supporting the development of more reliable and efficient memory and computing systems.

3.3.1. Electrical characterization – electrical transport mechanism and switching dynamic analysis. To differentiate between filamentary or interfacial type mechanism, the dependency of current responses with device area should be conducted. If LRS is not modulated by device area, it indicates that the process are governed by localized filamentary mechanism.[167] A filamentary memristor would theoretically exhibit apparent linear resistance scaling with area only if a constant areal density of filaments were maintained. However, this is practically impossible due to the stochastic nature of filament formation, which is influenced by random defect generation, non-uniform vacancy distribution, and spatial variations in ion migration pathways. In oxide memristor, scaling device area below $\sim 100\ nm^2$ may often leads to abrupt SET/RESET transitions, as single conductive filaments dominate transport and rupture stochastically. This contrasts with larger-area devices ($>1\ \mu m^2$), where analog-like conductance modulation arises from the collective reset of multiple filaments at varied voltages, mimicking gradual switching.[205] However, in interfacial mechanism, smaller areas may reduce the probability of distributed ionic defects trapping/detrapping at heterogeneous sites, suppressing analog behavior and favoring abrupt switching.[206]

Next, the conduction mechanism in the devices can be analyzed to better understand the origin of the switching behavior. Conduction mechanisms in semiconductor films are generally categorized into two main types: electrode-limited and bulk-limited. Electrode-limited mechanisms—such as Schottky

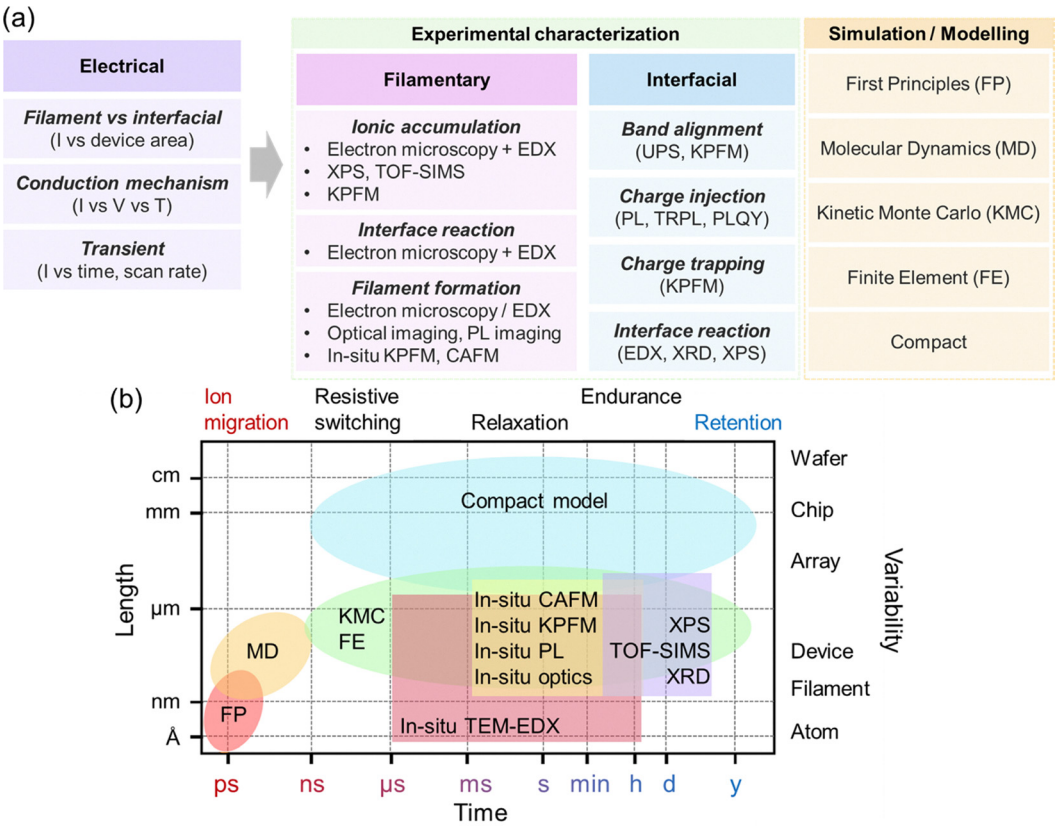

Fig. 12 (a) Conceptual illustration depicting the diverse approaches employed to investigate the fundamental switching mechanisms in perovskite-based memristive systems. (b) Overview of the spatial and temporal resolution capabilities of different modeling and characterization techniques used in device analysis adapted from ref. 204. Note: EDX is energy dispersive X-ray spectroscopy, TOF-SIMS stands for time-of-flight secondary ion mass spectrometry, KPFM denotes Kelvin probe force microscopy, XRD stands for X-ray diffraction, PL refers to photoluminescence, TRPL denotes time-resolved photoluminescence, UPS represents ultraviolet photoelectron spectroscopy, and PLQY stands for photoluminescence quantum yield.

emission, Fowler–Nordheim tunneling, direct tunneling, and thermionic-field emission—are primarily governed by the electrical properties at the electrode/semiconductor interface. Key factors include the barrier height and the effective mass of charge carriers. Studying these mechanisms provides insight into interface-related properties, such as the energy barrier and charge carrier dynamics across the contact. In contrast, bulk-limited mechanisms—such as Poole–Frenkel emission, hopping conduction, ohmic conduction, SCLC, ionic conduction, and grain-boundary-limited conduction—are controlled by the intrinsic properties of the semiconductor material. These include trap energy levels, carrier mobility, trap density and spacing, dielectric relaxation time, and the density of states near the conduction band. The dominant conduction mechanism in a device can be influenced by several factors, including temperature (T), electric field (E), device architecture, electrode material, semiconductor type, film thickness, and fabrication method. Since these parameters affect both the interface and the bulk properties of the material, a comprehensive evaluation of all these factors is essential when investigating conduction behavior in semiconducting systems.

Depending on the conduction mechanism, various relationship between current and voltages as well as temperature exist (Table 3).[207] Hence, to determine the dominant conduction mechanisms, temperature-dependent current–voltage (I–V) measurements (typically from 90 K to 400 K) can be performed. Curve fitting of I–V characteristics helps identify drift dominated (such as ohmic, SCLC, or Schottky emission) or hopping conduction (such as Poole-Frenkel emission or hopping conduction) behaviors.[208] Additionally, Arrhenius plots of inverse temperature ($1/T$) against log current or conductance are used to extract activation energies, offering insights into energy barriers affecting charge carrier or defect mobility.

Conduction in the LRS of devices is typically attributed to Ohmic behavior, resulting from the formation of conductive filaments or fully filled traps conduction.[209,210] On the other hand, conduction in HRS typically follows either ohmic,[210] SCLC,[211] Poole Frenkel emission,[212] or Schottky emission[209] mode depending on their device structures and voltage range. In memristor, the SCLC behavior may stem from the presence of deep-level trap states or the disruption of previously formed conductive pathways.[213] In addition, an appearance of NDR region appears is generally a characteristic of trap-assisted conduction at the interfaces which in some cases can be linked to Poole–Frenkel emission model[213] and SCLC.[190]

In filamentary mechanism, examining the dependence of switching voltage on the voltage sweep rate provides insight into the kinetics of the switching process and the role of defect

Table 3 Summary of conduction mechanism in semiconducting devices from ref. 207. The electric field (E) is defined as the voltage (V) divided by the thickness (d) of the semiconducting material, while I is the current and T is temperature during measurement

Conduction mechanism	Origin	I–V relationship	T dependent
Schottky emission	Thermal excitation of electrons over the potential barrier at metal/dielectric interface	$I \propto T^2 \exp(-\sqrt{E}/T)$	Strong
Fowler–Nordheim tunneling	Electrons tunnel through the metal/dielectric barrier due to the applied electric field	$I \propto E^2 \exp(-1/E)$	Weak
Direct tunneling	Electrons tunnel directly through the metal/dielectric barrier without needing thermal excitation.	$I \propto \exp(E)$	Weak
Thermionic-field emission	A combination of thermionic and field emission.	$I \propto E \cdot \exp(-1/T) \cdot \exp(E^2/T^3)$	Moderate
Poole–Frenkel emission	Electrons are emitted from traps within the material due to the electric field.	$I \propto \exp(-\sqrt{E}/T)$	Strong
Hopping conduction	Electrons move between localized trap states in the material.	$I \propto \exp(E/T)$	Moderate
Ohmic conduction	Movement of free electrons in the conduction band or holes in the valence band	$I \propto E$	Weak
SCLC	The current is limited by the space charge created by trapped carriers.	Follows different power laws (ohmic: $J \propto E$, trap-filled limit: $J \propto E^m$, Child's law: $J \propto E^2$)	Moderate
Ionic conduction	Movement of ions under an applied electric field	$J \propto \exp(-(1/T - E/T))$	Moderate

migration. Increasing the voltage scan rate leads to higher SET (V_{SET}) and RESET voltages (V_{RESET}) and RESET currents (I_{RESET}).[214] This is because at higher scan rates, the migrating species have less time to respond to the electric field, requiring more voltage to initiate switching. Conversely, at lower scan rates, the species are under the electric field's influence for longer, requiring less voltage for switching. Compliance current also plays a crucial role in controlling the size of the conductive filament during the forming and SET processes. It protects the device from hard breakdown and influences the on/off ratio, which significantly increases with higher compliance currents. This suggests that adjusting I_{CC} can optimize the memristor's switching characteristics. While LRS does not scale with device area, the forming voltage and on/off ratio of HOIP memristors decrease as the device area increases due to higher HRS. In addition, I_{RESET} increases with increasing device area.[214]

Transient response analysis provides further understanding by assessing how quickly the current changes during switching events. These studies shed light on the time-dependent dynamics of state transitions and defect interactions and therefore could differentiate between charge modulated or ion modulated memristor. For example, oxide based ionic-based memristors exhibit an exponential decay ($I \sim e^{(-\beta \cdot t)}$) of the LRS, in contrast to memristors that operate *via* charge trapping and de-trapping mechanisms, where the LRS follows a power-law decay ($I \sim t^{-\alpha}$).[215] In addition, ionic based memristor generally have longer retention time as well as time response as ion has longer time dynamics as compared to electronic charged related phenomena.[216] In the interfacial switching case, the charge trapping/detrapping and ionic self-doping mechanisms can be differentiated by measuring the device's switching time and relaxation time. This is due to the inherent difference in kinetics[217] where the capture time of electronic defects is reported to be much faster than their relaxation time, implying that charge trapping/detrapping memristors should exhibit fast switching but slow relaxation. In contrast, similar kinetics are observed for ions migrating toward or away from an interface, which leads to comparable rise and relaxation times in ionic-based devices. In filamentary case, ionic mobility increases exponentially with temperature which accelerate the filament dissolution. Hence, retention tests at elevated temperatures quantify filament stability, with activation energies from Arrhenius extrapolation guiding material selection for non-volatile memory applications.

3.3.2. Physical characterization – identification of migrating ions in filamentary devices. To investigate the ionic species involved in conductive filament formation, along with their concentration profiles and morphologies during SET (formation) and RESET (rupture) processes, multiple spectroscopic techniques can be employed. These include electron microscopy coupled with elemental analysis, optical spectroscopy, molecular/elemental characterization techniques, and various AFM-based spectroscopies such as conductive atomic force microscopy (CAFM) and Kelvin probe force microscopy (KPFM). While the strengths, limitations, as well as measurement artifacts of different spectroscopic techniques for probing ionic migration in halide perovskites have been extensively reviewed previously,[36] the following section delves deeper into how these methods can be specifically applied to reveal the underlying mechanisms in memristive devices.

In general, halide perovskites consist of a relatively soft ionic lattice structure, making them particularly vulnerable to damage under high-intensity excitation sources such as electron beams, photons, or X-rays during characterization. Additionally, these materials exhibit high sensitivity to environmental conditions, including exposure to moisture, oxygen, and elevated temperatures, which can further degrade their structural integrity and chemical stability. Therefore, careful control over the excitation intensity—such as reducing electron beam current or limiting photon and X-ray exposure—is crucial to prevent structural damage and ensure accurate measurements. Furthermore, maintaining a controlled testing environment (*e.g.*, inert atmosphere or vacuum conditions) is essential to minimize environmental degradation effects. Implementing these precautions helps reduce measurement artifacts and ensures reliable and reproducible characterization results.

3.3.2.1. Electron microscopy and its elemental analysis. Cross-sectional scanning transmission electron microscopy (STEM) or SEM combined with EDX provides direct insights into ionic transport within perovskite layers, crucial for understanding memristor mechanisms. By analyzing atomic concentration profiles before and after applying an electrical bias, EDX should reveal any atom redistribution caused by electric field. For instance, in graphene/$(PEA)_2PbBr_4$/Au devices, Br^- concentration is uniformly distributed throughout the perovskite layer before voltage application. After applying pulsed voltage stress, STEM imaging reveals Br^- ion accumulation at the perovskite/Au interface. This observation confirms Br^- ion migration as a key mechanism driving resistive switching behavior.[220] SEM-EDX analysis of Ag/perovskite/Ag lateral devices revealed a gradient distribution of Ag atoms across the film after electrical bias, while the halide-to-Pb ratio remained uniform. This indicates that the formation of Ag filaments is more prominent when reactive Ag electrodes are employed.[221] In other studies, TEM with EDX reveals trace amounts of Ag in the perovskite layer after bias application, which are not present in fresh devices. This direct observation of Ag presence in the perovskite layer supports the proposed mechanism that synaptic behavior originates from the migration of Ag^+ and I^- ions, accompanied by AgI formation and annihilation at the $CsPbI_2Br/MoO_3$ interface. The formation of this AgI composite layer gradually improves device conductance by enhancing charge transfer capabilities, while its instability under weak stimulations explains the short-term plasticity behaviors observed in electrical measurements.[195] Aside from AgI interlayer formation at perovskite/Ag interface, filament formation induced by the migration of Ag^+ in the AgI interlayer has also been directly imaged with TEM in cross-sectional Ag/$MAPbI_3$/FTO device (Fig. 13a).[218] In other studies, Br^- ion-related conductive filaments have also been observed. Cross-sectional TEM images reveal conical-shaped filaments with larger diameters (~30 nm) near the graphene electrode and smaller diameters (~15 nm) near the Au electrode, supporting the proposed mechanism of Br^- ion migration from graphene to Au under positive bias.[220] Additionally, TEM captures partial filaments in various stages of formation, providing a detailed view of filament growth. These findings directly link nanoscale ionic dynamics and filament formation to the device's resistive switching behavior. Together, EDX coupled electron microscopy

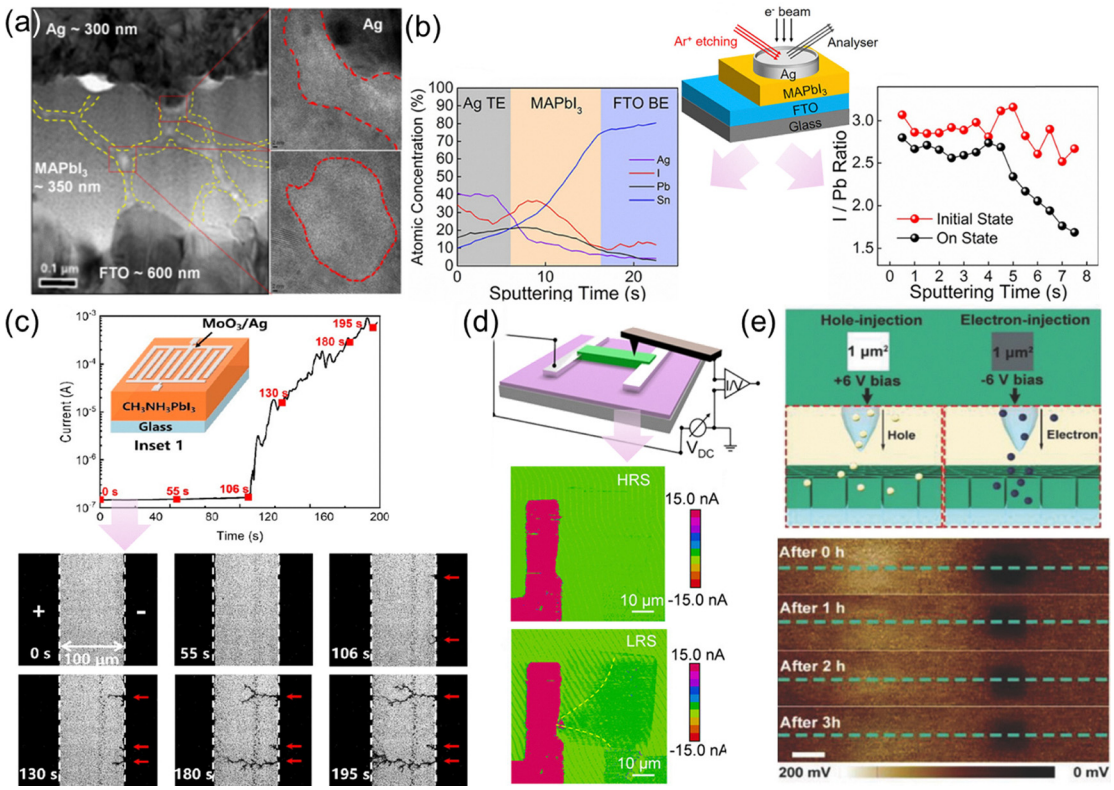

Fig. 13 (a) Cross-sectional STEM images of perovskite devices showing Ag migration at the interfaces (marked in red) and the formation of Ag conductive filaments (marked in yellow) reprinted from ref. 218, Copyright 2020, with permission from Elsevier. (b) The AES depth profiling setup (middle) together with the depth profiling result of the device after "writing" (left) as well as the I/Pb ratio of the perovskite before and after "writing" (right) reprinted with permission from ref. 89. Copyright 2018 American Chemical Society. (c) The current *versus* time (top) and *in situ* PL imaging of lateral device under constant voltage (10 V) at various timing (bottom), revealing the dynamic formation of Ag filaments within perovskite layers during "writing" reprinted with permission from ref. 210. Copyright 2024 American Chemical Society. (d) The CAFM setup (top) together with images of lateral perovskite memristors captured at HRS (middle) and LRS (bottom) reprinted with permission from ref. 219. Copyright 2020 American Chemical Society. (e) Schematic representation of a hybrid contact/KPFM mode setup (top), along with time-resolved KPFM data (bottom), demonstrating charge injection and trapping behavior in the perovskite layer reproduced from ref. 166 with permission from John Wiley and Sons, Copyright 2018.

and TEM comprehensively demonstrate how halide ion migration and filament formation govern memristor functionality.

3.3.2.2. Molecular or elemental analysis based spectroscopy. Molecular and elemental analysis using depth profiling techniques such as time-of-flight secondary ion mass spectrometry (TOF-SIMS), Auger electron spectroscopy (AES), and XPS can be employed to identify migrating species within the device. Depending on the device configuration (*i.e.* lateral *vs.* vertical), spatial mapping or depth profiling of molecular or elemental composition can be conducted to track ionic migration. For example, on vertical devices, TOF-SIMS depth profiling has revealed that, upon bias application, metal ions such as Ag^+ can penetrate into both the MoO_3 layer and the perovskite film.[210] Furthermore, *in situ* TOF-SIMS measurements on Au/$MAPbX_3$/Au lateral devices under electrical bias show that MA^+ ion migration is more prominent than that of halide ions (I^-/Br^-). The introduction of light exposure further enhances MA^+ migration while having minimal influence on halide ion movement.[53]

Similar to TOF-SIMS, AES and XPS could also be utilized to trace ionic migration in the devices. Migration of Ag atoms into perovskite layers as well as I^- migration closer to positive electrodes were observed with AES depth profiling (Fig. 13b) after bias application.[89] XPS depth profiling also provides evidence for the motion of Ag into the perovskite layer.[222] Beyond identifying migrating species, XPS is also a powerful tool for probing interfacial chemical reactions in perovskite-based devices. For instance, at the interface between perovskites and various metal electrodes (such as Ag, Al, Cr, Yb, and Au), redox reactions are expected to occur, involving the reduction of Pb^{2+} in the perovskite by the adjacent neutral metal film. XPS analysis revealed the presence of metallic lead (Pb^0) in all samples except those with Au electrodes, indicating that interfacial redox chemistry is electrode-dependent and suppressed when using inert metals like gold.[223] However, in other studies, XPS analysis of $MAPbI_3$/Au interfaces revealed migration of Pb and I species onto the Au surface, with binding energy shifts indicating interfacial redox reactions and underpotential deposition that accelerate degradation through volatile species formation. Comparisons with PbI_2/Au interfaces showed that methylammonium in $MAPbI_3$ promotes metallic Pb^0 formation and iodine loss *via* proton-assisted reactions, highlighting the distinct chemical behavior driven by organic cation presence.[224] These observations underscore how XPS can track elemental migration and chemical transformations at perovskite–metal interfaces by monitoring binding energy shifts and elemental concentration changes over time.

3.3.2.3. Optical microscopy. Aside from elemental analysis outlined above, the filament formation could also be visualized using *in situ* PL imaging.[210,221] Direct observation of conductive filament formation and rupture in real-time were monitored by applying an electric field to a lateral device structure (Ag/MoO_3/$MAPbI_3$/MoO_3/Ag). Ag filaments exhibit reduced PL emission, appearing as dark regions in PL imaging (Fig. 13c).[210] Under 470 nm excitation, they captured the entire switching process, revealing that filaments (observed as expanding dark regions) initially form near the negative electrode and continuously grow toward the positive electrode. This growth pattern corresponds perfectly with current measurements, showing a sharp increase when filaments connect both electrodes, signifying the transition from HRS to LRS. Similarly, when applying reverse bias, they could observe filament disconnection and reverse growth, providing direct visual evidence of the switching mechanism. Optical microscopy can also be utilized revealed the dissolution of Ag electrodes under electrical bias, suggesting that the released Ag contributes to the growth of conductive filaments.[221]

3.3.2.4. Atomic force microscopy (AFM). AFM based spectroscopy such as CAFM and KPFM offer valuable insights into the local electrical properties of halide perovskite memristors, helping to uncover their switching mechanisms. CAFM works by measuring the current flow through the material as a function of applied voltage, enabling researchers to map the spatial distribution of conductive pathways at the nanoscale. This technique is particularly effective for studying the formation and rupture of conductive filaments during switching cycles, which are key to understanding memristive behavior. Through current mapping, CAFM allows researchers to investigate how defects and ion migration contribute to filament formation, which is essential for device operation. For instance, CAFM measurements on lateral Ag/perovskite/Ag devices revealed distinct behaviors in different resistive states (Fig. 13d).[219] At LRS, higher surface currents are observed near the drain electrode, with the conductive area spreading more widely and gradually tapering toward the source electrode. In contrast, no significant current variation is observed across areas in HRS. These findings demonstrate that CAFM can effectively capture the tapered shape of conductive filaments, providing critical insights into their structure and dynamics during device operation. On the other hand, KPFM measures the contact potential difference (CPD) between the conductive AFM tip and the sample surface, providing insights into variations in local electronic states. This technique is particularly useful for studying the dynamics of electrons and ionic charge carriers. For instance, KPFM measurements on lateral Ag/perovskite/Ag devices under applied bias revealed potential changes at the perovskite/Ag interface, as well as a CPD gradient within the perovskite layer between the Ag electrodes. These observations suggest the accumulation of negatively charged species, likely halide anions, at the electrode/perovskite interface.[219]

3.3.3. Physical characterization – band alignment modulation in interfacial type devices. To investigate the underlying mechanisms in interfacial-type devices, three types of spectroscopic techniques can be utilized: (i) those that reveal the band alignment of the devices, (ii) techniques that assess their charge injection capabilities, and (iii) spectroscopic approaches that detect byproducts of interfacial reactions. For instance, ultraviolet photoelectron spectroscopy (UPS) and KPFM can be employed to examine the band alignment at the interface, serving as an indicator of whether carriers can be effectively injected into the adjacent layers. Additionally, optical spectroscopy techniques

such as time-resolved photoluminescence (TRPL), photoluminescence, and photoluminescence quantum yield (PLQY) provide direct insights into carrier injection dynamics across interfaces. Structural characterization methods, including X-ray diffraction (XRD), cross-sectional EDX, and XPS, can be employed to analyze the byproducts formed from interfacial reactions.

UPS is a powerful technique for probing the electronic structure and charge injection mechanisms in halide perovskite memristors. It provides crucial insights into the valence band positions (VBM) and Fermi level (E_F) alignment, enabling the assessment of carrier injection probabilities into adjacent layers. For example, UPS has been employed to investigate the energy band structures of silicon nanomembranes and $MAPbI_3$.[225] The band alignment between these two semiconductors can be constructed using their respective work functions and valence band positions obtained from UPS. The conduction band positions are then estimated by combining these UPS-derived valence band values with the optical bandgaps obtained from absorption spectra. This reconstructed band alignment reveals the probability of charge transfer from the perovskite layer to adjacent materials—for instance, how photo-generated holes in $MAPbI_3$ are transferred to the silicon nanomembranes, while the photogenerated electrons remain in the perovskite, providing critical insight into the device's working mechanism.

KPFM helps unveil the memristor mechanism by directly measuring surface potential changes associated with charge trapping and de-trapping events. In KPFM, the CPD between a conductive tip and the sample surface is measured, reflecting variations in local electronic states and charge distribution. For instance, *in situ* KPFM measurements on $CsPbBr_3$/PMMA/pentacene films under varied illumination wavelengths revealed systematic increases in CPD at shorter wavelengths, driven by photogenerated charges: holes transfer from $CsPbBr_3$ quantum dots to pentacene despite the existence of insulating PMMA in between, leaving electrons trapped in the perovskite layer.[166] Furthermore, the combination of biased contact mode and KPFM enables spatially resolved visualization of electron (under negative bias) or hole (under positive bias) injection into targeted regions of the perovskite layer (Fig. 13e). Subsequent CPD mapping showed distinct retention behaviors: electron-injected regions (bright contrast) retained approximately 70% of their initial surface potential after 3 hours, whereas hole-injected areas (dark contrast) retained only around 26%. These results confirm that persistent electron trapping within $CsPbBr_3$ quantum dots underpins the device's photonic memory and synaptic functionality, directly linking nanoscale charge dynamics to observed resistive switching behavior.

TRPL, steady-state PL, and PLQY are powerful optical techniques for probing charge transfer dynamics and trap-assisted recombination in halide perovskites. These tools are particularly valuable for identifying defect states and evaluating charge injection from perovskite layers into adjacent functional materials—processes that are critical to memory formation in perovskite memristors. A reduction in PL intensity, PLQY, or TRPL lifetime can signal either non-radiative recombination due to defects or efficient photo-induced carrier injection into neighboring layers. For instance, PL quenching has been observed when perovskites are paired with other semiconductor materials, supporting their role as photo-sensitizers capable of injecting carriers into channel layers, contributing to long-term memory effects.[200,201]

While steady-state PL captures radiative emission properties by measuring the intensity and spectral distribution of emitted light, TRPL offers complementary insights into carrier lifetime dynamics over broad timescales. PLQY quantifies emission efficiency by calculating the ratio of emitted photons to absorbed photons, providing a direct measure of a material's ability to convert absorbed light into luminescence. For example, steady state PL and TRPL was effectively employed to investigate the mechanism in $CsPbBr_3$ quantum dots-based memory transistor.[166] Introduction of a pentacene layer on $CsPbBr_3$/PMMA significantly quenched the PL signal, indicating efficient exciton dissociation and hole transfer from the perovskite to pentacene. TRPL further revealed reduced carrier lifetimes in the heterostructure compared to pristine $CsPbBr_3$/PMMA, confirming enhanced nonradiative recombination due to carrier extraction. These findings provide direct evidence for light-induced charge separation and trapping, central to the device's photonic memory and synaptic functionality.

Interfacial reactions between mobile ions in halide perovskites and chemically active electrode materials that modulate the carrier injection barrier could be probed by structural analysis such as XRD, XPS, and electron microscopy-EDX. Spatial mapping or depth profiling structural analysis of lateral or vertical devices can be performed to investigate interfacial reactions. For instance, interfacial reaction byproducts between NiO_x and perovskite layers have been identified through a combination of grazing incidence X-ray diffraction (GIXRD) and cross-sectional SEM, correlating with non-volatile switching behavior.[172] Using cross-sectional TEM combined with EDX, the formation of AgI at the $CsPbI_2Br/MoO_3/Ag$ interface has been demonstrated, playing a crucial role in modulating the device's resistance.[195] In addition, complementary XPS analysis, performed alongside TEM-EDX, can also be utilized to identify AgI formation at Ag/perovskite interfaces.[218] While TEM-EDX facilitates the spatial identification and quantification of elemental composition, XPS provides further insights into the chemical bonding states of the elements.

3.3.4. Theoretical models. To understand memristor switching mechanisms, aside from experimental characterization described above, simulations can also be conducted at different levels depending on the application. Physical modeling, including first-principles simulations, kinetic Monte Carlo models, and finite element analysis, investigates ion migration, conductive filament growth, and the interaction between microscopic and macroscopic performance factors. While these models provide detailed insights into processes like chemical distributions, temperature, and electric fields, they are limited in simulating circuit-level variations. On the other hand, compact models like SPICE focus on behavioral reproduction, making them more suitable for circuit integration, though they offer less physical detail. By linking first-principles, KMC, FE, and compact models in a multi-scale workflow, predictive

designs for stable, ultrafast perovskite memristors for neuromorphic systems can be achieved.

3.3.4.1. First principles calculation – atomic level. To investigate the conductive properties of stable states and the associated transition energies, first-principles (or *ab initio*) calculations are commonly employed. These quantum–mechanical simulations are performed without relying on empirical parameters but are instead grounded in the fundamental laws of quantum mechanics, and they often use large supercell models containing many atoms. *Ab initio* methods solve the Schrödinger equation (many electron wavefunctions) exactly, providing high accuracy but are computationally intensive and limited to small systems. DFT simplifies *ab initio* methods by using electron density instead of wavefunctions and approximates many-body effects through exchange-correlation functionals. This simplification reduces computational cost while maintaining a balance between efficiency and accuracy for larger systems. In memristive systems, especially those with specific doping configurations, device performance and reliability often hinge on the ionic defect formation energies and energy barrier for ionic migration, a key quantity effectively predicted by first principles methods. First-principles methods can also be utilized to calculate the VBM and CBM positions of perovskites, enabling the prediction of energy level alignment and contact barriers at perovskite/electrode or transport layer interfaces through analysis of band offsets, work function differences, and interfacial charge transfer effects. These simulations are also well-suited for modeling basic dynamic processes such as charging/discharging behavior, single halide ion migration, and resistance fluctuations.

For example, in $FAPbI_3$-based memristors, DFT simulations reveal how the migration of iodine vacancies (V_I)—believed to be responsible for filament formation—varies with the crystal structure. In the 1D hexagonal δ-phase, DFT calculations show that the migration barrier along the *c*-axis (0.48 eV) is significantly lower than that in the *ab*-plane (0.9 eV), favoring directional filament growth and easier RESET processes. In contrast, the 3D trigonal α-phase exhibits long-range vacancy interactions due to its smaller bandgap and overlapping electronic states, making filament rupture—and thus RESET—less favorable.[229] These insights, only attainable through first-principles methods like DFT, underscore how structural anisotropy governs memristive behavior. Expanding on this approach, DFT-based high-throughput screening was applied to 696 halide perovskite compositions across four structural types to identify optimal materials for fast and stable switching. Key descriptors (including formation energy, defect-formation energy, and halide vacancy migration barriers) were evaluated to assess thermodynamic stability and switching potential. Among the candidates, dimer-structured $Cs_3Sb_2I_9$ has a significantly lower vacancy migration barrier (0.47 eV) than its layered counterpart (0.57 eV), suggesting faster ion migration and thus quicker switching (Fig. 14a). These predictions were experimentally validated, with the dimer-based device exhibiting ultra-fast switching ($\sim$20 ns), while the layered form showed much slower response ($>$100 ns). By bridging atomic-scale defect energetics with device-level performance, DFT offers a powerful framework for designing next-generation memristor materials.[226]

However, significant challenges remain in bridging the gap between atomistic simulations and real-world devices. First principles methods struggle to accurately capture the complexities of polycrystalline, amorphous, or multi-layered structures, and their high computational cost limits their applicability to long-term or multi-physics simulations.

3.3.4.2. Molecular dynamics simulations. While first principles calculations are highly effective for calculating ground-state properties such as band structure, defect formation energies, and static charge distributions, it cannot directly capture time-dependent phenomena like ionic motions or thermal effects. To simulate such dynamic processes—particularly under applied electric fields—*ab initio* molecular dynamics (AIMD) is required. AIMD extends *ab initio* by incorporating real-time atomic motion, enabling the observation of field-induced structural evolution and its impact on electronic properties. In the case of monocrystalline methylammonium bismuth iodide ($MA_3Bi_2I_9$) nanowire-based memristors, AIMD simulations offered crucial insight into the origin of conductance modulation. Unlike conventional models that attribute switching behavior to halide ion migration and defect dynamics, the simulations revealed a distinct mechanism driven by the rotation of MA^+ clusters under an electric field (Fig. 14b). This reorientation induces charge exchange between MA^+ and the $Bi_2I_9^{3-}$ framework, leading to bandgap narrowing, increased n-type doping, and enhanced conductivity—correlating well with experimentally observed LTP. Thus, AIMD played a pivotal role in uncovering non-defect-based switching behavior in perovskite memristors, offering a deeper understanding of their synaptic plasticity.[227] Not limited to ions, MD simulations can also be used to study the ferroelectricity of perovskite/PVDF nanocomposites by examining the distribution of dipole moments within the material. These simulations reveal how poling enhances polarization by aligning the dipoles along the applied electric field. Additionally, the simulations demonstrated that the poled PVDF matrix stabilizes Frenkel defects in the perovskite through interfacial coupling, allowing the enhanced polarization to be retained even after the electric field is removed.[230]

3.3.4.3. Kinetic Monte Carlo simulations. To complement atomic-level insights from first-principles calculations, KMC simulations can be employed to explore stochastic atomic-scale processes over time in the devices. First-principles methods, such as DFT, accurately determine key material properties like migration barriers, charge distributions, and defect formation energies using quantum mechanics. Next, KMC simulations use these calculated energy barriers as inputs to stochastically model the time evolution of processes—like ion migration or filament growth—over much longer timescales, making KMC ideal for studying dynamic device behavior and long-term switching phenomena in memristors. Hence, this combination allows researchers to bridge the gap between atomistic precision and realistic device-scale dynamics in memristors. In contrast to MD simulations, KMC is particularly suited for

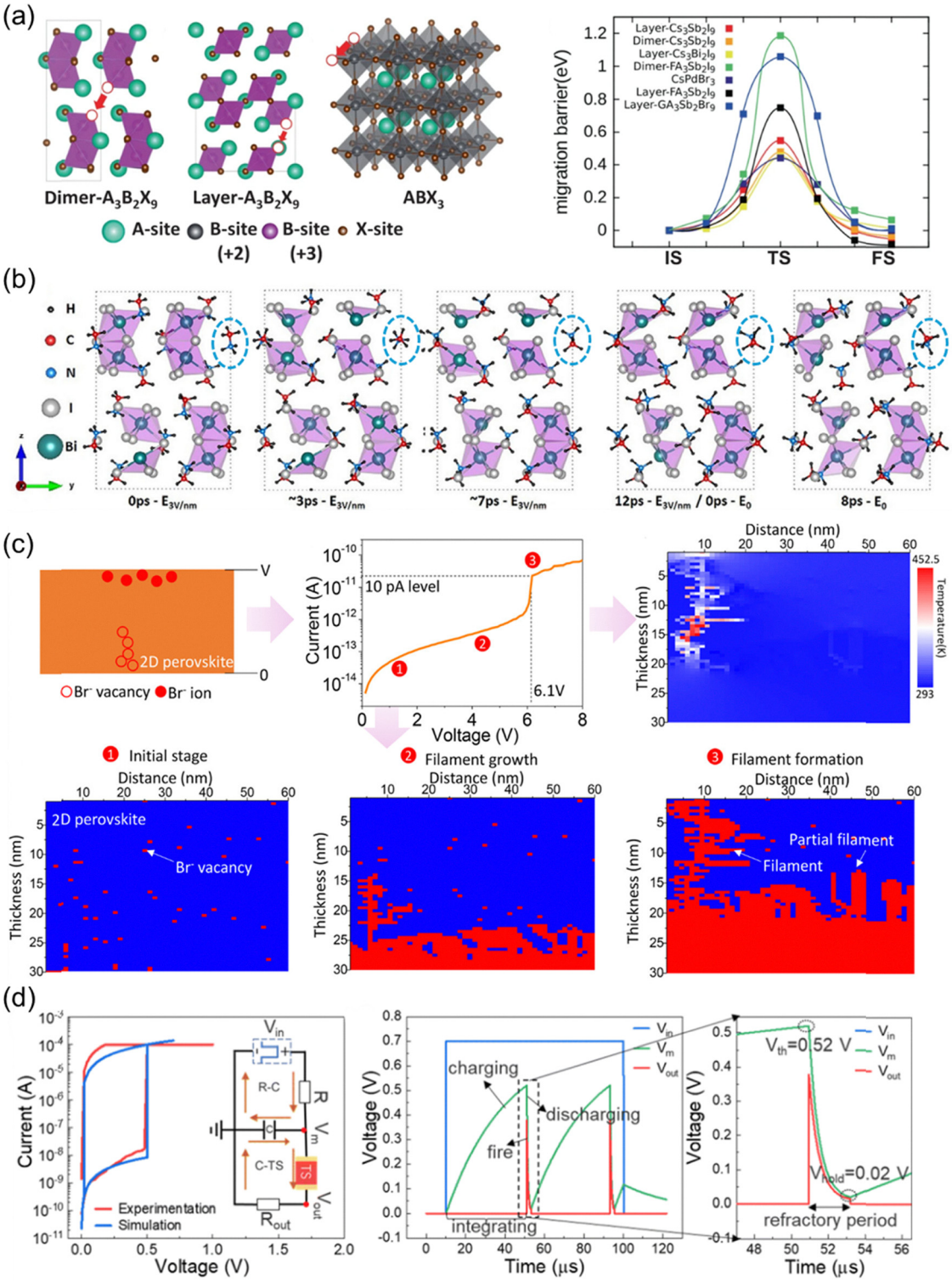

Fig. 14 (a) The crystal structure utilized (left) and the halide vacancy migration barrier (right) calculated with first principles method, reprinted from ref. 226. (b) The evolution of $MA_3Bi_2I_9$ crystal structure under an electrical filed, simulated with molecular dynamics where rotation of MA^+ ions is postulated under electric field, reprinted from ref. 227. (c) The basic structure of Monte Carlo simulation for $(PEA)_2PbBr_4$ film (top left), together with its simulated current–voltage evolution (top middle), temperature profile (top right), and the simulated cross section of the devices highlighting filament formation (bottom); reprinted with permission from ref. 220. Copyright 2017 American Chemical Society. (d) SPICE simulation of memristors showing the current–voltage relationship (left) and voltage *versus* time evolution (right), reproduced from ref. 228 with permission from the Royal Society of Chemistry.

scenarios involving nanosecond timescales or long-term retention. Being stochastic and event-driven, KMC stands out because it focuses on the occurrence of specific events over time rather than tracking every moment, making it more efficient for these types of simulations.[231]

For example, KMC simulation was used to model how iodine vacancies (V_I) form, migrate, and interact under varying voltages in 3D VCM devices, helping to explain the creation and evolution of conductive filaments in perovskite memristors. By simulating electric field, temperature, and defect dynamics at each lattice point, the model revealed how different compliance currents influence filaments width, resistance states, and switching voltages. It also clarified how Joule heating accelerates switching and affects retention, endurance, and the stability of resistive states.[232] Monte Carlo simulations using a trap assisted tunneling model were employed to understand how conductive filaments form in VCM based $(PEA)_2PbBr_4$ 2D perovskite memristors. The simulations, which assume Br^- ion migration drives filament growth, successfully reproduced key experimental results, including switching voltage, current levels, and thermal effects (Fig. 14c). The process unfolds in three stages: initial ion accumulation, partial filament formation, and complete filament growth, which aligns with TEM and AFM observations. The model also explains how elevated temperatures influence device resistance, further validating trap assisted tunneling as a mechanism for memristive switching behavior.[220]

3.3.4.4. Finite element analysis. First-principles atomistic simulations offer detailed insights into key material properties relevant to memristor operation, such as halide vacancies and ion migration, but they are computationally expensive and limited to small-scale systems. In contrast, FE is a numerical technique that models macroscopic device behavior by solving partial differential equations over discretized meshes. FE enables simulation of electrical, thermal, and mechanical interactions—such as current–voltage characteristics, heat dissipation, and stress distribution—with high spatial resolution. It is particularly effective in modeling resistive switching behavior, including the formation and rupture of conductive filaments, although it typically relies on empirical models and may not fully capture stochastic effects.

To address the stochastic nature of memristor switching, KMC simulations offer a complementary approach by modeling atomic-scale processes like ion migration and filament dynamics over time. While KMC captures variability and endurance in switching behavior, it also demands detailed knowledge of transition rates and can be computationally intensive. Ultimately, both FE and stochastic methods like KMC and MD depend on accurate input parameters and assumptions. Integrating FE with first-principles methods helps bridge the gap between atomic-scale mechanisms and device-level performance, improving the overall predictive power and reliability of memristor simulations.

To integrate microstructural analysis, first-principles calculations, and COMSOL based FE to uncover the mechanisms behind fast and reliable switching in Cs_2TiBr_6 memristors. AIMD simulation confirm the structural stability and low formation energy of bromide vacancies (V_{Br}), enabling their field-induced migration. These ordered vacancies form well-defined conductive pathways and generate a localized electric field superposition, enhancing vacancy diffusion and mitigating randomness in conductive filament growth. To further explore the dynamic switching process, a COMSOL-based FE model is used to simulate the formation and rupture of filament by the tracking vacancy concentration, electric potential, and temperature during SET and RESET operations. The model incorporates physical laws such as Fick's diffusion, Fourier's heat conduction, and current conservation to explain how V_{Br} migrate under bias, how Joule heating assists filaments rupture, and how localized temperature affects conductivity. The simulated *I–V* characteristics closely match experimental results, validating the model's predictive power. Together, these approaches reveal how vacancy structure and thermal effects govern filament dynamics and memristor performance.[143]

In addition to electrically driven ion migration, light-induced ion migration has also been simulated. *Ab initio* calculations focused on iodine vacancies in neutral (V_I) and positively charged (V_I^+) states showed that under illumination, electron excitation from defect states into the conduction band altered the vacancy's charge state, reducing the ion migration barrier from 0.74 eV to 0.41 eV. This behavior, linked to changes in Pb–Pb distances, explains how light enhances ion mobility in 2D perovskites. To complement this understanding, a FE model in COMSOL was developed to simulate electrostatic potential, temperature, and charge transport in a carbon nanotube (CNT)/perovskite photo-memristor. The model demonstrated how doping and gate voltage variations influence the CNT potential, validating photogating effects. Ion redistribution in the perovskite altered the local field near the CNT, affecting current flow, with p-type doping enhancing this effect. Despite some discrepancies with experimental data, the simulations confirmed the importance of perovskite dielectric behavior and photogating in device performance.[233]

3.3.4.5. Compact models for circuit design. Modeling of memristors can be categorized into different levels based on device application requirements. Physical modeling (such as first principles, KMC, and FE) delves into the underlying mechanisms, such as ion migration and the relationship between microscopic distributions and macroscopic performance. It provides detailed insights into processes like conductive filament growth and rupture, allowing for the simulation of chemical distributions, temperature, and electric fields. However, it is limited in simulating circuit-level variations. In contrast, compact modeling focuses on behavioral reproductions using simulation tools like simulation program with integrated circuit emphasis (SPICE), which are more suitable for circuit integration. Compact models rely on empirical assumptions and mathematical fitting to measured data, making them simpler but less physically detailed. This distinction allows researchers to select the appropriate model based on their need for either an in-depth understanding of physical processes or practical integration into circuit designs.[231]

The SPICE model is typically developed based on equations or circuits that describe the current–voltage relationship and state variable dynamics, incorporating various parameters that capture the ion drift mechanism within the perovskite layer. These parameters are fitted using various experimental data to accurately reproduce the device's behavior.[234] This enables large-scale circuit-level simulations, which help designers explore the potential of perovskite memristors in applications like power-on-chip or artificial neural networks. For instance, SPICE was used to simulate the leaky integrate-and-fire dynamics of artificial neurons based on volatile switching memristors. The memristor's *I–V* behavior was modeled using Verilog-A, allowing the simulation of how the memristor acts as a neuron by integrating input signals and firing when a threshold is reached (Fig. 14d). This approach helps validate the memristor's ability to mimic biological neuron functions, such as generating spike currents and recovering to a resting state, which is crucial for spiking neural networks applications.[228] By simulating these dynamics, SPICE simulations help in understanding how memristors can be used to build efficient and scalable neuromorphic computing systems. In other studies, SPICE-based analytical models have been employed to fit experimental data on memristor performance across different testing protocols, revealing that current conduction in these devices is governed by tunneling processes in the OFF state and ohmic behavior in the ON state.[214] This methodology not only validates the memristive behavior of halide perovskite based devices, which exhibit bipolar resistive switching, but also facilitates the optimization of memristor performance by adjusting testing parameters like compliance current and scan rate.

4. Perovskite based memristors

Building on the perovskite composition effects detailed in Section 2 – particularly their influence on ionic migration speeds – and the memristive mechanisms explored in Section 3, this section examines how these factors collectively govern key device metrics. The ionic migration rate, dictated by perovskite composition (for example, the type of halide or A-site cations), directly modulates resistive switching behavior. Material parameters such as grain size and defect density, which are often shaped by fabrication methods like solution processing or annealing, also play a critical role in determining ion migration rates. Smaller grains or higher defect concentrations can accelerate ion diffusion by creating low-energy pathways, while dense, crystalline films can suppress unintended leakage currents. Thus, compositional design and synthesis-driven microstructure synergistically define the performance of perovskite memristors. While the intrinsic ionic migration rate, governed by composition, defect density, and lattice strain, fundamentally determines memristive switching metrics, device engineering strategies are equally important for achieving optimal performance. This section will discuss key design considerations, including substrate selection, perovskite fabrication protocols, electrode materials, and interface engineering. These work together to modulate resistive switching behavior by controlling ion migration pathways, interfacial redox kinetics, and film uniformity. Halide perovskite memristors generally consist of several layers – substrate, bottom electrode, halide perovskite, buffer layers, and top electrode (Fig. 15). The following discussion will examine each layer's specific impact on device performance and outline strategies to enhance memristor performance. Three primary strategies to improve device efficiency are interfacial engineering, compositional engineering, and electrode engineering; these will be discussed in depth in a later section.

4.1. Effect of configuration

The configuration and orientation of the electrodes play a crucial role in determining the device's mode of operation. Halide perovskite neuromorphic devices usually have either 2 or 3 terminals and will be explained in the next section. While both configurations exist, the majority of the works reviewed here are on 2T structures.

4.1.1. Two terminals. 2T devices can be arranged in either a vertical or a lateral configuration. In a vertical device, the various films are sandwiched between the bottom and the top electrodes. In this case, the distance between the two electrodes is usually <1 μm, allowing operation at low voltages. Memristors as vertical devices are fabricated as either dot or crossbar arrays. In dot arrays, the bottom electrode is usually a continuous sheet extending to all devices, and the top electrode is patterned as square or circular dots. In crossbar arrays, both electrodes are patterned as parallel bars oriented orthogonally to each other. Generally, the halide perovskite films are not patterned and extend throughout the substrate area. So, the individual device area is defined as the area of the top electrode in dot arrays, and the area of intersection of the top and bottom electrodes in crossbar arrays. The area of the device is a crucial design parameter for interfacial processes. For example, in filamentary memristors, a higher device area reduces the high-resistance state, as the conduction occurs through the entire device area, but does not heavily affect the low-resistance state, as the conduction is through local filaments. Contrarily, both conductance states scale with device area for memristors operating *via* interfacial mechanisms.[171] Between dot and crossbar arrays, the percentage of published literature is heavily skewed towards the former, owing to the ease of fabrication and testing. While it is acceptable to conduct mechanistic studies of the memristor on dot arrays, the eventual implementation of memristors in applications such as in-memory computing must be on crossbar arrays. It must be noted that device performance is not necessarily extrapolable from dot to crossbar arrays, as several factors, such as probe tip pressure, sneak path, and line resistance, are not considered.[235,236] The later sections will discuss this in more detail.

In a lateral device, the two terminals are deposited on the same plane, either at the bottom or top of the perovskite film. The distance between the electrodes is usually >1 μm, which increases the operation voltage. In vertical devices, the various functional layers could be stacked simply by serial deposition. The lateral configuration does not have that option unless

sophisticated patterning techniques are used. A major advantage of lateral devices is that the perovskite film between the electrodes is exposed. This can be leveraged in multimodal memristors.[237] The two terminals can be used to feed and read electrical signals, and simultaneously, the exposed perovskite film can receive optical inputs without necessitating transparent electrodes. Lateral devices are also well-suited for mechanistic studies. The exposed perovskite film can be subjected to various material characterization techniques to probe the phenomena *in situ.*[210]

Besides vertical and lateral, researchers have also developed special device architectures to enhance the performance. To regulate the growth of stochastic conductive filaments in halide perovskite memristors, a novel electrode architecture can be developed. For example, an electrode with a tip-shaped Au bottom contact significantly enhances the local electric field at the tip, thereby guiding the growth of conductive filaments in a more confined and localised manner (Fig. 15, 2nd from the right).[238] Compared to conventional planar structures, the tip-induced field results in a lower and more uniform set voltage (~ -0.11 V), reduced power consumption, and a remarkably high on/off ratio of 10^8. By mitigating the stochasticity of filament formation, this approach improves both device reliability and switching consistency. The intensified electric field at the tip ensures more reliable filament formation during the set process and more complete rupture during reset, enhancing endurance and uniformity. As a result, the tip-engineered device exhibits outstanding cycling stability (over 4000 cycles) and data retention exceeding 10^4 seconds.

4.1.2. Three terminals. As discussed earlier, the 3T architecture is adopted in building mem-transistor wherein perovskites are used as photosentizer, floating gate, or active layer. In an electrical mem-transistor with perovskites as the active channel material, the gate electrode can be leveraged as a self-selecting device, which is critical for suppressing sneak path currents in a crossbar architecture, which will be discussed further in Section 5.2. This has been demonstrated in a gate-tunable quadruple cation halide perovskite memtransistor.[174] Mem-transistor's conductance modulation (from HRS to LRS) can be achieved by applying the drain voltage, similar to lateral 2T devices, while further conductance states fine tuning are achievable with gate modulation at LRS.[173,174] Besides using SiO_2, a standard gate dielectric, ionically active or ferroelectric gate dielectric materials are also explored, which enable further fine control of the conductance state over a longer time period. In an ion-gel (PVDF-HFP and [$EMIM^+$][$TFSI^-$]) gated perovskite (PEA_2SnI_4) mem-transistor, the operation voltages were dramatically reduced owing to the high capacitance of the dielectric.[239] Moreover, the operation mechanism involving the migration of $EMIM^+$ cation provided a linear and symmetric conductance modulation, highly desirable in constructing artificial neural network accelerators. The retention time of the mem-transistors can be further modulated with ferroelectric gate dielectric such as P(VDF-TrFE), where gate voltage application would partially halt ion relaxation in the device.[175]

The additional electrode also allows different sources of inputs to be received by the mem-transistor. This advantage has been conceived in multimodal neuromorphic devices where optical and electrical inputs are simultaneously programmed to conduct complex in-sensor computing tasks. In a triple-cation halide perovskite mem-transistor, the perovskite layer was used as both the semiconducting channel and the photosensitive material. The device was used to demonstrate optical learning and electrically tunable forgetting. The multimodal operation also allowed reconfigurability between 'AND' and 'OR' gates. Alternatively, the halide perovskite layer can simply be used as a photosensitizer. In an amorphous oxide transistor, based on indium gallium zinc oxide (IGZO), $CsPbBr_3$ quantum dots were spin-coated to aid in realizing light-dependent non-volatile memory.[237] Another report on multimodal 3T mem-transistors that are both optically and electrically (from the gate) sensitive includes $Cs_{0.05}MA_{0.15}FA_{0.7}PbBr_{0.5}I_{2.4}$ as the active channel to

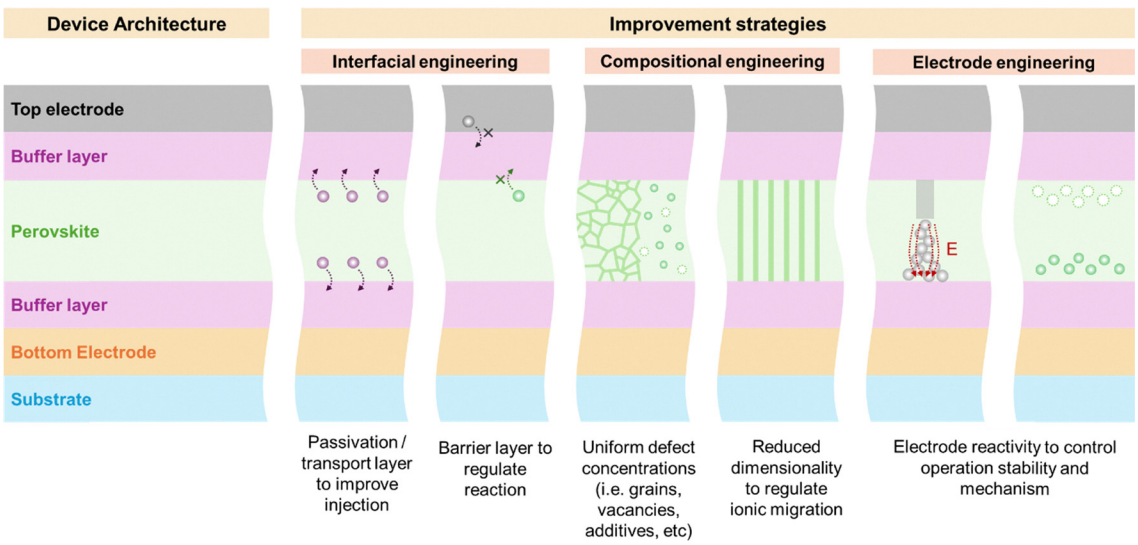

Fig. 15 Strategies to improve the performance of halide perovskites-based memristors.

induce gate-tunable photo-response. This structure allows photo-detecting pixels with reconfigurable logic functionalities and flexible learning and forgetting behaviors.[194]

4.2. Versatile substrate selection for perovskite memristor devices

Due to the low-temperature processability of halide perovskites, a wide variety of substrates can be used-including both conventional rigid substrates and flexible alternatives. This versatility enables halide perovskites to be adapted for diverse applications, ranging from traditional electronic devices to next-generation flexible and wearable technologies. Glass substrates coated with transparent conductive oxides, such as ITO and FTO, have been used predominantly in halide perovskite memristors. Other rigid substrates, such as Si/SiO_2, have also been utilised for memristor applications. Notably, halide perovskites possess favorable mechanical properties, such as a low shear modulus, which imparts good ductility and flexibility.[240] Their low-temperature processability further allows synthesis on polymeric substrates, making it possible to fabricate devices on flexible and bendable materials such as polyethylene terephthalate (PET), polyimide (PI), poly(ethylene 2,6-naphthalate) (PEN), polydimethylsiloxane (PDMS), carbon cloth, fiber, and paper.[241–245] This opens new avenues for applications such as flexible and wearable electronics.[246]

The first flexible halide perovskite memristor was demonstrated in a 2T configuration using $MAPbI_3$ thin films on a PET substrate.[247] The switching operation was stable for >100 bending cycles with a bending radius of 7.5 mm (Fig. 16a and b). Operational stability at a low bending radius of 5 mm was increased to >400 switching cycles by adding hydroiodic acid (HI) into the $MAPbI_3$ precursor for an improved morphology.[248] Halide perovskite-based flexible memristors have been considered for various neuromorphic use cases, such as synapses,[249,250] neurons,[228] nociceptors,[251] reservoir computing,[252] and photomemristors.[244] Recently, a 16×16 memristor crossbar array was reported using a halide perovskite 1D inorganic lattice, (propyl)-pyridinium lead iodide, which is the largest flexible crossbar array implementation till date (Fig. 16c and d).[122] Apart from the substrate and the active layer, the flexibility of electrodes must not be overlooked and will be discussed in a later section. While flexible perovskite transistors have been reported previously,[253,254] to date, no reports have been found on flexible 3T perovskite memory transistors.

An unorthodox form factor conducive to integration in smart textiles was demonstrated by a fibrous crosspoint memory based on halide perovskites (Fig. 16e–g).[255] $MAPbI_3$ was dip-coated on Al fibres and interwoven with bare Al fibres. Non-volatile filament memristors were formed at each intersection point with 10^4s of retention and 500 cycles of endurance. The unique architecture maintained stable resistive switching across different bending angles of the interwoven fibres, displaying potential application in electronic textiles. Apart from the substrate and the switching layer, the flexibility of the electrode must not be overlooked and will be discussed in the following section. Despite the progress in flexible halide perovskite memristors, large-scale integration into wearable electronics has remained elusive. Several interesting works have showcased use cases such as waterproof luminescent textiles[256] and triboelectric nanogenerators.[257]

4.3. Perovskite compositions

In memristors, halide perovskite layers function either as the switching medium or a photosensitive component, depending on the operational mechanism. Key factors such as crystal structure, dimensionality (2D *vs.* 3D), and defect formation energy critically influence ion migration dynamics, which directly impact device performance.

The perovskite composition critically governs memristor performance (Table 4) by modulating both electronic properties and ionic migration dynamics. For instance, quasi-2D perovskites – engineered by incorporating large organic cations into 3D frameworks – exhibit wider bandgaps that elevate Schottky barriers at electrode interfaces, suppressing leakage currents in the HRS and boosting on/off ratios.[106] Additionally, the large organic cations positioned between the quasi-2D perovskite layers provide improved environmental protection through the hydrophobic properties of their alkyl amine groups. This hydrophobicity prevents moisture penetration into the active layer, significantly enhancing device storage stability under ambient conditions.[105] Concurrently, ionic migration rates – pivotal for switching energy and retention time – can be tailored through compositional design. For example, the E_A for A-site cation migration can be tuned depending on the choice of A-site cation, as bulkier FA^+ and MA^+ cations exhibit higher E_A compared to the smaller Cs^+ cation. This leads to longer relaxation times and enhanced PPF in FA- and MA-based memristors.[60] Incorporating bulky 2D molecules into the 3D perovskite structure to create a quasi-2D structure helps suppress ionic migration, thereby enhancing memory retention by stabilizing the internal ionic distribution while maintaining its energy consumption comparable to biological synapses (1–10 fJ per synaptic event).[258] While a higher ionic migration rate can lower the energy needed for switching, it may also compromise the retention time of the memristor, as ions can easily diffuse back to their original positions. Therefore, achieving a balanced ionic migration rate is crucial to maintain both low switching energy and adequate retention time.

Aside from the compositional engineering described above, defect engineering serves as a powerful tool to optimize perovskite memristors, enabling precise control over resistive switching by targeting halide vacancies and trap densities. In VCM-based devices, controlling halide vacancies in perovskite films offers an effective strategy to enhance the HRS and reduce variability in conductive filament formation. For instance, moderate incorporation of iodide ions into $CsPb(Br_{1-x}I_x)_3$ quantum dots has been shown to suppress the generation of random bromine vacancies on the $CsPbBr_3$ QD surface.[155] This suppression leads to a significant increase in HRS resistance and improves the on/off current ratio by nearly two orders of magnitude. In addition to boosting switching performance, iodine doping enhances the structural stability and charge

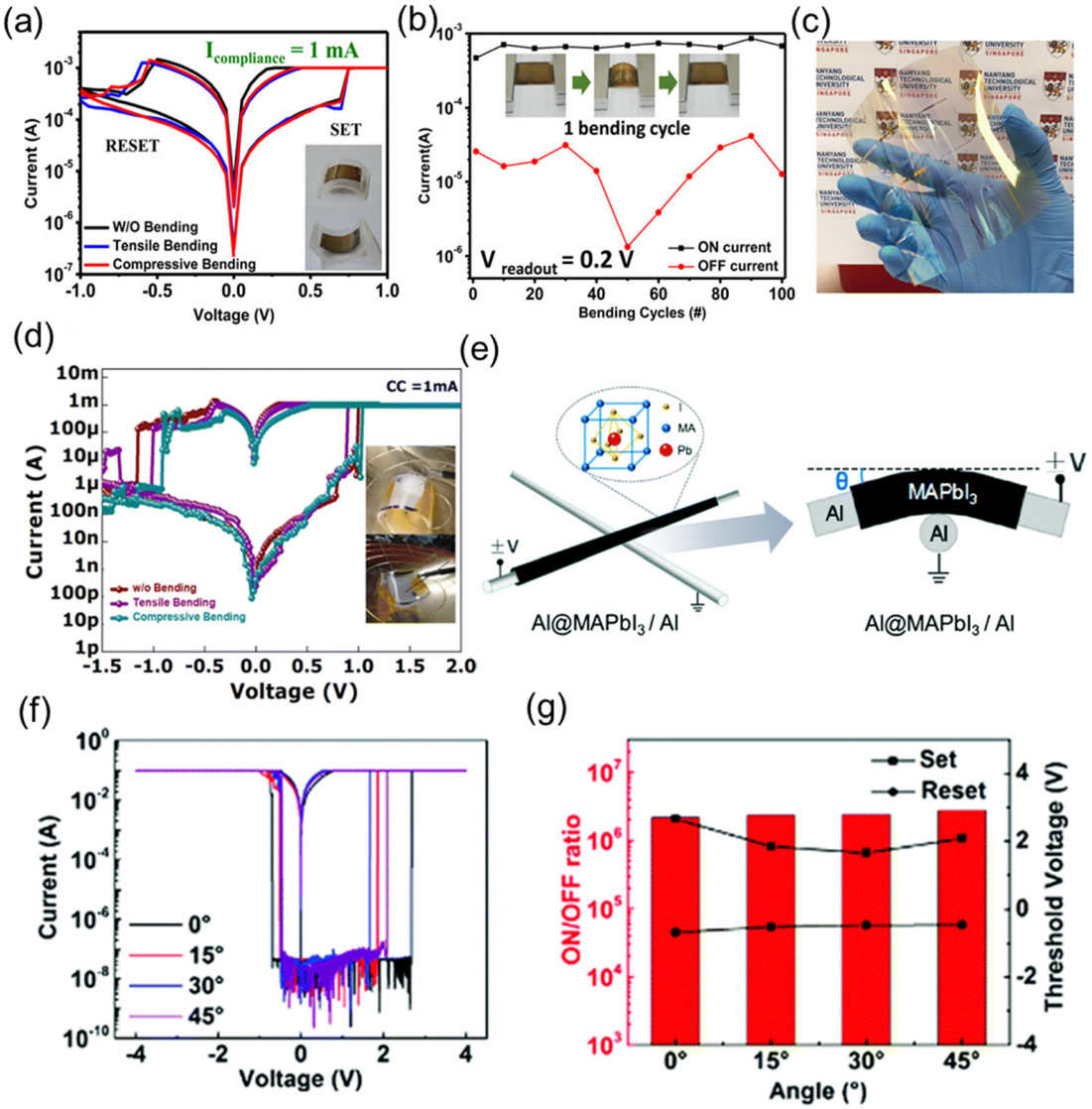

Fig. 16 (a) The first halide perovskite-based halide perovskite memristor on PET substrate. *I*–*V* characteristics without and with bending stresses (tensile and compressive bending radius = 1.5 cm).[247] (b) Bending stability of repetitive bending cycles (>100). (a) and (b) Reprinted with permission from ref. 247 Copyright 2016 American Chemical Society. (c) Photograph of the large-area dot-point memristor array (~50 000 elements over 100 cm^2) fabricated on a flexible PET substrate.[122] (d) *I*–*V* resistive switching characteristics of the flexible memristors under extreme bending conditions (tensile and compressive bending radius = 1.5 cm). (c) and (d) Reproduced from ref. 122 with permission from the Royal Society of Chemistry. (e) Fibrous crosspoint perovskite RRAMs illustration with an architecture of Al@$MAPbI_3$/Al.[255] (f) *I*–*V* curves at different angles (0°, 15°, 30°, and 45°), (g) SET/RESET voltage, and the corresponding on/off ratios. (e)–(g) Reproduced from ref. 255 with permission from the Royal Society of Chemistry.

transport properties of the QDs. Notably, it increases the ion migration barriers near vacancy sites, thereby minimizing the stochastic nature of filament formation. As a result, the devices exhibit greater resistive switching stability and improved overall reliability. Another effective strategy to control memory characteristics in halide perovskite devices is tuning the trap density. Reducing trap densities *via* surface passivation led to a more rapid saturation of trap occupancy compared to unpassivated, defect-rich devices.[197] Furthermore, such passivation approaches have proven successful in diminishing the long-term memory effects, indicating that the extent and duration of memory can be engineered by managing defect populations at the surface.[196] Bulk defect passivation has also been shown to be successful in tuning the memristor relaxation time in a 3T Sn-based memristor.[192] Hence, defect engineering-whether through vacancy suppression or trap management-offers complementary strategies to modulate switching endurance, reliability, on/off ratio, and retention time in perovskite memristors.

While Section 2 thoroughly reviewed ionic migration rates across perovskite families – including 3D, low-dimensional, and lead-free variants (*e.g.*, Sn-, Bi-, or Cu-based halides) – these analyzes often overlook/embed the role of processing parameters in modulating intrinsic material properties. To address this gap, this section focuses on perovskite engineering strategies that tune ionic migration dynamics and material behavior by examining external factors such as deposition

Table 4 The comparison of the performance parameters for representative perovskite non-volatile memristors

Structures/materials	On/off ratio	V_{SET}/V_{RESET} (V)	Endurance (cycles)	Retention (s)	Stability	Ref.
3D Organic–inorganic hybrid perovskites						
ITO/$MAPbI_3$/Al	10^3	+3/−3	300	—	60 days	259
Al@$MAPbI_3$/Al	10^6	+1.66/−0.47	500	10^4	—	255
ITO/$MAPbI_3$/ZnO/Au	10^2	+1/−0.6	—	—	30 days	186
ITO/$MAPbI_3$:$ADNH_3I$/Al	10^8	−0.3/+2	2×10^3	10^4	30 days	260
Pt/$FAPbI_3$/Ag	10^6	+0.17/−0.19	2×10^3	—	30 days	261
Au/$MAPbI_3$ nanowire in porous alumina membrane/Ag/ITO	10^7	+0.19 to +4.8/−0.078 to −3.6	6×10^6	$\sim 8.7 \times 10^7$	—	161
Al/$MAPbCl_3$ nanowire in porous alumina membrane/Ag	10^7	+3/−2.6	3×10^6	$\sim 7 \times 10^9$	>300 days	162
3D all-inorganic perovskite						
Ag/$CsPbBr_3$/Ag	10^9	+0.8/−0.4	150	10^4	—	262
ITO/$CsPbBr_3$/Ag	10^2	+2.5/−0.55	100	—	—	263
ITO/$CsPbBr_3$/Au	10	+0.29/−0.22	400	400	—	264
ITO/PMMA/$CsPbBr_3$ quantum dots/PMMA/Ag	10^5	+2.6/−2.8	5×10^3	10^5	—	189
Quasi 2D or 2D perovskite						
Graphene/$(PEA)_2PbBr_4$/Au	10	+2.8/−1	100	10^3	—	220
Si/SiO_2/Ti/Pt/$(PEA)_2Cs_3Pb_4I_{13}$/Ag	10^9	+0.2/−0.1	200	2×10^3	14 days	105
ITO/PEDOT:PSS/$(3\text{-AMP})(MA)_{n-1}Pb_nX_{3n+1}$/PMMA/Ag	10^3	+0.52/	10^3	2.2×10^4	200 days	108
ITO/$(BDA)MA_2Pb_3I_{10}$/PMMA/Au	—	±1.8 to ±3	50	10^4	7 months (film)	110
Lead-free perovskite						
ITO/$Cs_3Sb_2I_9$/Al	10^4	+0.4/−3.2	100	10^4	—	265
ITO/$MA_3Sb_2Br_9$/PMMA/Ag	10^2	−0.2/+0.45	300	10^4	—	266
ITO/$Cs_3Bi_2Br_9$/Ag	10	+1/−0.5	3.2×10^3	10^3	—	267
ITO/SnO_2/$Cs_2AgBiBr_6$/NiOx/Ag	50	+0.7/−0.7	300	10^3	—	268
Au/$Cs_2AgBiBr_6$@PMMA/ITO	10^4	+1.5/−1.5	10^3	10^4	—	269
Al/$Cs_3Cu_2I_5$/ITO	65	−0.36/+0.17	200	10^4	—	148
ITO/$Cs_3Bi_2I_9$/Au	10^3	+0.3/−0.5	10^3	10^4	30 days	146
ITO/$Cs_2AgInCl_6$/Au	$\sim 10^3$	~+1/−0.85	1500	10^4	7 days	152
ITO/$Cs_2AgInCl_6$/Ag	$\sim 10^4$	~+0.8/−0.7	1129	—	—	
ITO/$Cs_2AgBiBr_6$/Au	>10	+1.53/−3.4	10^3	10^5	>3 months	150
1D or 0D perovskite						
ITO/PEDOT:PSS/$PrPyr[PbI_3]$/PMMA/Ag	10^5	+0.5/−3	450	10^4	—	270
ITO/PEDOT:PSS/$PrPyr[PbI_3]$/PMMA/Ag	10^3	+0.7/−1	2×10^3	10^5	—	122
Pt/PEDOT:PSS/Cs_4PbBr_6/Au	10^2	+0.4 to +1.4/−0.2 to −0.55	100	10^4	—	123

techniques and processing conditions, and their direct impact on device performance. We have summarized the various deposition techniques used to fabricate perovskite memristors, along with the key parameters that influence film properties and a comparison of their advantages and disadvantages, in Table 5.

4.3.1. Spin coating. Spin coating remains the predominant technique for fabricating halide perovskite thin films. For solution-processed materials, solute-solvent interactions play a critical role in determining film quality, where solvent properties like volatility, basicity, and polarity govern crystallization thermodynamics and kinetics.[271] Key parameters influencing the morphology, grain

Table 5 Summary of the advantages and disadvantages of various processing techniques of halide perovskites

Technique	Advantages	Film quality	Scalability	Challenges
Spin coating (solution)	• Low-cost and versatile • Ease of tunability *via* solvent/antisolvent engineering and additives	Moderate to high	Low (batch processing)	• Non-uniform films at large area • Solvent toxicity • Interface compatibility issues due to difficulty in finding orthogonal solvents
Vapor deposition (vapor)	• Solvent-free and highly uniform • Compatible with complex architectures	High	Medium (batch processing)	• Equipment-intensive • Difficulty in controlling organic evaporation • Precursor volatility mismatch
Blade coating (solution)	• Continuous deposition • Efficient material use • Tunable *via* preheating, speed, gas quenching, *etc.*	Moderate to high	High (R2R-compatible)	• Underexplored for memristor applications
Single crystals (solution)	• Defect and grain boundary-free • Excellent optoelectronic quality	Excellent	Low	• High ion migration barrier • Slow and hard to scale

size, thickness, and properties of perovskite films include solvent selection, precursor ratio/concentration, antisolvent treatment, and precursor additives. These factors can be tailored to optimize perovskite memristor performance for target applications and will be elaborated further below.

Typical spin-coating precursors involve dissolving metal halides and organic ammonium salts in polar aprotic solvents such as dimethyl formamide (DMF), dimethyl sulfoxide (DMSO), γ-butyrolactone (GBL), *N*-methyl-2-pyrrolidone (NMP), *etc.* Solvent engineering through binary or ternary mixtures (*e.g.*, DMF: DMSO) can optimize film properties.[272] For instance, DMF alone produces fibrous, pinhole-riddled films due to rapid solvent evaporation, while adding DMSO slows crystallization *via* stronger Pb^{2+} coordination and reduced volatility, yielding denser films with larger grain sizes.[273] This principle was applied in Dion-Jacobson perovskite 3-(aminomethyl) piperidinium lead iodide ($3AMPPbI_4$)-based filamentary memristors, where varying the DMF : DMSO ratio modulated grain size: smaller grains increased grain boundary density, enhancing ionic migration and filament formation while reducing the high-resistance state and on/off ratio (Fig. 17a).[154] Growing concerns over the toxicity of solvents like DMF[274] have spurred interest in greener alternatives.

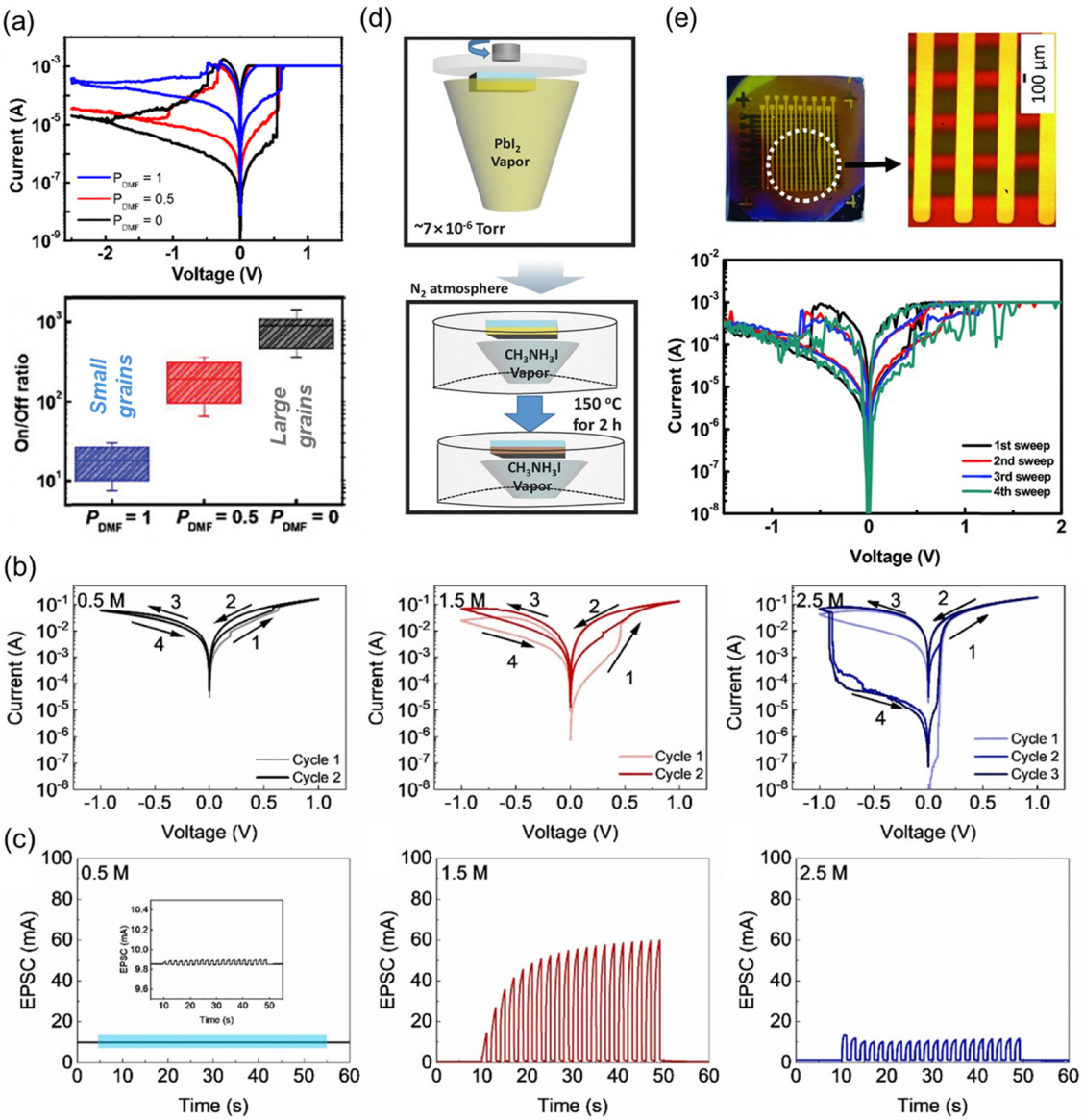

Fig. 17 (a) *I*–*V* characteristics of the (3AMP) PbI_4 devices (top) and statistical distribution of ON/OFF ratio with different DMF percentage in DMF: DMSO solvent to modulate the grain sizes (bottom). Reprinted with permission from ref. 154 Copyright 2022 American Chemical Society. (b) Properties of the synaptic devices made from thin films, 0.5 M, 1.5 M, and 2.5 M. *I*–*V* characteristics at a sweeping rate of 0.1 V s^{-1} under dark conditions.[275] (c) Photocurrent generated by 20 light pulses with an intensity of 12 mW cm^{-2} and a duration of 1 s (light wavelength: 450 nm), under the applied voltage of −0.02 V. (b) and (c) Reprinted from ref. 275, Copyright 2025, with permission from Elsevier. (d) Schematic illustration of sequential vapor deposition. The PbI_2 is thermally evaporated in vacuum first, and the MAI vapor is used to convert the PbI_2 layer to the $MAPbI_3$ perovskite thin film.[279] (e) Photograph and optical microscopy images of the fabricated device and the *I*–*V* curves. (d) and (e) Reproduced from ref. 279 with permission from John Wiley and Sons, Copyright 2017.

Acetonitrile (ACN), with comparable polarity and a low boiling point (82 °C), enables thermal annealing-free crystallization. This facilitated room-temperature synthesis of flexible $MAPbI_3$-based synaptic devices, where rapid crysatallization minimized disordered electronic states and improved charge transport, achieving ultralow energy consumption (~13.42 aJ per synaptic event).[163]

The stoichiometric ratio of A-site and B-site precursors also impacts defect density and ionic mobility. Excess A-site or B-site cations influence defects and carrier concentrations.[191] In spin coating, the thickness of the film can be controlled by changing the precursor concentration. For example, the thickness of $MAPbI_3$ can be varied from 90–300 nm, where thicker films showed higher set voltages, LRS, and HRS.[89] Similarly, in $MAPbBr_3$-based photomemristors, precursor concentrations of 0.5 M, 1.5 M, and 2.5 M were tested, with the 1.5 M device achieving the widest conductivity modulation range (Fig. 17b and c).[275] These findings underscore that precursors optimization (*e.g.*, ratio, concentration) could be modulated to tailor perovskite for specific application requirements.

During spin coating, antisolvent (a solvent miscible with the precursor solvent but does not dissolve perovskite) is often introduced to induce supersaturation, promoting homogeneous nucleation, and finally enhancing film uniformity. The selection of antisolvent (*e.g.*, toluene, chlorobenzene) and the timing/method of its application (*e.g.*, dripping *vs.* vapor exposure) critically influences film morphology and device performance. For example, the effect of antisolvent dripping was compared in a $MAPbI_3$-based filamentary memristor.[276] Films spin-coated with toluene as the antisolvent were much smoother (RMS roughness = 9.51 nm) than those without (RMS roughness = 37.4 nm). Devices without antisolvent required higher set voltages due to increased contact resistance from uneven surfaces, highlighting how antisolvent directly influences the interfacial quality and electrical behavior.

Another effective strategy to control memory characteristics in perovskite devices is tuning the trap density. Reducing trap densities *via* surface passivation led to a more rapid saturation of trap occupancy compared to unpassivated, defect-rich devices.[197] Furthermore, such passivation approaches have proven successful in diminishing the long-term memory effects, indicating that the extent and duration of memory can be engineered by managing defect populations at the surface.[196] Bulk defect passivation has also been successful in tuning the memristor relaxation time in a 3T Sn-based memristor.[192] The influence of the defect density on the device performance was further studied by varying the defect density between 3.34–33 × 10^{15} cm^{-3} through solvent engineering in a filamentary memristor.[277] The lowest set voltage was observed for the film with the lowest defect density. This was explained by correlating the onset of the trap-filled limited conduction region with the filament formation process. A higher defect density implied a higher trap-filled limited voltage and hence a higher set voltage.

4.3.2. Vapor deposition. Aside from spin coating, perovskite films could also be deposited *via* vapor deposition methods. While spin coating is widely used for its simplicity, low cost, and rapid processing, it faces challenges in achieving film uniformity over large areas due to unpredictable fluid dynamics of liquid precursors, restricting its practicality to substrates smaller than 10 cm^2. Additionally, film thickness is limited by the solubility of perovskite precursors in solvents, and uniformity heavily depends on the solvent–substrate contact angle. Substrates must also be flat and smooth to avoid disrupting precursor flow during spinning, which complicates integration with textured surfaces. In contrast, vapor deposition methods, such as thermal evaporation, bypass many limitations of solution processing. Perovskites can be deposited *via* single-source evaporation (using pre-synthesized perovskite powder) or co-evaporation (separately vaporizing metal and organic precursors to react on the substrate). Vapor deposition excels in producing uniform, pinhole-free films over large areas and is generally less sensitive to substrate topography, making it suitable for scalable manufacturing.

Vapor deposition of halide perovskites has been shown to produce more uniform films than solution processing.[278] Exploiting this, a highly uniform inorganic perovskite memristor for reservoir computing was demonstrated.[195] $CsPbI_2Br$ thin film was deposited using dual-source evaporation. In the 4-bit test for reservoir computing, the standard deviation in the final conductance from 20 devices was ≈2.5%. The low variation resulted in a superior image recognition performance.

Vapor deposition technique also enables uniform deposition of perovskite on top of textured surfaces.[279] In this architecture, an insulating SiO_2 layer was deposited on the substrate, and via-holes were patterned using photolithography followed by reactive ion etching (Fig. 17d and e). Sequential thermal evaporation of PbI_2 and methylammonium iodide (MAI) filled these *via*-holes with $MAPbI_3$, forming isolated perovskite-active regions embedded within the SiO_2 matrix. This approach prevented crosstalk between adjacent devices by leveraging the insulating properties of SiO_2, enabling scalable fabrication of perovskite memristor arrays. Such vapor-deposition-based methods for creating patterned perovskite device arrays will be explored in greater detail in Section 5.

The challenge of identifying orthogonal solvents (which do not attack underlying layers) inhibits the deposition of multiple perovskite layers *via* solution processing. Vapor deposition circumvents this limitation, enabling precise stacking of perovskite films with tailored properties. This capability was demonstrated in a bipolar photomemristor featuring two stacked perovskites with distinct bandgaps, which achieved retinomorphic color perception through wavelength-dependent conductivity modulation.[280]

However, spin coating remains the popular choice due to the highly sophisticated equipment required for vapor deposition, as well as its complexity in adjusting the perovskite composition and properties. This stems from high vapour pressure, low evaporation enthalpy,[281] and omnidirectional evaporation properties[282] of organic halides like MAI and FAI, which make it extremely challenging to precisely control their evaporation rates during deposition. This mismatch in evaporation behavior between lead compounds and organic halides complicates their co-evaporation process, often leading to issues like cross-contamination and interference between different source materials. As a result, instead of relying on a single-step vacuum

deposition, sequential deposition approaches, either entirely dry or combining dry and wet processes, are considered more suitable and scalable for future industrial manufacturing of perovskite-based devices.[283] Additionally, with the vapor deposition method, halide perovskites also lose the edge of exceptional, low-cost solution processability over other semiconductors.

4.3.3. Blade coating. Spin coating and vapor deposition are inherently batch processes: spin coating processes one substrate at a time, while vapor deposition handles one batch per cycle. In contrast, blade coating enables continuous, high-throughput fabrication through roll-to-roll compatibility, making it industrially scalable. In blade coating, a liquid precursor is dispensed onto the substrate and spread uniformly using a blade, significantly improving material efficiency compared to spin coating. Key parameters like blade height, shearing speed, precursor concentration, and viscosity can be modulated to control film thickness and morphology. Moreover, morphology can also be tailored by preheating the substrate and gas quenching.[284] Entirely roll-to-roll manufacture of perovskite solar cell modules in ambient conditions on a flexible substrate has been demonstrated.[285] Blade coating remains underexplored for halide perovskite memristors, with only a handful of studies reported to date. One notable example is a blade-coated quasi-2D perovskite memristor based on $(BA)_2MA_4(Pb_{0.5}Sn_{0.5})_5I_{16}$ (Fig. 18a).[286] This forming-free device demonstrated robust performance, including endurance exceeding 2000 cycles, retention over 10^5 seconds, and several synaptic functionalities. The results highlight blade coating's potential to produce high-quality perovskite films for memristor applications, despite its current underutilization in the field.

4.3.4. Single crystals. While perovskite thin films dominate memristor research, single-crystal variants have emerged as promising alternatives due to their inherently lower defect density and absence of grain boundaries – traits that suppress non-radiative recombination while enhancing carrier mobility and light absorption.[287,288] These properties make single crystals ideal for optoelectronic applications, yet they present a paradox for resistive switching: defects and grain boundaries in polycrystalline films facilitate ion migration, the core mechanism enabling memristive behavior. Single crystals exhibit a sixfold higher activation energy for ion migration (1.05 eV) compared to polycrystalline films (0.27 eV),[289] posing challenges for memristor applications where controlled ion motion is critical. Despite this,

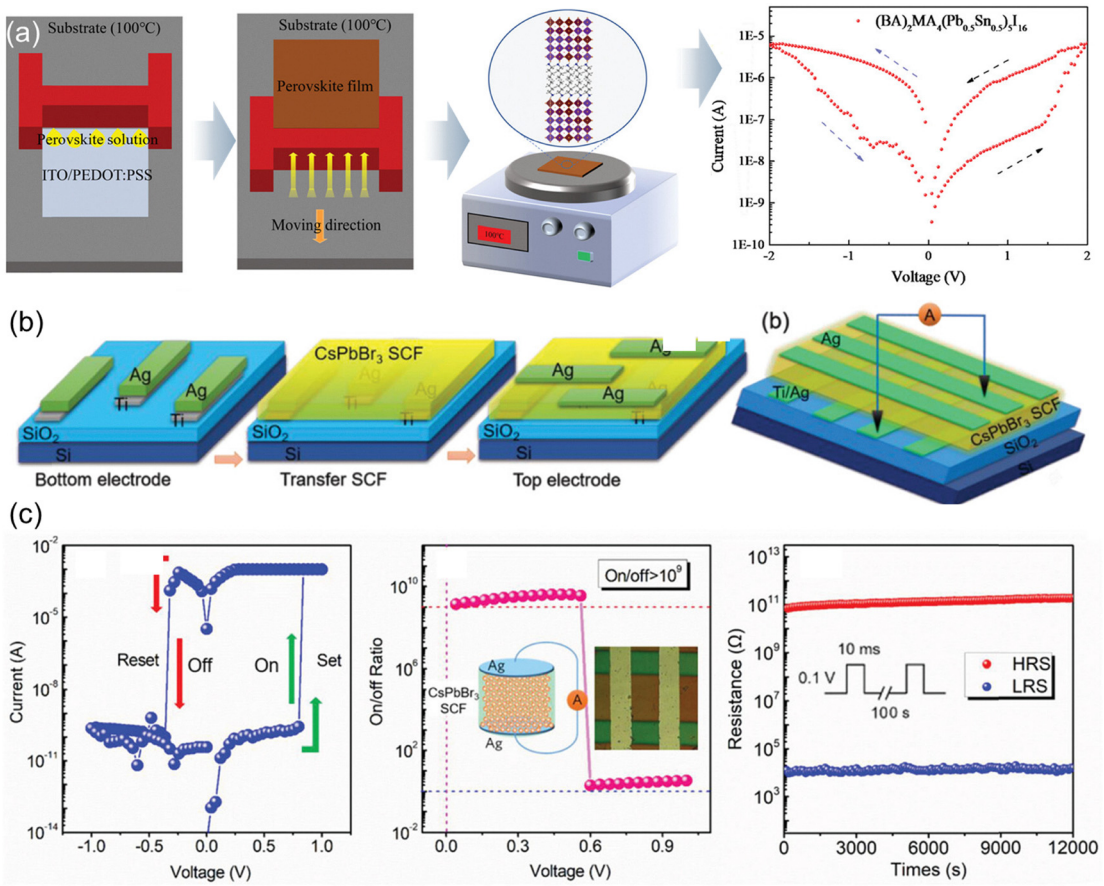

Fig. 18 (a) Schematic diagram of the perovskite deposition by blade coating together with *J*–*V* curve of the devices based on quasi-2D Sn–Pb perovskite. Reproduced from ref. 286 with permission from John Wiley and Sons, Copyright 2023. (b) Schematic illustration of $CsPbBr_3$ SCF-based RRAM device with $Ag/CsPbBr_3/Ag/Ti/SiO_2/Si$ structure.[262] (c) A typical *I*–*V* curve of bipolar $Ag/CsPbBr_3/Ag$ device, the on/off ratio is plotted as a function of voltage and the retention of $Ag/CsPbBr_3/Ag$ device by adding a series resistance of 10 kΩ. (b) and (c) Reproduced from ref. 262 with permission from John Wiley and Sons, Copyright 2021.

recent studies demonstrate that single-crystal memristors can achieve exceptional performance through tailored design.

A high on/off ratio is generally expected in single-crystal devices due to their low non-radiative recombination and reduced leakage current, which result in a lower HRS current. For example, a filamentary memristor based on a $CsPbBr_3$ single-crystal film grown by antisolvent vapor-assisted crystallization demonstrated an impressive on/off ratio greater than 10^9 (Fig. 18b and c).[262] Similarly, a grain boundary–free, 2D-layered $CsPb_2Br_5$ microsheet memristor exhibited a high on/off ratio exceeding 10^8.[290] In addition, when anisotropic 2D perovskites are employed, anisotropic resistive switching has been observed: with active metal electrodes, non-volatile switching occurs in the vertical direction, while volatile switching is seen in the lateral direction. This behavior is attributed to the absence of grain boundaries, which allows the intrinsic crystal structure to govern ion migration and overall device operation. Furthermore, the growth of single crystals can be patterned, enabling the formation of memristor device arrays.[291] Notably, a UV-responsive photomemristor array has also been demonstrated using on-site and epitaxially grown $Cs_3Cu_2I_5$ single crystals, further highlighting the versatility of single-crystal perovskite memristors for advanced applications.

4.4. Buffer layer

In the 2T configuration, while the metal-insulator-metal (MIM) architecture, where a halide perovskite layer is sandwiched between two metallic electrodes, remains the standard for memristors, the integration of buffer layers has become increasingly common to enhance device performance and enable novel operational mechanisms. Buffer layers can serve dual roles: they may act as functional layers, directly participating in the device's resistive switching behavior, or as protective layers, encapsulating the sensitive perovskite to shield it from moisture and oxygen. These layers can be incorporated either below or above the perovskite layer, with different considerations depending on their placement.

When the buffer layer is deposited beneath the perovskite, there are generally no restrictions on the deposition technique or precursor used. However, if the perovskite is deposited using solution processing, it is crucial to ensure that the precursor solvent does not adversely affect the underlying buffer layer. Additionally, the buffer layer must exhibit sufficient wettability to allow for uniform perovskite coverage, and its surface roughness should be minimized to promote high-quality film growth. In contrast, depositing a buffer layer above the perovskite presents unique challenges: high-energy deposition methods such as sputtering can damage the perovskite due to plasma emission and energetic particle bombardment.[292] Solution processing is possible, but only with solvents that do not dissolve the perovskite, while vapor-phase techniques like chemical vapor deposition (CVD) and atomic layer deposition (ALD) are viable if the precursor reactivity and processing temperatures are compatible with perovskite stability.[293] In the literature, buffer layers are broadly categorized as either semiconductors, which can modulate charge injection and filament stability, or dielectrics, which serve to block ion and carrier diffusion and passivate defects.

4.4.1. Semiconducting buffer layer. Semiconductor buffer layers are frequently employed as hole-transporting layers (HTL) or electron-transporting layers (ETL) in halide perovskite devices. This asymmetry arises from energy level offsets at the perovskite–semiconductor interface: ETLs selectively block electrons, while HTLs block holes. By modulating this energy barrier *via* interfacial reactions or self-doping-the semiconductor layer can directly influence resistive switching in interfacial-type memristors. Furthermore, the inherent carrier selectivity of these materials introduces rectification behavior, a critical feature for self-rectifying memristors that minimizes sneak path in crossbar arrays. The mechanisms and advantages of such rectification will be explored in detail in Section 5.

In general, buffer layers or transport layers that facilitate efficient carrier injection and controlled ion migration greatly enhance memristor operation and stability. For example, replacing conventional poly[bis(4-phenyl)(2,4,6-trimethylphenyl) amine] (PTAA) with MeO-2PACz self-assembled monolayers (SAM) as the HTL substantially enhances device performance, as evidenced by systematically reduced V_{SET} values and narrower V_{SET} statistical variation. This improvement stems from stronger conductive filament formation facilitated by superior SAM/perovskite interfacial properties, as SAM effectively passivates interfacial defects that typically compromise device stability.[294] The stronger filament formation is reflected in lower V_{SET} values, along with substantially improved cycling endurance and retention characteristics. In other studies, ETL (such as TPBI (2,2′,2″-(1,3,5-benzinetriyl)-tris(1-phenyl-1-*H*-benzimidazole))) could be used to regulate Ag filament behavior during SET and RESET. TPBI facilitates efficient electron injection into the switching layer, thereby enhancing the oxidation of Ag filaments and improving filament rupture efficiency, which enhanced device's reliability (Fig. 19a).[295]

Poly(3,4-ethylenedioxythiophene): poly(styrenesulphonate) (PEDOT: PSS) was one of the earliest used buffer layers in halide perovskite memristors. Available in both conducting and semiconducting forms, depending on the ratio between PEDOT and PSS, PEDOT: PSS can be easily solution-processed under ambient conditions, which facilitates straightforward film fabrication.[296] It also received attention from the memristor community for its ability to be electrochemically doped and de-doped, causing a change in its conductivity.[297–299] Despite its potential as an electrochemically active layer, most studies have employed PEDOT: PSS primarily as an HTL in photomemristors or as a smooth substrate to promote high-quality perovskite film formation in electrical memristors. For example, an Au/$MAPbI_3$/PEDOT: PSS/ITO device was demonstrated as an energy-efficient synapse, where the resistive switching mechanism was attributed to interfacial self-doping of the perovskite layer, and the device could operate even without the PEDOT: PSS layer.[300] Additionally, several reports have highlighted the use of PEDOT: PSS in filamentary memristors to improve the morphology of the perovskite layer.[136,301,302]

In addition to organic transport layers, inorganic materials such as metal oxides and transition-metal dichalcogenides (TMDCs) can also serve as effective buffer layers in halide

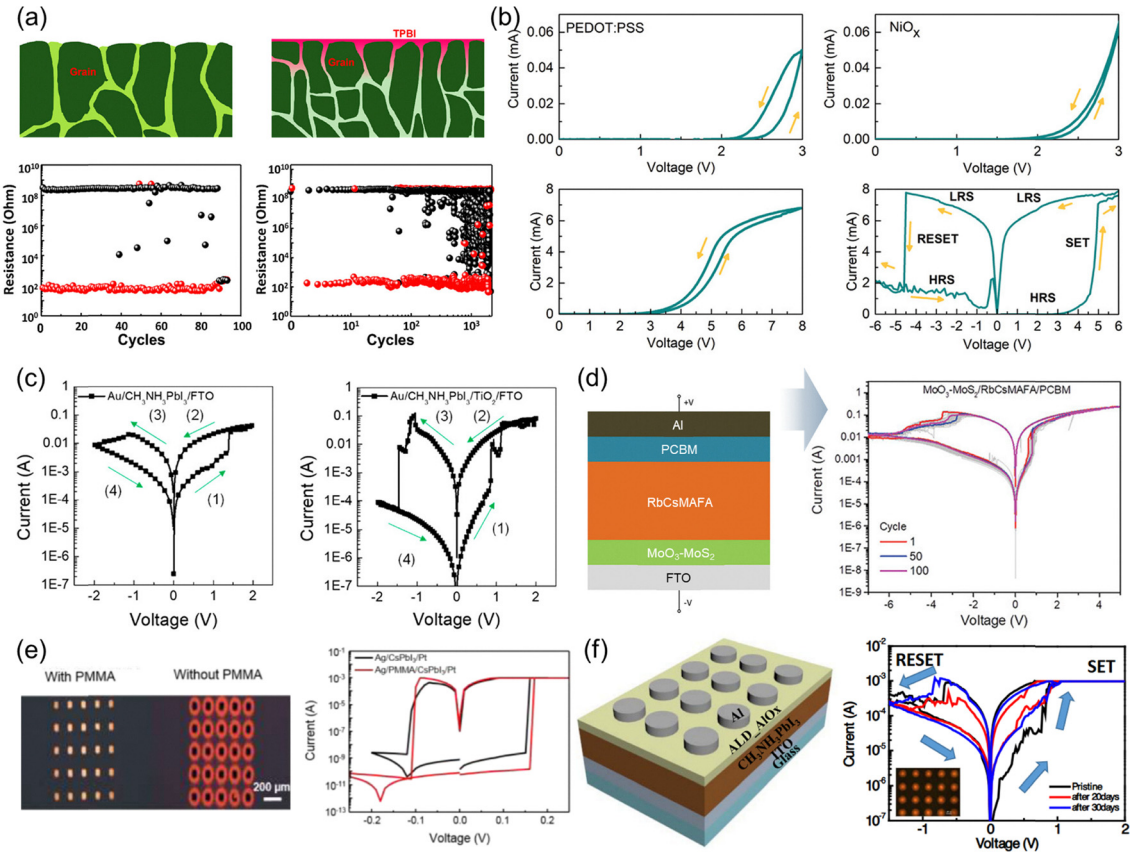

Fig. 19 (a) Schematic illustrations of $MAPbBr_3$ by CF and $MAPbBr_3$ by TPBI dissolved in CF. Endurance properties of the Ag/$MAPbBr_3$/Pt (<100 cycles) and Ag/TPBI/$MAPbBr_3$/Pt (>1000 cycles) devices. Reprinted with permission from ref. 295 Copyright 2024 American Chemical Society. (b) Current–voltage (*I*–*V*) sweep characteristics of the memristive barristors with PEDOT: PSS and NiO_x as HTL depicting diffusive and drift kinetics, respectively. Reproduced from ref. 172 with permission from John Wiley and Sons, Copyright 2021. (c) *I*–*V* curves of Au/$MAPbI_3$/FTO (ON/OFF ratio = 11.13) and Au/$MAPbI_3$/TiO_2/FTO (ON/OFF ratio = 1530.71) devices. Reprinted with permission from ref. 303 Copyright 2021 American Chemical Society. (d) Schematic illustration of a perovskite memristor based on a MoO_3–MoS_2 buffer layer. *I*–*V* curves of the memristor for 100 consecutive cycles applying DC sweep voltages. Reproduced from ref. 304, under the terms of the Creative Commons CC BY 4.0 license (https://creativecommons.org/licenses/by/4.0). (e) Optical microscope images of Ag/PMMA/$CsPbI_3$/Pt and Ag/$CsPbI_3$/Pt cells after 12 hours. *I*–*V* characteristics comparing Ag/$CsPbI_3$/Pt device with Ag/PMMA/$CsPbI_3$/Pt device. Reproduced from ref. 309 with permission from John Wiley and Sons, Copyright 2017 (f) resistive switching characteristics of the AlO_x-encapsulated perovskite device over storage time in ambient air; inset top view of the memristor. Reproduced from ref. 186, under the terms of the Creative Commons CC BY 4.0 license (https://creativecommons.org/licenses/by/4.0).

perovskite memristors. For instance, NiO_x has been employed as an HTL in $MAPbBr_3$-based memristors, where it facilitated non-volatile switching through defect-assisted filament formation, in contrast to the volatile memristive behavior observed with the organic PEDOT: PSS layer, which is attributed to its ion-permissive nature (Fig. 19b).[172] Another widely used inorganic buffer layer is TiO_2. Comparisons between devices with and without a compact TiO_2 layer between the FTO substrate and the perovskite revealed a significant reduction in OFF-state (4–5 orders of reduction) current upon the inclusion of TiO_2, while the ON-state current remained largely unaffected.[153] Similar findings were reported in other studies, where HRS increased due to a negative bias-induced energy barrier at the perovskite/TiO_2 interface (Fig. 19c).[303] Beyond metal oxides, TMDCs such as MoS_2 have also been integrated with halide perovskites. For example, a composite of MoO_3 and MoS_2, synthesized by sulfurizing sub-stoichiometric MoO_3, was utilized as an interfacial layer in a double memristive device with RbCsMAFA quadruple cation perovskite (Fig. 19d).[304] The presence of the MoO_3–MoS_2 layer significantly enhanced the on/off ratio compared to devices lacking this interfacial layer.

4.4.2. Dielectric buffer layer. Dielectric materials are generally not favored in halide perovskite-based optoelectronic devices because they hinder efficient carrier collection and injection. However, in halide perovskite memristors, dielectric layers are frequently employed to regulate both carrier and ion migration. Their primary role is to increase HRS and to prevent undesirable reactions between the halide perovskite layer and the active metal electrode. As a result, dielectric layers are typically deposited on top of the halide perovskite, which in turn limits the range of suitable deposition techniques.

Insulating polymer layers such as poly(methyl methacrylate) (PMMA) have proven effective encapsulants for halide perovskites, primarily due to their low oxygen permeability and water transmission rates.[305] PMMA also enhances the thermal stability of halide perovskite films by passivating grain boundary defects at the film/air interface.[306,307] Notably, PMMA can be

dissolved in weakly polar solvents like toluene and chlorobenzene, which do not affect halide perovskites, allowing for straightforward deposition of thin films *via* spin coating and other solution-based techniques. This compatibility was first demonstrated in devices such as Ag/PMMA/$MAPbI_3$/Mo, where the inclusion of a PMMA layer resulted in a significant improvement in the on/off ratio (to 10^6).[308] The protective effect of PMMA was further highlighted in Ag/PMMA/$CsPbI_3$/Pt/Ti/SiO_2/Si devices, where the absence of PMMA led to observable reactions between the Ag electrode and the perovskite within hours, while its presence enhanced device stability and on/off ratio (Fig. 19e).[309] The ion-blocking capability of PMMA, however, remains a subject of debate. Some studies suggest that PMMA effectively prevents the migration of electroactive metal ions, making halide vacancy filaments the dominant resistive switching mechanism. In contrast, other reports indicate that while PMMA does not completely block ion migration, it does regulate and moderate the process, thereby preventing detrimental runaway interfacial reactions and supporting more stable device operation.[187]

While insulating metal oxides can serve as effective dielectric layers, their processing conditions (such as temperature and solvent requirements) are often incompatible with halide perovskites. As a result, the range of viable deposition techniques for metal oxides on halide perovskites is limited, necessitating careful adjustment of processing parameters. For instance, ALD of AlO_x on halide perovskites requires modifications due to the moisture sensitivity of the perovskite layer; oxidation of the ALD precursor, trimethyl aluminum (TMA), is typically carried out using ozone instead of water, and the processing temperature is lowered to accommodate the thermal sensitivity of the material.[310] These optimized conditions have been successfully applied in devices, where the addition of a low-temperature ALD AlO_x layer led to improved on/off ratios and enhanced stability (Fig. 19f).[186] Recently, further improvements in the uniformity and compactness of ALD AlO_x films have been achieved by carboxyl-functionalizing the perovskite surface, which also resulted in greater suppression of Ag ion migration from the top electrode.[311] This method holds promise for enhancing device endurance in memory applications. Additionally, dielectrics such as AlO_x and SiO_2 have been utilized in halide perovskite device arrays to reduce crosstalk by providing lateral isolation of pixels. These advanced techniques and their implications for device performance will be discussed in more detail in Section 5.

4.5. Top electrode

The top electrode is the terminal functional layer of the device stack. As the earlier sections have discussed, the design or material of the top electrode could be at the centre stage of the device operation. Hence, several factors must be considered before choosing the top electrode. Moreover, the form factor and arrangement of the electrodes are critical in determining the device's mode of operation. Lastly, as halide perovskite memristors extend to large areas and flexible substrates, the mechanical properties of the top electrodes also become critical. The following section will delve deeper into these regards.

4.5.1. Reactivity effects. Metals are the popular choice for the electrode owing to their high conductivity and ease of deposition. Apart from the conductivity, the correlated properties, chemical reactivity, and work function of the metal electrode are important factors that govern the performance of halide perovskite memristors.

The reactivity of the metal electrode factors in two integral phenomena – metal ion migration and interfacial reactions. As described in the earlier sections, the first step for the ECM mechanism of resistive switching is the oxidation of the metal to form a cation that migrates through the halide perovskite film. The tendency for this step is quantified by the oxidation potential of the metal. Therefore, a positive potential must be applied to initiate this process. This potential also attracts the mobile halide ions towards the metal electrode, leading to interfacial reactions to form metal halides, which also affect the device operation.[312,313] The role of metal reactivity has been explored by considering three highly reactive (Ag, Cu, and Al) and two lowly reactive (Au and Pt) metals in an FTO/PEDOT: PSS/$MAPbI_3$/Metal/Au device (Fig. 20a).[178] In case of the less reactive metals, the current–voltage curves showed counterclockwise hysteresis at various sweeping rates. This behavior could be attributed to halide vacancy migration. However, traces of Au could be found in the perovskite layer after prolonged operation, indicating migration despite the inert nature of Au.[314] This suggests that using an Au electrode device as a control test to reject ECM as the switching mechanism could be erroneous. On the other hand, in the case of highly reactive metals, large capacitive peaks are observed at low scan rates, which is indicative of metal oxidation. These oxidised metal ions are conducive to the ECM mechanism. In ECM-based devices, metals with lower work functions tend to be more chemically reactive and susceptible to oxidation. Based on this trend, their relative reactivity generally follows the order: Cu < Ag < Al. While Al is highly reactive, it quickly forms a passivating Al_2O_3 layer, which acts as an insulating barrier. This layer restricts ion migration but still permits switching under high electric fields. Ag, on the other hand, exhibits moderate oxidation and readily forms mobile Ag^+ ions that can migrate into the perovskite matrix. These ions interact with halides and generate vacancies, which are beneficial for achieving stable switching at lower voltages than Cu. Due to this property, Ag electrodes are commonly used in perovskite memristors for their ability to form fast conductive filaments. However, rapid electrochemical reactions between Ag and the perovskite layer can lead to electrode degradation and perovskite decomposition, ultimately compromising retention and endurance. This necessitates the usage of stable buffer layers as discussed previously. To prevent this, chemically stable metals such as Bi have also been used as a barrier layer between Ag and the perovskite layer. Its high reaction energy barrier and robust crystalline lattice effectively restrict the diffusion of metal ions into the perovskite, thereby maintaining the structural and functional integrity of the device. As a result, memristors incorporating an Ag/Bi bilayer electrode exhibit enhanced endurance, stable switching characteristics, long retention times exceeding 10^4 seconds, and improved

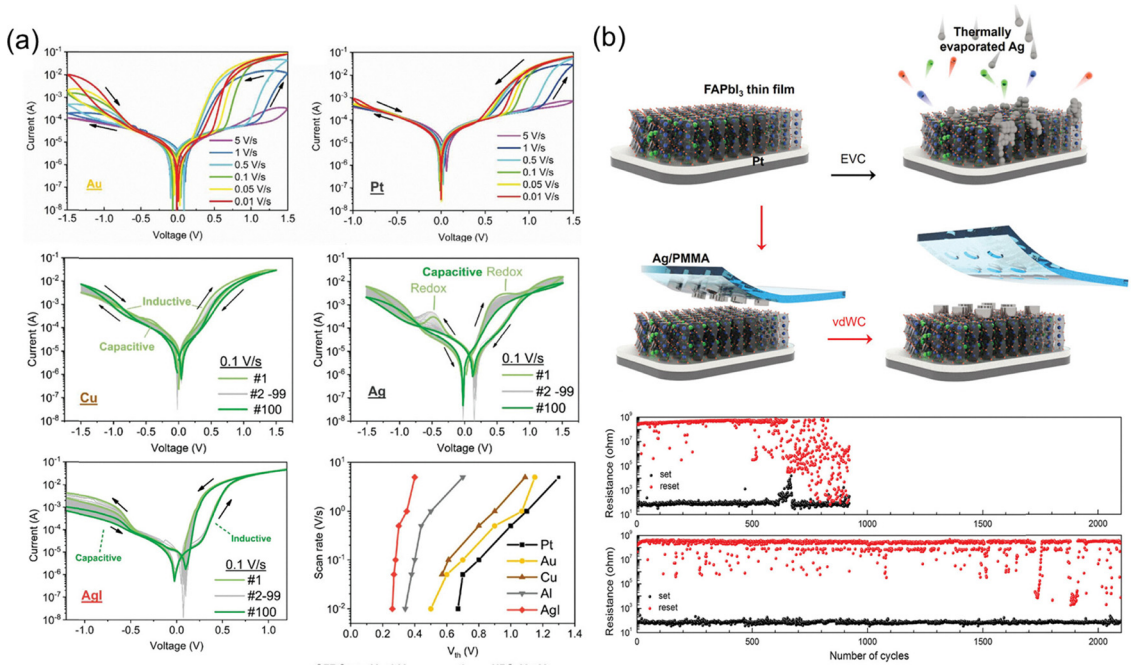

Fig. 20 (a) *I–V* curves of FTO/PEDOT:PSS/$MAPbI_3$/metal/Au (metal = Pt, Au, Cu, Ag, and AgI). Decrease in the threshold voltage with the reactivity of the metal electrode. Reproduced from ref. 178 with permission from John Wiley and Sons, Copyright 2023. (b) A schematic diagram for metal contact deposition based on conventional thermal evaporation (EVC) or transfer of pre-deposited metal contact (vdWC). The endurance measurement of Si/Pt/$FAPbI_3$/Ag devices based on EVC (<1000 cycles) and vdWC (>2000 cycles). Reproduced from ref. 261 with permission from John Wiley and Sons, Copyright 2023.

environmental stability. Moreover, the relatively low work function of the Ag/Bi bilayer helps reduce the built-in potential at the electrode–perovskite interface. This promotes efficient filament formation and stabilization, contributing to enhanced device performance and reliability.[315]

4.5.2. Effect of deposition technique. Metal thin films are typically deposited using thermal or electron-beam (e-beam) evaporation. In these methods, the metal is heated under high vacuum until it vaporizes, and the resulting metal vapor travels upward to condense onto the substrate. However, the high-energy metal atoms in the vapor can potentially damage the underlying halide perovskite layer during deposition. To mitigate this effect, evaporation at low rates and using buffer layers are recommended. A gentler method of depositing the metal electrode has been introduced in a Si/Pt/$FAPbI_3$/Ag device (Fig. 20b).[261] Here, the electrodes were evaporated on a different substrate and then physically laminated on the perovskite film by transferring using PMMA. This transfer formed an intact metal/perovskite van der Waals junction. The superiority of this method was validated by comparing it with thermally evaporated contacts. In the conventional deposition, penetration of Ag into the bulk of the perovskite could be observed, which compromised the long-term and high-temperature stability of the device. However, this method requires high dexterity as the lamination is manual.

Alternative materials systems, such as conductive carbon allotropes,[220,316] and liquid metals,[317] have also been explored to form a more benign electrode/perovskite interface. Additionally, vapor-deposited metals are also difficult to scale up. To integrate into an industrial roll-to-roll process flow, the electrodes must also be printable. Fully printed halide perovskite LEDs have been demonstrated, which used blade-coated carbon nanotubes and Ag nanowires as the bottom and top electrodes, respectively.[318] Such techniques are yet to be implemented in halide perovskite memristors.

5. Scaling challenges: fabrication and system integration

Perovskite memristors have emerged as a promising platform for neuromorphic computing, as their operational mechanisms closely mimic those of biological synapses, enabling the emulation of human brain functions.[162,319] As described in previous section, traditional oxide-based memristors, such as those employing transition metal oxides, often suffer from high operating voltages and fewer level of conductance states. In contrast, perovskite memristors leverage ion migration and defect-assisted resistive switching mechanisms to achieve low-power operation, multi-level data storage, and tunable switching characteristics. These features make them particularly useful for applications in artificial synapses, reconfigurable logic circuits, and neural network-based computing systems.[320]

Memristor arrays are fundamental to neuromorphic computing because neural network (NN) architectures – such as fully-connected (FCNN), recurrent (RNN), convolutional (CNN), and spiking neural networks (SNN) – mimic the function of the human brain, with layers of interconnected neurons and synapses. The core computational task in these networks is matrix multiplication, where the outputs of pre-neurons are multiplied by

synaptic weights to generate the responses of subsequent layers. While most artificial neural networks are currently implemented in software using graphic processing units (GPUs) and tensor processing units (TPUs), these approaches demand rapid access to the memory and significant bandwidth, making it both hardware- and power-intensive. Memristor-based crossbar arrays offer a hardware solution by enabling efficient matrix computations: the conductance of each memristor can be programmed to represent a synaptic weight, and applying voltages across the array allows direct, analog computation of matrix products according to Kirchhoff's current law (Fig. 21a and b), greatly improving scalability and efficiency.

Despite the clear need for array architectures in advancing neuromorphic computing, most current studies remain limited to simple dot-array configurations. While these are useful for basic characterization, they fall short of the requirements for high-density integration in practical systems.[321,322] Realizing functional memristor arrays-especially crossbar arrays-is the next critical step for system-level applications. However, significant challenges remain, including achieving low device-to-device variability, precise pattern alignment, accurate electrode definition, material compatibility, and other array-level read/write challenges.[162,279,319] Addressing these fabrication and reliability barriers is essential for unlocking the full potential of perovskite memristors in scalable neuromorphic hardware implementations.[323]

This section provides a comprehensive discussion of current strategies for array fabrication, patterning techniques, and large-area deposition in perovskite memristors. To begin, we will review the challenges associated with developing functional perovskite memristor arrays, focusing on both fabrication hurdles and array-level reliability issues. Subsequently, the section will explore solutions and approaches that enable successful crossbar integration.

5.1. Challenges associated with perovskite memristor arrays

5.1.1. Array-level read/write challenges. While larger arrays offer significant advantages in computational density, energy efficiency, and scalability for complex applications, their miniaturization introduces additional challenges beyond fabrication, such as IR drop, sneak paths, and crosstalk (Table 6). When considering memristor arrays, as shown in Fig. 21a, the resistance of the word lines (WL) and bit lines (BL) can add series resistance, thus distorting the output current calculated using Kirchhoff's law. Discrepancies in the output current result in erroneous signals fed forward to subsequent neural network layers, yielding inaccuracy in the NN task. The underlying principle for distortions in output current is the potential drops along the WL and BL due to series resistances, which reduces the voltage across the memristor from its intended value. To address this, programming solutions have been proposed in which the conductance of the memristor is scaled to compensate for the voltage drop, effectively offsetting the total reading current to match the ideal case where line resistance is zero.[324–327] From a materials perspective, reducing the interconnect resistance and employing memristors with low LRS currents are effective strategies to minimize current flow through the interconnects and thereby reduce IR drop.

Sneak path current refers to unintended current that flows from the selected word line through an unselected memristor and subsequently into the selected bit line, leading to erroneous current readings, as shown in Fig. 21c.[328] As the size of a memristor crossbar array increases, these sneak path currents become more significant, interfering with the accurate reading of a memristor's state by introducing additional currents not related to the selected device. In small arrays, sneak paths may be manageable, but as the array grows, the number of possible sneak paths increases dramatically, making it harder to distinguish between LRS and HRS of each memristor. The key metric affected by sneak paths is the read margin-the difference in output current between the ON and OFF states of a memristor. As sneak path currents increase with array size, they reduce the read margin, making it difficult to reliably determine the state of any given device. If the read margin becomes too small (for example, less than 10% difference between states), the risk of read errors and misinterpretation rises sharply. This sets a practical upper limit on the array size: beyond a certain point,

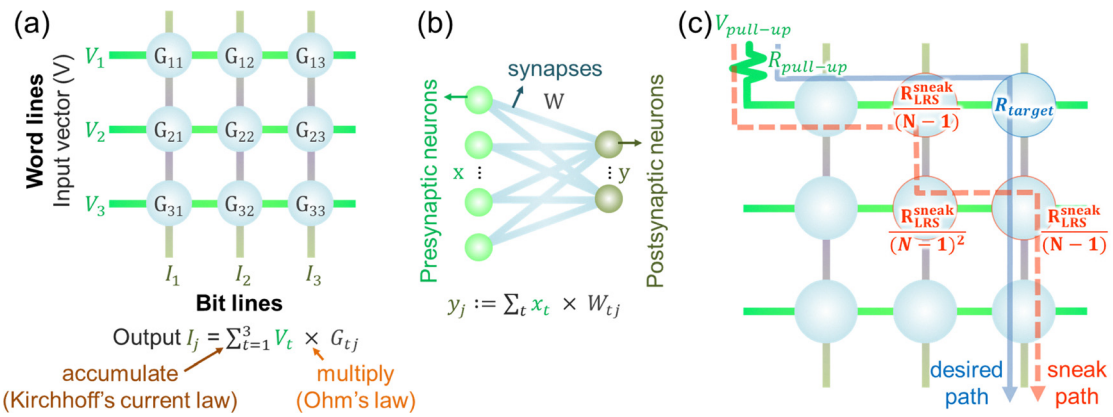

Fig. 21 (a) The principle of computation matrix products with memristor crossbar array, as well as (b) the principle of synapses as it scales and sums incoming presynaptic neurons signal. (c) The equivalent circuit of crossbar array showing the current direction and the largest sneak path current when all neighbouring memristor is in LRS.

Table 6 The challenges of memristor array fabrication from system level testing point of view

	IR drop	Crosstalk	Sneak path
Causes	Increased interconnect resistance in larger arrays.	Thermal/electrical interference between adjacent cells or layers.	Unintended current paths through non-target cells due to shared row/column lines.
Impact	Voltage drops across wires distort programming and read accuracy	Degrades cell reliability (*e.g.*, resistance drift, unintended switching, thermal retention failure).	• Read/write errors due to parasitic currents bypassing target cells. • Parasitic power loss • Signal distortion
Scope	Global	Localized to neighbouring cells or layers	Global across the entire array due to parallel cell connections
Materials and array design mitigation	• Decreasing interconnect resistance • Using a memristor with a low LRS current to reduce current flow through the interconnect	• Use materials with good heat distribution and thermal stability to avoid localization hotspots or consider patterning perovskite arrays. • Balance miniaturization by maintaining the aspect ratio to 100.	• Integrating selectors (self-selecting device or additional selector) to isolate cells and block parasitic current

reliable operation is no longer possible without additional circuit elements or special device engineering.

The maximum feasible size of a crossbar array (N×N) can be estimated by considering the worst-case scenario, where all memristors except the selected one are in LRS (Fig. 21c). Using Kirchhoff's law, the equivalent sneak path resistance (R_{Sneak}) experienced by the selected memristor (R_S) can be calculated. A read voltage (V_{read}) is applied to the selected memristor (R_S) through a series resistance ($R_{\text{pull-up}}$). This resistance arises from three components (eqn (1)).[110,329,330]

$$R_{\text{sneak}} = \frac{R_{\text{LRS}}}{(N-1)} + \frac{R_{\text{LRS}}}{(N-1)^2} + \frac{R_{\text{LRS}}}{(N-1)} \tag{1}$$

The first term in eqn (1) is the equivalent resistance of all memristors that are in parallel to the selected memristor, while the second term arises from the equivalent resistance of all memristors except those in the word line and bit line, since current cannot flow back to the selected word line or bit line, thereby reducing the resistance to $\frac{R_{\text{LRS}}}{(N-1)^2}$. The last term is for the equivalent resistance obtained when current flows back to the selected bit line. To calculate the maximum crossbar size, the change in readout voltage (ΔV_{RS}) of the selected memristor under LRS and HRS must be considered, and the margin must be more than 10% which will help in distinguishing the conductance state of the memristor given by eqn (2). However, it must be noted that the equations consider that all the unselected word lines and bit lines are open-circuited.

$$\Delta V_{RS} = \left(\frac{R_{\text{pull-up}}}{\left(R^{S}_{\text{LRS}} \| R_{\text{sneak}}\right) + R_{\text{pull-up}}} - \frac{R_{\text{pull-up}}}{\left(R^{S}_{\text{HRS}} \| R_{\text{sneak}}\right) + R_{\text{pull-up}}} \right) \times V_{\text{read}} \tag{2}$$

To address sneak path effects, several strategies have been developed. Smart programming techniques, such as biasing unselected devices at fractional voltages (*e.g.*, $V/2$ or $V/3$), can effectively reduce unwanted currents. For example, a half-bias read voltage scheme were implemented where all unselected word lines and bit lines were maintained at $V_{\text{read}}/2$ instead of 0 V, reporting a rectification factor of 514 at 0.54 V.[331] Using an Au/triple-cation perovskite/ITO device structure, they achieved an on/off ratio greater than 10^3 and retention of 10^4 s at 85 °C. According to their analysis (see eqn (1)), the self-rectifying behavior of the device resulted in very high resistance for unselected paths, thereby enabling a maximum array size of 1747 × 1747. Interestingly, increasing the V_{read} voltage led to a reduction in the maximum achievable array size. Kim *et al.* have also utilized $V/3$ programming techniques to minimize sneak path current in 7 × 7 arrays of low dimensional based perovskite crossbar array.[110]

From a device perspective, incorporating a diode or selector device in series with the memristor (1D1R or 1S1R architectures), or using self-rectifying memristors, can further mitigate sneak paths. Selector devices are effective because they can open-circuit unselected devices or create a high-impedance path by proper biasing. In self-rectifying memristors, the selector function is built into the device stack, often by forming a type-II heterojunction similar to a PN junction in a silicon diode. These approaches are designed to maximize the equivalent sneak path resistance, minimize parasitic currents, and enable the realization of larger crossbar arrays without compromising the ability to distinguish between different memristor states. Section 5.2 will discuss these mitigation schemes in greater detail.

On the other hand, crosstalk results from unwanted capacitive or electromagnetic coupling between adjacent word lines and bit lines. Mitigating crosstalk becomes especially important when the device thickness and inter-device spacing are of similar magnitude. In high-density integrated memristor arrays, electrical crosstalk can occur when unintended conductive filaments form between electrodes of adjacent devices. To prevent this, the electric field (E) between neighbouring cells must remain below the threshold required for filament formation. Studies have shown that if the inter-device spacing is at least 100 times the device thickness, crosstalk can be effectively avoided.[332] This is based on the observation that no switching occurs below 1 mV in devices with a thickness of 60 nm. Under this condition, the

critical electric field can be expressed $E = V/d$, where V is the voltage and d is the distance between electrodes. For a typical operating voltage of 100 mV, this corresponds to a minimum spacing of approximately 6 μm between adjacent devices. Aside from electrical crosstalk mentioned above, thermal crosstalk is also a concern, as adjacent lines can inadvertently alter the conductance state of neighbouring devices. To address these issues, patterning the active memristor array can be an effective strategy and will be discussed further in Section 5.3.[332]

5.1.2. Fabrication challenges: addressing device-to-device variation and patterning issues. From a fabrication perspective, challenges remain in achieving both uniform array formation and consistent film quality, both of which are essential for minimizing device-to-device variability. Achieving a uniform memristor film is crucial for the reliable operation of crossbar arrays. Device variability, which is closely linked to film uniformity, directly impacts the stability and performance of perovskite memristor arrays. As such, scalability should not come at the expense of uniformity. Common fabrication techniques-such as spin coating, spray coating, and inkjet printing-can lead to variations in film thickness, which in turn negatively affect the switching characteristics and reproducibility of the devices. To address this, novel fabrication techniques that ensure uniform film thickness over large area should be considered. Various perovskite deposition methods have already been reviewed in Section 4.2. For large-scale production, it is essential to maintain precise control over material deposition and ensure consistent film quality to minimize device variability. Additionally, optimizing process parameters and employing post-processing treatments, such as annealing or surface modification, can further help address issues of non-uniformity. Focusing on these aspects is key to advancing the manufacturing technologies required for reliable, high-density perovskite memristor arrays.

Among fabrication techniques, spin-coating remains the most employed method for fabrication of perovskite memristor. Without array patterning, Kim *et al.* successfully fabricated a 250 nm-thick, vertically oriented DJ phase two-dimensional perovskite film *via* spin-coating, ensuring the formation of high-quality, 100% yield memristor arrays (7 × 7 crossbar arrays) with individual device dimensions of 100 × 100 μm^2, as shown in Fig. 22a and b. Experimental results demonstrated that the DJ-phase crossbar array exhibited multi-level analog storage capabilities, extended data retention (~10^4 s), low power consumption (~2.81 pJ), and high stability, maintaining memristive characteristics even after 7 months of storage. Low cycle to cycle variation (~1.85%) as well as device to device variation have also been achieved here by measuring the

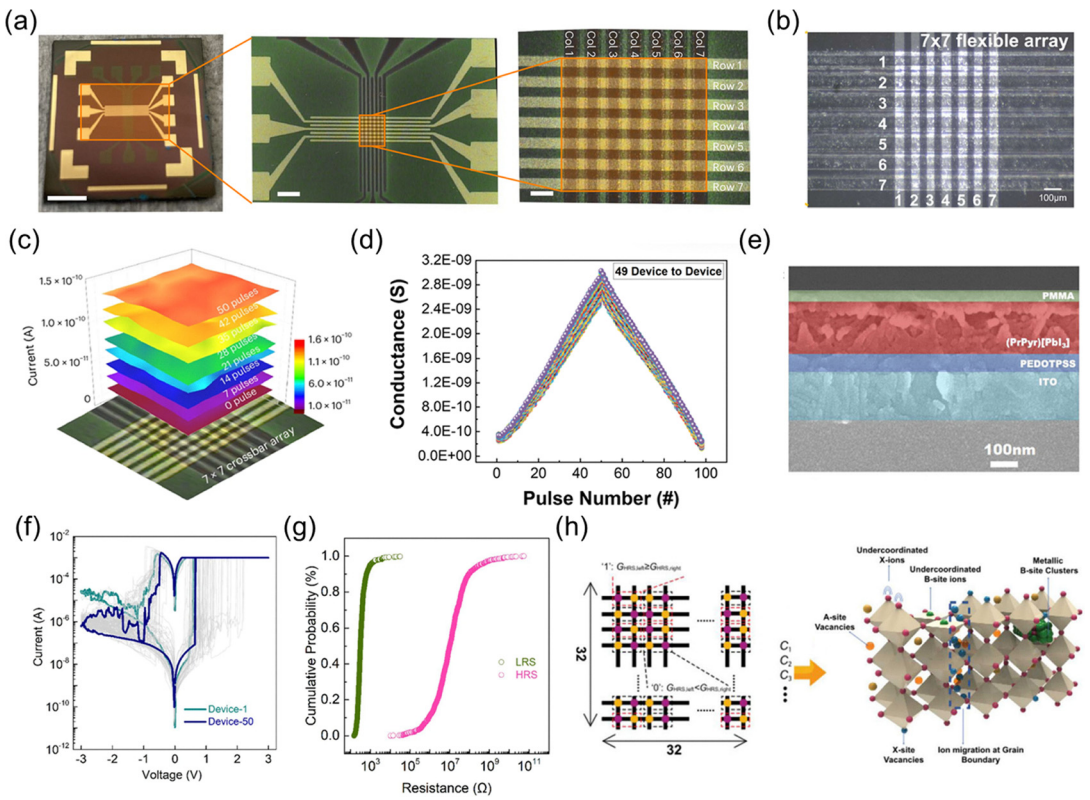

Fig. 22 (a) Optical images of 7 × 7 DJ 2D perovskites crossbar array. Scale bars: 0.5 cm (left), 1 mm (middle), and 200 μm (right). (b) Optical image of the crossbar array built on flexible substrates. (c) A 3D mapping of eight distinguishable analogue states along with the synaptic pulses in a crossbar array. (d) Potentiation and depression behaviors of EPSCs with 49 different devices to verify device-to-device uniformity of the linearity and symmetry. (a)–(d) Reproduced from ref. 110 with permission from Springer Nature, Copyright 2024. (e) Cross-section SEM of PrPyr[PbI_3] perovskite memristor. (f) *I*–*V* switching curves of HP memristors (g) The distribution of the LRS (green) and HRS (pink) across 1024 devices. (h) Halide perovskites can serve as entropy sources for designing new types of PUVs. (e)–(h) Reproduced from ref. 270 with permission from Springer Nature, Copyright 2021.

potentiation and depression behaviors of EPSCs with 49 different devices, as shown in Fig. 22c and d. Additionally, they also reported a flexible 7 × 7 memristor array based on the RP phase perovskite on a polyimide substrate (Fig. 22b), confirming that the spin-coating process is compatible with various substrates in perovskite memristor fabrication.[110] In another study, when spin-coating was employed for the fabrication of large-scale arrays as shown in Fig. 22e, John *et al.* demonstrated a 32 × 32 one-dimensional PrPyr[PbI_3] perovskite memristor array on a flexible substrate, comprising 1024 memristor units (1 kb)---one of the largest perovskite memristor arrays reported to date. Due to high device to device variation (Fig. 22f) and cycle to cycle variation (Fig. 22g), the array was utilized to generate a 512-bit cryptographic key and successfully passed the MNIST randomness test, enabling a physically unclonable function (Fig. 22h).[270] Inducing vertical orientation in $PEA_2MA_4Pb_5I_{16}$-based perovskite reduces device-to-device variance (from 2.6 to 0.96) and cycle-to-cycle variation (from 6.05 to 1.38) of the 8 × 8 crossbar arrays.[333]

In addition to the growing demand for uniform large-area arrays, there is an increasing need for high-resolution micro- and nanoscale structuring of perovskite memristors. In the context of memristor arrays, patterning plays a crucial role in ensuring electrical isolation, minimizing crosstalk, and enhancing integration density. While some crossbar architectures may rely primarily on patterned electrodes to define memory cells, precise patterning of the active perovskite layer becomes increasingly important as device dimensions shrink. At the micro-scale, perovskite patterning prevents lateral spreading of the perovskite film beyond the defined electrode boundaries, which could otherwise result in electrical bridging or inter-cell interference. At the nanoscale, especially for device footprints below 1 μm^2, patterning the perovskite itself is essential to control switching behavior, enhance device reproducibility, and realize high-density integration. Therefore, recent research has focused on developing lithography-compatible and solvent-tolerant patterning techniques that enable fine perovskite structuring without compromising material performance, which will be discussed further in Section 5.3. The key to miniaturizing perovskite devices lies in the successful miniaturization of the active layer, spin-coating itself is a technique for large-area uniform film deposition, and additional masking or etching steps are required to meet high-resolution patterning demands.

In addition, while patterning electrodes on top of perovskite is essential for building functional crossbar arrays, the process is complicated by the inherent softness and ionic nature of perovskite materials. Conventional photolithography, which typically involves steps such as spin-coating photoresist, exposure to chemical developers, and sometimes plasma etching, poses significant challenges when applied directly to perovskite layers. The perovskite's delicate crystal structure is highly susceptible to damage from thermal stress, as high-temperature processing can degrade its stability. Critically, many of the solvents and chemicals commonly used in photolithography-such as acetone and isopropanol-can dissolve or corrode perovskite films, leading to poor device performance or outright failure.

5.1.3. Environmental stability challenges. As mentioned in Section 3.1, the endurance of perovskite-based memristors is generally lower than that of oxide counterparts, which can be traced back to material stability issues arising from the environment (light, moisture, oxygen, heat) and/or electrical bias triggers. Hence, strategies to improve material stability would also result in better device endurance. Zhang *et al.* achieved an endurance of up to 3 × 10^6 cycles, which they attributed to the electrical isolation of the perovskite using a porous alumina membrane (side and bottom) and top surface passivation provided by UV-curing epoxy.[162] To establish electrical connectivity to the device, wire bonding must first be performed on the pad, followed by the application of the UV-curing epoxy. Additionally, a shorter pulse duration, such as 100 μs, helps minimize degradation triggered by the electrical bias.

To date, measurements of perovskite-based memristors are generally done in a vacuum or inert environment. As a result, literature data available are not significantly affected by environmental stressor degradation but are dominantly affected by electrical bias-induced instability. However, practical applications must account for environmental effects, which necessitates robust encapsulation while still ensuring electrical connectivity to the device. Encapsulation strategies with minimal heat application, originating from the photovoltaic field (*e.g.* UV-cured epoxy, spin coated PMMA, e-beam SiO_2,[334] and ALD Al_2O_3[335,336]), may be considered for adaptation in this application as the field matures.

5.2. Sneak path mitigation – selectors and self-rectifying memristor

To mitigate sneak path currents, one could utilize either a selector device (*e.g.*, diode or bipolar switch) that can be integrated in series with the memristor (which is positioned between the word line and bit line) or a self-rectifying memristor. Selector devices prevent unintended current leakage by requiring a minimum threshold voltage to activate its LRS. By ensuring that only selected devices receive sufficient voltage to trigger the selector, the circuit design effectively suppresses sneak paths. Specifically, unselected devices remain in their HRS because their selectors do not experience the critical potential drop needed for activation.

For example, Kang *et al.*[337] demonstrated the advantage of using a commercial 1N4007 diode as the selector device to suppress sneak path currents. They employed unipolar $MAPbI_3$ as the switching material, achieving an on/off ratio of up to 10^8. By adopting a 1D1R (one diode-one resistor) architecture, they further attained a rectification ratio of 1.5 × 10^5. A 2 × 2 array was fabricated in both 1R (standalone memristor) and 1D1R configurations (Fig. 23a and b). In the experiment, one memristor (the target device) was programmed to a HRS, while the remaining three were set to a LRS. When reading the target device's state at V_{read} = 0.5 V, the 1R system erroneously registered 508 Ω (LRS, Fig. 23a), whereas the 1D1R system correctly maintained 207 MΩ (HRS, Fig. 23b), highlighting the selector's critical role in mitigating sneak currents. However, it is to be noted that the 1D1R architecture can only be adopted

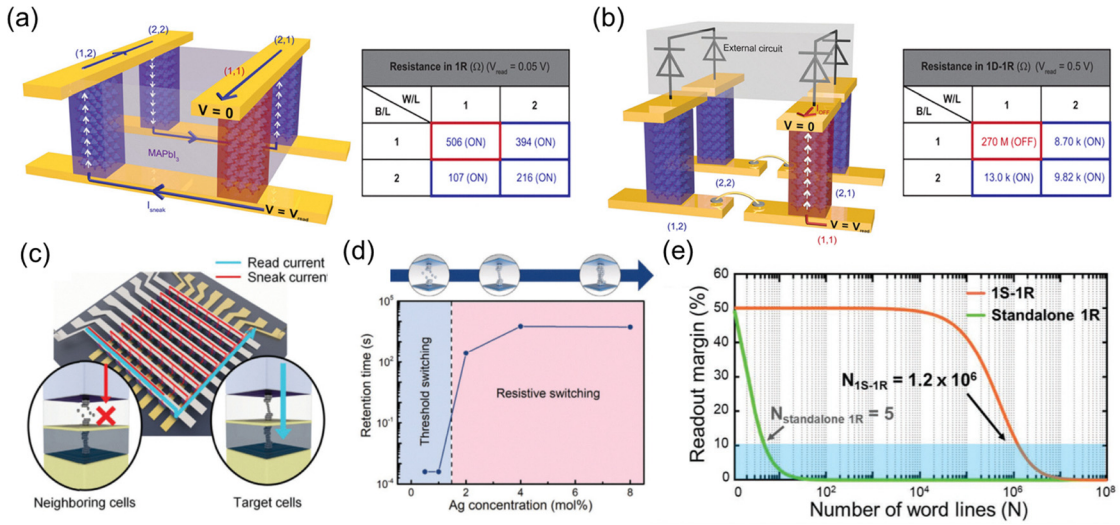

Fig. 23 A 2 × 2 array of memristors was considered, and the selected memristor (highlighted in red box) was programmed to HRS while the rest were in LRS. The readout resistance of the selected memristor when (a) no selector is used and when (b) a diode is used as a selector. (a) and (b) Reproduced from ref. 337 with permission from John Wiley and Sons, Copyright 2019. (c) Working principle of the threshold switch (TS) in series with the resistive switch (RS), wherein TS is used as a selector device. (d) Evolution of retention time with increased Ag content in $MAPbI_3$ film, which is used as a switching layer. (e) The maximum array size calculation was done using eqn (1). Only 5 × 5 array can be built if an array of RS is utilized for crossbar, while it increases to $1.2 \times 10^6 \times 1.2 \times 10^6$ when TS is connected in series with RS. (c)–(e) Reproduced from ref. 330 with permission from John Wiley and Sons, Copyright 2022.

for memristors exhibiting unipolar switching. Im *et al.* addressed sneak paths using a threshold-switching (TS) device paired with a memristor in a 1S1R (one selector-one resistor) configuration (Fig. 23c). In this design, the TS device acts as a series switch. Applying a positive voltage (0.25 V) activates the TS, enabling memristor switching. To reset the memristor, a voltage exceeding −0.6 V is required, as the TS triggers at −0.6 V to facilitate the reset process. Both the TS and memristor utilized $MAPbI_3$ perovskite, with architectures tailored for each: Ag/PMMA/$MAPbI_3$:Ag (1 mol%)/Au for the TS and Au/$MAPbI_3$:Ag (3 mol%)/Au for the memristor (Fig. 23d). The maximum size of 5 × 5 crossbar array was predicted if 1R structure was implemented,[330] while $(1.2 \times 10^6) \times (1.2 \times 10^6)$ if implemented as a 1S1R structure (Fig. 23e). Here, the TS and memristor were interconnected *via* copper wire bonding to establish a functional series configuration.

Despite the advantages of integrating selector devices with memristors in crossbar arrays to mitigate sneak currents, successful demonstrations of such hybrid systems-particularly involving perovskite memristors-remain scarce due to significant fabrication challenges. Material incompatibility is a primary barrier: perovskite layers are sensitive to processing conditions, and depositing conventional diode materials atop them often requires high-temperature steps or harsh solvents that degrade the perovskite's structural integrity and switching properties. To address these challenges, novel fabrication techniques such as vapor deposition could be adopted. For instance, one device layer (*e.g.*, the perovskite active material) might be spin-coated, while subsequent selector layers are deposited *via* vapor methods. The compatibility of vapor deposition with perovskite materials – particularly its ability to avoid solvent-induced degradation – have been outlined in Section 4.3B. Alternatively, self-rectifying memristors which inherently suppress sneak currents without requiring external selector devices could be utilized.

Self-rectifying memristors are a type of bipolar switching device characterized by a high current ratio between positive and negative set or read voltages ($\pm V$). Self-rectification can be achieved through various strategies, including interface engineering, modifying the perovskite composition, or incorporating specific additives. These approaches effectively suppresses sneak path currents without the need for additional components, such as external selector devices, thereby simplifying device architecture and fabrication. For example, Pham *et al.* leveraged the Schottky barrier between tungsten electrodes and $MAPbI_3$ perovskite to achieve self-rectification, yielding a rectification ratio exceeding 100.[338] He *et al.* explored interface engineering by inserting an amorphous ZnO layer between the metal electrode and perovskite.[339] By adjusting UV exposure time, they modulated rectification and demonstrated sequential logic functions (true, false, AND, NOR, XOR, XNOR) within a single device. In other examples, PMMA was utilized as an interlayer material along with DJ perovskite (3-(aminomethyl)-piperidinium, 3AMP) as the active material, where configuration exhibited self-rectification ratio of nearly 10^3 (calculated as the ratio of reverse-bias minimum current to forward-bias maximum current).[108] Song *et al.* investigated self-rectifying behavior in memristors by analyzing reactions between metal contacts and a one-dimensional (1D) perovskite, ($(IFA)_3PbI_5$, Fig. 24a), with varying electrode materials.[212] The device displayed self-rectification with a silver electrode (Fig. 24b) but exhibited resistive switching with a gold electrode (Fig. 24c). To probe this mechanism, AgI layer was deposited atop the perovskite before evaporating Ag, achieving self-rectification (Fig. 24d). XPS depth profiling revealed Ag migration into the perovskite during

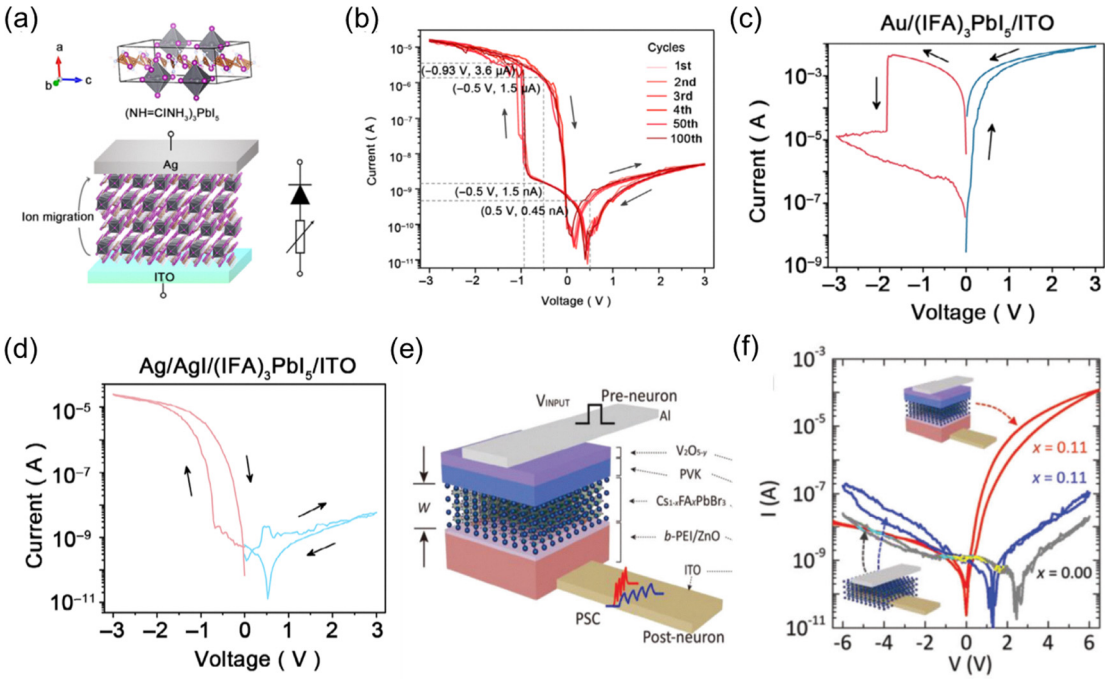

Fig. 24 (a) Schematic illustrations of the crystal structure of $(NH{=}ClNH_3)_3PbI_5$ (abbreviated as $(IFA)_3PbI_5$) (upper) and the three-layer device structure of Ag/$(IFA)_3PbI_5$/ITO (below). Due to AgI formation, it forms a PN junction near the top electrode and perovskite interface (bottom-right) (b) *IV* curve of the self-rectifying memristor showing rectification ratio of 3 orders with V_{read} of 0.5 V. (c) Top electrode was replaced with gold to verify the mechanism. No rectification was observed with gold. (d) A layer of AgI was deposited over the perovskite to test the hypothesis. Similar switching characteristics are obtained as Ag/$(IFA)_3PbI_5$/ITO device structure. (a)–(d) Reproduced from ref. 212 with permission from John Wiley and Sons, Copyright 2024. (e) Device stack adopted for making 8 × 8 crossbar array. (f) Self-rectifying response of the device obtained with varied *X* values in $Cs_{1-x}FA_x$. (e) and (f) Reproduced from ref. 328 with permission from John Wiley and Sons, Copyright 2023.

operation, forming an AgI-rich n-type region near the Ag electrode. This created a PN junction with the p-type perovskite, yielding a rectification ratio of 3×10^3 at $\pm 0.5V_{read}$.

Beyond interfacial engineering described above, modulating perovskite composition or incorporating additives can tailor device band alignment to induce self-rectifying behavior. For instance, an 8 × 8 crossbar array using $Cs_{1-x}FA_xPbBr_3$ quantum dots (Fig. 24e) demonstrated self-rectifying analog switching. By varying the Cs/FA ratio (x = 0–0.15, Fig. 24f), optimal FA incorporation (x = 0.11) enabled 89.08% accuracy in MNIST pattern recognition.[328] In another examples, blending the ferroelectric polymer [P(VDF-TrFE)] with 2D perovskite BA_2PbI_4 in a lateral heterojunction configuration produced a rectification ratio exceeding 10^6 at ±0.1 V.[340]

5.3. Crosstalk mitigation – active layer patterning

As device dimensions shrink to the nanometer scale, the memristive behavior of single cells exhibits significant differences from larger sizes. Currently, there is no universally accepted guideline to define what qualifies as an "ultra-high-density" crossbar array in perovskite memristors. Nevertheless, several commonly used metrics helps characterize array density and integration levels. These include the pitch size (*i.e.*, the center-to-center distance between adjacent cells), the normalized device footprint (*e.g.*, area per bit), and the overall integration density (*e.g.*, number of devices per cm^2).[322,341] But at the same time, compact electrode designs may induce crosstalk or even short circuits, severely compromising system stability. Increasing the spacing between devices is an effective way to reduce crosstalk, but this approach inherently limits how many memristors can be integrated within a given area-a critical trade off as the demand grows for both large-area arrays and high-resolution micro- and nanoscale structuring. In this context, precise patterning is essential not only for electrical isolation and minimizing crosstalk, but also for maximizing integration density. While some crossbar architectures rely primarily on patterned electrodes to define memory cells, the need for accurate patterning of the active perovskite layer becomes increasingly important as device dimensions shrink. Various methods available to patterned perovskite arrays will be indicated below.

5.3.1. Template-assisted nanoscale patterning technique. To achieve higher density deposition technologies, such as template assisted patterning can be considered. Hwang *et al.* addressed this issue by employing a sequential vapor deposition method to construct a 16 × 16 crossbar array.[279] The fabrication process as shown in Fig. 25a, involved lithography and etching on a silicon substrate to create 250 nm *via*-holes, followed by sequential vapor deposition of PbI_2 and MAI to form the $MAPbI_3$ memory layer. Finally, thermal evaporation was used to deposit Au electrodes. The memristor device operates based on iodine vacancies, forming conductive filaments (CFs) and exhibiting bipolar resistive switching. Notably,

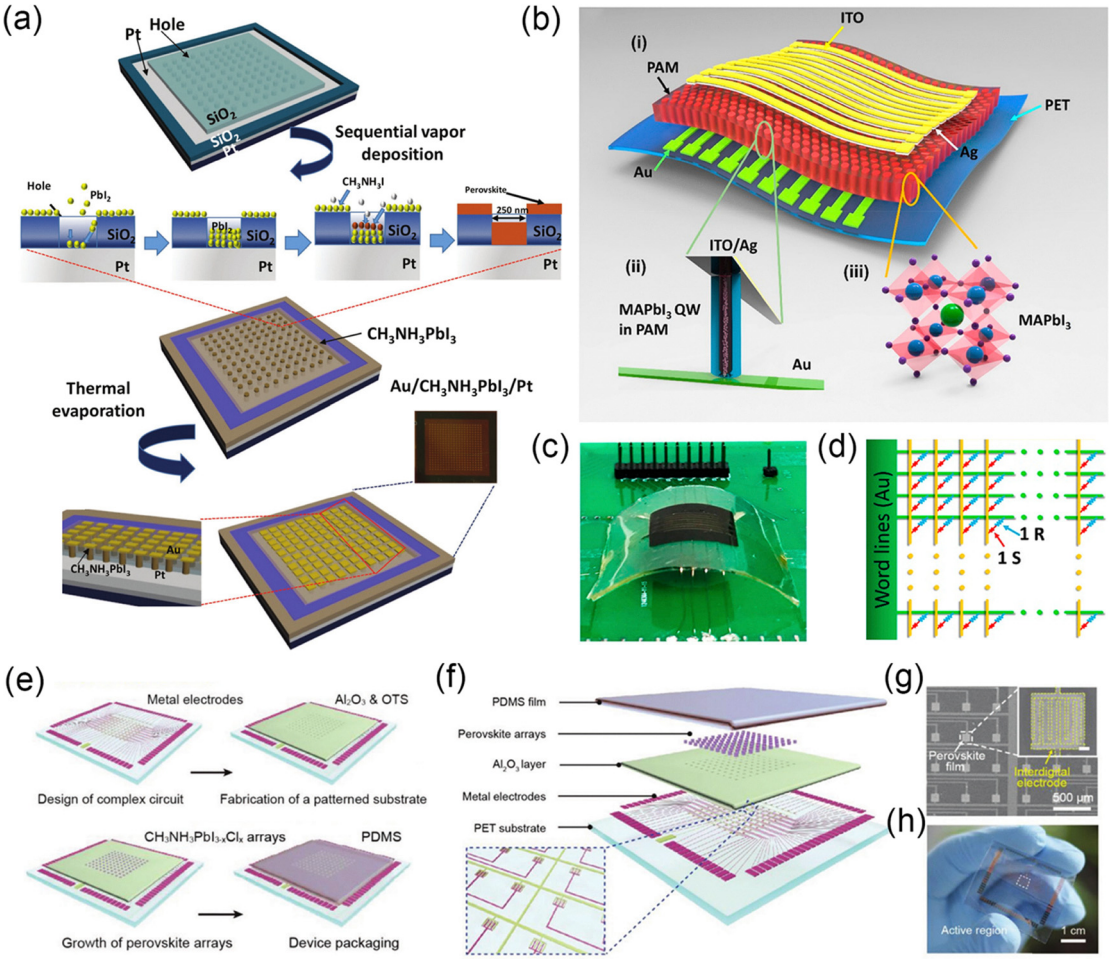

Fig. 25 (a) Schematic diagram of a flexible memristor array based on $MAPbI_3$ quantum wires. Reproduced from ref. 279 with permission from John Wiley & Sons, Copyright 2017. (b) Optical image of a flexible 8 × 8 memristor array. (c) Schematic diagram of the memristor array drive setup. (b) and (c) Reproduced from ref. 279 with permission from John Wiley & Sons, Copyright 2017. (d) Schematic diagram of the organic–inorganic perovskite memristor fabrication process based on making 250-nanometer through-holes on a wafer. Reprinted with permission from ref. 161. Copyright 2021 American Chemical Society. (e) Schematic of the device fabrication process with photolithography-assisted Al_2O_3 hydrophilic patterning technique. (f) Structure and fabrication process of flexible PD arrays. (g) SEM image of PD arrays; zoom in on the area shows the single device structure. (h) Optical image of 10 × 10 high-resolution flexible photodetector arrays. (e)–(h) Reproduced from ref. 343 with permission from John Wiley & Sons, Copyright 2018.

it demonstrated low operating voltages ($V_{SET} \approx 0.6$ V, $V_{RESET} \approx -1.5$ V), high-speed switching (200 ns), and long data retention ($>10^5$ s). Using a similar approach, Poddar *et al.* developed a unique strategy for fabricating ultra-miniaturized perovskite devices. They demonstrated an ultra-high-density 3D crossbar array (8 × 8 crossbar array) based on $MAPbI_3$ nanowires – Fig. 25b shows the structure of this flexible memristor array.[161] The growth of perovskites was confined *via* vapor deposition combined with nanopore templates. In this study, a porous alumina membrane was employed to further reduce the through-hole size to 10 nm, enabling fabrication on PET substrates and imparting mechanical flexibility to the device (Fig. 25c). The sneakpath currents between neighboring cells was effectively inhibited through the 1S–1R structure (Fig. 25d), resulting in the memristor array exhibiting an ultra-fast switching speed of 100 ps, a storage unit area of 76.5 nm^2, ultra-low power consumption (~1 pJ), and an extended operational lifetime (>2 years of data retention).

Notably, nanoengineered templates provide an effective approach for miniaturizing perovskite photodetector devices. Gu *et al.* employed the vapor–solid–solid reaction (VSSR) method to fabricate a uniformly arranged three-dimensional (3D) $MAPbI_3$ nanowire array within a porous alumina membrane template, constructing a 32 × 32 perovskite array.[342] The array exhibited an ultra-high nanowire density (4 × 10^8–10^9 cm^{-2}), with each nanowire featuring a diameter of ~100–400 nm and a length of 2 μm. Furthermore, the vertically aligned nanowire configuration effectively mitigated signal inhomogeneity caused by random orientation. Alternative process integrations can also be employed to fabricate perovskite photodetector arrays. Wu *et al.* successfully fabricated a 10 × 10 high-resolution lateral arrays based on $MAPbI_{3-x}Cl_x$ perovskite films.[343] The authors first employed a photolithography-assisted Al_2O_3 hydrophilic patterning technique (Fig. 25e–h), rendering the micronized regions of the substrate hydrophobic, thereby ensuring that the perovskite precursor solution remained confined to these regions for

controlled crystallization. The resulting array could be utilised for fabricating lateral perovskite memristors.

5.3.2. Photolithographic patterning. As the key micro-nanofabrication technology in the semiconductor industry, photolithography has been trialled for perovskite optoelectronic device fabrication. Liang *et al.* utilized ultrathin encapsulation-assisted photolithography and etching techniques to fabricate a 48 × 48 perovskite device array with a device structure of ITO/NiO_x/$MAPbI_3$/C_{60}/BCP/Ag.[344] The authors first fabricated a predefined bottom electrode using a standard photolithography process followed by sputtering of ITO. SU-8 photoresist was then employed to confine the perovskite regions and serve as a template for subsequent solution-based deposition. This approach enabled the successful preparation of a 40 μm × 40 μm patterned perovskite array (Fig. 26a), demonstrating its suitability for large-scale array applications. Perovskite materials are highly sensitive to polar solvents and etchants used in lithography processes, which can potentially degrade their structural integrity and compromise device performance. Therefore, research on low-damage lithography techniques should be prioritized. Zou *et al.* proposed a dry lift-off method using parylene as an intermediate layer, enabling solvent-free processing to avoid damage to the perovskite materials.[345] This approach achieved high-resolution perovskite patterning with a feature size down to 4 μm. Moreover, the multi-round patterning capability of parylene, which can be peeled off repeatedly while preserving the underlying structures, allows for the stacking of multiple perovskite materials in a layer-by-layer fashion.

However, the perovskite array is still micron-sized, for further optimization in high-end optoelectronic applications, advancements in nanoscale lithography remain essential. Lin *et al.* proposed a strategy of orthogonal processing and orthogonal lithography to achieve scalable micro- and nano-scale device fabrication using solvents that are non-destructive to perovskite materials.[346] In their study, the authors examined the effects of 12 different solvents (including water, ethanol, isopropanol, dichloromethane, and *N*,*N*-dimethylformamide) on 3D perovskites ($MAPbBr_3$) and 2D layered perovskites ($(C_6H_5C_2H_4NH_3)_2PbI_4$). The results indicate that chlorobenzene and hexane do not alter the optical or electrical properties of perovskites, making them ideal orthogonal solvents. This method successfully incorporated orthogonal solvents into the entire electron beam lithography (EBL) process, including both development and lift-off, enabling nanoscale patterning (channel length ~380 nm) without the need for etching (Fig. 26b). Importantly, it preserved the optoelectronic properties of ultrathin perovskite nanosheets, offering a promising route for the scalable nanoelectronic integration of halide perovskites.

5.3.3. Nanoimprint lithography based patterning. In the miniaturization of perovskite devices, nanoimprint lithography (NIL) potentially offers lower cost and broader material compatibility compared to photolithography and EBL. Since NIL utilizes mechanical imprinting, it can directly form nanopatterns on perovskite films, enabling high-throughput manufacturing and demonstrating great potential for miniaturization and large-scale integration of perovskite memristors. Jeong *et al.* proposed a low-temperature patterning strategy based on polymer-assisted nanoimprinting, in which polyethylene oxide was blended into the perovskite precursor film to inhibit rapid crystallization during impronting, while PVDF-TrFE served as a backfilling and structural stabilizing layer (Fig. 26c).[347] This approach enabled the fabrication of $CsPbBr_3$ and $CsPbI_3$ nanopatterned structures with a minimum line width of 200 nm, under mild conditions of ≤100 kPa pressure and 80 °C temperature

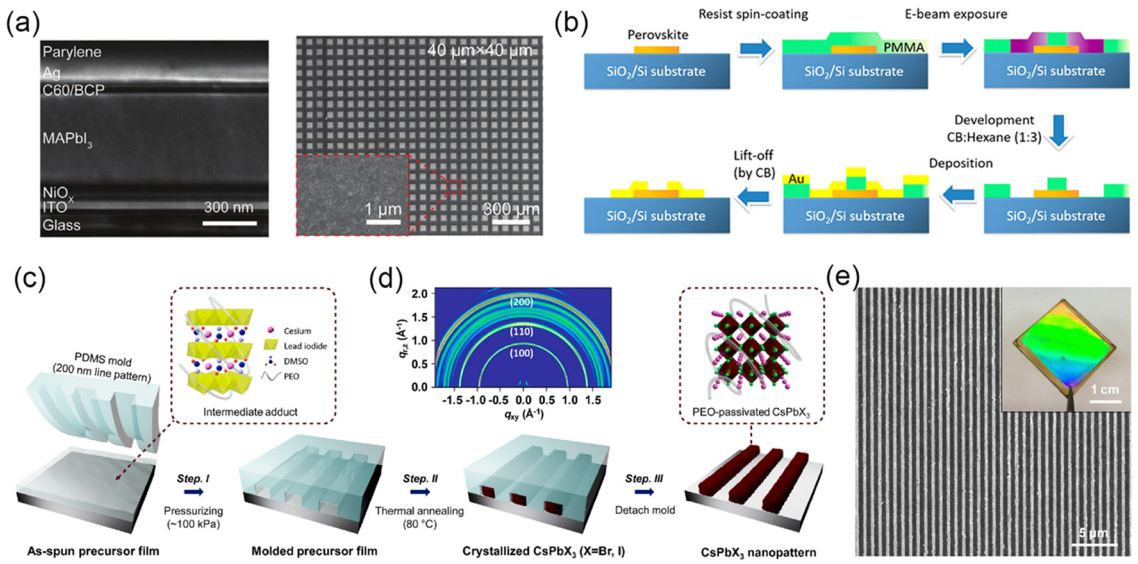

Fig. 26 (a) Cross-sectional SEM image of ITO/NiOx/$MAPbI_3$/C_{60}/BCP/Ag photodetector and SEM image of 40 μm × 40 μm perovskite array. Reproduced from ref. 344 with permission from John Wiley & Sons, Copyright 2021. (b) Schematic diagram of the photolithography process using orthogonal solvents. Reprinted with permission from ref. 346. Copyright 2019 American Chemical Society. (c) Schematics of polymer-assisted nanoimprinting. (d) GIWAXS pattern of the $CsPbI_3$ nanopattern. (e) Image and photograph of $CsPbI_3$ nanowires after large-area polymer-assisted nanoimprinting. (c)–(e) Reprinted with permission from ref. 347. Copyright 2020 American Chemical Society.

(Fig. 26d and e). The method is compatible with various substrates, including flexible PET, and offers a universal platform for the scalable fabrication of high-resolution perovskite-based patterned devices. Similarly, Wang *et al.* reported three distinct structural patterns—planar, nanopillar, and nanograting—were successfully fabricated on the $MAPbI_3$ film using NIL.[348] These structures led to notable improvements in the perovskite crystal quality, and perovskite ($MAPbI_3$) grain size increased from 68 nm to 188 nm. Similar studies have shown that NIL can suppress the formation of PbI_2 through pressure-induced crystallization.[349] Overall, NIL not only enables miniaturization and array fabrication but also enhances crystallization quality, making it a promising approach for high-performance optoelectronic integrated systems.

5.3.4. Large area/high throughput memristor array fabrication. To date, there have been relatively few reports on large-area perovskite memristor arrays, primarily due to the nascency of the field. However, large-area fabrication is a critical step toward industrialization, and it is prospective that advanced solution-based fabrication techniques developed for other perovskite-based optoelectronic devices could be adapted for the scalable construction of memristor arrays. Solution-based fabrication techniques, including inkjet printing, spray coating, and blade coating, have emerged as promising strategies for scalable, cost-effective, and high-throughput fabrication. These methods leverage the excellent solution processability of metal halide perovskites, enabling low-temperature, large-area, and high-throughput device fabrication on various substrates, including flexible and transparent platforms, which have been widely utilized in large-area perovskite optoelectronic devices such as solar cells, photodetector and LEDs. Owing to the structural similarities between these optoelectronic devices and perovskite memristors, many of the fabrication steps can be adapted for memristor fabrication. In the following sections, we will explore each of these solution-based approaches, focusing on their principles, advantages, challenges, and recent advancements in large-area perovskite device fabrication.[350,351]

Inkjet printing has become one of the core technologies for preparing high-resolution, patternable, and scalable perovskite devices due to its maskless, digitally controlled, and non-contact characteristics. Schröder *et al.* employed combinatorial inkjet printing to fabricate a wide-spectrum selective perovskite photodetector array.[352] As shown in Fig. 27a, by precisely tuning the mixing ratio of $MAPbI_3$, $MAPbBr_3$, and $MAPbCl_3$, the detector's absorption edge was adjusted from 410 nm to 790 nm, achieving a spectral resolution of 8 nm (Fig. 27b). This strategy provides a solution for multi-perovskite composite memristors, avoiding the uniformity problems of traditional processes (such as multi-step solution processing). Nässström *et al.* reported a combinatorial inkjet printing method, integrated with an optimized droplet arrangement algorithm, to fabricate $CsPb(Br_xI_{1-x})_3$ metal-halide perovskite film arrays, which was proved in Fig. 27c with GIWAXS results.[353] The resulting arrays contained 10 distinct perovskite compositions within an 8×8 mm^2 area, achieving a tunable bandgap ranging from 1.8 to 2.3 eV, making them suitable for applications in photodetectors, LEDs, and solar cells. Interestingly, inspired by inkjet printing, Duan *et al.* developed a hybrid electrostatic fluid dynamic printing method, achieving spatial gradient perovskite micro/nanopatterns with an unprecedented 1 μm resolution.[354] By precisely modulating the driving voltage of the multi-channel nozzle, this method enables the fabrication of gradient line arrays and concentric dot arrays with tunable band gaps. The adjustable array size ranges from 700×700 μm^2 to 60×60 mm^2, all achieved through a single-step printing process, facilitating filter-free, chip-level multispectral detection and artificial visual imaging. This approach overcomes the size limitations (which is an important parameter for perovskite memristor) of traditional lithography and inkjet printing, thereby significantly enhancing the integration and manufacturing flexibility of perovskite optoelectronic devices. In Fig. 27d and e, Gu *et al.* employed polymer-assisted crystallization technology to successfully inkjet-print a large-area, high-density perovskite layer on the flexible substrate, this photodetector achieving 96.8% retention of its initial photocurrent after 15 000 consecutive bending cycles, demonstrating its exceptional mechanical stability.[355]

Spray coating is a cost-effective, high-throughput solution-processing technology with significant potential for the fabrication of large-area perovskite-based devices. Compared to inkjet printing, spray coating enables the rapid deposition of functional layers over large-area substrates and is particularly well-suited for roll-to-roll (R2R) manufacturing, making it a highly attractive technique for scaling up industrial production.[358] Deng *et al.* proposed an all-sprayed process, integrating two-dimensional $CsPbBr_3$ nanosheets as photosensitive materials and MXene as conductive electrodes, to fabricate a high-density 1665-pixel light detection array (72 cm^2, 24 units per cm^2).[359] This strategy highlights the potential of the all-sprayed fabrication approach in wearable optoelectronics, flexible sensing/memory systems, and high-efficiency optical communication. The spray-coating process can also be utilized for the fabrication of non-planar optoelectronic devices. As shown in Fig. 27f, Feng *et al.* realized for the first time a hemispherical narrow-bandwidth photodetector fabricated *via* a spray-coating technique, utilizing quasi-two-dimensional $PEA_2FA_{n-1}Pb_nX_{3n+1}$ perovskite as the photosensitive material.[356] The film thickness was precisely controlled by adjusting the number of spray layers and solution concentration, enabling narrow-band spectral selectivity with a full width at half maximum (FWHM) of <20 nm and 180° viewing angle coverage (Fig. 27g). Compared to conventional planar devices, this approach eliminates the need for complex optical lenses or photolithography processes and allows for the direct fabrication of 9×9 microarray perovskite devices.

Blade coating is an efficient and cost-effective solution deposition technique that has been used for high throughput fabrication of perovskite devices. In recent years, research have been conducted to optimize crystal quality, enable patterned deposition, expand flexible device applications, and enhance optoelectronic performance through blade-coating processes, leading to notable advancements in the field.[360] Hsiao *et al.* reported a vertical transmission photodetector based on an n-type 3D $MAPbI_3$/p-type quasi-2D (Q-2D) $BA_2MA_2Pb_3I_{10}$ perovskite heterojunction, achieving a self-powered operating mode

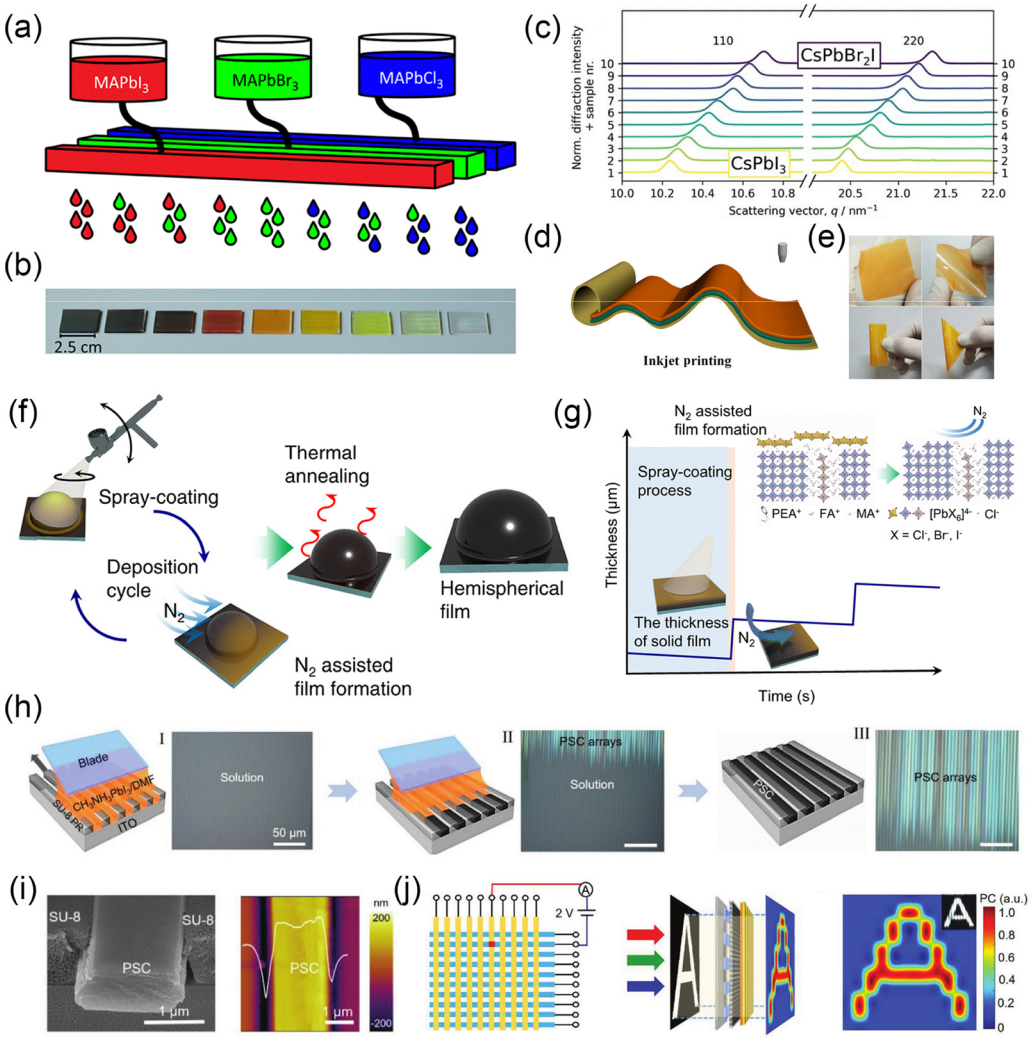

Fig. 27 (a) Schematic diagram of combined printing. (b) Co-sited halide gradient variation in methylammonium-based metal halide perovskites. (a) and (b) Reproduced from ref. 352 with permission from John Wiley & Sons, Copyright 2021. (c) Azimuthal composite waterfall plot of the GIWAXS pattern of $CsPb(Br_xI_{1-x})_3$.[353] (d) Inkjet printing of large-scale flexible perovskite films. (e) Photos of perovskite films printed under different mechanical bending conditions. (d) and (e) Reproduced from ref. 355 with permission from Springer Nature, Copyright 2021. (f) Schematic diagram of the film fabrication process through spray-coating on the hemispherical narrow-bandwidth photodetector. (g) Schematic diagram of solid film thickness during spraying and nitrogen flow.[356] (h) Schematic diagram of the preparation of perovskite arrays using the microchannel-confined crystallization (MCC) strategy. (i) Cross-sectional SEM image of $MAPbI_3$ perovskite. (j) Schematic diagram of the 10 × 10 photodetector array measurement setup and projection imaging method. (h)–(j) Reproduced from ref. 357 with permission from John Wiley & Sons, Copyright 2020.

for the first time while enhancing the stability and optoelectronic performance of the device.[361] The research team fabricated a large-area perovskite layer *via* doctor-blade coating and utilized self-doping to modulate the conductivity types of the 3D and Q-2D layers, forming a well-defined n–p junction.

Beyond enhancing the uniformity of large-area films, the blade coating process can also be integrated with other techniques to fabricate miniaturized devices or pattern perovskite materials. Photography combined with blade coating can also be used for high throughput preparation of perovskite single-crystal arrays. As shown in Fig. 27h and i, Deng *et al.* utilized photolithographically defined microchannel structures to precisely regulate the transport and crystallization of perovskite solutions, in combination with blade coating, to achieve the large-scale fabrication of 10 × 10 perovskite single-crystal arrays.[32] Then, a vertical photodetector array integrated based on this technology successfully demonstrated imaging capabilities, demonstrating its potential in smart sensing, imaging systems, and optoelectronic chip integration (Fig. 27j). Additionally, Chen *et al.* developed a NIL + blade coating approach to directly fabricate a 550 nm pitch nanograting on a flexible COC substrate. The perovskite precursor solution was utilized to self-assemble and fill the grating, successfully yielding a high-quality $MAPbI_3$ nanostructured film. This method eliminates the need for additional etching, particularly suitable for making high-density perovskite memristor arrays. Looking ahead, this strategy can be integrated with flexible roll-to-roll (R2R) manufacturing and ultra-high-resolution micro-nanolithography, advancing the

industrial application of flexible perovskite optoelectronic devices.[362]

6. Demonstration of memristors for neuromorphic applications

As discussed in the previous section, memristors can be classified into two types based on the retention time of their states: volatile and non-volatile. These two categories exhibit distinct switching behaviors and physical mechanisms, which determine their suitability for various neuromorphic computing applications. Volatile memristors are characterized by their spontaneous conductance decay once electrical or optical stimulation is removed, whereas non-volatile memristors maintain their conductance state persistently after stimulation. This fundamental difference underpins their use in different computational scenarios.

Both volatile and non-volatile memristors enable neuromorphic computing but serve distinct roles.[363] Volatile memristors are particularly well-suited for dynamic, event-driven tasks such as in-sensor or near-sensor computing applications. In contrast, non-volatile memristors excel in static, high-precision tasks such as artificial neural networks (ANNs) and long-term data storage. Non-volatile memristors benefit from the stable and persistent conductance, achieving high accuracy at the expense of greater energy consumption, whereas event-driven nature of volatile memristors, offer superior energy efficiency but typically lower accuracy and higher latency. As a result, volatile memristors are best used for processing streaming or temporal data near sensors, while non-volatile memristors are preferable for complex, high-precision processing tasks. For example, in reservoir neural network applications, volatile memristors can serve as the reservoir layer, while non-volatile memristors function as the trainable readout layer to perform classification of neural firing pattern.[182] Various applications have been demonstrated in the literature, and these will be discussed in detail in this section.

The utilization of memristors in neuromorphic systems depends critically on their endurance and their retention time. In the context of synaptic training, memristors require high endurance, typically greater than 10^6 cycles, to withstand the frequent weight updates during backpropagation.[364] Additionally, a moderate-to-long retention time, exceeding 10^3 seconds, is essential to retain the learned weights between training epochs. For selector devices, which are employed to control access in crossbar arrays, a short retention time of less than 10 seconds is desirable to ensure volatility and prevent interference with adjacent cells. During synaptic inference, where memristors are primarily used for reading pre-trained weights with only occasional updates, the endurance requirement is moderate, typically between 10^4 and 10^6 cycles. However, a long retention time, greater than 10 seconds, is necessary to preserve the pre-trained weights over extended periods of inference operations.

However, it is important to note that, despite the goal of implementing neural networks directly on perovskite array devices, most reported applications currently involve extracting data from the array and then performing neural network simulation externally to accomplish the task. Most publications simulate results using data from individual dot array devices, while a few go further by using data from actual crossbar arrays. Nevertheless, in all cases, neural network simulations are still performed off-chip. Some studies have demonstrated that the array is capable of displaying images or handwritten digits, but tasks (such as training to accomplish classification, recognition, *etc.*) is still off-chip. To date, publications demonstrating on-chip training using perovskite arrays remain rare, probably due to their issue with device-to-device variation, cycle-to-cycle variation, and endurance.

6.1. Emerging applications of volatile perovskite memristors

The conductance state of volatile perovskite memristors can change rapidly in response to electrical stimulation, but tend to decay over time, making it difficult to retain for extended periods.[172,365] It is worth mentioning that in literature, ''volatile memristor'' and ''diffusive memristor'' are sometimes used interchangeably, but they are not entirely equivalent concepts. ''Volatile'' describes the behavior of the conductivity state, not the specific physical mechanism. As discussed in previous sections, the origins of volatility can be diverse. In contrast, ''diffusive'' denotes a particular physical mechanism, typically involving ion migration and spontaneous redistribution, which is one possible pathway to achieving volatile behavior. However, there is not a big difference in electrical behavior. For example, such devices exhibit a transiently enhanced current response after pulsing, which gradually returns to the baseline state, a characteristic suited for neuromorphic functions involving short-term memory.[366] In typical neuromorphic systems, short-term retention times are considered to lie within the range of a few milliseconds to several seconds, depending on the application scenario and synaptic model (*e.g.*, short-term plasticity such as paired-pulse facilitation or depression) employed.[341,365,367] In the study of volatile perovskite memristors, researchers often employ a range of time-sensitive and multimodal characterization techniques to investigate their transient behavior, dynamic plasticity, and optoelectronic synergistic responses. Typically, *I–V* scanning is first performed to identify the presence of volatile switching behavior. Subsequently, pulse-induced conductance measurements and conductance–time decay curves are used to emulate specific biological functionalities, such as short-term synaptic plasticity and relaxation dynamics. In addition, light modulation or optoelectronic co-stimulation can be introduced to enrich the regulatory mechanisms, enabling perovskite memristors to function in a broader range of neuromorphic and in-sensor computing scenarios.[368] This chapter systematically reviews the core role of volatile perovskite memristors in a variety of brain-inspired computing paradigms, including synaptic short-term plasticity, neuron emulation, reservoir computing, and nociceptor simulation.

6.1.1. Short-term synaptic plasticity for transient feature enhancement, dynamic noise filtering and emulating neural dynamics. Short-term synaptic dynamics, including STP, EPSC,

and spike-rate dependent plasticity (SRDP), are essential mechanisms that emulate biological functions such as short-term memory, instantaneous enhancement, and rapid forgetting in artificial neurons. The key to the ability of volatile perovskite memristors to simulate short-term synaptic dynamics lies in their short-term memory, nonlinear response, pulse dependence, as well as dual regulation capabilities by both electrical and optical triggers. Halide perovskite naturally fulfils these requirements owing to their ion migration dynamics, enabling relaxation time from sub-microseconds to seconds by adjusting pulse frequency or bias amplitude. In oxide- or chalcogenide-based memristors, volatility is typically achieved through filament rupture or defect relaxation, which often leads to abrupt, binary conductance decay and limited control of temporal constants. Table 7 lists the device characteristics and test methods required for these functions.

Zawal *et al.* and Gong *et al.* demonstrated a dual-channel artificial synapse with both electrical and optical modulation capabilities by constructing memristors based on $MAPbI_3$ and $FAPbI_3$, respectively.[369,370] Fig. 28a and b shows the schematic diagram of the biological synapse and the memristor structure. These devices exhibit PPF, which is hallmark characteristics of STP in volatile memristors. Furthermore, by incorporating photoresponsive behavior of perovskite materials, the devices exhibit light-dependent volatile behavior (Fig. 28c), providing a promising route for optical synaptic devices in applications such as intelligent perception. Xiao *et al.* fabricated a volatile memristor with a device stack of Au/$MAPbI_3$/PEDOT:PSS/ITO. Its ion migration mechanism and p–i–n structure switchability are the sources of its volatility and simulated synaptic behavior. The device successfully reproduced key neural functions such as STP, LTP, SRDP, and four types of STDP behaviors and enabled efficient modulation under both electrical and optical inputs.[300]

In general, these properties of volatile perovskite memristors can be strategically harnessed for a variety of neuromorphic computing tasks. For instance, devices exhibiting STP and pulse-dependent conductance modulation are particularly suited for front-end sensory signal conditioning, such as transient feature enhancement and dynamic noise filtering, where short-term memory and rapid adaptation are advantageous.[143,160] On the other hand, devices that respond to optical stimulation or demonstrate optoelectronic STDP are promising candidates for vision-inspired computing and near-sensor preprocessing of dynamic visual inputs, since light-induced volatility enables the integration of sensing and transient memory, thereby emulating early-stage biological perception-processing mechanisms.[371,372]

Table 7 Short-term synaptic dynamics emulated by halide perovskite memristors

Synaptic behavior	Device requirements	Test method	Potential application
STP	Volatile conductance with time-dependent decay	Train of identical pulses; monitor decay	Transient feature enhancement or denoising process[143,160]
EPSC	Transient current response with exponential decay	Single pulse; measure current *vs.* time	Sensory signal characteristics (*e.g.*, visual, olfactory adaptability)[17,373]
SRDP	Conductance change depends on spike frequency	Vary spike train frequency; ΔG *vs.* freq	Simulation of auditory properties (*e.g.*, the function of hair cells)[374]

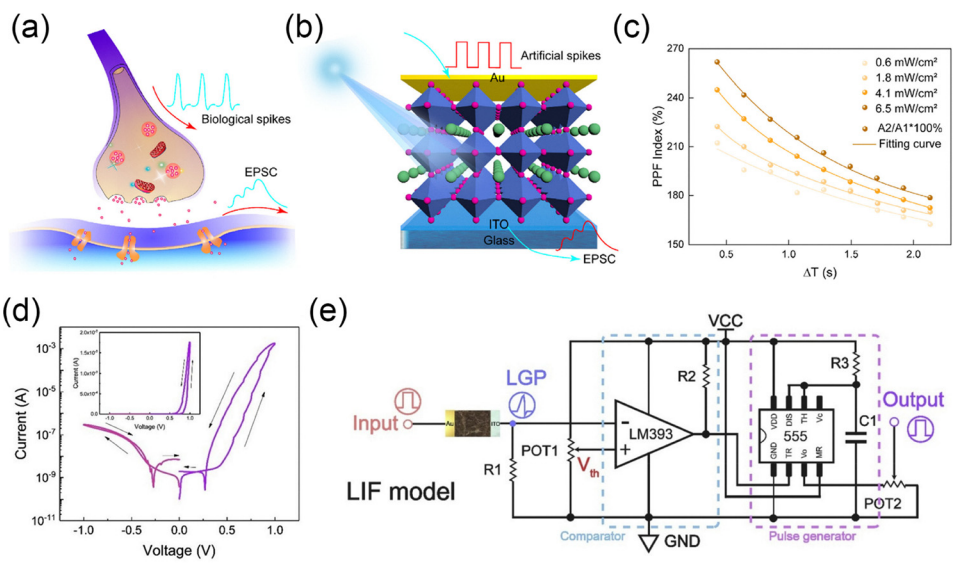

Fig. 28 (a) The schematic diagram of the biological synapse and (b) the memristor structure. (c) PPF index with different light intensity. (a)–(c) Reproduced from ref. 370 with permission from the Royal Society of Chemistry, Copyright 2021. (d) The volatile behavior of Au/$MAPbI_3$/ITO memristor. (e) LIF model circuit design with integrated perovskite memristor. (d) and (e) Reproduced from ref. 170 with permission from the Royal Society of Chemistry, Copyright 2020.

Therefore, by leveraging these functional characteristics, volatile perovskite memristors can be tailored for application-specific and highly parallel information processing architectures, paving the way for next-generation neuromorphic and in-sensor computing systems.

In addition to emulating short-term synaptic functions, due to the volatility of the device, the conductance gradually decays without stimulation, and it can also be used to simulate the leakage of membrane potential. Yang *et al.* proposed a volatile perovskite memristor with an Au/$MAPbI_3$/ITO structure, which exhibits volatile characteristics (Fig. 28d) and linearly tunable multi-level conductance states. The device successfully mimics key neuronal behaviors such as leaky integration, integration-and-fire, and post-firing discharge, thereby serving as a functional substitute for biological neurons in the leaky integrate-and-fire (LIF) model (Fig. 28e).[170] These findings highlight the potential of volatile perovskite memristors as hardware building blocks for spiking neural networks and event-driven neuromorphic systems. Their ability to instantaneously respond to sensory stimuli, update memory, and realize natural information fading makes them particularly well-suited for developing low-power neuromorphic architectures with integrated sensing, processing, and memory functionalities.

6.1.2. Reservoir computing layer for temporal data processing. Reservoir computing (RC) is a computational model based on recurrent neural networks (RNNs), designed specifically for processing time series data. The core principle of RC is to leverage the dynamic response of nodes within a fixed-structure reservoir to process the temporal information of the input signal. Unlike traditional neural networks, which require training of all weights, RC differentiates itself by maintaining a fixed structure for the reservoir, with training focusing solely on the connection weights between the reservoir and the output layer. This unique feature significantly reduces computational complexity and enhances the efficiency of the model.[375,376] In RC (Fig. 29a), the reservoir layer is required to exhibit three essential characteristics: fading memory, nonlinear responses to input sequences, and a dynamically tunable state space.[182] These requirements align well with the properties of volatile perovskite memristors, which exhibit conductance decay over time, strong nonlinear ion migration dynamics, and pulse-dependent transient responses that can be finely modulated by parameters such as frequency, amplitude, and duration. Additionally, the inherently nonlinear ionic–electronic coupling and photoresponsivity behaviour of perovskite devices provide a rich dynamic state space, enabling complex temporal encoding of input sequences. Therefore, parameters such as volatility, nonlinearity, and energy efficiency play decisive roles in determining reservoir performance, and the tunability of perovskite memristors offers a unique platform for efficient, temporal computing.

Benefiting from the ultra-high density of volatile conductance states in volatile perovskite memristors, the device's relaxation behavior can be evaluated using a single electrical pulse, as demonstrated in Fig. 29b.[377] The relaxation characteristics vary with perovskite concentration, it can also be regulated by factors such as film thickness and pulse parameters. Specifically, both the pulse amplitude and width can be used to tune the relaxation time, offering fine control over the device's transient dynamics. The nonlinear responses to input sequences is a hallmark of the device's attenuated memory behavior, which can be modulated through voltage pulses of varying amplitude. Fig. 29c presents the current responses under a pulse train test, where each sequence contains 28 identical voltage pulses with amplitudes ranging from 1.5 V to 2.2 V, a pulse width of 2 ms, and a pulse interval of 2 ms. In Fig. 29d, the peak current values of the 28 pulses in each sequence are extracted and plotted. The results show that different pulse amplitudes generate distinct time-dependent conductance profiles, illustrating the device's ability to perform nonlinear mapping of input sequences into a multi-dimensional conductance space.[378]

For RC, dynamically tunable conductance states are required, and multi-bit encoding can be achieved through pulse patterning. 3-Bit (8-state) and 4-bit (16-state) logic encoding can be programmed with pulse sequences. Taking the 4-bit code ''1101'' as an example, ''1'' denotes a pulse input with voltage, while ''0'' represents a low-level input. As shown in Fig. 29e, the device can reliably distinguish 16 discrete conductance states ranging from 0000 to 1111, forming the basis for programmable state representation. This encoding capability is leveraged as a reservoir layer for tasks such as image-based signal transformation. In the example shown in Fig. 29f, an input image (*e.g.*, a handwritten digit) is divided into four feature segments, each mapped into the 16-state encoding scheme *via* pulse stimulation. These outputs, which represent transient high-dimensional reservoir states, are then fed into a software-defined or non-volatile hardware classifier (Fig. 29g) to complete the final recognition task. Thus, the volatile perovskite memristor serves as a spatiotemporal encoder, while the actual classification relies on stable readout units. This is the typical RC architecture where the reservoir is dynamic and untrained, but the readout is deterministic and trainable.[377]

Building upon this concept, a study published in 2022 proposed a vertically structured volatile memristor array (Au/$MAPbI_3$/ITO) exhibiting excellent analog switching and decay characteristics, as shown in Fig. 29h and i. The authors constructed a complete RC system by mapping image grayscale values into voltage pulse sequences, which were then applied to the memristor array to generate temporal dynamic reservoir states.[378] Similarly, a study published by John *et al.* reported a reconfigurable $CsPbBr_3$ nanocrystal memristor capable of switching between volatile and non-volatile modes by tuning the compliance current (I_{CC}). In this work, the volatile mode was related to the formation and breakage of Ag conductive filaments (Fig. 29j and k), and this mode was specifically employed to construct the reservoir layer, enabling effective capture of temporal variations in the input pulse streams.[182] These studies highlight the enormous potential of volatile perovskite memristors in RC systems: the former work emphasizes analog encoding and high-dimensional dynamic mapping for input information, while the latter study focuses on multi-mode adaptability and biological signal processing. These advances offer critical support for the development of high-

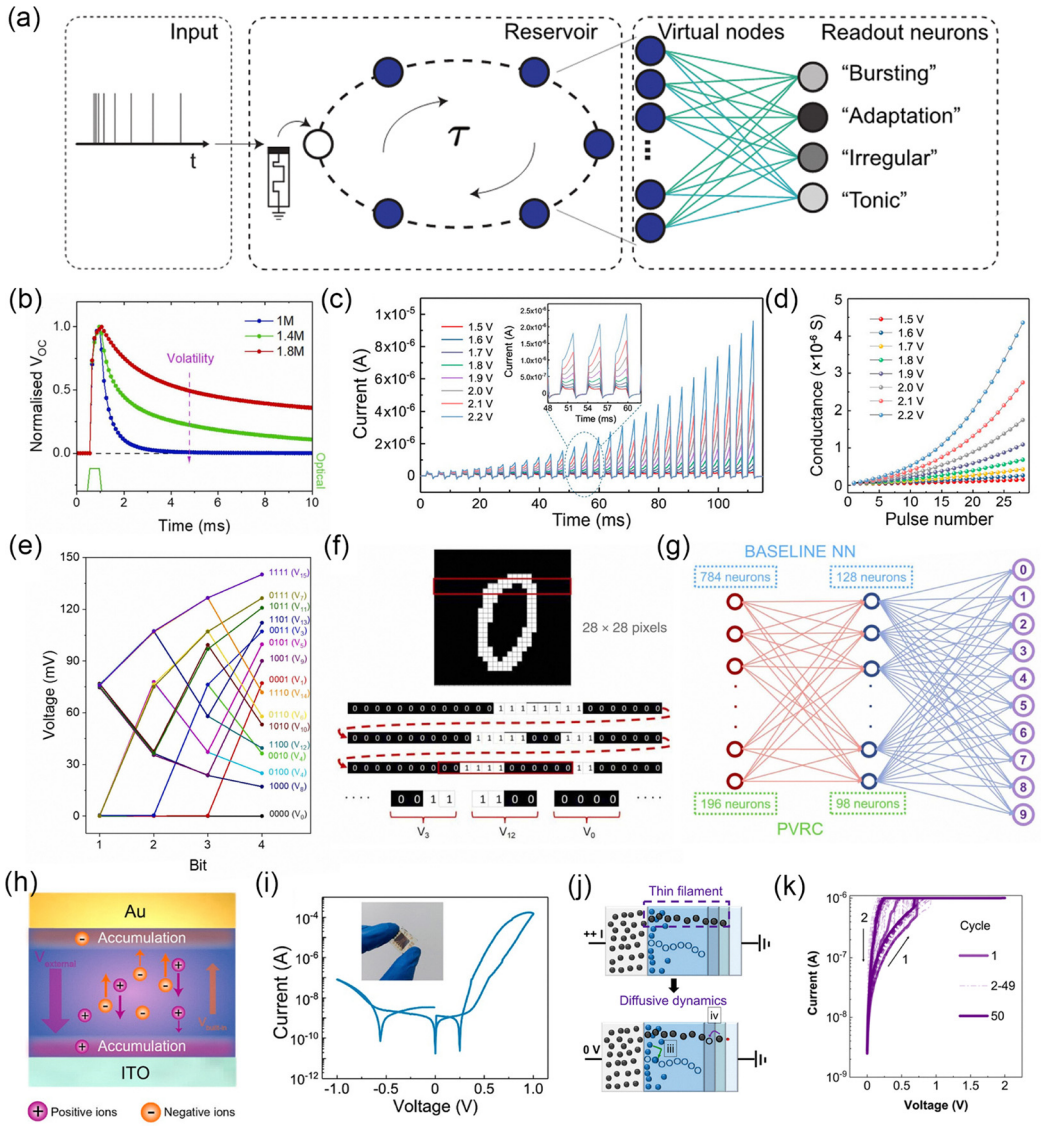

Fig. 29 (a) Schematic diagram of reservoir computing system, including input layer, reservoir layer, and training layer. Reproduced from ref. 182, under the terms of the Creative Commons CC BY 4.0 license (https://creativecommons.org/licenses/by/4.0). (b) Response to a single light pulse with different perovskite concentrations – 1 M, 1.4 M, and 1.8 M. (c) The current response of the perovskite memristor to different pulse sequences, which contain 28 identical voltage pulses. Inset: A zoomed-in view of the current response. (d) The trend of the memristor conductance variation extracted from *c*. (e) 16 unique reservoir states obtained at the end of the 4-bit pulse train, from '0000' to '1111'. (f) Schematic diagram of segmenting a handwritten digit into groups of 4 pixels corresponding to the input pulses. (g) Schematic diagram of training the output results of the reservoir layer. (b)–(g) Reprinted from ref. 377, Copyright 2024, with permission from Elsevier. (h) The memristor structure of Au/$MAPbI_3$/ITO. (i) *I*–*V* curve of volatile behavior, with the inset is a device photograph. Reprinted with permission from ref. 378. (h) and (i) Copyright 2022 American Chemical Society. (j) Volatile memristor involving silver conductive filaments. (k) *I*–*V* curve of digital volatile behavior. (j) and (k) Reproduced from ref. 182, under the terms of the Creative Commons CC BY 4.0 license (https://creativecommons.org/licenses/by/4.0).

precision, low-power, flexible, and programmable neuromorphic hardware platforms and further underscore the unique advantages of perovskite memristors in emulating spatiotemporal information processing.

While both the STP and RC systems exploit the volatile dynamics of perovskite memristors, their roles and system architecture differ significantly. STP primarily describes the local, device-level plastic behavior of individual synapses, which can be utilized for simple signal filtering, preprocessing, or short-term memory emulation. In contrast, RC represents a network-level computational framework that leverages a collection of dynamic elements (the reservoir) to project input signals into a high-dimensional temporal state space. This enables efficient encoding of complex spatiotemporal correlations, making RC particularly suitable for tasks involving nonlinear time-series processing, such as speech recognition and sequential decision making. Therefore, while both approaches can be extended and integrated into larger neuromorphic systems, RC provides additional advantages in capturing temporal evolution and contextual dynamics across multiple time steps.

6.1.3. Artificial nociceptor. In biological systems, nociceptors are specialized sensory receptors that detect pain signals. Located in the peripheral nervous system, these receptors are responsible for sensing harmful stimuli from potential sources of injury, such as mechanical damage, extreme temperatures, or chemical irritants, and conveying these signals to the brain, thereby triggering a pain response.[172,379,380] They exhibit characteristic behaviors such as threshold-triggered switching, short-term memory (relaxation), non-adaptivity, and sensitization (allodynia/hyperalgesia) to injure stimuli. These complex physiological functions can be emulated in hardware using perovskite memristors, which feature threshold-dependent conductance transitions, self-recovering conductive states, and stimulus accumulation sensitivity. Fig. 30 shows the working principle of biological nociceptors and artificial nociceptors. When a noxious stimulus arrives, the nociceptor generates an action potential and transmits it to the central nervous system for signal processing. Similarly, a voltage pulse applied to a diffuse high-voltage memristor produces a significant current output, which is higher than the turn-on voltage of the resistor. From the device level, the key parameters governing artificial nociceptors are threshold voltage, relaxation time, and sensitivity to cumulative stimuli, which can be precisely engineered in perovskite memristors through their intrinsic ionic dynamics, offering a distinct advantage over abrupt filamentary mechanisms in oxide systems. Table 8 shows the method of using volatile halide perovskite memristors to mimic nociceptor function.

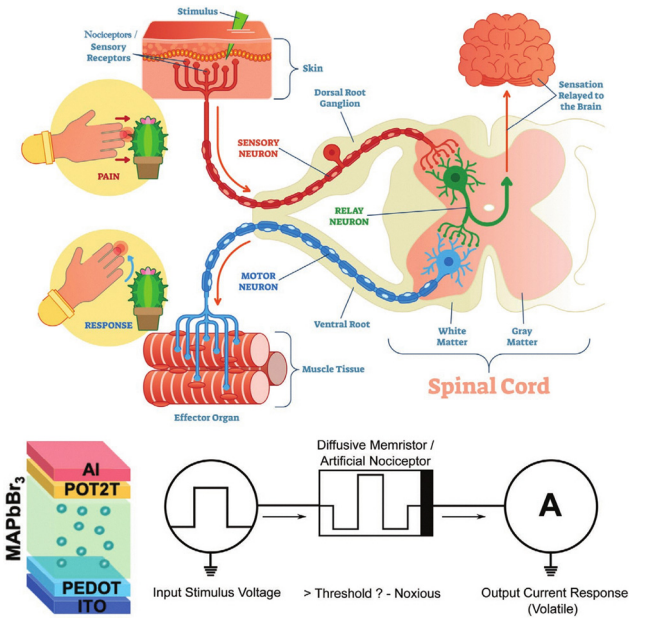

Fig. 30 The working principle of biological nociceptors and schematic diagram of using memristors to construct artificial nociceptors. Reproduced from ref. 172 with permission from John Wiley & Sons, Copyright 2021.

In a study published in 2021, John *et al.* developed a volatile perovskite memristor based on an ITO/PEDOT:PSS/$MAPbBr_3$/PO-T2T/Al structure.[172] The device operates *via* interface-induced ion diffusion and reversible charge modulation, exhibiting typical diffusive switching characteristics. Under voltage stimulation, the device displays a distinct threshold-triggered response, short-term conductance enhancement, and spontaneous recovery, effectively mimicking the three-stage dynamics of biological nociceptors: perception–amplification–self-healing. Notably, it replicates key nociceptive behaviors, including hyperalgesia and allodynia. They refer to an enhanced sensitivity to pain or noxious stimuli. In the context of the artificial nociceptive system, the phenomenon is characterized by a reduction in the threshold voltage and an increased current response, and these two types of sensitizations will take effect when injure stimulation is introduced. Fig. 31a and b shows the response of the nociceptor after injury of different amplitudes and durations, and the hypersensitive response can be recovered over time, as shown in Fig. 31c, which corresponding to the self-relaxation behavior of ions in perovskite film. When integrated into a neuromorphic robotic system and combined with tactile fabric and non-volatile synaptic devices, a closed-loop architecture for "artificial pain perception–decision–movement" was achieved, enabling associative learning and escape responses.

In contrast to ion diffusion-based switching, Im *et al.* constructed a volatile memristor using Ag-doped $MAPbI_3$, where the volatile behavior stems from the formation and rupture of Ag conductive filaments, as shown in Fig. 31d.[381] The device exhibited a low threshold voltage ($\sim$0.2 V), therefore, a low voltage of 1 V can be used as an injury stimulus. As shown in Fig. 31e and f, the device also demonstrates hyperalgesia and allodynia. The nociceptor was integrated with a pressure sensor to form a 5 $\times$ 5 "electronic skin" array. This system could detect the impact of a steel ball, enabling three-dimensional pain localization and recognition. Additionally, Patil *et al.* reported a Pd/$MAPbI_3$-based diffusive memristor on a flexible ITO/PET substrate, demonstrating essential nociceptive features such as

Table 8 Emulation of nociceptor functions using volatile halide perovskite memristors

Nociceptor function	Device requirements	Test method
Threshold response	The voltage exceeds a certain threshold to have a significant conductivity change	Pulse test with different amplitude, width to find the critical point
Relaxation	Volatile conductance with time-dependent decay	Observe the time for the current response caused by a pulse return to the initial state
No-adaption	Enhanced continuous pulse response	Pulse train test to observe the change of current response
Sensitization (allodynia/hyperalgesia)	Increased response after strong stimulation	First use a large pulse to test the device to introduce injury and then use conventional testing to observe the difference before and after the injury is introduced.

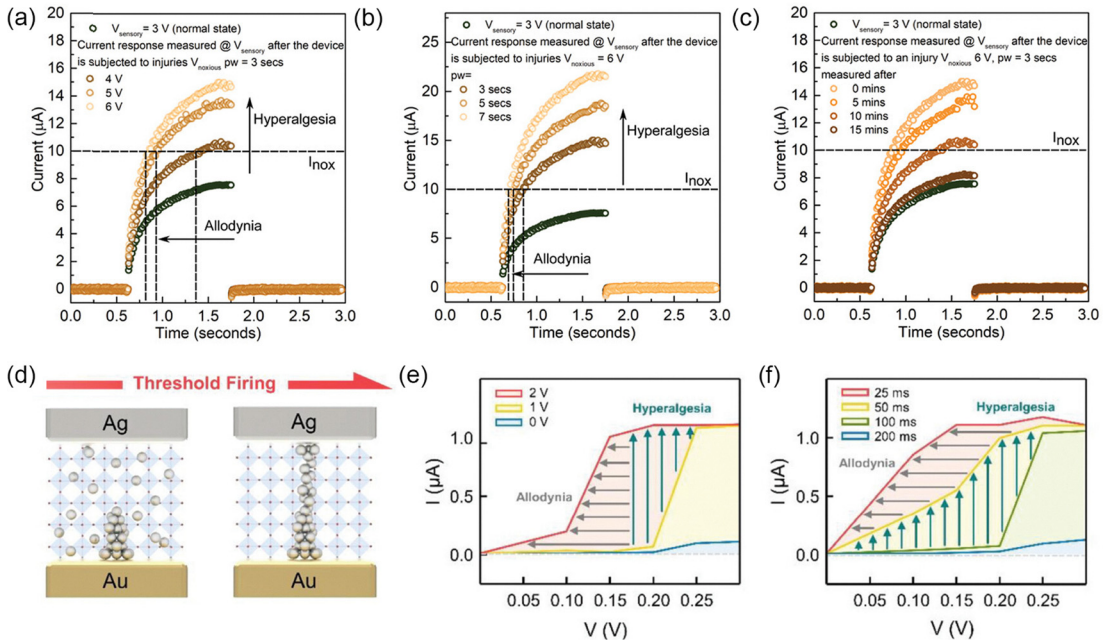

Fig. 31 (a) The sensitizations behaviors of allodynia and (b) hyperalgesia. (c) The healing process with time. (d) Schematic representation of threshold firing in the diffusive memristors. Reproduced from ref. 172 with permission from John Wiley & Sons, Copyright 2021. (e) The sensitization in the artificial nociceptors characterized by hyperalgesia and (f) allodynia, respectively. Reproduced from ref. 381 with permission from John Wiley & Sons, Copyright 2023.

threshold switching, non-adaptivity, relaxation, and sensitization responses, including allodynia and hyperalgesia.[367] The device was further developed into a thermal sensing (thermoreceptor) system, showcasing its multimodal pain perception capability. Collectively, these studies demonstrate the broad application potential of volatile perovskite memristors in neuromorphic perception, smart e-skin, and human–machine interactive systems. Their unique integration of diffusive switching, flexibility, and sensory adaptability provides a hardware foundation for future biologically inspired neural platforms with situational awareness and adaptive response functionalities.

6.2. Applications of non-volatile memristors

Non-volatile memristors retain their conductance states for extended durations, typically hours to weeks, making them ideal for applications requiring stable memory. Their retention properties are evaluated through standardized testing elucidated in Section 3.1.3. For a memristor to qualify as non-volatile, it must exhibit negligible conductance drift over time while maintaining clear separation between distinct states; overlapping conductance levels during testing indicate insufficient reliability. The number of stable, non-overlapping states directly determines functional versatility. Devices with two well-defined conductance states can serve as binary logic gates and when extended to multiple programmable states, these devices enable the implementation of weights in neural networks for in-memory computing. Similarly, in in-sensor computing, multiple photoresponsivity states are essential for tasks, such as feature extraction using CNN. Those applications will be reviewed in depth in the next section.

6.2.1. Efficient boolean logic and arithmetic operations. Perovskite-based devices have demonstrated significant potential in performing Boolean logic and arithmetic operations, which are essential for digital computation and underpins the operation of modern digital computers. These devices are ideal for in-memory computing, which eliminates the Von Neumann bottleneck by performing computations directly within memory, reducing data transfer and power consumption. Boolean logic relies on binary values (0s and 1s) to perform operations like AND, OR, and NOT, which are foundational to digital computation. From the viewpoint of digital logic, the most critical device parameters are the on/off ratio, state retention and endurance, the controllability of the threshold, and logic configuration. For implementation in memristors, this requires two stable, non-overlapping conductance states to represent these binary values. The integration of electrical and optical inputs is a critical feature enabling reconfigurable logic in memristive devices. Light of varying wavelengths (*e.g.*, visible, UV) has been demonstrated as a tool for writing and erasing states, while electrical signals modulate conductance.[370,382–384] Device states are then read electrically to determine computational outcomes. For instance, AND/OR gates are achieved by tuning light intensity, and hybrid electrical-optical systems enable programmable resistance. Researchers implemented AND, OR logic operations using light intensity as a bias. When two electrical pulses were applied, illumination with a low-intensity light (1.6 mW cm^{-2}) enabled AND operation (Fig. 32a), whereas increasing the light intensity to 6.5 mW cm^{-2} resulted in an OR operation (Fig. 32b).[370] In another work,[383] visible light was utilized to induce filament

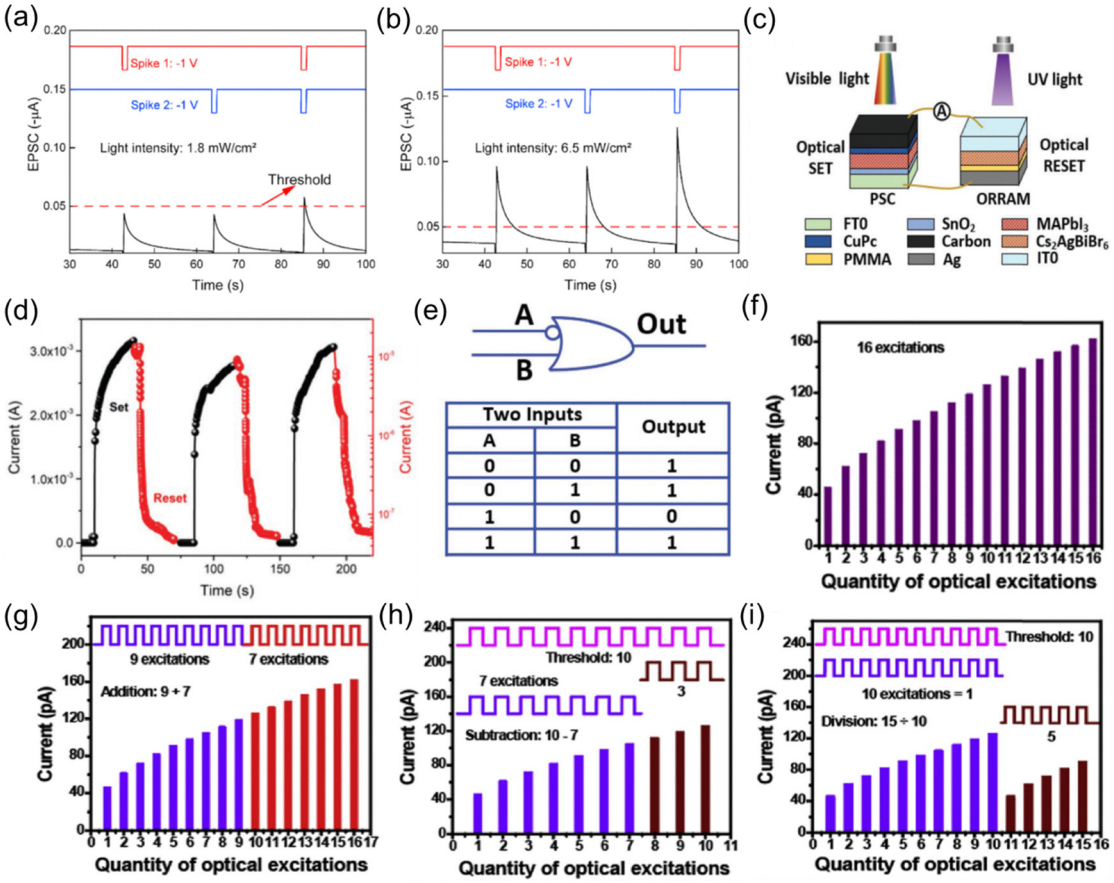

Fig. 32 (a) AND logic operation and (b) OR logic operation implemented by tuning the light irradiation. A threshold of −0.05 μA was set and when the EPSC was higher than the threshold, the output was 1 else 0. (a) and (b) Reprinted from ref. 370, Copyright 2021, with permission from Elsevier. (c) Schematic diagram of device operation where visible light is used for (d) setting and UV light is utilized for resetting as well as (e) the truth table of the device when operated as logic computation device. (c) and (d) Reprinted from ref. 383, Copyright 2022, with permission from John Wiley and Sons. (f) Linear EPSC with 16 optical excitation and corresponding current mapping to *i*th optical pulse. (g)–(i) Arithmetic operations of addition, subtraction, and division were demonstrated. A threshold of 10 was set in the substation and division case. (f)–(i) Reprinted from ref. 384, Copyright 2020, with permission from Elsevier.

formation (LRS) and UV light to break the filament (HRS), enabling a two-state system suitable for performing logical operations as shown in Fig. 32c–e. These results were achieved by selecting appropriate threshold values, demonstrating the potential of optically controlled in-memory computing in perovskite devices. Compared with oxide- or phase-change-based memristors, perovskite memristors uniquely exploit their strong visible light-matter interaction: optical stimuli at visible wavelengths can write/erase the state, while electrical input pulses can probe the logic function. This hybrid optical–electrical control allows *in situ* reconfiguration of the truth table (*e.g.*, AND/OR switching by changing light intensity) within the same cell.

Arithmetic operations (addition, subtraction, multiplication, division) extend this capability using multistate memristors, where EPSC linearly correlates with input signals. For example, Huang *et al.* have leveraged the linear relationship between EPSC potentiation and input signals (Fig. 32f) to implement basic arithmetic operations.[384] Addition and multiplication are performed by directly correlating EPSC levels with pulse counts (Fig. 32g), while subtraction and division rely on a thresholding method (Fig. 32h and i). For subtraction, the threshold is set to the EPSC of the larger operand. For example, to compute 10−7 (Fig. 32h), 7 pulses are initially applied, and the remaining pulses required to reach the threshold (10) are counted, yielding a result of 3. For division (Fig. 32i), the EPSC of the divisor served as the threshold, and counting was reset each time the threshold was reached, with the remainder being the number of pulses just before the threshold value was met.[382,384] For example, to obtain result of 15/10, EPSC of 10 pulses serves as the threshold. Pulses equivalent to dividend are applied (15 in this case), and if EPSC reaches the threshold, the device is reset to the initial state (1 time here when 10 pulses are applied). Post device reset, only 5 pulses are left which are applied. Since the threshold EPSC is not met, these 5 pulses count as remainder while the number of resets count as quotient (1 in this case).

6.2.2. Artificial synapses. In biology, the primary function of a synapse is to facilitate communication between neurons and other cells, enabling the transmission and storage of information within the nervous system. Artificial synapses in

memristors emulate biological synaptic plasticity, where repeated stimulation strengthens connections (LTP), and disuse weakens them (LTD). This mimics the transition from short-term memory to long-term memory in biological systems.[385,386] As explained in Section 3.1.6, beyond emulating the short-term to long-term memory transition, memristors must exhibit additional critical characteristics to function as artificial synapses. Linear and stable conductance modulation is desired, characterized by smooth long-term potentiation/depression (LTP/LTD) curves (Fig. 33a) with minimal variability to ensure reliable synaptic weight updates during learning. Pulse-driven adaptability is also required, enabling precise tuning of potentiation (strengthening) and depression (weakening) through adjustments to pulse amplitude, width, or number. Furthermore, spike-timing-dependent plasticity must be demonstrated, where conductance changes depend on the relative timing of pre- and post-synaptic spikes (Fig. 33b–f), thereby enabling biologically inspired learning rules like Hebbian or anti-Hebbian mechanisms. From a device standpoint, the essential parameters governing long-term synaptic plasticity include the linearity and symmetry of conductance modulation, retention and endurance stability, and energy efficiency during weight update. These properties are typically evaluated using standardized testing protocols, including pulse amplitude modulation (varying voltage while keeping pulse count constant) and pulse number modulation (varying pulse count while maintaining amplitude), as summarized in Table 9. Unlike memristors with abrupt filamentary switching and large cycle-to-cycle variations, halide

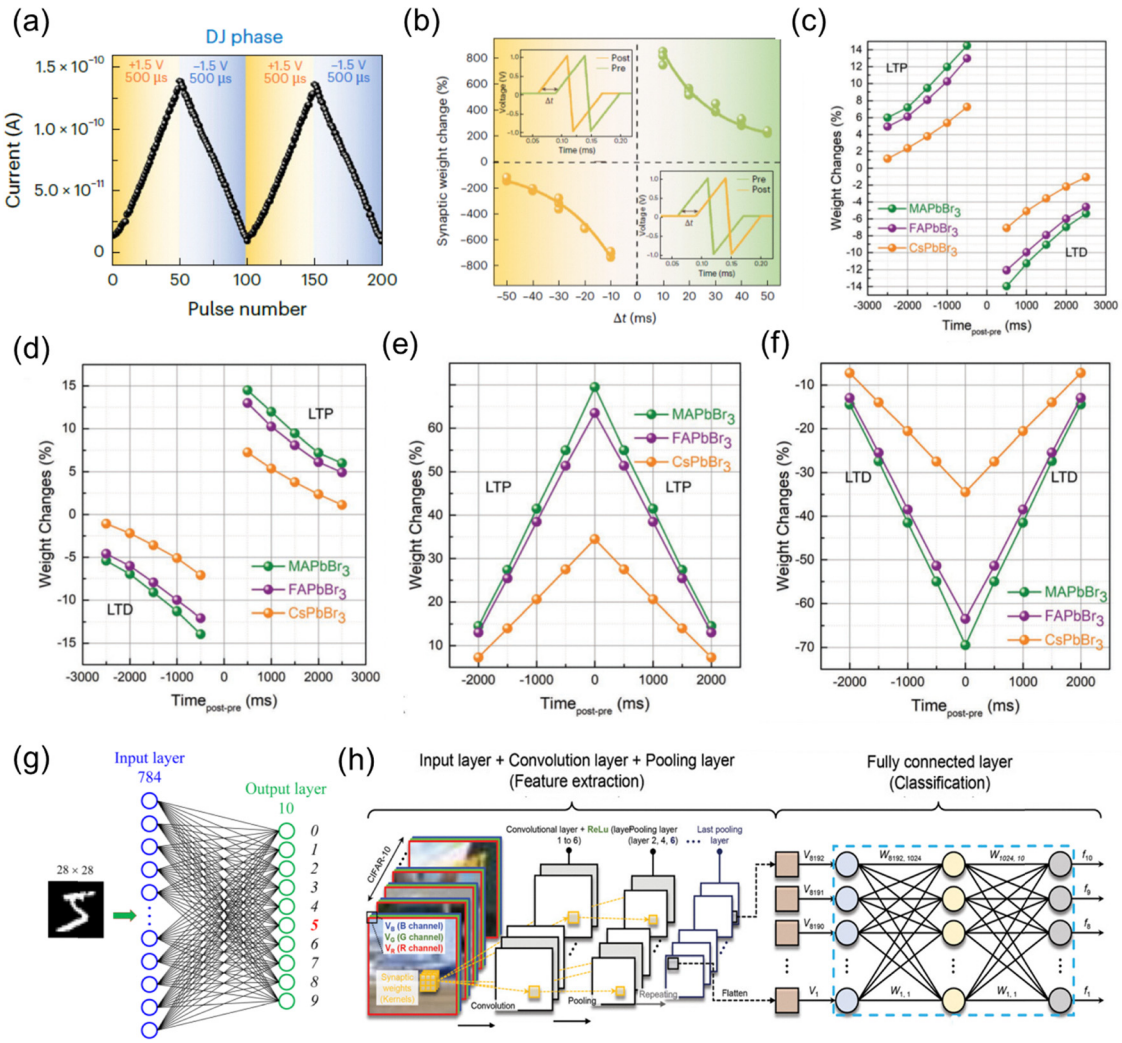

Fig. 33 (a) LTP and LTD of DJ phase ($BDA_2MA_{n-1}Pb_nI_{3n+1}$, n =3) perovskite. DJ phase exhibits linear potentiation and depression curve which is highly desired since it enables access to various conductance states while most perovskite displays a non-linear curve like the RP phase. (b) STDP curve characteristics from the DJ phase and inset display the input provided to the synaptic device wherein pre and post are the presynaptic and postsynaptic voltages, respectively. (a) and (b) Reproduced from ref. 110 with permission from Springer Nature, Copyright 2025. (c)–(f) Various Hebbian learning rules are depicted wherein: (c) antisymmetric anti-Hebbian (d) antisymmetric Hebbian (e) symmetric anti-Hebbian (f) symmetric Hebbian from devices made from (Cs/MA/FA)$PbBr_3$. (c)–(f) Reproduced from ref. 60 with permission from John Wiley and Sons, Copyright 2018. (g) Illustration of architecture adopted in fully connected neural network (FCNN). Reproduced from ref. 387 with permission from the Royal Society of Chemistry (h) Illustration of CIFAR-10 dataset together with a CNN model with memristor device. Reproduced from ref. 388 with permission from John Wiley and Sons, Copyright 2022.

Table 9 Emulation of artificial synapses using non-volatile memristor

Characterization name	Device requirements	Test methods	Memristor type
Pulse amplitude dependency	Response of ionic species to the applied electric field	Apply voltage pulses with increasing amplitude after every sequence	Transition
Pulse number dependency	Time-sensitive ion dynamics	Vary the number of pulses applied to the device	Transition
Multi-level state characterization	Ability to hold intermediate resistance states	Pulse or bias input signal to generate and measure multiple stable resistance levels	Non-volatile
Long term plasticity	Gradual conductance modulation	Long-term potentiation/depression (LTP/LTD) pulse protocols	Non-volatile
Spike-timing-dependent plasticity	Temporal and gradual ionic response to applied signal	Apply asymmetric paired spikes and measure weight change	Non-volatile

perovskite-based synapses utilize gradual, analog memristors with minimal variability, a superior performance achieved by the mixed ionic–electronic transport and defect-tolerant lattice inherent to the halide perovskite material. The ion migration dynamics can be finely controlled through pulse amplitude, duration, or optical excitation, enabling near-linear weight evolution and high precision in synaptic learning.

A crossbar array, when configured with memristors that function as artificial synapses, forms a grid where WL act as presynaptic neurons input transmitting electrical signals (input voltage, V_i^{pre}), and BL collect post-synaptic neurons output currents from synaptic connections (output current, I_j^{post}). These currents are summed *via* Kirchhoff's law to emulate neuronal integration. At each intersection, synaptic devices store weights as conductance values (*e.g.*, G_{ij}, representing the synaptic weight between input i and neuron j). This architecture enables vector–matrix multiplication $\left(I_j^{post} = \sum_i G_{ij} \cdot V_i^{pre}\right)$ – a foundational operation in neural networks – performed in parallel for energy-efficient computation. This architecture enables efficient, parallel processing, making it highly suitable for various classification tasks such as image recognition, speech recognition. A wide range of benchmarks is available for evaluating the performance of memristor-based hardware neural networks, as shown in Table 10. Numerous studies leverage this dataset to train and evaluate the efficacy of classification capabilities of memristor crossbar arrays, facilitating direct comparison with state-of-the-art technologies. By exploiting the key properties of memristors, such as analog conductance tuning and non-volatility, these devices hold great promise for energy-efficient and scalable classification applications for various neural networks, such as FCNN, CNN, and SNN, which are discussed in detail below.

A FCNN is one of the simplest and most fundamental types of neural networks, where every neuron in one layer is connected to all neurons in the subsequent layer, as shown in Fig. 33g. This architecture is commonly employed in hardware-based neural networks reported in the literature due to its structural simplicity and ease of implementation.[319] In one of the works,[389] Lao *et al.* implemented an FCNN using a lead-free perovskite-based device composed of $Cs_2AgBiBr_6$ in an ITO/perovskite/PMMA/Ag configuration. The device demonstrated stable LTP and LTD switching behavior for over 20 days, with an energy consumption of approximately 188.6 pJ. To evaluate the neural network's reliability, off-chip simulation was performed using a three-layer network trained on the MNIST handwritten digit dataset (Table 10). The system achieved accuracies of 83.4% and 91.3% after 5000 and 60 000 training iterations, respectively. In another work,[390] $CsCu_2I_3$ was used as the switching layer between ITO and gold electrodes. These devices showed remarkably stable LTP and LTD characteristics over 160 days. To assess their applicability in neuromorphic computing, off-chip simulations were conducted using both the MNIST handwritten digit and Fashion-MNIST datasets (Table 10). The system achieved accuracies of 95.2% and 84.5%, respectively, demonstrating the strong potential of lead-free perovskite materials in energy-efficient and reliable hardware neural networks.

A CNN is a type of artificial neural network widely used for image recognition and other vision-related tasks. In this architecture, there are multiple convolutional layers, each of which processes the output from the previous layer using a set of small learnable filters or kernels (as illustrated in Fig. 33h). These convolutional layers are effective at extracting spatial features and performing dimensionality reduction, thereby significantly lowering the number of parameters and computational complexity compared to fully connected networks. By compressing and abstracting information through convolution and pooling layers, CNNs reduce the need for large, densely connected neural networks, which helps minimize operational power and memory requirements.[391] After the convolutional and pooling layers, FCNN is typically used to perform the final classification task, mapping extracted features to output labels

Table 10 Benchmark datasets for neural network applications with halide perovskite systems

Dataset name	Description	NN applied using perovskite memristor
MNIST	Handwritten digits (0–9); 28 × 28 grayscale images	ANN,[108,252,328,370,387,389,390,395,396] CNN,[110,264] SNN[60,122,315]
Fashion-MNIST	Grayscale images of clothing items (10 classes); same format as MNIST	ANN,[390] CNN[110]
CIFAR-10	32 × 32 RGB images in 10 classes (*e.g.*, airplane, car, bird)	CNN[110]
CIFAR-100	Like CIFAR-10 but with 100 fine-grained classes	CNN[110]
ImageNet	Large-scale visual database for image classification (1000 classes)	CNN[110]

such as image categories. The feasibility of implementing a CNN in hardware using a perovskite memristor was demonstrated by Luo *et al.*[264] In this work, Au/$CsPbBr_3$/ITO device was utilized, which exhibited LTP and LTD characteristics essential for synaptic behavior. The CNN was simulated for handwritten digit recognition using the MNIST dataset (Table 10). An accuracy of 79% was achieved when +2 V and −2 V were applied as the write (potentiation) and erase (depression) pulses, respectively. A significantly higher accuracy of 96.7% was obtained when using +0.5 V and −0.8 V as the write and erase pulses. Kim *et al.* implemented a CNN using a 2D DJ phase vertically oriented perovskite (n = 3) memristor,[110] which demonstrated excellent linear LTP and LTD behavior. A multilayer perceptron (MLP) was employed in conjunction with CNN-based architecture to perform image recognition tasks. Experimentally fitted device models were used to simulate the performance of the hardware system. The simulation results showed high classification accuracies across multiple datasets: 98.75% for MNIST, 92.29% for CIFAR-10, 73.83% for CIFAR-100, and 77.24% for the ImageNet dataset (Table 10), indicating the potential of DJ phase perovskite memristors for scalable neuromorphic computing.

A SNN is a type of artificial neural network that more closely mimics the biological neural processing observed in the human brain. Unlike traditional neural networks that use continuous activation functions, SNNs rely on discrete spikes or electrical pulses to transmit information. Neurons in an SNN fire only when their input signal potential exceeds a certain threshold, introducing temporal dynamics and event-driven computation into the model. This enables significantly lower power consumption and makes SNNs well-suited for energy-efficient neuromorphic hardware implementations.[392] Information in SNNs is encoded in the timing and frequency of spikes, which allows them to capture both spatial and temporal features. Learning mechanisms such as STDP enable synaptic updates based on the precise timing of spikes, offering a biologically plausible learning paradigm. Implementation of memristor in a spiking neural network was demonstrated by John *et al.*,[60] wherein memristors were made using a $MAPbBr_3$ perovskite film as a switching layer. The device leveraged ion drift and diffusion to produce both volatile and non-volatile responses, which mimic short-term and long-term synaptic plasticity, respectively. STDP characteristics were experimentally demonstrated, forming the basis for temporal learning in an SNN architecture. Through spike-based input for pattern recognition, the SNN achieved an accuracy of 80.8% using MNSIT dataset (Table 10). Here, a two-layer NN was trained in simulation wherein the first layer to which spiking input was applied had random weights, while the second layer weight update was implemented using a winner-take-all mechanism.[393] In this mechanism, only the neuron with the highest activation is active, while other neurons are inhibited. In another work,[315] a novel Ag–Bi alloy electrode was adopted, wherein ITO/$MAPbI_3$/Bi (40 nm)/Ag (130 nm) stack was considered. This structural configuration helps in suppressing the electrochemical reaction by silver, resulting in consistent, stable switching. The memristor exhibited endurance of 800 cycles and retention greater than 10^4 seconds while exhibiting a gradual conductance modulation while using spikes for writing the memristor. Using this device, SNN was simulated by implementing classification tasks using the MNIST handwritten digits dataset (Table 10). The SNN achieved a recognition accuracy of 86.68% by adopting two-layer SNN architecture developed by Diehl *et al.*,[394] for unsupervised learning of digit recognition using STDP. SNN is an excellent form of unsupervised learning that can be implemented using memristor crossbar arrays.

6.2.3. Memristor based associative learning for adaptive neuromorphic circuits. Associative learning in memristors is a fundamental mechanism that enables neuromorphic systems to mimic biological learning by linking correlated inputs. Rooted in Hebbian theory and classical conditioning,[397] this learning paradigm allows memristors to adjust their conductance based on the timing and frequency of input signals. This principle has been used to replicate Pavlov's classical conditioning,[398] where a conditional stimulus (*e.g.*, a bell) becomes associated with a unconditioned stimulus (*e.g.*, food), eventually triggering a learned response (*e.g.*, salivation) as depicted in Fig. 34a.

Wang *et al.* demonstrated association learning through the classical conditioning experiment in their device by utilizing 2 amplitudes of voltage pulses as unconditional and conditional stimuli.[400] In the work, a triple cation halide perovskite memristor was made, where low voltage electroforming (at 0.5 V) was observed. High voltage pulse train (1.2 V) mimicked unconditional stimulus (US) while a low voltage (0.6 V) mimicked conditional stimulus (CS). Initially, the device does not respond to CS. The device was trained by applying both CS and US to build an association, and after learning, it responded to CS. Lead-free perovskite was utilized by Luo *et al.*,[401] by adopting Al/$Cs_3Sb_2X_9$/ITO structure where X = Cl, Br, I, and demonstrated associative learning capability in the $Cs_3Sb_2Cl_9$ device since it exhibited superior performance, including low switching voltage (<0.6 V), high on/off ratio, and long endurance (750 cycles). To implement associative learning, voltage pulses were utilized as conditional stimuli and optical pulses as unconditional stimuli, and the association was built between the stimuli. The device initially responded only to light stimuli, but after association of stimuli, the device responded to voltage pulses, which is a conditional stimulus. Learning and forgetting features were demonstrated utilizing the 2T lead-free perovskite. Periyal *et al.* showed the association learning capability in their device by utilizing electro-optical pulses in a 3T memristor.[237] Halide perovskite quantum dots ($CsPbBr_3$) photosensitized amorphous indium gallium zinc oxide (IGZO) transistors were implemented, which enabled electro-optical programming, light-dependent memory. Optical pulses were utilized as unconditioned stimuli, while electrical pulses were used as the trigger for conditioned stimuli. Initially, the device responds only to optical stimuli, but after repeated concurrent training with both stimuli, it develops an association, responding to electrical pulses alone. The learning persisted for 30 minutes and fades beyond mimicking the forgetting behavior of the human brain. However, the association was reestablished by retraining the device (Fig. 34a).

Beyond associative learning, reinforcement learning (RL) has also gained traction in memristor-based neuromorphic

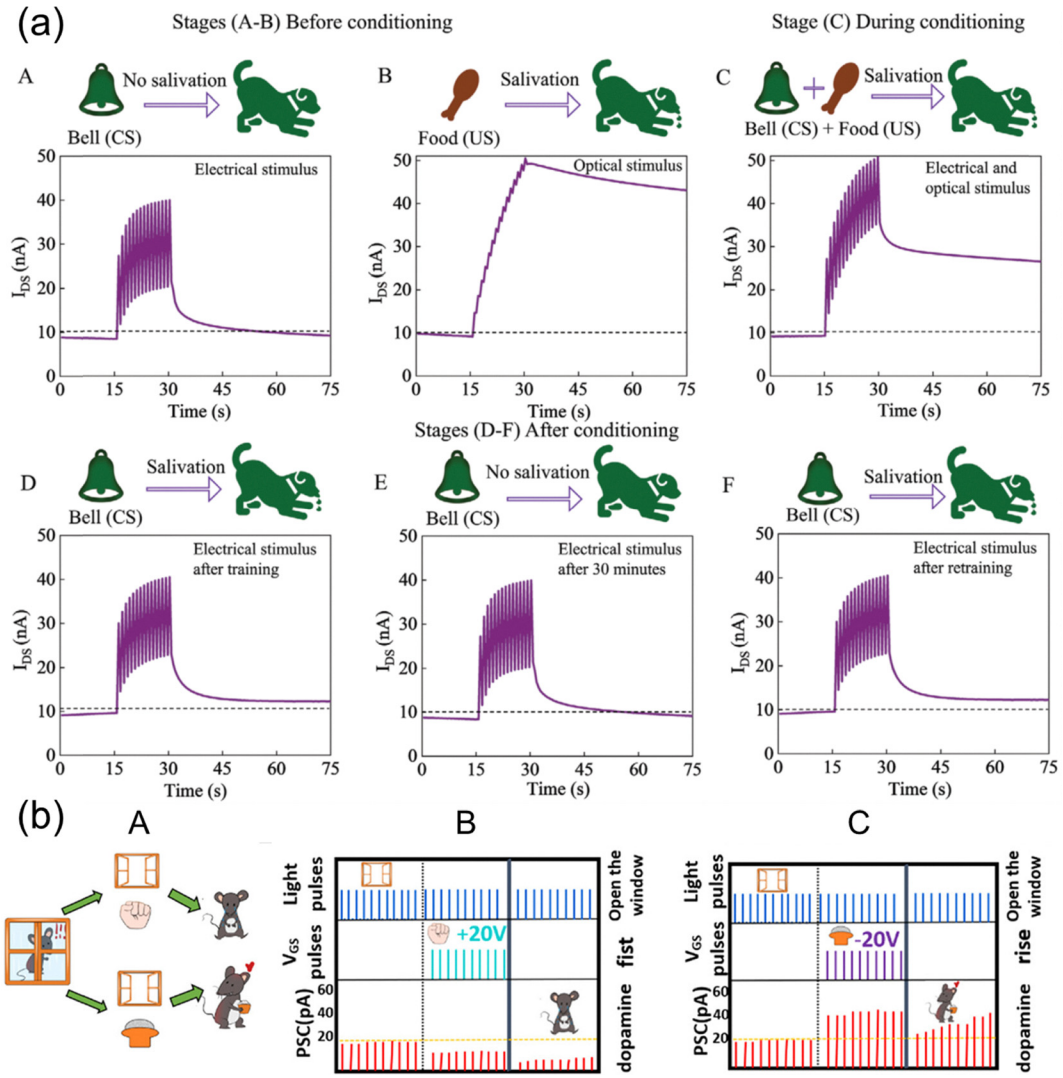

Fig. 34 (a) The classical conditioning experiment wherein the dog (device) does not salivate (low output signal) when subjected to the bell (conditional stimulus) (A) but salivates (high output signal) when subjected to food (unconditional stimulus) (B) before conditioning. During conditioning, wherein both the bell (CS) and the food (US) are subjected to the dog (device), it salivates (high output signal) (C). After conditioning, the dog (device) salivates (high output signal) when subjected bell (CS) (D). Learning is lost after some time (30 minutes here) and hence stops responding to CS (E), emulating the forgetting behavior. However, after retraining, the dog (device) can respond to the bell (CS), showing the relearning capability. Reproduced from ref. 237 with permission from John Wiley and Sons, Copyright 2020. (b) Schematic of the secretion mechanism of dopamine under reward or punishment stimulation in biology (A). Releasing mechanism of dopamine under punishment simulated by light and positive voltage spikes (B). The output PSC is low, showing lower dopamine. The releasing mechanism of dopamine under reward is simulated by light and negative voltage spikes (C). The output PSC is high, showing enhanced dopamine. Reprinted with permission from ref. 399. Copyright 2021 American Chemical Society.

systems. In RL, learning occurs through feedback from the environment in the form of rewards or penalties, guiding the system toward desired outcomes.[402] In hardware, this is implemented by modulating the memristor's conductance based on the success or failure of an action, analogous to synaptic weight updates. For instance, if a particular output leads to a reward signal, the memristor's synaptic weight is potentiated; if not, it may be depressed as punishment. Apart from demonstrating the classical conditioning experiment for associative learning, Duan *et al.* has shown reinforcement learning in the devices.[399] 3T device was adopted with a complex structure of Si(Gate)/SiO_2/IGZO/$CsPbBr_3$ NPs/IGZO/Ti(drain/source electrode). For demonstrating classical conditioning, optical pulses were used as US, and negative voltage pulses were used as CS. Learning and forgetting features were demonstrated in this experiment. For reinforcement learning, inspiration was drawn from how the brain adjusts behavior by associating stimuli with positive or negative outcomes, in particular, how dopamine levels rise or fall in response to reward or punishment. In the experiment (Fig. 34b), light pulses represented a CS (like opening a cage door), and voltage spikes were used to simulate either reward or punishment. When the light was repeatedly paired with positive voltage pulses (+10 V), the device's response (postsynaptic current) decreased, mimicking the effect of punishment, where

the brain learns to avoid that action. Conversely, pairing the light with negative voltage pulses (−10 V) caused the response to increase, simulating a reward, where the system learns to favor that action. This behavior reflects reinforcement learning and these dynamic supports goal-directed learning, enabling autonomous adaptation and decision-making in tasks such as navigation, pattern recognition, or control systems.

7. Conclusion and future outlook

This review provides a comprehensive overview of perovskite memristors, covering materials design, device fabrication, switching mechanisms, and their integration into neuromorphic systems. The low DFE and E_A of perovskite also ensure fast ionic migration, which is critical for reducing the switching time and energy consumption of memristors. However, a balance in ionic activity is necessary to optimize switching time and energy consumption without compromising retention time and endurance. The compositional and structural richness of perovskites—including 3D frameworks and low-dimensional (2D, 1D, 0D, and vacancy-ordered) structures—offers a wide range of electronic and ionic properties. This diversity enables tailored engineering of memristive behavior. While lead halide perovskites remain the most studied, significant attention is shifting toward lead-free systems such as Sn-, bismuth-, and copper-based compounds and double perovskites like $Cs_2AgBiBr_6$, with a particular focus on their ionic migration characteristics.

Ionic transport in perovskites arise either from intrinsic ionic migration or external ions originating from electrodes. The migration rate can be influenced by the environmental conditions including light, heat, and moisture. Various crystallographic engineering approaches—including A-site alloying with $FA^+/MA^+/Cs^+$, halide substitution ($Cl^-/Br^-/I^-$), and bulky A-site cation alloying to induce dimensionality reduction—have been employed to modulate ionic and electronic transport. To probe ion migration, *in situ* and *ex situ* bias dependent techniques such as X-ray diffraction, ToF-SIMS, photoluminescence and absorption measurements are widely used. Additionally, DFT simulations provide insight into activation energies and defect formation pathways, although reported values vary significantly due to model assumptions and environmental conditions.

Beyond intrinsic material properties which can be tailored through materials design, the performance of perovskite memristors is also heavily influenced by fabrication techniques. Solution-based methods like spin coating and blade coating, as well as vapor-phase approaches such as thermal evaporation, directly affect film uniformity, grain boundaries, and defect densities—factors that impact switching behavior. In spin coating, parameters like solvent selection, antisolvent timing, and annealing temperature determine nucleation dynamics and film morphology. Substrate choice (rigid *vs.* flexible), interface passivation, buffer layers, and electrode materials also play crucial roles in modulating device performance and reliability. Given the complex interplay between materials and process parameters, future technical breakthroughs must encompass high-throughput combinatorial platforms necessary for rapid optimization. These ideally should integrate robotic synthesis, rapid characterization techniques (*e.g.*, impedance spectroscopy to evaluate electronic and ionic conductivity, hyperspectral absorption or PL imaging to assess film uniformity), and machine learning-based optimization frameworks.

Switching in perovskite memristors generally falls into two mechanisms: conductive filament formation and interfacial modulation. However, most reported devices rely on electrochemically active metal electrodes such as Ag, where switching occurs through the formation and rupture of Ag^+ metallic filaments. While this mechanism often yields reliable switching at the single-device level, it obscures the intrinsic role of ionic migration within the perovskite lattice, as it relies heavily on the migration rate of external Ag^+ ions. Moreover, filament-based switching introduces a high degree of stochasticity, leading to significant device-to-device and cycle-to-cycle variation, which poses a serious barrier to achieving reproducibility and long-term reliability in large-scale arrays. Interfacial mechanisms, including ion migration or carrier trapping detrapping that induced interfacial barrier modulation, are gaining attention for their potential to deliver more uniform and tunable switching without the need for filamentary conduction. Since perovskites are soft, ionically mobile materials, accurate understanding of these mechanisms requires *in operando* characterization (such as KPFM, CAFM, TEM) to minimize measurement artefacts. Simulations at multiple scales—from atomic-level transport and filament dynamics to array-level modeling of sneak paths and crosstalk—are essential to supplement experimental studies and inform device design.

Scaling perovskite memristors into functional arrays introduces multifaceted challenges. Present limitations include non-uniform perovskite film formation (which increases device-to-device variability) and the technical complexities of patterning electrodes post-perovskite deposition. The inherent sensitivity of soft perovskite films to solvents, heat, and vacuum conditions complicates both direct lithographic processing-often causing non-uniformity or material damage-and the subsequent lithographic patterning of top electrodes. Customized soft inorganic shadow masks present a potential solution to eliminate post-deposition lithography steps. Furthermore, conventional spin coating produces full-coverage films, complicating device isolation and exacerbating crosstalk risks in crossbar architectures. Patterned perovskite layers are therefore critical for minimizing crosstalk in high-density arrays. To pattern perovskite active layer, inkjet and spray coating allow for digital, maskless deposition but suffer from non-uniform film thickness and poor edge definition. Blade coating and photolithography offer higher uniformity and resolution but are limited by compatibility with soft, solvent-sensitive films. Nanoimprint lithography shows promise for high-resolution patterning but remains confined to rigid substrates. Thus, developing orthogonal patterning strategies and scalable deposition methods remains a critical bottleneck for perovskite memristor integration into practical circuits. Additionally, sneak path issues could also reduce the reliability of array reading by introducing undesired

conduction paths which cause erroneous current reading. Although integration of selectors (*i.e.* 1S1R and 1D1R) help suppress undesired conduction paths, they add complexity as building selector devices on top of perovskite devices is challenging due to the stringent solvents, heat, and vacuum restriction. In the future, novel fabrication techniques to enable fabrication of selectors devices on top of perovskite memristors or development of self-rectifying memristor are needed to mitigate sneakpath current issues.

A diverse range of neuromorphic applications has been demonstrated, leveraging the unique properties of both volatile and non-volatile devices. Volatile memristors have been implemented in functions such as reservoir layers in reservoir computing, artificial nociceptors, short-term plasticity for signal enhancement, and spiking artificial neurons. Non-volatile memristors, by contrast, have enabled static applications including digital logic, artificial synapses for memory storage, and adaptive learning systems. Additionally, the frequency-dependent and dynamic transient behavior of volatile perovskite memristors has opened up new possibilities in event-based computation, frequency-selective pulse encoding, and low-power short-term caching systems. These applications rely on the device's sensitive and time-dependent responses to external stimuli, making them especially promising for real-time, adaptive signal processing.

Despite these advances, most neuromorphic tasks using perovskite memristors are still performed off-chip. While perovskite memristors show great promise for implementing neural networks directly on device arrays, practical challenges—such as retention instability, limited endurance, and significant device-to-device and cycle-to-cycle variability—have prevented full *in situ* integration. As a result, most studies extract conductance or switching data from perovskite dot arrays or small crossbar arrays and perform the neural network simulation externally. Even when visual outputs such as image display or handwritten digit recognition are demonstrated, core computational tasks like training and classification are typically executed using conventional processors outside the memristor array. True on-chip learning demonstrations remain rare, primarily due to the unresolved issues with variability and device degradation under repeated cycling.

Looking forward, the development of perovskite memristors can be advanced through targeted materials and device engineering strategies. Approaches such as high throughput materials compositional engineering, interfacial modification, dimensional control, and electrode design offer promising pathways to tune ionic migration and henceforth critical dynamic parameters—such as retention time, conductance decay rate, and response speed—based on specific application requirements. For instance, short-term synaptic tasks may require decay times ranging from milliseconds to seconds, while event-driven applications benefit from faster response dynamics on the order of microseconds. Therefore, achieving dynamic tunability across this broad temporal spectrum is essential for enhancing the functional flexibility of memristive systems. In addition, application-oriented demonstrations increasingly highlight the importance of multi-element integration.

Beyond the development of tunable and personalized memristors, stability remains the decisive challenge. Perovskite memristors must sustain consistent operation against repeated electrical cycling, environmental stressors, and mechanical deformation. Hence, future technical breakthroughs must focus on stabilizing the perovskite against electrical cycling. This demands proper control of the ionic migration rate through materials engineering or optimized testing protocols, as uncontrolled ion migration causes premature device failure. Furthermore, given that measurements are currently performed largely in inert environments, adopting robust encapsulation techniques from other fields will be crucial to combat environmental stressors in the future. To circumvent the toxicity issue in Pb-based perovskite memristors, future research must also prioritize the development of lead-free alternatives.

For crossbar architectures and flexible large-area arrays, reports must address not only the achievability of high-density integration but also quantify low device-to-device variation. Therefore, developing novel fabrication techniques that yield reproducible and uniform perovskite arrays (both morphology and defect density) should be a primary future goal. Other future research should include the development of perovskite patterning techniques essential for integration with adjacent Si-based circuitry on a chip. Additionally, mitigating sneak-path current issues will require either stabilizing the perovskite for the fabrication of selector devices on top of memristors or the development of self-rectifying memristors.

Aside from in-memory computing, placing halide perovskite memristors within sensors could enable in-sensor processing or computing, thus minimizing data transfer to central node. This unique integration potential is driven by the ability to print perovskite onto large-area or flexible substrates[122] and could lead to revolutionary neuromorphic hardware designed to match the geometry of various sensors. Targeting in-sensor processing also simplifies integration, as the perovskite does not require placement within the on-chip Si-based circuitry. Its ability to strongly sense light and integrate it into the switching process also opens a new opportunity in neuromorphic vision, retinomorphic applications[280] or self-powered neuromorphic system.[377] Furthermore, the inherent device-to-device variability present currently in this technology can be leveraged for hardware security applications, such as physical unclonable functions (PUFs).[270] This variability offers a unique, intrinsic fingerprint for cryptographic security, transforming a manufacturing drawback into an asset.

In summary, perovskite memristors offer a compelling platform for next-generation memory and neuromorphic computing due to their rich ionic-electronic interplay, structural tunability, photosensitivity, and low processing cost. However, scalable and stable device integration is limited by challenges in materials stability, patterning, switching control, switching stability, and array uniformity. Future advancements will depend on deeper mechanistic understanding through *in situ* characterizations, robust fabrication protocols compatible with array-level integration, and co-optimization of material properties and device architecture for tailored applications.

Conflicts of interest

There are no conflicts to declare.

Data availability

No primary research results, software or code have been included and no new data were generated or analysed as part of this review.

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