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Detection of traps in thin-film transistors using evolutionary algorithms†

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In this work, we present a novel approach to analyzing the current-related characteristics of thin-film transistors (TFTs). We introduce a method to detect and quantify different types of trapped charges from current–voltage curves exhibiting hysteresis, as well as to track the evolution of charge density over time during experiments. To achieve this, we use a previously developed compact model for TFTs that accounts for contact effects and includes a time-dependent threshold voltage. This model is combined with an evolutionary parameter extraction procedure for trap detection. We demonstrate that our time-dependent threshold voltage model is highly adaptable to varying conditions. In fact, our method, which has been successfully applied to detect traps induced by hysteresis, is also capable of identifying unexpected traps from environmental factors. While our evolutionary procedure is slower than traditional methods, which typically rely on extracting constant values for the threshold voltage and sub-threshold swing, it offers a distinct advantage in that it can differentiate between the effects of various traps from a single current–voltage curve and allows continuous monitoring of trapped charge density throughout the experiment. To validate our approach, we conduct an experiment involving the measured output and transfer characteristics of poly(3-hexylthiophene) (P3HT) transistors with varying channel lengths, tested in a room-temperature environment.

1 Introduction

Over the past few decades, solution-processed electronic devices, particularly organic thin-film transistors (OTFTs), have attracted significant attention due to their potential applications in fields such as sensors,[1] actuators,[2] displays[3] and memory devices.[4] A key phenomenon in these devices is charge carrier trapping, which can have both detrimental and beneficial effects. On one hand, reducing charge traps is crucial, as their presence degrades device performance and stability.[5–7] On the other hand, certain types of trapped charges can enhance the performance of TFT-based gas sensors,[8–11] memories,[7] photodetectors,[12] and artificial synapses.[13] The degree of charge trapping can be controlled through modifications in film deposition techniques and device structure.[14] In fact, highly purified crystals can provide insights into the fundamental limits of organic semiconductors, in terms of the lowest number of traps and the highest values for the charge carrier mobility.[15]

Numerous methods have been proposed to detect and characterize electronic traps in organic semiconductors.[15–18] A review of these methods can be found in ref. 7 and 19. Some techniques, such as electric force microscopy (EFM) and Kelvin probe force microscopy (KPFM),[17,20] allow for the spatial mapping of traps, while others relate the microstructure and electrical transport properties of organic semiconductors. Optical and thermal methods[21,22] offer additional trap characterization by probing radiative and non-radiative electronic transitions between localized band gap states, with thermal techniques able to reach deeper band gap states. Also, it is known that traps affect the noise characteristics of electronic devices.[23–25]

Electrical measurements also provide abundant methods for trap characterization.[18,19] Space-charge limited current (SCLC) measurements in metal–organic–metal diodes[15] primarily focus on traps within the bulk of the semiconductor. In OTFTs, where interfacial traps play a significant role due to charge accumulation near the semiconductor–dielectric interface, simpler methods extract trap information from transfer characteristics by analyzing the threshold voltage (V_T) and sub-threshold

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swing (V_{SS}), often using the ideal MOS model without contact effects.[16,26] More elaborate techniques calculate trap density-of-states (DOS) by correcting for contact effects and analyzing field-effect conductivity through gated four-terminal measurements at different temperatures.[16,27–30] Some of these methods are compared in ref. 16. These methods, while effective, typically assume that trapping and release times are much shorter than the measurement time, *i.e.*, they have no current hysteresis and as such, do not account for current hysteresis.

Other electrical techniques, such as impedance spectroscopy (IS), analyze material responses to applied AC voltage as a function of frequency. Specific IS approaches, including capacitance–voltage (C–V) analysis,[31,32] the equivalent circuit modeling of the impedance spectrum,[33,34] and capacitance–frequency (C–f) analysis,[35,36] provide additional ways to study traps.

Despite the progress made with these methods, the research community continues to seek further advancements, particularly in understanding the dynamics of trap states.[7] This is especially challenging when multiple types of traps are present. Environmentally induced traps, in particular, often remain undetected in electrical measurements, even with careful design of organic electronic devices.[37,38] These unintended traps may arise over the course of a device's lifetime or during specific experiments, yet their effects can go unnoticed. Moreover, contact effects complicate the characterization process, making it difficult to distinguish between the impacts of traps and those of the contacts.

In this work, we present an analysis method to detect and quantify different types of trapped charges, which combines an evolutionary parameter extraction procedure with a previously developed compact model for OTFTs.[39–43] This model accounts for both contact effects[39–42] and a time-dependent threshold voltage, $V_T(t)$, which evolves in response to the trapped charge concentration during hysteresis cycles of the electrical characteristics of OTFTs.[43] The time-dependent $V_T(t)$ model is adapted to consider both expected and unexpected traps – those that can be minimized through careful growth process control,[14,44] and those introduced by environmental exposure (*e.g.*, moisture, oxygen) during device operation.

In order to test our procedure, we selected P3HT for the active layer precisely because its high sensitivity to environmental factors guarantees measurable, time-dependent changes in current–voltage characteristics, enabling systematic analysis of trapping dynamics. The experimental details are described in Section 2. Section 3 summarizes the drift model, including the dynamic $V_T(t)$ and trapped charge density models. The results are presented in Section 4, with conclusions in the last section. The evolutionary parameter extraction procedure is detailed in Appendix A.

2 Experimental details

2.1 P3HT based OTFTs

The poly(3-hexylthiophene) (P3HT) used as the active layer in the OTFTs is sourced from Sigma-Aldrich. It has a regioregularity greater than 90%, an average molecular weight (M_w) ranging from 15 to 45 kDa (kg mol^{-1}), and exhibits p-type semiconductor properties with high electronic quality. To prepare the active layer, 10 mg of P3HT is dissolved in 1 mL of chlorobenzene (CB) and stirred magnetically at 80 °C for 24 hours. The solution is then deposited onto prefabricated chips using a spin-coating process, with a rotation speed of 5000 rpm, acceleration of 500 rpm s^{-1}, and a coating time of 60 seconds. Following deposition, the films are annealed at 100 °C for 20 minutes to enhance film quality.

The P3HT layer is applied to chips fabricated by FRAUNHOFER IPMS, which are commercial substrates measuring 15 × 15 mm^2 in a bottom-gate-bottom-contact (BG-BC) configuration. Fig. 1 illustrates the transistor structure and chip layout. The gate electrode is made of heavily n$^+$-doped silicon with a dopant concentration of approximately 3 × 10^{17} cm^{-3}. The gate insulator is a 230 ± 10 nm layer of thermally oxidized silicon (SiO_2), providing a capacitance per unit area of C_{ox} = 15 nF cm^{-2}. The interdigitated contact electrodes consist of a 10 nm indium tin oxide (ITO) adhesion layer and a 30 nm gold (Au) conductive film. Each substrate contains 16 transistors with varying channel

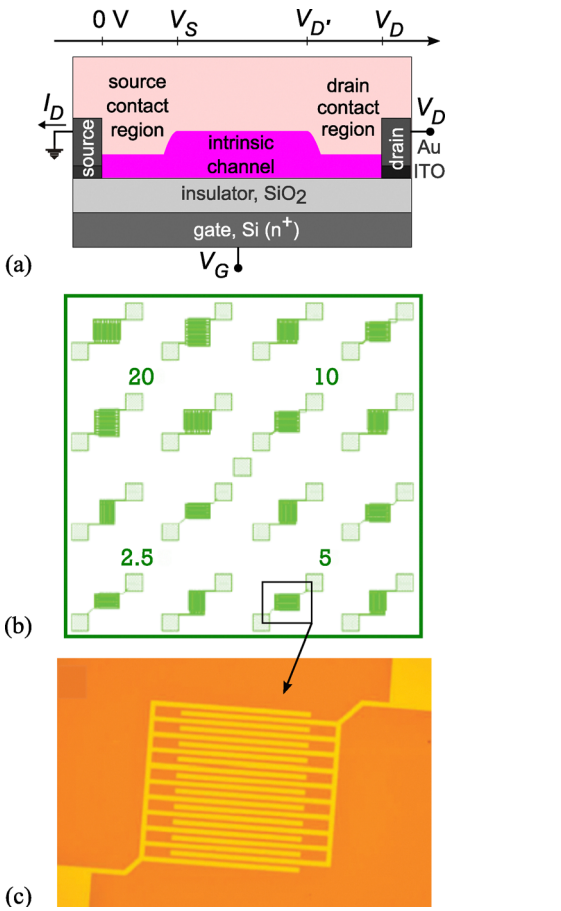

Fig. 1 (a) Diagram of the P3HT-based transistors indicating the contact regions and intrinsic channel of the bottom-contact structure, and the voltage at their borders. Usually the drain contact region is negligible, $V_{D'}$ = V_D.[45] (b) Lay-out with 16 transistors of four different channel lengths. (c) Detail of one of the transistors.

lengths of L = 2.5, 5, 10 and 20 μm, while the width of each transistor is W = 10 mm.

2.2 Current characteristics of the transistors

The output (I_D–V_D) and transfer (I_D–V_G) characteristics of the P3HT-based OTFTs are presented with symbols in Fig. 2 and solid lines in Fig. 3, respectively. The output characteristics in Fig. 2 were measured at a fast scan rate showing no hysteresis. The transfer characteristics of Fig. 3 were measured with a drain voltage of V_D = −30 V, while the gate voltage V_G was swept at a scan rate (SR) of 1000 mV s^{-1} (with V_G steps of 0.1 V every 100 ms). Note that the transfer characteristics were measured close to the linear region to mitigate artifacts from contact resistance and gate-bias-dependent mobility. Saturation-region methods, which rely on square-law assumptions for their transfer characteristics, are prone to significant errors (overestimation and underestimation of carrier mobility) in disordered systems.[46,47] P3HT devices fabricated on SiO_2 dielectrics are known to operate reliably at gate voltages up to 100 V or more without significant deviation from ideal transistor behavior.[48,49] In Fig. 2, the apparent absence of current saturation is attributed to short-channel effects, a well-documented phenomenon in organic transistors with reduced channel lengths.[50] Among these, channel-length modulation plays a central role. The drift-based transport model introduced in Section 3 explicitly incorporates this effect through the channel-length modulation parameter, λ, ensuring a physically meaningful description of the output characteristics.

The transfer characteristics in Fig. 3a–d clearly exhibit a memory effect. Two distinct regions can be identified:

(i) loop-1 a closed hysteresis loop spanning most of the range for $-V_G$ (approximately −5 V to +18 V), and

(ii) loop-2 an open loop in the remaining measurement range for $-V_G$ (approximately −10 V to −5 V).

The behavior of closed loops like loop-1 has been extensively studied in previous research,[51–54] including dynamic analyses.[43] However, to our knowledge, the anomalous behavior observed in loop-2 has not been explored. Specifically, the origin of this second region, as well as the reduction in its size with increasing channel length (L), remains unexplained.

The combined analysis of these two loops in relation to the existence of traps in the transistor is the main objective of the work. We aim, not only to detect traps, but also to monitor the time evolution of the trapped charge density along the measurement of the transfer characteristics shown in Fig. 3. As the main tool for the dynamic characterization of OTFTs, we consider an unified compact model that describes the electrical characteristics of TFTs. It includes the effects of the intrinsic channel of the transistor, the source and drain contact regions, and a time-dependent threshold voltage $V_T(t)$ (Fig. 1a).

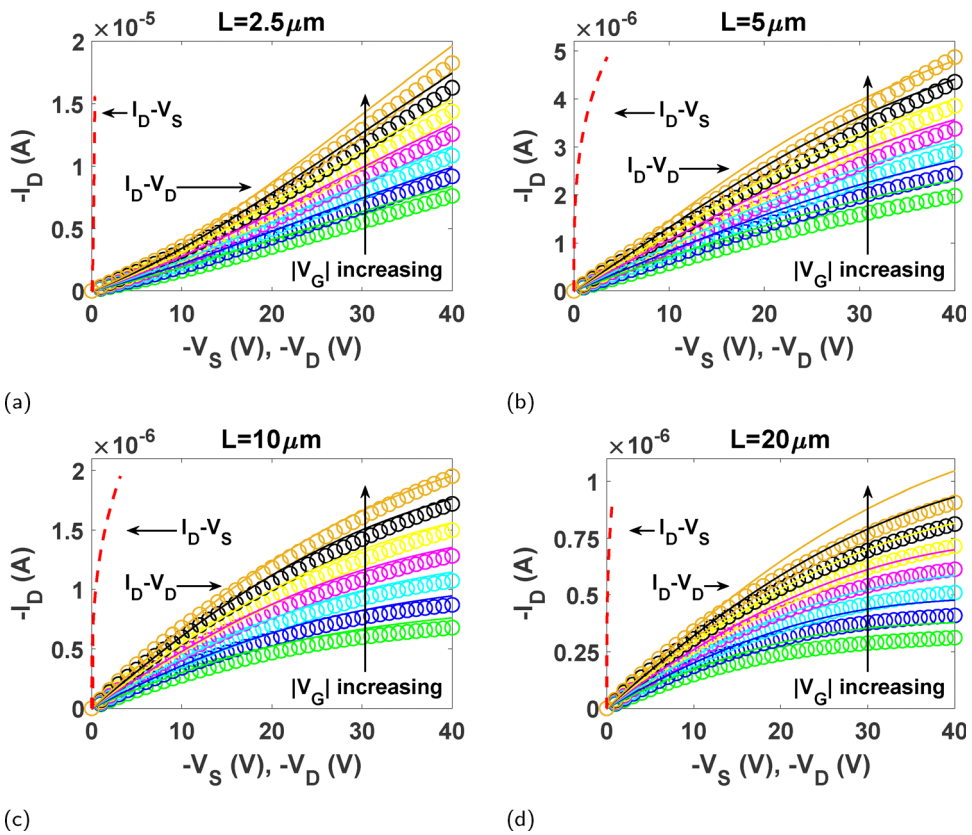

Fig. 2 (a)–(d) Comparison of experimental output characteristics of P3HT based transistors with different channel lengths (symbols), with our calculations (solid lines), using the parameters of Table 1. V_G is swept following this sequence of values: 0, −4, −8, −12, −16, −20 and −24 V. Close to the ordinate axis, the I_D–V_S curves at the contacts, calculated with eqn (3), are represented in dashed red lines.

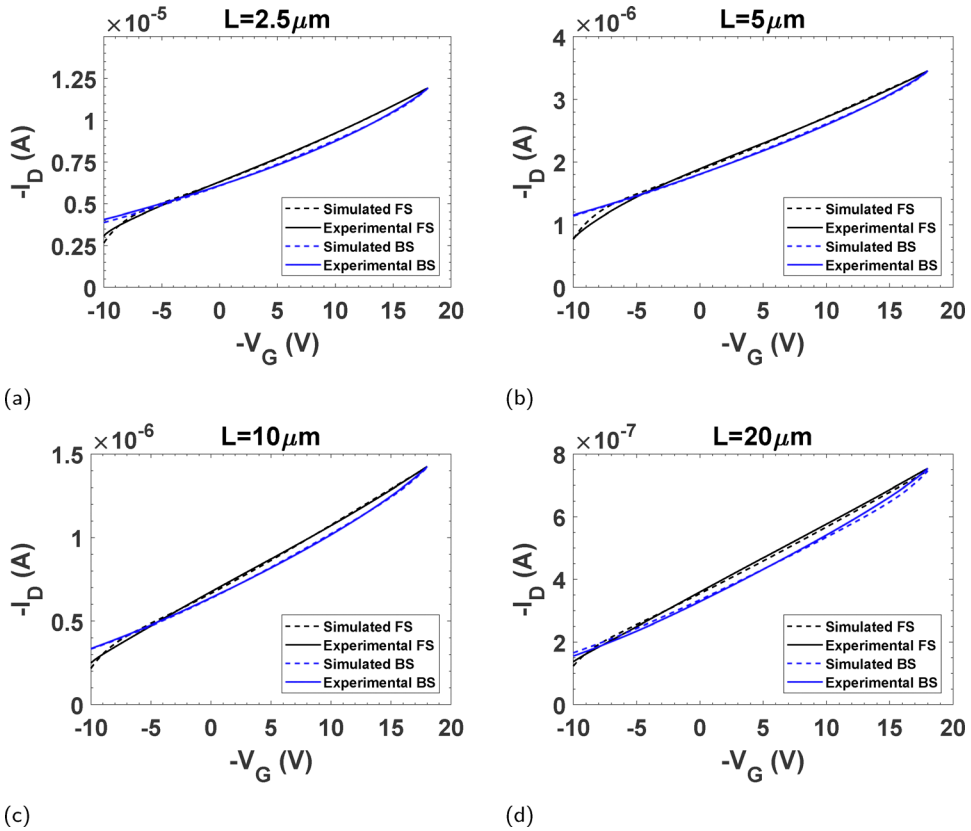

Fig. 3 (a)–(d) Comparison of experimental transfer characteristics (solid lines) for P3HT-based transistors with different channel lengths (Fig. 2) with simulated results (dashed lines) using parameters from Table 1. Time-dependent variables Q_{tL} (Fig. 5), V_T (Fig. 6), and V_{SS} (Fig. 7) were incorporated. OFF-to-ON voltage sweeps (black) and ON-to-OFF sweeps (blue) are shown. V_D = −30 V.

The deduction of the complete model is detailed in ref. 43. For completeness, the key equations are summarized in the next section.

3 Generic drift model for OTFTs

3.1 Model for the intrinsic region

Organic thin-film transistors (OTFTs) are governed by charge transport mechanisms rooted in two widely accepted theories:

(1) Charge drift in tail-distributed traps (TDTs)

(2) Variable range hopping (VRH)

A unifying feature of these models is the empirically observed relationship between mobility μ and gate voltage:

$$\mu = \mu_0(V_G - V_T)^{\gamma}, \quad (1)$$

where γ is the mobility enhancement factor and μ_0 represents mobility at $V_G - V_T$ = 1 V. Parameter γ reflects the interplay between the characteristic energy width ($E_0 = kT_0$) of an exponential tail distribution in the density of states (DOS) and the absolute temperature T, such that: $\gamma = 2(T_0/T - 1)$.[55]

3.1.1 Advantages of the compact modeling approach. By adopting V_T and γ as primary parameters, our framework circumvents the need for complex physical derivations. This simplification aligns with the core objective of compact modeling that prioritizes accurate electrical behavior prediction over exhaustive mechanistic detail. The drain current, I_D, is derived by integrating the channel conductance, which depends on both mobility and charge density. Substituting eqn (1) into this framework yields: $I_D \propto \mu_0(V_G - V_T)^{\gamma}$.

3.1.2 Validation and applicability. This generic charge-drift model for the intrinsic TFT channel (Fig. 1a) has been rigorously validated across diverse OTFT architectures and materials systems,[39,56–67] and is written as:

$$I_D = \mu_0 C_{ox}\frac{W}{L'}\frac{V_{EODR}(V_G,V_S)^{(2+\gamma)} - V_{EODR}(V_G,V_{D'})^{(2+\gamma)}}{2+\gamma},$$
$$L' = L/(1+\lambda|V_{D'} - V_S|), \quad (2)$$
$$V_{EODR}(V_G,V) = V_{SS}\ln\left[1+\exp\left(\frac{V_G - V_T - V}{V_{SS}}\right)\right],$$

which uses the asymptotically interpolation function $V_{EODR}(V_G,V)$ in order to consider the sub-threshold regime, $V_{EODR}(V_G,V) \approx V_{SS}\exp[(V_G - V_T - V)/V_{SS}]$, as well as the above-threshold regime, $V_{EODR}(V_G,V) \approx (V_G - V_T - V)$, with either $V = V_S$ or $V = V_{D'}$, and V_{SS} is the sub-threshold swing of the TFT.

The rest of the variables are V_G, the gate terminal voltage, V_D, the drain terminal voltage, and V_S and $V_{D'}$ are the values of the potential at the edges of the intrinsic channel in contact with the source and drain regions, respectively. Thus, V_S is the voltage drop at the source contact and $V_{DD'} = V_D - V_{D'}$ is the

voltage drop at the drain contact (Fig. 1a). C_{ox} is the capacitance per unit area of the gate insulator and W and L are the channel width and length, respectively. L' is the effective channel length modulated by the coefficient λ. If the channel length modulation effect is negligible, λ can be assumed zero and $L' \approx L$, minimizing the computational time of eqn (2). The model accounts for all transistor operating modes – linear, saturation, sub-threshold, and even reverse biasing. The success of eqn (2) lies in balancing physical interpretability with computational efficiency, making it a cornerstone for both device analysis and circuit simulation.

3.2 Model for the contact regions

To complement the intrinsic channel model (2), we incorporate a model that describes the electrical characteristics of the source and drain contact regions. While the intrinsic model already accounts for contact effects, drain contact effects are typically negligible in most OTFTs, as the potentiometry measurements showed in ref. 45. This simplification leads to $V_{DD'} \approx 0$ V and $V_D \approx V_{D'}$, meaning that only the source contact model is necessary.

The source contact model, proven effective in various scenarios,[41,42] can describe both space-charge-limited transport in low-energy contact barriers[40] and injection-limited transport in Schottky barriers.[61,68–70] The drain current I_D is related to the voltage drop at the source contact V_S by:

$$I_D = M_S \times V_S^{m_s}, \quad \forall m_s \in \mathbb{Z}: 0 < m_s \leq 2, \tag{3}$$

where m_s is a constant that classifies transport behavior: for $0 < m_s < 1$, the model describes injection-limited transport in Schottky barriers (a convex function); for $1 < m_s \leq 2$, it describes space-charge-limited transport (a concave function), with $m_s = 2$ yielding the classical Child's law; and $m_s = 1$ corresponding to Ohmic contacts, where I_D and V_S are linearly related:

$$I_D = V_S/R_S, \tag{4}$$

where R_S is the source contact resistance. In this last case, the parameter M_S coincides with the contact conductance: $M_S = 1/R_S$.

The parameter M_S in eqn (3) depends on the gate voltage[40] as:

$$M_S = \alpha_s(V_G - V_T)^{1+\gamma}, \tag{5}$$

where α_s is a proportionality constant. This dependence has been justified for ohmic[71] and non-linear contacts.[58,72–75] This electric field dependence of M_S, which was physically justified for $m_s = 1$ (ohmic contacts)[40] and $1 < m_s \leq 2$ (space-charge-limited contacts),[40] was later assumed and checked for $0 < m_s < 1$ (Schottky contacts).[41] The sub-threshold regime can be incorporated into eqn (5) and is modeled using an asymptotic interpolation function[59] similar to the one used in V_{EODR} (eqn (2)):

$$M_S = \alpha_s \left\{ V_{SS} \ln\left[1 + \exp\left(\frac{V_G - V_T}{V_{SS}}\right)\right]\right\}^{1+\gamma}. \tag{6}$$

Note that for staggered configurations, the voltage drop at the drain contact may be significant,[62,76,77] requiring an additional model for the drain contact, as was detailed in ref. 42.

This generic drift model (2)–(6) is valid for static situations, but it does not account for trapping and de-trapping effects that cause the threshold voltage and sub-threshold swing to evolve over time. To address this, we incorporate models[43] for these time-dependent effects, discussed below.

3.3 Dynamic behavior of the trapped charge density: $V_T(t)$ and $V_{SS}(t)$

A shift in the threshold voltage ΔV_T is linked to the variation of trapped charge density in the semiconductor or its interface with the insulator. This relationship[78–80] is given by:

$$\Delta V_T = -\frac{\Delta Q_{tL}}{C_{ox}}. \tag{7}$$

where Q_{tL} represents the average trapped charge density along the channel in C cm^{-2}.

Similarly, the sub-threshold swing V_{SS} can change with the bulk or interface trapped charge density.[16,81,82] Assuming the trap densities are energy-independent, V_{SS} can be related to an equivalent trapped charge density Q_{tL}:[16]

$$V_{SS} = \frac{kT}{q}\ln 10 \times \left(1 + \frac{qQ_{tL}}{C_{ox}}\right). \tag{8}$$

The variations in V_{SS} are related to Q_{tL} by:

$$\Delta V_{SS} = \frac{kT}{q}\ln 10 \times \left(\frac{q\Delta Q_{tL}}{C_{ox}}\right). \tag{9}$$

where q is the free carrier charge.

The time-dependent behavior of V_T and V_{SS} at a particular instant t_j can be related to their values at a previous instant t_{j-1} from eqn (7) and (9), respectively as:

$$V_T(t_j) = V_T(t_{j-1}) - \left[\frac{Q_{tL}(t_j) - Q_{tL}(t_{j-1})}{C_{ox}}\right], \tag{10}$$

and

$$V_{SS}(t_j) = V_{SS}(t_{j-1}) + \frac{kT}{q}\ln 10 \times \left[q\frac{Q_{tL}(t_j) - Q_{tL}(t_{j-1})}{C_{ox}}\right], \tag{11}$$

with Q_{tL} in C cm^{-2} in eqn (10) and Q_{tL} in C cm^{-2} eV^{-1} in eqn (11).[43]

3.3.1 Model for Q_{tL}. Our framework for modeling the dynamic response of trapped charge integrates two critical dimensions of trap behavior: physical origin and voltage-dependent dynamics. First, it distinguishes between traps based on their location relative to the intrinsic conduction channel. Intrinsic traps (b1) arise from structural imperfections inherent to semiconductor fabrication processes, such as grain boundaries formed during film crystallization or unintended dopant clustering in solution-processed materials. These defects reside within or near the conduction pathway, directly distorting charge transport through localized energy barriers. In contrast, extrinsic traps (b2) originate from environmental interactions or interfacial defects – for instance, moisture infiltration at the dielectric–semiconductor boundary or oxidation of metal contacts.

Unlike intrinsic traps, these external defects influence device behavior indirectly through long-range electrostatic effects, modulating carrier injection efficiency rather than bulk transport.

Second, our model explicitly incorporates the terminal voltage dependence of trap activity. The filling and emptying kinetics of both intrinsic and extrinsic traps are dynamically governed by the applied gate, V_G, and drain, V_D, voltages. This enables time-resolved analysis of charge trapping under operational conditions, revealing how transient voltage changes redistribute trapped charges over timescales spanning milliseconds to hours. By coupling spatial trap distributions with voltage-dependent kinetics, our framework captures critical phenomena such as bias-stress instability and hysteresis – key challenges in organic and hybrid transistor reliability.

This dual approach – linking trap microenvironments to macro-scale electrical behavior – provides a versatile tool for diagnosing degradation mechanisms and optimizing device stability across material systems.

The evolution of the trapped charge can be described with a first-order linear differential equation or a continuity equation for trapped charges (eqn (12)). One term is proportional to the trapped charge density and is controlled by a time constant τ. Another term is modeled as a generation term proportional to the drain current I_D with a parameter β, where the flow of free charge carriers can be seen as a mechanism that favors the trapping:[43]

$$\frac{dQ_{tL}}{dt} = \beta I_D - \frac{Q_{tL}(t)}{\tau}. \quad (12)$$

Eqn (12) can be solved at discrete time intervals, allowing the calculation of the trapped charge Q_{tL} at a specific time t_j for n_{traps} traps. Each trap has a unique time constant τ_r, with $r = 1 \ldots n_{traps}$:

$$\begin{aligned} Q_{tL}(t_j) &= \sum_{r=1}^{n_{traps}} Q_{tL,r}(t_j), \text{ where} \\ Q_{tL,r}(t_j) &= Q_{tL,r}(t_{j-1}) e^{-\frac{t_j - t_{j-1}}{\tau_r}} + \beta_r \tau_r I_D \left(1 - e^{-\frac{t_j - t_{j-1}}{\tau_r}}\right). \end{aligned} \quad (13)$$

This equation applies to traps close to the intrinsic channel (denoted as b1), where variations in the trapped charge arise from changes in both V_G and V_D. Specifically, when $V_D \neq 0$ V and $I_D \neq 0$ A, the transistor transitions to a new steady state.

There are cases where the term βI_D in eqn (12) can be neglected. These include:

(i) $V_D = 0$ V (*i.e.* $I_D = 0$ A), or

(ii) Traps located far from the intrinsic channel, which are insensitive to the drain current – case (b2).

In these scenarios, the trapped charge Q_{tL} evolves towards a new steady state Q_{t0}, at a rate governed by the time constant τ. The rate of change is described by:

$$\frac{dQ_{tL}}{dt} = -\frac{Q_{tL}(t) - Q_{t0}}{\tau}, \quad (14)$$

where $Q_{t0} = Q_{t0}(V_G, V_D)$ represents the steady-state value of Q_{tL} at a given bias point (V_G, V_D).

Eqn (14) can also be solved at discrete time intervals, allowing the calculation of Q_{tL} at each time t_j for n_{traps} traps, with each trap having a different time constant τ_r:

$$\begin{aligned} Q_{tL}(t_j) &= \sum_{r=1}^{n_{traps}} Q_{tL,r}(t_j), \quad \text{where} \\ Q_{tL,r}(t_j) &= Q_{tL,r}(t_{j-1}) e^{-\frac{t_j - t_{j-1}}{\tau_r}} + Q_{t0,r}\left(1 - e^{-\frac{t_j - t_{j-1}}{\tau_r}}\right). \end{aligned} \quad (15)$$

A detailed physical justification for the model described in eqn (12) and (14) can be found in ref. 43.

Finally, it is important to note that the drift model is developed for N-type TFTs, where I_D, V_D and V_G are positive in the above-threshold region. In P-type TFTs, these quantities are typically negative. To account for this sign difference, the following steps are recommended:

(i) Change the sign of the experimental values for I_D, V_D and V_G,

(ii) Apply the model equations as though the device were an N-type transistor,

(iii) After completing the analysis, reverse the signs of I_D, V_D and V_G, as well as the resulting values of V_T.

4 Results

4.1 Extraction of fitting parameters

This section aims to determine the value of the set of parameters necessary to evaluate all the equations of the model (2), (3), (10), (11), (13) and (15). An advanced fitting technique based on an evolutionary procedure is applied to the output characteristics I_D–V_D, represented by symbols in Fig. 2, and the I_D–V_G curves shown with solid lines in Fig. 3. The evolutionary procedure is outlined in Appendix A and the set of fitting parameters is named individual x (eqn (17)) in Appendix A.

The procedure focuses on identifying common parameters across all four transistors, particularly those linked to the fabrication process, such as the mobility-related parameters μ_0 and γ, as well as the threshold voltage V_T and the early voltage per unit length V'_A. The source contact region is modeled using the parameters m_s and M_S (eqn (3)). The effects of the contact region in OTFTs diminish with increasing channel length.[83,84] As shown in Fig. 2, the experimental I_D–V_D curves evolve from concave to convex at low drain voltages as the channel length L increases. For L = 2.5 μm, a distinct concave behavior at low V_D indicates a space charge limited current (SCLC) regime, characteristic of short-channel transistors. This behavior suggests that the evolutionary procedure will be sensitive to the concave–convex transition, providing distinct values for m_s based on channel length.

Despite this, the voltage drop across the contact region should remain similar for all transistors, as the fabrication process is uniform, with only L varying. The differences in m_s should be balanced by adjusting M_S. It is important to note that shorter channel lengths result in lower I_D values for the same bias point. For a quadratic relationship between I_D and V_D in

the contact region, the slope of this curve decreases at lower I_D, revealing information about the contact conductance, which is linked to M_S (eqn (3)).

From an analytical perspective, the parameter extraction procedure may yield higher values of M_S for shorter channels, compensating for the increased m_s. A crucial check will be whether the voltage drop across the contact region remains consistent across the four transistors.

The variation in threshold voltage depends on the evolution of the trap charge density (eqn (7)). However, the initial value of $V_T(0)$ is unknown and depends on the experimental conditions. Before conducting both I_D–V_G and I_D–V_D experiments, the samples are held at the same gate voltage, V_G = 10 V. Thus, $V_T(0)$ is assumed to be the same in both experiments. Once the experiments commence ($t > 0$), $V_T(t)$ remains constant throughout the I_D–V_D experiment, while it evolves with changes in the trap charge density (eqn (10)) during the transfer characteristics.

Initially, only one type of trap, with charge density $Q_{tL,1}$, is considered. Since the procedure evaluates charge density increments during I_D–V_G experiments, we assume an arbitrary initial value of $Q_{tL,1}(0) = 0$ C cm^{-2}. As $-V_G$ varies from −10 to +18 V, it increases the number of free charge carriers (holes) in the conducting layer, causing the traps to become positively charged. If the analysis detects additional traps, their charge densities ($Q_{tL,2}(0)$,…,$Q_{tL,n_{traps}}(0)$) will be included in the set of fitting parameters x (eqn (17)).

Other parameters related to the traps include the time constant τ and the factor β. The time constant τ is specific to the type of trap, but remains consistent across the four transistors. The parameter β, which modulates the drain current (eqn (12)), is dependent on the local electric field along the channel, as described in ref. 43. For this reason, it is preferable to treat β as distinct for each transistor and, if necessary, separate the forward and reverse sweeps in the transfer characteristics (β_{rf} and β_{rb}, respectively, for trap #r).

The sub-threshold swing V_{SS} is sensitive to the trap charge density (eqn (8)) and its variation (eqn (9)). Determining the initial value $V_{SS}(0)$ provides insights into the trapped charge density, which we assumed to be $Q_{tL,1}(0) = 0$ C cm^{-2}. V_{SS} is typically extracted from the slope of the I_D–V_G curve in the sub-threshold region. However, our procedure can extract it from I_D–V_G curves above threshold, as the generic drift model (2) is highly sensitive to this parameter at any bias point. V_{SS} offers information about various traps:

(i) Traps formed during fabrication, whose density is assumed constant across different L, and

(ii) Traps created unintentionally, whose density may vary depending on the length of the transistor or exposure to external conditions.

4.2 Steps

After classifying parameters as either common $P_C \in \{\mu_0, \gamma, V_T(0), V'_A, Q_{tL,r}(0), \tau_r\}$ or varying across transistors $P_D \in \{m_s, M_S, V_{SS}(0), \beta_{rf}, \beta_{rb}\}$ in the four sets of transistors, the extraction procedure proceeds as follows:

• Step 1: estimate parameters μ_0, γ, V_T and V'_A by analyzing the current characteristics of the four transistors using the traditional MOS model[41,42,58,59,85,86] and the H_{VG} method.[87]

• Step 2: define the initial search space for all parameters in the set x (eqn (17)), considering only one type of trap (r = 1), with parameters τ_1, β_{1f} and β_{1b}, and $Q_{tL,1}(0) = 0$ C cm^{-2}.

• Step 3: run the evolutionary procedure on the four transistors. For brevity, the initial fitting results for the L = 5 μm transistor are shown in Fig. 4a (parameters in Table 2). This channel length was selected as a representative case to balance clarity and comprehensiveness, that is, to avoid extreme scaling effects (*e.g.*, pronounced contact resistance in shorter channels or bulk-limited transport in longer channels) while capturing the core behavior of the system. The following observations are entirely applicable to the other three transistors. The fitting errors (eqn (19)) are O_1 = 16.06% and O_2 = 7.87%. Despite a good overall fit, loop-2, corresponding to the lowest values of $-V_G$, remains poorly fitted. This suggests the presence of a second trap (#2), which influences loop-2 behavior. The analysis of loop-2 in Fig. 4a reveals an exponential transient at the start of the forward sweep (FS), consistent with the evolution of

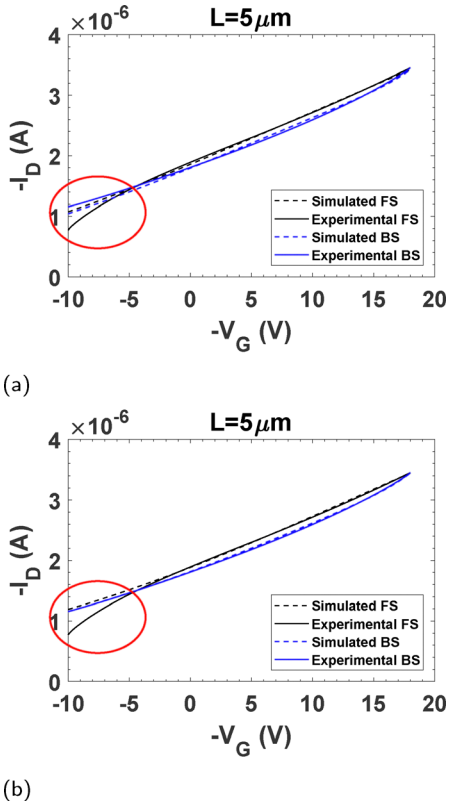

Fig. 4 Comparison of the experimental transfer characteristics of the P3HT based transistor with L = 5 μm (solid lines; shown also in solid lines in Fig. 3b), with our calculations (dashed lines). (a) The extraction procedure and calculation considers an individual (eqn (17)) with only one trap. The values of the parameters are in Table 2. (b) The extraction procedure considers an individual (eqn (17)) with two traps. The values of the parameters are in Table 1. Later, the I_D–V_G curve is calculated with only one trap. The voltage sweep from OFF-to-ON is in black lines and from ON-to-OFF in blue lines. V_D = −30 V.

Table 1 Extracted values of the parameters composing the individual representation x – μ_0 is in $cm^2\ V^{-1}\ s^{-1}$, M_S is in $A\ V^{(-2-\gamma)}$, V'_A is in $V\ cm^{-1}$, $Q_{tL,2}$ is in $C\ cm^{-2}$, τ_1 and τ_2 are in s, V_T is in V and V_{SS} is in V – $Q_{tL,1}(0) = 0$ C cm^{-2} in the four cases – checked boxes indicate the experiment is aimed to fit

	Value				Fitting	
x	$L = 2.5$ μm	$L = 5$ μm	$L = 10$ μm	$L = 20$ μm	I_D–V_D	I_D–V_G
$x_1 = \mu_0$	3.00×10^{-5}	3.00×10^{-5}	3.00×10^{-5}	3.03×10^{-5}	☒	☒
$x_2 = \gamma$	0.25	0.25	0.25	0.25	☒	☒
$x_3 = V_T$	37.48	34.83	32.62	35.89	☒	☒
$x_4 = V_{SS}$	22.01	22.44	13.04	3.53	☒	☒
$x_5 = m_s$	1.76	0.30	0.34	0.30	☒	☒
$x_6 = M_S$	1.00×10^{-4}	3.34×10^{-6}	1.32×10^{-6}	1.04×10^{-6}	☒	☒
$x_7 = V'_A$	92 819	118 164	90 466	100 344	☒	☒
$x_8 = \beta_{1f}$	-1.23×10^{-10}	-1.00×10^{-10}	-1.17×10^{-7}	-1.42×10^{-7}	☐	☒
$x_9 = \beta_{1b}$	-1.05×10^{-3}	-3.49×10^{-3}	-8.45×10^{-3}	-1.97×10^{-2}	☐	☒
$x_{10} = \tau_1$	2	2	2	2	☐	☒
$x_{11} = \tau_2$	1.3	1.3	1.3	1.3	☐	☒
$x_{12} = Q_{tL,2}(0)$	11.9×10^{-8}	12.0×10^{-8}	8.74×10^{-8}	5.43×10^{-8}	☐	☒

trapped charge density. This transient can be explained with a trapped charge density evolving like in eqn (15) with an initial charge $Q_{tL,2}(0)$ and final steady state $Q_{t0,2} = 0$ C cm^{-2}, *i.e.* $Q_{tL,2}(t) = Q_{tL,2}(0)\exp(-t/\tau_2)$. Accordingly, in this experiment the threshold voltage at $t = 0$ s must be initialized, not at $V_T(0)$, but at $V_T(0) - Q_{tL,2}(0)/C_{ox}$. Identical trends were observed across all devices, confirming the universal applicability of our model.

• Step 4: add trap #2 to the set x (eqn (17)), including the initial charge density $Q_{tL,2}(0)$ and time constant τ_2, then rerun the evolutionary procedure for improved fits.

• Step 5: analyze parameter values in the set x (eqn (17)). For common parameters P_C, calculate the average ($\langle P_C \rangle$) and deviations (ΔP) across the four transistors. Refine the search space by reducing the range of P_C to $[\langle P_C \rangle - \Delta P, \langle P_C \rangle + \Delta P]$ and repeat until acceptable convergence is reached. Parameters that do not converge to common values, such as m_s, M_S, $V_{SS}(0)$, β_{1f}, β_{1b}, $Q_{tL,2}(0)$ are analyzed individually.

The best fit results from the procedure outlined in Appendix A are shown in Fig. 2 (solid lines for I_D–V_D curves) and Fig. 3 (dashed lines for I_D–V_G curves). The corresponding fitting parameters are summarized in Table 1. The extracted mobility ($\mu_0 = (3.01 \pm 0.02) \times 10^{-5}$ $cm^2\ (V\ s)^{-1}$), mobility enhancement factor ($\gamma = 0.25$), threshold voltage ($V_T = 35 \pm 2$ V), Early voltage per unit length ($V'_A = (10.0 \pm 1.7) \times 10^4$ V cm^{-1}), and time constants ($\tau_1 = 2$ s, and $\tau_2 = 1.3$ s) reflect mean values and their deviations (within the range $\langle P_C \rangle \pm \Delta P$) across all channel lengths. That is, the actual values for these common parameters should be located in an interval defined by their mean value $\langle P_C \rangle$ and their deviation $\pm\Delta P$. The observed deviations lie within expected tolerances for disordered semiconductors, underscoring the model's robustness to fabrication variability. The extracted values of the early voltage per unit length (V'_A) confirm the presence of short-channel effects, as predicted in Section 2.2. These effects begin to manifest in devices with a channel length of approximately 10 μm, and become increasingly pronounced as the channel length is reduced to 2.5 μm, consistent with the onset of channel pinch-off and modulation effects. The remaining parameters exhibit clear dependence on L, as detailed in Table 1. Further analysis of the trapped charge density ($Q_{tL}(t)$), threshold voltage ($V_T(t)$), and sub-threshold swing ($V_{SS}(t)$) (see Fig. 5–7) is presented in the next section.

4.3 Discussion

Fig. 5 highlights two distinct regions: the initial transient, occurring during the first 10 seconds, which corresponds to $Q_{tL,2}(t)$, and the subsequent region, corresponding to $Q_{tL,1}(t)$. To isolate the effect of trap #2, the I_D–V_G curve for $L = 5$ μm (previously shown with dashed lines in Fig. 3b) was recalculated with the same parameter values from Table 1, except that $Q_{tL,2}(0) = 0$ C cm^{-2}. The result is depicted with dashed lines in Fig. 4b and compared with experimental data (solid line). When trap #2 is neglected, our calculations match the experimental data in loop-1 but not in loop-2. Specifically, if trap #2 is absent, no transient response is observed at the beginning of the forward sweep (dashed black line in Fig. 4b). A similar behavior is reported in Fig. 2 of ref. 88, where OTFT transfer characteristics with and without self-assembled monolayers (SAMs) are shown. Their transfer characteristics measurements without SAMs exhibit a transient behavior similar to ours, while no such behavior is detected with SAMs.

The trapped charge density variation in trap #2, represented by $Q_{tL,2}(0)$, decreases as L increases (see Fig. 5 and Table 1). The maximum variation of the trapped charge density in trap #1, $\Delta Q_{tL,1_{max}}$, remains independent of L, fluctuating around $\Delta Q_{tL,1_{max}} = (2.0 \pm 0.3) \times 10^{-8}$ C cm^{-2}, which is smaller than

Table 2 Extracted values of the parameters composing the individual representation x used in Fig. 4a, considering a single trap for the case $L = 5$ μm, with $Q_{tL,1}(0) = 0$ C cm^{-2}

x	Value
$x_1 = \mu_0$	6.32×10^{-5} $cm^2\ V^{-1}\ s^{-1}$
$x_2 = \gamma$	0.0
$x_3 = V_T$	37.58 V
$x_4 = V_{SS}$	8.46 V
$x_5 = m_s$	0.78
$x_6 = M_S$	3.17×10^{-5} $A\ V^{(-2-\gamma)}$
$x_7 = V'_A$	119 995 V cm^{-1}
$x_8 = \beta_{1f}$	-4.15×10^{-9}
$x_9 = \beta_{1b}$	-3.20×10^{-3}
$x_{10} = \tau_1$	1.8034 s

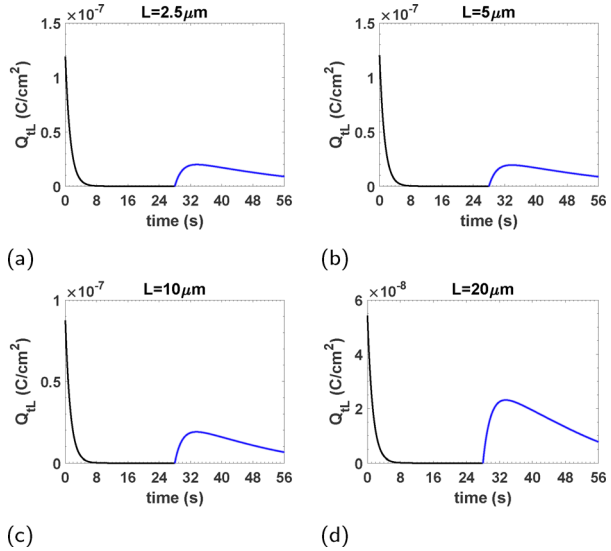

Fig. 5 (a)–(d) Time evolution of Q_{tL} (trapped charge density) calculated using eqn (13) and (15) and the parameters of Table 1 during the measurements of the transfer characteristics of P3HT based transistors with different channel lengths in Fig. 3.

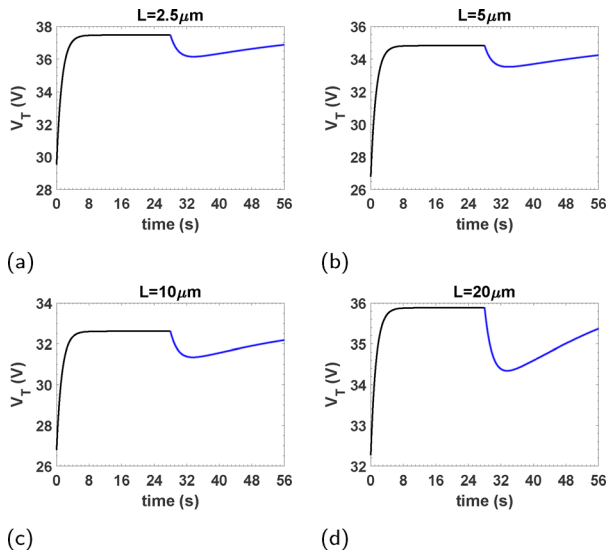

Fig. 6 (a)–(d) Time evolution of V_T (threshold voltage) calculated from eqn (10) and the parameters of Table 1 during the measurements of the transfer characteristics of P3HT based transistors with different channel lengths in Fig. 3.

the variation in trap #2. The trapped charge density variations in the I_D–V_G curves (Fig. 5) affect both V_T (Fig. 6) and V_{SS} (Fig. 7). It is important to note that the generic charge drift model (2) is highly sensitive to the values of these two parameters. Although the measurements do not cover the sub-threshold region, even small variations in V_{SS} can significantly impact the fit to experimental data.

In addition to $Q_{tL,2}(0)$, $V_{SS}(0)$ also shows a clear decrease as L increases. Using the values of $V_{SS}(0)$ in eqn (8), we estimate the global trap charge density $N_t = N_{t,1} + N_{t,2}$ in the transistor, where

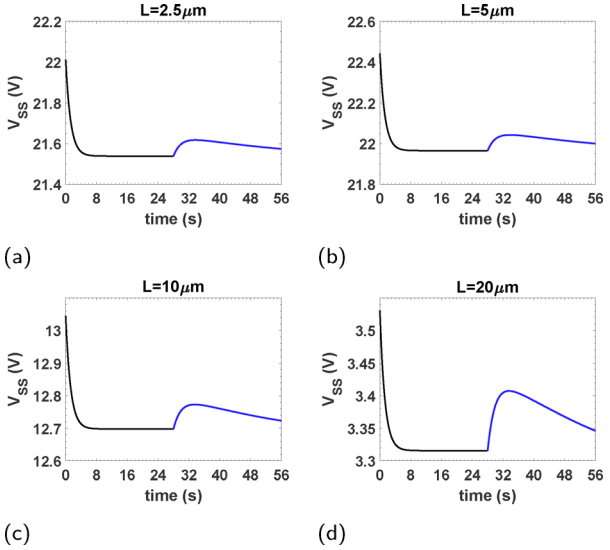

Fig. 7 Time evolution of V_{SS} (sub-threshold swing) computed *via* eqn (11) and the parameters of Table 1 during the measurements of the transfer characteristics of P3HT based transistors with different channel lengths in Fig. 3.

$N_{t,1}$ and $N_{t,2}$ correspond to traps #1 and #2, respectively. The resulting values of N_t are provided in Table 3 and illustrated in Fig. 8 as a function of the maximum trapped charge density variation in trap #2, $\Delta N_{tL2} = Q_{tL,2}(0)/q$. A proportional relationship is observed in Fig. 8, where only 2–8% of the total trapped charge varies during the experiment. These values suggest that trap #1 is present with constant concentration across all four transistors, likely related to the fabrication process. In contrast, the trapped charge density and its variation in trap #2 clearly depend on the channel length of the transistor, and can be related to unexpected traps originated from environmental species.

Li and colleagues[89] investigated the humidity dependence of electrical performance in different OTFTs, showing that moisture sensitivity varies with channel length. They attributed performance degradation under high relative humidity (RH) to charge trapping at grain boundaries by polar water molecules. In our study, assuming the same concentration of environmental molecules (*e.g.*, humidity, atmospheric contaminants) surrounding all transistors, the trap density will be higher in transistors with smaller volumes and shorter lengths. Specifically, the surface area exposed to the environment, including source and drain fingers and the organic channel, increases 1.8 times from the shortest (2.5 μm) to the longest (20 μm) channel transistor (Fig. 1b). The exposed surface area

Table 3 Calculated values of $N_t = qQ_{tL}$ from eqn (9) and $\Delta N_{tL2} = Q_{tL,2}(0)/q$ using the parameters of Table 1 for the four transistors

L (μm)	N_t (cm^{-2})	ΔN_{tL2} (cm^{-2})
2.5	3.46×10^{13}	7.45×10^{11}
5	3.53×10^{13}	7.53×10^{11}
10	2.05×10^{13}	5.47×10^{11}
20	5.48×10^{12}	3.39×10^{11}

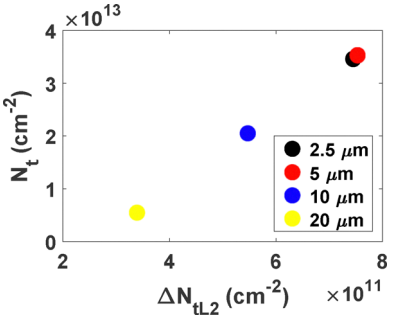

Fig. 8 Relation between the value of the density of trapped charges N_t in the transistor, extracted from the parameter V_{SS} and eqn (9), and the maximum variation of the density of trapped charges in trap #2, determined as $\Delta N_{tL2} = -Q_{tL,2}(0)/q$, as a function of the channel length.

of the organic channel increases eightfold, enhancing interactions with environmental species. Assuming absorption of environmental molecules by the organic channel, this results in a 4.5-fold increase in potential trap density from the shortest to the longest channel transistor. This observation aligns with the factor of 6.3 derived from N_t values in Table 3.

A final observation regarding the size of the hysteresis loops in the transfer curves of Fig. 3 concerns the initial gate voltage V_G ($V_G \geq 10$ V), which is intentionally selected. This starting point ensures that no free carriers are present to occupy the fabrication-induced trap states (referred to as trap #1). As a result, the initial trapped charge density for these states is set to zero, *i.e.*, $Q_{tL,1}(0) = 0$ C cm^{-2}. In contrast, the initial occupancy of trap #2, associated with unexpected traps introduced by environmental species, depends on external factors such as the concentration of environmental molecules and the effective device surface area exposed to ambient conditions. Consequently, the corresponding initial charge density, $Q_{tL,2}(0)$, and hence the observed open-loop hysteresis in the transfer curves of Fig. 3, are primarily influenced by these environmental conditions and are not expected to depend on the initial value of V_G.

As noted above, the different values of m_s and M_S extracted for the four transistors, which model the contact region, warrant further analysis. For practical reasons, M_S is assumed to be constant across all values of V_G. However, M_S can vary with V_G as shown in eqn (5). This simplification may lead to less accurate fits between calculations and experimental data, as seen in Fig. 2d (solid lines and symbols). Nevertheless, useful qualitative insights and qualitative information can still be gained from m_s and M_S. The value of m_s primarily reflects the concave or convex shape of the I_D–V_D curves. For $L = 2.5$ μm, $m_s = 1.75$ suggests a nearly quadratic I_D–V_S relation in the contact region, operating in the SCLC regime. For the other three transistors, $m_s < 1$, indicating convex shapes in the output characteristics (Fig. 2b–d). To compensate for the smaller m_s values in these cases, M_S decreases as L increases, as discussed in Section 4.1. The resulting I_D–V_S curves are represented by dashed red lines in Fig. 2a–d.

To refine our understanding of the contact region and improve agreement between calculations and experimental data, we proceed with an additional step: calculating the contact voltage V_S from eqn (2) as:

$$V_S = V_G - V_T - V_{SS} \times \ln\left[\exp\left(\frac{\left(\frac{I_D L'(\gamma+2)}{W\mu_0 C_{ox}} + V_{EODR}(V_{D'})^{(\gamma+2)}\right)^{\frac{1}{\gamma+2}}}{V_{SS}}\right) - 1\right]. \quad (16)$$

where I_D, V_G and $V_{D'} = V_D$ in eqn (16) are the experimental values. The values of the rest of parameters are in Table 1.

4.3.1 Experimental validation. The experimental I_D–V_S curves in Fig. 9a–d exhibit a distinct convex-to-concave transition as channel length increases, consistent with the evolution of m_s (transport-behavior constant) in Table 1. This transition arises from chemical modifications at the metal–organic interface, such as oxidation or environmental contamination, which alter the energy barrier for charge injection. These changes shift the dominant conduction mechanism from space-charge-limited transport (governed by bulk traps in the semiconductor) to Schottky-barrier-limited transport (dictated by interfacial traps).

Notably, the voltage drop across the source contact region remains consistent (~1–2 V) across all channel lengths (Fig. 9), underscoring its independence from device geometry and reinforcing the contact-limited nature of the transition. While minor irregularities in the curves reflect experimental noise inherent to direct data extraction, the overarching trend remains robust. This phenomenon mirrors observations in ammonia gas sensors,[41] where adsorbed gas molecules modulate interfacial barriers, inducing analogous curvature changes in I_D–V_S characteristics. Such parallels highlight the broader relevance of interfacial trap dynamics in organic and hybrid electronic systems, offering insights for designing stable, high-performance devices.

4.3.2 Broader implications. The insights gleaned from trap #2 dynamics extend far beyond the immediate scope of P3HT-based transistors, offering critical lessons for advancing the stability and performance of modern electronic devices. Device stability – a perennial challenge in organic electronics – is profoundly influenced by these interfacial traps. When organic transistors operate under ambient conditions, environmental species such as oxygen and moisture infiltrate the metal–semiconductor interface, amplifying trap #2 densities. This accelerates performance degradation through mechanisms like threshold voltage shifts and hysteresis, hallmarks of unstable charge injection.[90] To combat this, strategies such as encapsulation (*e.g.*, using atomic layer-deposited oxides to block environmental ingress) and interface engineering (*e.g.*, introducing self-assembled monolayers to passivate traps) emerge as viable solutions, directly informed by our understanding of trap #2 behavior.[91]

Further, the principles governing trap #2 are not confined to organic systems but apply to a broad spectrum of hybrid and emerging semiconductor technologies. For instance, in oxide-based TFTs (*e.g.*, InGaZnO), interfacial traps at dielectric–semiconductor boundaries similarly dictate bias-stress instability, a

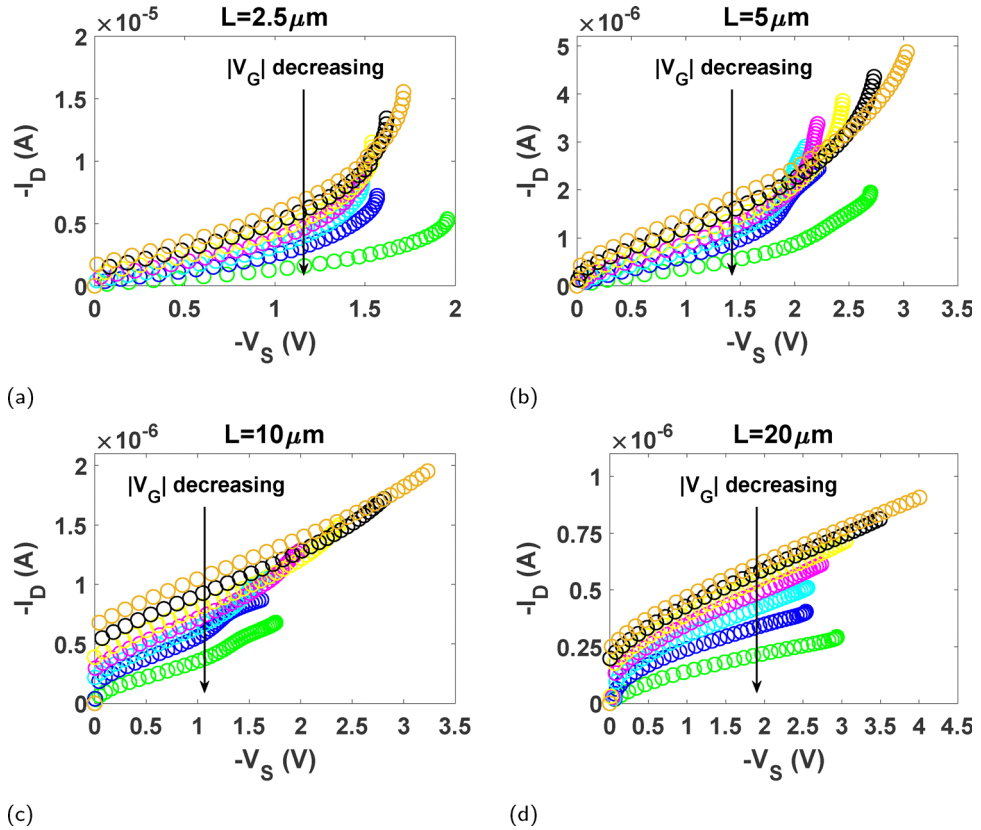

Fig. 9 (a)–(d) I_D–V_S curves at the contacts extracted from eqn (16), in which the experimental values of the P3HT based transistors with different channel lengths shown in Fig. 2, and the parameters of Table 1 are introduced.

critical concern in display electronics.[92] Likewise, perovskite transistors – a rising star in optoelectronics – suffer from ion migration and interfacial defect formation, phenomena that align seamlessly with our charge-trapping model.[93] Even in crystalline systems, where traps are less prevalent, the framework retains utility by simplifying to classical models under low-disorder conditions, bridging the gap between traditional and next-generation semiconductors.[25]

4.3.3 Applicability. We highlight the adaptability of our evolutionary parameter extraction procedure to accommodate unexpected phenomena, such as the presence of unanticipated traps. The experimental data analyzed in this work follows a typical measurement procedure that can be employed in any research or industrial laboratory. The applicability of our method is not restricted to P3HT–SiO_2 transistors. For instance, we applied our procedure to pentacene-based organic thin-film memory transistors with PMMA dielectric, enabling precise interpretation of hysteresis cycles in their electrical characteristics.[94]

4.3.4 Universality across disordered semiconductors. The framework supported by eqn (2) applies to organic, oxide, or hybrid semiconductors, addressing limitations of classical MOS models. Disordered materials exhibit gate-bias- and temperature-dependent mobility (due to the absence of band-like transport at room temperature)[95] and inherent contact resistance,[96] both of which are explicitly incorporated into our analysis.

4.3.5 Relevance to emerging technologies. Inorganic-based transistors (*e.g.*, oxide semiconductors) are highlighted for their low processing temperatures, high carrier mobility, and uniformity,[97–99] yet they face similar challenges in modeling charge transport.

4.3.6 Generalized charge-trapping dynamics. Time-dependent threshold voltage shifts [eqn (7), (12) and (14)] describe trapping-induced instabilities applicable to any charge-trap memory transistor.[98,100] Even crystalline systems benefit from this approach, as eqn (2) simplifies to the classical MOS model under conditions of negligible contact effects and constant mobility.

4.3.7 Final remarks. In hindsight, a few suggestions can be made to improve the characterization process. These suggestions include:

- Performing measurements in the sub-threshold region, though this is not strictly necessary.
- Measurements at different scan rates could aid in the characterization process.
- Possibly use slower scan rates that would reveal hysteresis in the output characteristics, though this would complicate the analysis as V_T and V_{SS} would vary over time.[43]
- Combining measurements from encapsulated and non-encapsulated transistors, or conducting measurements under varying environmental conditions (*e.g.*, reduced humidity or a nitrogen atmosphere), would also help in future characterization efforts.

• In this work, no additional time-dependent measurements were necessary to detect the traps. However, if traps with significantly different lifetimes were present, the additional transient current measurements in response to voltage pulses would be required.[51]

5 Conclusions

A novel approach to analyzing the current characteristics in OTFTs was proposed, emphasizing the importance of important details to extract information about traps. This approach employs an evolutionary parameter extraction procedure, based on a compact model that evaluates the drain current and accounts for the dynamic evolution of both the threshold voltage and trapped charge density in OTFTs. The procedure was tested using current characteristics with hysteresis measured in P3HT-based transistors with varying channel lengths.

By analyzing the time evolution of the threshold voltage during the voltage sweep in the transfer characteristics, we were able to detect the presence of different types of traps. Typical hysteresis loops in the transfer characteristics were attributed to traps created during the fabrication process, with a concentration that remains independent of the channel length. In contrast, anomalous loops observed in the experimental data were interpreted as arising from a second type of trap. The number of trapped charges and their variation associated with this second type of trap both depend on the channel length and exhibit a linear relationship. This suggests that these unexpected traps originate from environmental species (*e.g.*, adsorbed water or oxygen), being absorbed into different volumes of the semiconductor and resulting in varying trapped charge densities.

Author contributions

J. A. Jiménez-Tejada: writing – review & editing, writing – original draft, validation, supervision, project administration, methodology, investigation, conceptualization. A. Romero: writing – review & editing, writing – original draft, visualization, software, methodology, formal analysis, data curation. S. Mansouri: data curation, methodology, resources, supervision, validation, visualization, writing – review & editing. M. Erouel: data curation, resources, supervision, validation, visualization. L. El Mir: data curation, resources, supervision, validation, visualization. M. J. Deen: writing – review & editing, validation, investigation.

Data availability

The data supporting this article have been included as part of the ESI.†

Conflicts of interest

There are no conflicts to declare.

Appendix A: evolutionary parameter extraction procedure

This appendix introduces an advanced fitting technique based on an evolutionary procedure. It is designed to reduce the workload of the expert or decision maker (DM) during parameter extraction. This method has been successfully applied to the characterization of thin-film transistors (TFTs) in both static[41,42,59,85,101,102] and dynamic regimes, including current transients and hysteretic current characteristics.[43] The analyses are conducted using the open-source evolutionary tool ECJ (A Java-based Evolutionary Computation Research System).[103] In this work, the evolutionary parameter extraction procedure is adapted to extract trap-related information from transfer characteristics with hysteresis, as well as from abnormal behavior observed at low gate voltages (loop-2). The key steps of the adapted procedure are outlined in the following subsections.

A.1 Individual representation (set of fitting parameters)

The evolutionary procedure defines the ''individual'' of the population, denoted by x, which represents the set of fitting parameters necessary to calculate all equations in the model (2), (3), (10), (11), (13) and (15):

$$x = \left(\mu_0, \gamma, V_{\mathrm{T}}(0), V_{\mathrm{SS}}(0), m_{\mathrm{s}}, M_{\mathrm{S}}, V'_{\mathrm{A}}, Q_{tL,r}(0), \beta_r, \tau_r\right). \quad (17)$$

Here, $r = 1,\ldots,n_{\mathrm{traps}}$; n_{traps} represents the various trap types or total number of traps; and $V'_{\mathrm{A}} = 1/(\lambda L)$ is the early voltage per unit length. The terms $V_{\mathrm{T}}(0)$ and $V_{\mathrm{SS}}(0)$ correspond to the initial values of $V_{\mathrm{T}}(t)$ and $V_{\mathrm{SS}}(t)$ for a specific experiment.

A.2 Measurement discretization and timing

Initially, the experimental I_{D} data, measured during the output or transfer characteristics, must be linked to the time instances t_j at which each measurement is taken. Specifically, $I_{\mathrm{D}} = I_{\mathrm{D}}(V_{\mathrm{G}}(t_j),V_{\mathrm{D}}(t_j))$, where $j \in \mathbb{Z}$, with $1 \leq j \leq t_N$, and t_N represents the total number of discrete time values. The measurement protocol is as follows:

(1) Transfer characteristics:

• $V_{\mathrm{D}} = -30$ V

• $V_{\mathrm{G}}(t_j) = V_{\mathrm{G}}(t_{j-1}) \pm \mathrm{SR} \times (t_j - t_{j-1})$, where SR = 1000 mV s^{-1} and $(t_j - t_{j-1})$ = 100 ms.

The positive sign corresponds to the forward sweep (FS) (sweeping $-V_{\mathrm{G}}$ from -10 to 18 V), while the negative sign corresponds to the backward sweep (BS) (sweeping $-V_{\mathrm{G}}$ from 18 to -10 V).

(2) Output characteristics:

• $V_{\mathrm{D}}(t_j) = V_{\mathrm{D}}(t_{j-1}) + \mathrm{SR} \times (t_j - t_{j-1})$ with $-V_{\mathrm{D}} \in [0,40]$ V

• V_{G} remains fixed at values such as 0 V, -4 V, -8 V, -12 V, -16 V, -20 V, or -24 V.

• SR and $(t_j - t_{j-1})$ can vary, as no hysteresis is detected.

• V_{G} is held for several seconds at $V_{\mathrm{D}} = 0$ V to stabilize the trapped charge, and then V_{D} is swept with a large SR.

The numerical estimation of I_{D}, calculated using our model (2), (3), (10), (11), (13) and (15), is denoted by $\widehat{I_{\mathrm{D}}}\left[V_{\mathrm{G}}(t_j), V_{\mathrm{D}}(t_j), x\right]$.

A.3 Fitness function

The evolutionary parameter extraction procedure is applied independently to each of the four transistors with varying channel lengths. For each case, it solves a multi-objective optimization problem (MOP)[85] with two objectives

- O_1: output characteristics
- O_2: transfer characteristics

Both objectives aim to minimize the error O_k, where $k = 1, 2$, between the experimental values $I_D = I_D(V_G(t_j),V_D(t_j))$ and the model-based estimations $\widehat{I_D}[V_G(t_j), V_D(t_j), x]$.

The normalized root mean squared error (NRMSE) is used to quantify the errors for both objectives:[104]

$$\mathrm{NRMSE}(y,\hat{y}) = \sqrt{\frac{\sum_{z=1}^{w}(y_z-\hat{y}_z)^2}{\sum_{z=1}^{w}(y_z-\bar{y})^2}}, \tag{18}$$

where y represents the data set to accurately approximate, $\hat{y}$ is its estimate, w is the number of data points, and $\bar{y}$ is the mean value of the complete data set y.

Thus, our MOP, denoted as O, is defined as $O = (O_1,O_2)$, where

$$O_k(x) = \mathrm{NRMSE}\Big(I_D(V_G(t_j), V_D(t_j)), \widehat{I_D}[V_G(t_j), V_D(t_j), x]\Big), \quad k = 1, 2. \tag{19}$$

These objectives ensure that we accurately reproduce the experimental I_D–V_D and I_D–V_G curves by optimizing the parameters encoded in x within the model.

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