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Impact of hydrogen-controlled thermal ALD SiO_2 insulators on IGZO channel FETs to optimize the electrical performance†

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Oxide semiconductors (OS) are attractive materials for 3D device applications such as monolithic stacked, channel-all-around, and gate-all-around structures, owing to their low off-current, high field-effect mobility, 3D processability, and superior large-area uniformity. However, the electrical and reliability properties of OS channel field effect transistors (FETs) are sensitively affected by gate insulator (GI) conditions, such as hydrogen content. For this reason, a silicon dioxide (SiO_2) GI was generally fabricated under sufficient atomic layer deposition (ALD) reaction conditions, such as high deposition temperature, ozone reactant density, or oxygen plasma, to reduce the hydrogen content. However, higher oxidation conditions of ALD reactants lower the conductivity of the IGZO channel at a top-gate FET. Herein, we propose optimizing the properties of FETs by lowering the hydrogen content of a low-temperature deposited thermal ALD SiO_2 GI using a post-annealing process. Furthermore, the effects of hydrogen as a mobile ionic charge are presented. The 250 °C deposited SiO_2 gate insulator FET exhibits a high field-effect mobility of 21.1 $cm^2\ V^{-1}\ s^{-1}$, threshold voltage of 0.4 V, and subthreshold swing of 100 mV dec^{-1} with superior stabilities of −0.19 and +0.25 V shift during positive and negative-bias stress, respectively, by lowering the hydrogen content.

1. Introduction

The oxide semiconductor (OS) represented by IGZO (In–Ga–Zn–O) has significant advantages as a channel layer in field-effect transistors (FETs) of flat-panel displays, sensors, complementary FETs, and memory devices because of their attractive properties such as reasonable field-effect mobility (μ_{FE} > 10 $cm^2\ V^{-1}\ s^{-1}$), large-area uniformity, extremely low off-current (<10^{-18} μA μm^{-1}), and 3D structure processability.[1–10] 3D processability of the OS is desirable for next-generation scaled FETs, such as monolithic stacked, channel-all-around, and gate-all-around structures.[11–14] Various deposition methods, such as physical vapor deposition (PVD), chemical vapor deposition (CVD), sol–gel, and atomic layer deposition (ALD), have been reported for the fabrication of the OS on various substrates.[15–20] The ALD method has advantages for OS deposition in precise thickness control, superior step coverage at high step coverage, and large-scale uniformity.[21,22] Choi *et al.* fabricated a 3 nm thick In_2O_3 channel FET with superior electrical and reliability properties using ALD by controlling the deposition temperature and crystalline orientation.[10] Furthermore, Kim *et al.* achieved a high mobility (~114.31 $cm^2\ V^{-1}\ s^{-1}$) IGZO-channel FET by emulating a single crystal-like structure with excellent (>90%) step coverage at a 5.5 : 1 aspect ratio using ALD process condition modulation.[23]

Research on optimizing the ALD process of the gate insulator (GI) is also required to improve the electrical and reliability properties of OS-channel FETs. The charge trap density of the insulator degrades the reliability of an FET by trapping electron carriers at the interface and in the bulk of the insulator.[20,24] Furthermore, hydrogen and carbon impurities in the GI affect the electrical properties and density of state of the OS by diffusing into the channel during the deposition and post-annealing processes.[25,26] Significantly, the GI effect on the FET is more dominant in top-gate (TG) structure FETs because the GI deposition process is performed above the channel layer,

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and the post-annealing process is conducted with the channel and GI layers stacked.[27,28] However, TG FETs have advantages over bottom-gate (BG) FETs, such as a 3D structure, because the GI of the TG FET acts not only as the dielectric but also as the passivation layer, which requires long-term durability and a stacked structure. Consequently, research on the hydrogen impurity diffusion effect of the GI and the optimization of TG FET is essential.

Kim *et al.* reported that the trap density and hydrogen content of the GI affect the electrical properties and reliability of FETs by trapping or generating free electrons.[29] The authors proposed a stacked heterostructure GI composed of Al_2O_3 and SiO_2 to optimize FET properties by controlling the trapping and impurity effects. Furthermore, Kim *et al.* achieved superior positive-bias temperature stress reliability test results (threshold voltage (V_{th}) shift after ten years: −0.01 V under 2 MV cm^{-1} gate field stress and 120 °C) by increasing the Al_2O_3 deposition temperature and lowering carbon impurities to minimize the impurity effect for the OS-channel layer.[20]

Among GI materials, silicon dioxide (SiO_2) exhibits superior physical and chemical properties such as scratch resistance, hardness, chemical inertness, high dielectric strength (>10 MV cm^{-1}), and a large bandgap (~8.9 eV).[29–31] However, ALD-deposited SiO_2 films contain hydrogen impurities due to the chemical reaction route and mechanism, especially for amine ligand silicon precursors such as 1,2-bis(diisopropylamino) disilane (BDIPADS), diisopropylaminosilane (DIPAS), di-*sec*-butylaminosilane (DSBAS), and bis(*t*-butylamino)silane (BTBAS).[32–34] The SiO_2 ALD mechanism involves the following steps: (1) precursor adsorption *via* hydrogen bonding (Si–H); (2) oxidation and ligand exchange reactions from hydrogen (Si–H) to hydroxyl (Si–OH); and (3) precursor adsorption by eliminating hydrogen (Si–O–Si–H). However, in the case of insufficient oxidation reactions, hydrogen impurities can remain in the SiO_2 films. Consequently, SiO_2 deposition is generally conducted under suitable oxidation conditions, such as high temperatures and reactant reaction energies (*e.g.*, ozone density or plasma power).

However, sufficient GI oxidation deposition conditions highly degrade the electrical properties of the IGZO channel layer. It is desirable that the deposition temperature of SiO_2 is below 400 °C because the carrier concentration of IGZO decreases at ozone-exposed temperatures, and Zn desorption occurs above 400 °C.[35,36] The high reactant reaction energies also degrade the electrical properties of IGZO channel FETs. Oh *et al.* reported that the ozone-exposed IGZO channel FET was excessively deactivated, along with increasing hysteresis in the transfer curve, because ozone increases oxygen interstitials (O_i) and decreases carrier concentration due to the contribution of O atoms to the V_O sites of IGZO by the excess oxygen source.[37] Consequently, a study is needed to optimize the electrical properties of IGZO channel TG FETs under the low oxidation conditions of GI deposition for 3D structured scaled next-generation FET application. In this study, we optimize the electrical (V_{th}: 0.4 V, μ_{FE}: 21.1 cm^2 V^{-1} s^{-1}, hysteresis: 0.07 V, S. S.: 100 mV dec^{-1}) and reliability (+0.25 and −0.19 V V_{th} shifts during 3 h at ±1 MV cm^{-1}) properties of the OS-channel TG FET by lowering the hydrogen content by controlling the post-annealing and GI deposition conditions.

2. Results and discussion

Fig. 1 shows the SiO_2 film analysis results in terms of the growth per cycle (GPC), refractive index (RI), current density, and dielectric constant with respect to the deposition temperature. The GPC results show that the ALD process window is above 250 °C, yielding similar GPC values originating from the self-limiting reaction (Fig. 1(a)). The breakdown voltage was increased (10.4, 11.6, 11.7, and 12.0 MV cm^{-1}), whereas dielectric constant values decreased (4.4, 4.3, 4.3, and 4.1) with the deposition temperature (250, 300, 350, and 400 °C), as shown in Fig. 1(b) and (c). Impurities, such as carbon, nitrogen, potassium, and sodium, were not detected in the SiO_2 films within the ALD window (Fig. S1, ESI†). The enhancement of the insulating properties of SiO_2 with the deposition temperature could originate from the complete reaction of the precursor surface adsorption and oxidation with increasing thermal energy.[32,33]

To evaluate the film density and binding state of SiO_2, XRR and XPS analyses were performed, as shown in Fig. 2. The film density increased from 2.03 to 2.16 g cm^{-3} for an increase in the SiO_2 deposition temperature from 250 to 400 °C (Fig. 2(a)). Furthermore, the incomplete oxidation binding state area fraction of SiO_2 films (Si^{x+}) decreased with increasing SiO_2 deposition temperature; 7.9, 5.2, 2.8, and 0% for deposited at 250, 300, 350, and 400 °C, respectively. The Si 2p XPS spectra were deconvoluted into two subpeaks according to the NIST database version 5.0. The binding energy of the complete (Si^{4+}) and incomplete (Si^{x+}, especially Si^{2+}) oxidation states of silicon oxide were 103.8 ± 0.1 and 102.2 ± 0.1 eV, respectively.[38] According to a previously reported ALD deposition mechanism, the decrease in the incomplete oxidation state of silicon oxide with increasing deposition temperature is reasonable. Nam *et al.* reported that the GPC, density, and O/Si ratio of SiO_2 increased with the deposition temperature because the incorporation of a hydrogen-related group of films decreased due to the reaction between surface adsorbate species and was nearly complete at higher temperatures.[32] And hydrogen related oxygen binding area fraction decreased slightly with SiO_2 deposition temperature; 17.3, 16.0, 16.2, and 13.5% for deposited at 250, 300, 350, and 400 °C, respectively. The O 1s XPS spectra were deconvoluted into two subpeaks. The binding energy of Si–O and Si–OH were

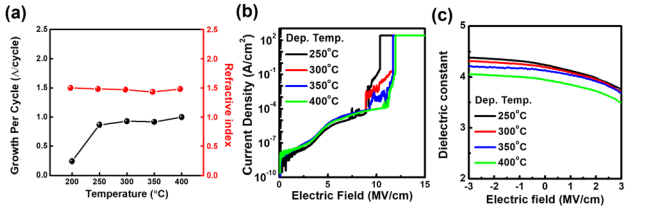

Fig. 1 (a) The GPC and RI results of SiO_2 films according to the SiO_2 deposition temperature. The dielectric properties result from (b) current density and (c) dielectric constant at the MIM diode according to the electric field.

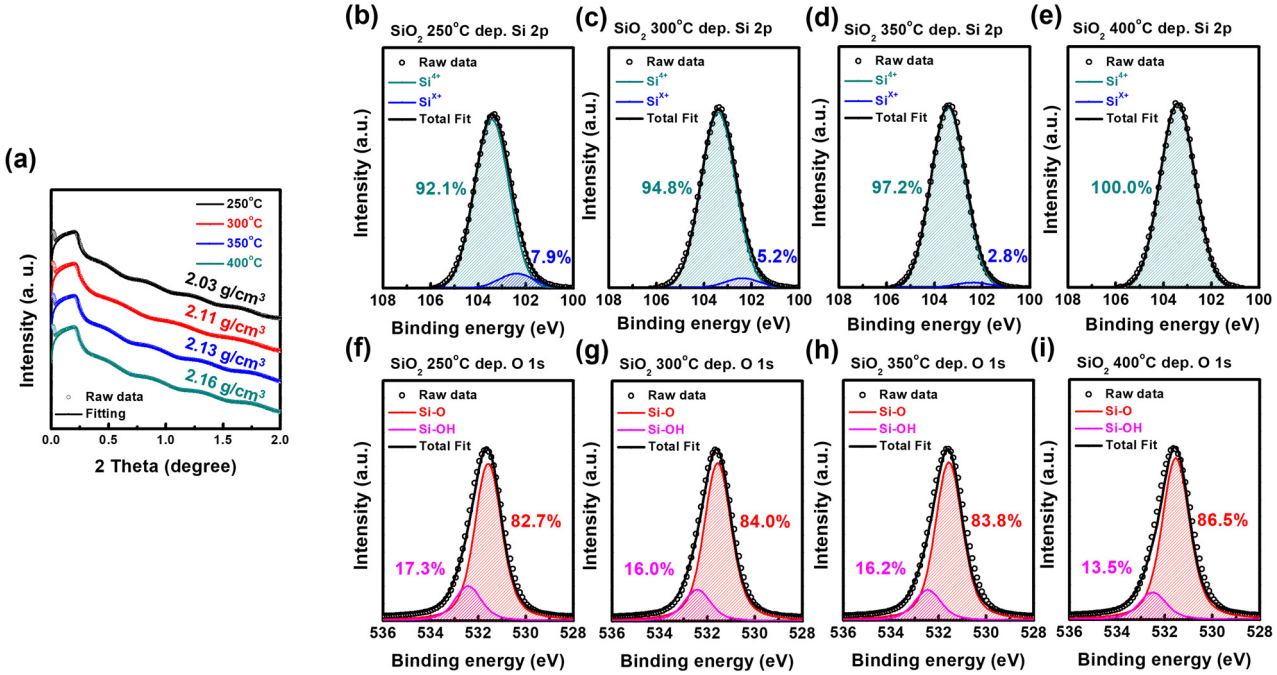

Fig. 2 (a) XRR measurement and fitting results for extracted film density (inlet) and XPS deconvolution results of silicon and oxygen binding state at a SiO_2 deposition temperature of (b) and (f) 250, (c) and (g) 300, (d) and (h) 350, and (e) and (i) 400 °C.

531.6 ± 0.1 and 532.3 ± 0.1 eV, respectively.[38,39] However, above 10% of the hydrogen-related oxygen binding area percentage was maintained even at 400 °C SiO_2 deposition temperature. This result indicates that an additional post-annealing process is needed to reduce the hydrogen content of SiO_2 GI and optimize the electrical properties of IGZO channel FETs. Consequently, Fig. 1 and 2 show that the SiO_2 film properties such as the breakdown voltage, dielectric constant, density, and binding state are superior at higher deposition temperatures, originating from the complete ALD reaction and oxidation.

Fig. 3(a)–(d) shows the *I*–*V* transfer curves of IGZO-channel TG FETs at different SiO_2 GI deposition temperatures. The post-annealing process was not conducted after FET fabrication. Except for the SiO_2 deposition temperature, the process conditions of the FET, such as the IGZO cation ratio, deposition temperature, and electrode material, were the same. The transfer curve of the FET exhibited a counterclockwise hysteresis independent of the SiO_2 deposition temperature. The mobile ionic charge and electrical dipoles of GI possibly result in the counterclockwise hysteresis of the FET.[40] Here, the mobile ionic charge of the GI has the potential to cause counterclockwise hysteresis because SiO_2 has a low dielectric constant of approximately four and is not a ferroelectric material. In general, hydrogen, potassium, lithium, and sodium ions act as mobile ionic charges.[41] Hydrogen impurities in SiO_2 are a potential reason for the counterclockwise hysteresis of the FET because potassium and sodium were not detected by XPS analysis (Fig. S1, ESI†). The trend of the hysteresis values on SiO_2 deposition temperature is similar to the trend of the hydrogen-related binding area percentage, as shown in Table 1 and Fig. 2(f)–(i). Hydrogen impurities in SiO_2 and optimization of the electrical properties are discussed later. Increasing the deposition temperature of the SiO_2 GI of the FET lowered the on-current, and V_{th} showed a positive shift. These results indicated that the electrical properties of the IGZO channel were affected by the SiO_2 deposition process. Fig. 3(e)–(h) presents the XPS O 1s peak deconvolution results for the bonding state of oxygen in IGZO. XPS analysis was conducted on the SiO_2 (10 nm)/IGZO (50 nm) stacked structure and the SiO_2 layer was Ar ion-etched before the analysis. The XPS depth profile was conducted to define the IGZO bulk region to deconvolution, as shown in Fig. S2 (ESI†). The XPS O 1s peak of IGZO was deconvoluted into three subpeaks: metal and oxygen binding (M–O), oxygen deficiency (O_{def}), and hydrogen-related binding (O–H), which corresponded to 529.8 ± 0.1, 531.1 ± 0.1, and 532.1 ± 0.1 eV, respectively.[22] The percentage of O_{def} and O–H peak area decreased with the SiO_2 deposition temperature increase because of the ozone exposure and post-annealing effect during the SiO_2 GI deposition.[42,43] This indicated that the conductivity of IGZO was lowered by the reduction of oxygen vacancy and hydrogen-related bonding, which generated electron carriers during ozone exposure and the reaction during SiO_2 deposition.[22,44] Consequently, although the film quality of the SiO_2 dielectric was improved by increasing the deposition temperature, the conductivity of IGZO was degraded by ozone exposure during deposition.

To improve the hysteresis voltage of the FET, a post-annealing process was conducted at 500 °C in an Ar atmosphere for 1 h to reduce the hydrogen content in SiO_2. The electrical parameters extracted from the *I*–*V* transfer curves of the as-deposited and post-annealed FET are summarized in Table 1. The output curves are presented in Fig. S3 (ESI†). Fig. 4(a)–(d) show that the counterclockwise hysteresis was improved in the post-annealed

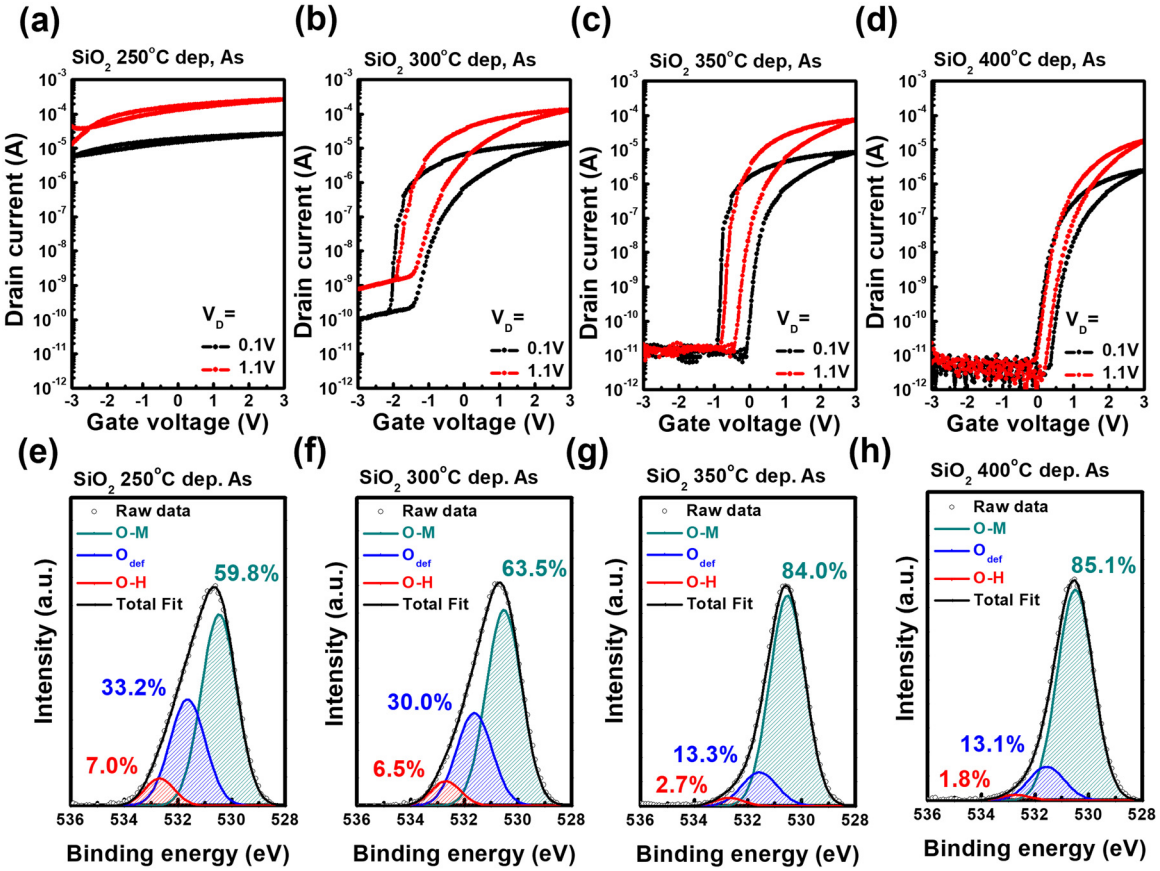

Fig. 3 (a)–(d) *I*–*V* transfer curves of FETs and (e)–(h) XPS O 1s peak deconvolution results of IGZO in SiO_2/IGZO stacked films according to the SiO_2 deposition temperature; (a), (e) 250, (b), (f) 300, (c) and (g) 350, and (d) and (h) 400 °C, respectively. The post-annealing process was not conducted.

Table 1 Electrical properties summary of IGZO channel FETs according to SiO_2 GI deposition temperature and with and without the post-annealing process

SiO_2 dep. Temp.	250 °C		300 °C		350 °C		400 °C	
Post process	As	Anneal.	As	Anneal.	As	Anneal.	As	Anneal.
V_{th} [V]	N/A	0.4 ± 0.1	−2.0 ± 0.1	0.2 ± 0.1	−1.0 ± 0.1	0.1 ± 0.1	0.5 ± 0.1	0.2 ± 0.1
μ_{FE} [$cm^2\ V^{-1}\ s^{-1}$]	N/A	21.1 ± 1.2	69.3 ± 9.1	19.0 ± 1.1	53.5 ± 0.5	18.4 ± 0.2	19.9 ± 1.9	17.4 ± 0.5
Hysteresis [V]	N/A	0.07 ± 0.01	1.77 ± 0.02	0.22 ± 0.03	0.82 ± 0.02	0.35 ± 0.01	0.56 ± 0.02	0.60 ± 0.08
Mobile ionic charge density [cm^{-2}]	8.0×10^{11}	5.5×10^{10}	6.6×10^{11}	1.4×10^{11}	4.2×10^{11}	2.1×10^{11}	4.1×10^{11}	4.1×10^{11}
S.S. [V dec^{-1}]	N/A	0.10 ± 0.01	0.13 ± 0.05	0.14 ± 0.01	0.09 ± 0.04	0.13 ± 0.01	0.11 ± 0.02	0.14 ± 0.02

FETs, regardless of the SiO_2 deposition temperature. However, more than 1 V of hysteresis was still exhibited except for the 250 °C SiO_2 deposited FET. The μ_{FE} decreased with the SiO_2 deposition temperature because of the decreasing IGZO conductivity; 21.1, 19.0, 18.4, and 17.4 $cm^2\ V^{-1}\ s^{-1}$ for deposited at 250, 300, 350, and 400 °C, respectively. Consequently, whereas the SiO_2 film properties improved with the deposition temperature, the electrical properties of the post-annealed FET were superior at lower temperatures. As shown in Fig. S4 (ESI†), the optimal annealing temperature was 500 °C. The post-annealing process significantly decreases the on-current. The 200 °C deposited SiO_2 GI FETs exhibit inferior electrical properties compared to 250 °C deposited SiO_2 GI FETs because the 200 °C is not within the ALD process window (Fig. S5, ESI†). XPS analysis was conducted on the SiO_2/IGZO structure after post-annealing to observe the oxygen-binding state of IGZO, and the results are shown in Fig. 4(e)–(h). The O_{def} binding percentage decreased with increasing SiO_2 deposition temperature, a trend similar to that observed for the as-deposited films. However, the O_{def} binding percentages were lower than those of the as-deposited films, regardless of the SiO_2 deposition temperature. Because the post-annealing atmosphere was argon, the increased M–O binding of IGZO could have originated from the insertion of oxygen-related molecules during SiO_2 reduction or reaction with ozone.

To confirm the origin of the counterclockwise hysteresis of the SiO_2 GI FET, the ionic mobile charge density (Q_M) was extracted from the charge-pumping BTS method by measuring the difference of flat-band voltage after the bias stress (the

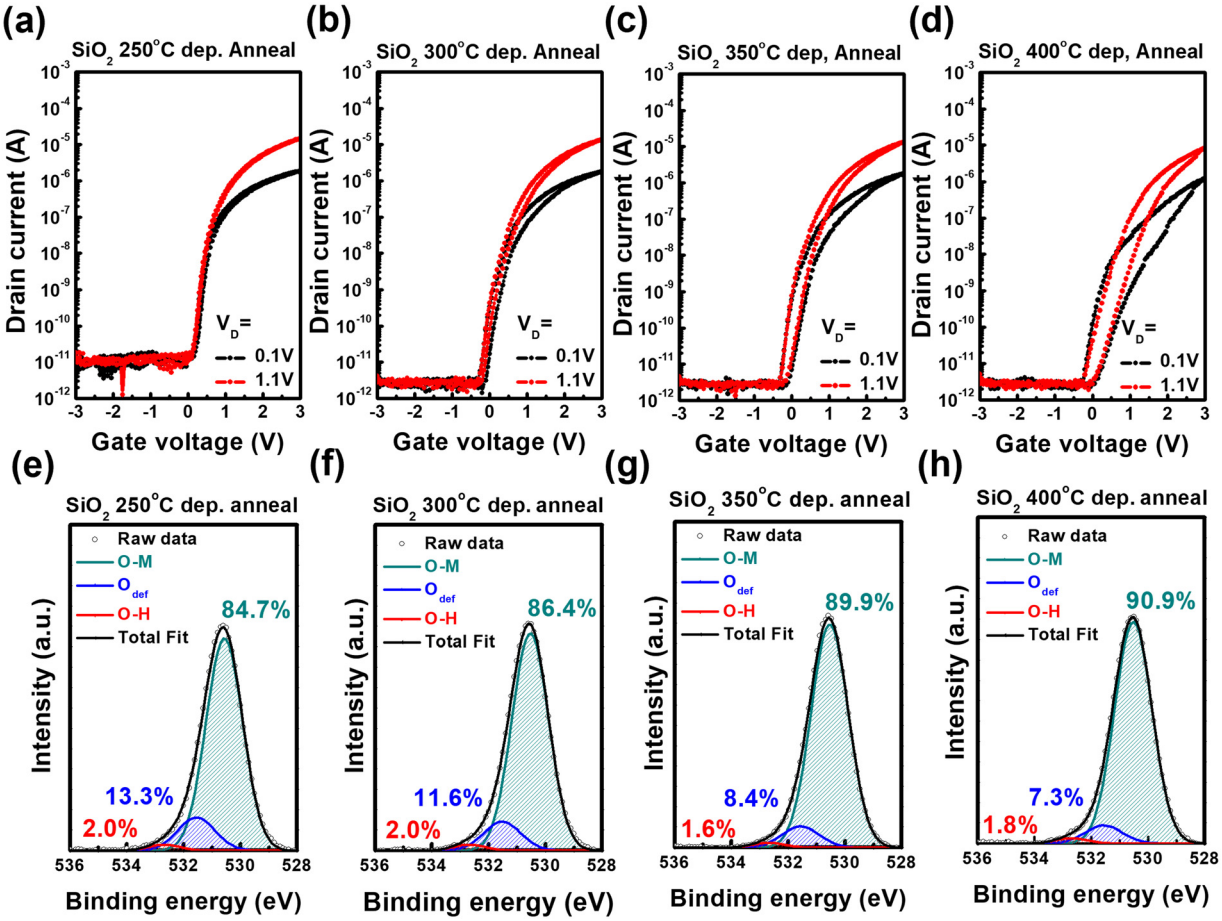

Fig. 4 (a)–(d) *I*–*V* transfer curves of FET and (e)–(h) XPS O 1s peak deconvoluting results of IGZO in SiO_2/IGZO stacked films according to the SiO_2 deposition temperature; (a) and (e) 250, (b) and (f) 300, (c) and (g) 350, and (d) and (h) 400 °C, respectively. Post-annealing was conducted at 500 °C in an Ar atmosphere for 1 h.

temperature and stress were 200 °C and ±1 MV cm^{-1}, respectively). The *C*–*V* measurements were conducted in the MOS region of TG FET, as shown in Fig. 5(a). The calculated dielectric constant results measured at 1000 Hz of frequency and used to extract the electrical properties of FETs are presented in Fig. S6 (ESI†). Compared to the results shown in Fig. S6 (ESI†), it was confirmed that a flat-band voltage difference occurred owing to the ionic mobile charge. Interestingly, the trend of Q_M corresponded to the hysteresis trend of the FETs (Fig. 5(b)–(i)); Q_M decreased with the SiO_2 deposition temperature in the as-deposited films, whereas the opposite trend was observed for the post-annealed films. Furthermore, the Q_M values decreased significantly after post-annealing, independent of the SiO_2 deposition temperature. This result indicates that a counterclockwise hysteresis occurs owing to the mobile ionic charge originating from the hydrogen content of SiO_2.[45]

A D-SIMS depth profile analysis was conducted to compare the hydrogen intensities of SiO_2 and IGZO in terms of the GI deposition temperature. As shown in Fig. 6, the hydrogen content of IGZO as-deposited increased with a decrease in the SiO_2 deposition temperature. Because the IGZO fabrication conditions, such as deposition temperature and ozone density, were equal, the different hydrogen contents of IGZO would originate from the diffusion by SiO_2. The hydrogen content coincided with the trend of the mobile ionic charge density of SiO_2 and the counterclockwise hysteresis of the FET after the post-annealing process. This confirmed that the hydrogen content of SiO_2 acted as a mobile ionic charge and increased the counterclockwise hysteresis. Interestingly, more hydrogen content of SiO_2 and IGZO diffuses out at lower SiO_2 deposition temperatures during the post-annealing process; the hydrogen reduction percentages of SiO_2 and IGZO were 48.7% and 63.9%, 21.4% and 58.8%, 4.0% and 51.1%, and 4.4% 21.1% at a SiO_2 deposition temperature of 250, 300, 350, 400 °C, respectively. Because hydrogen from SiO_2 and IGZO diffuses out through the SiO_2 films, the hydrogen reduction percentage differences possibly originate from the quality of the SiO_2 film, such as its density. Fig. S8 (ESI†) shows that the reduction of SiO_2 did not occur during the post-annealing process. The hydrogen contents of SiO_2 are presented in Fig. S9 (ESI†). Furthermore, as shown in Fig. S10 (ESI†), the hydrogen atomic density trend according to the deposition temperature and post-annealing process of SiO_2 films was double-checked by RBS and ERD analysis.

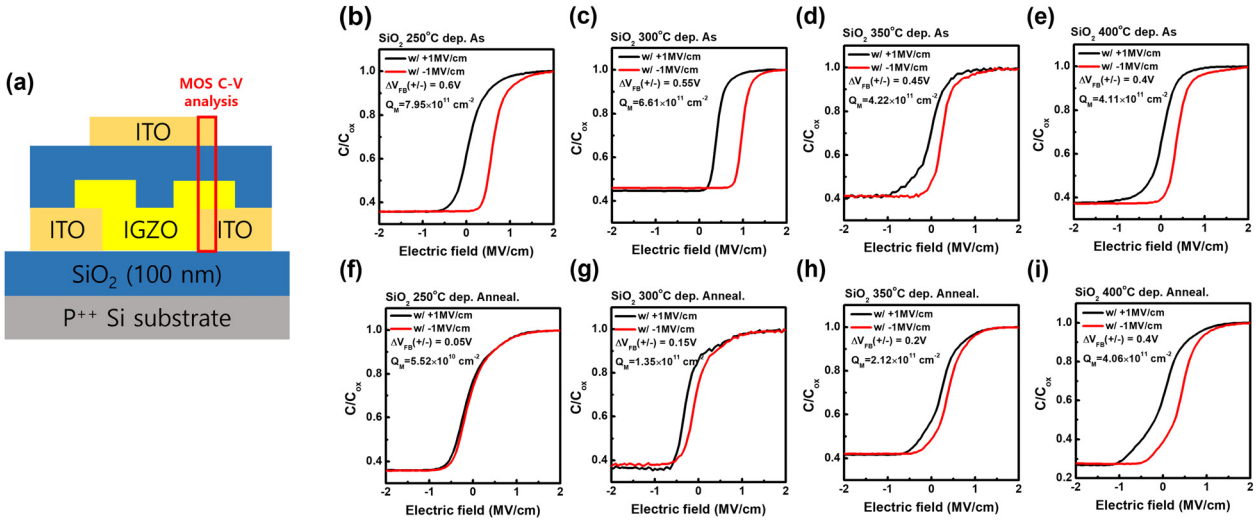

Fig. 5 (a) Schematics of the TG FET and MOS C–V analysis using the charge-pumping BTS technique. The C–V analysis results and extracted ionic mobile charge density for as-deposited and post-annealed FETs according to a SiO_2 deposition temperature of (b) and (f) 250 °C, (c) and (g) 300 °C, (d) and (h) 350 °C, and (e) and (i) 400 °C.

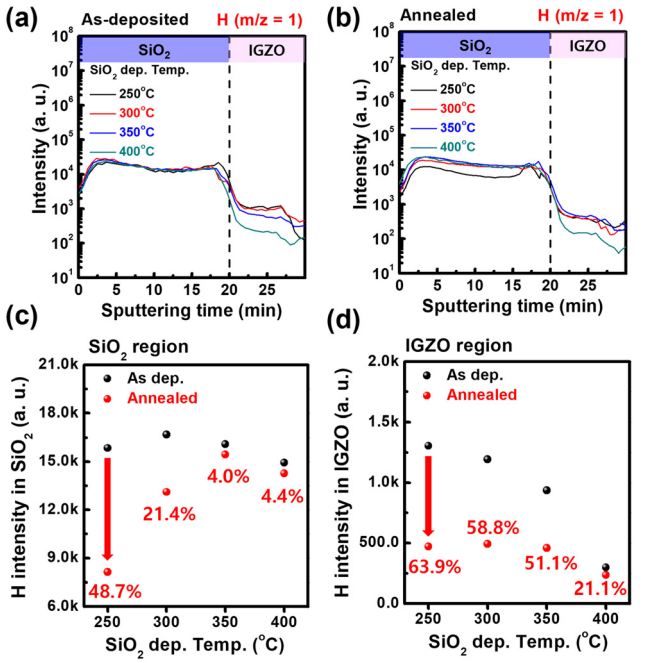

Fig. 6 D-SIMS depth profiles of hydrogen intensity for (a) as-deposited and (b) annealed SiO_2/IGZO films according to the SiO_2 deposition temperature. Hydrogen intensity results of the (c) SiO_2 and (d) IGZO regions.

Because the mobile ionic charge and hydrogen content of the GI degraded the reliability properties of the FET, positive- and negative-bias stress (PBS and NBS, respectively) reliability tests were conducted at 0.1 V of V_{DS}. The transfer curves and V_{th} shift values are presented in Fig. 7 and Fig. S11 (ESI†). The V_{th} shifts of PBS (1 MV cm^{-1}) and NBS (−1 MV cm^{-1}) at 3 h were −0.19 and +0.25 V, −0.45 and +0.45 V, −0.50 and +0.49 V, and −0.56 and +0.49 V at SiO_2 deposition temperatures of 250, 300, 350, and 400 °C, respectively. An abnormal negative V_{th} shift during PBS originated from the electron carrier generation by hydrogen diffusion to the channel.[46] And an abnormal positive V_{th} shift during NBS originated from the hydrogen mobile ionic charge migration to the gate electrode.[47]

The V_{th} shift increased with the SiO_2 deposition temperature because the hydrogen content of the post-annealed SiO_2 increased with the deposition temperature. Consequently, considering not only the GI film quality but also the hydrogen content trend during the post-annealing process is necessary for optimizing the properties of the transistor. It is because the hydrogen content of GI can affect the electrical and reliability properties by acting on the ionic mobile charge trap density and film quality such as density affects the hydrogen diffusion.

3. Conclusions

In this study, we optimized the electrical and reliability properties of an IGZO-channel TG FET by controlling the hydrogen content of SiO_2. The film quality of the as-deposited SiO_2, including the breakdown voltage, dielectric constant, density, binding state, and hydrogen impurity content, increased with increasing deposition temperature. However, the conductivity of IGZO decreased with increasing SiO_2 deposition temperature because of the reaction with ozone and lowering of the oxygen vacancy state, which generates carriers during deposition. Because the hydrogen content of SiO_2 acts as a mobile ionic charge trap, which degrades the FET properties, a post-annealing process is required. The percentage of diffused-out hydrogen decreased with the SiO_2 deposition temperature. The 250 °C deposited SiO_2 GI FET exhibits a high μ_{FE} of 21.1 cm^2 V^{-1} s^{-1}, V_{th} of 0.4 V, and S. S. of 100 mV dec^{-1} with a superior stability of −0.19 and +0.25 V shift during PBS and NBS at 1 MV cm^{-1} stress conditions for 3 h by lowering the hydrogen content. These results show that considering the

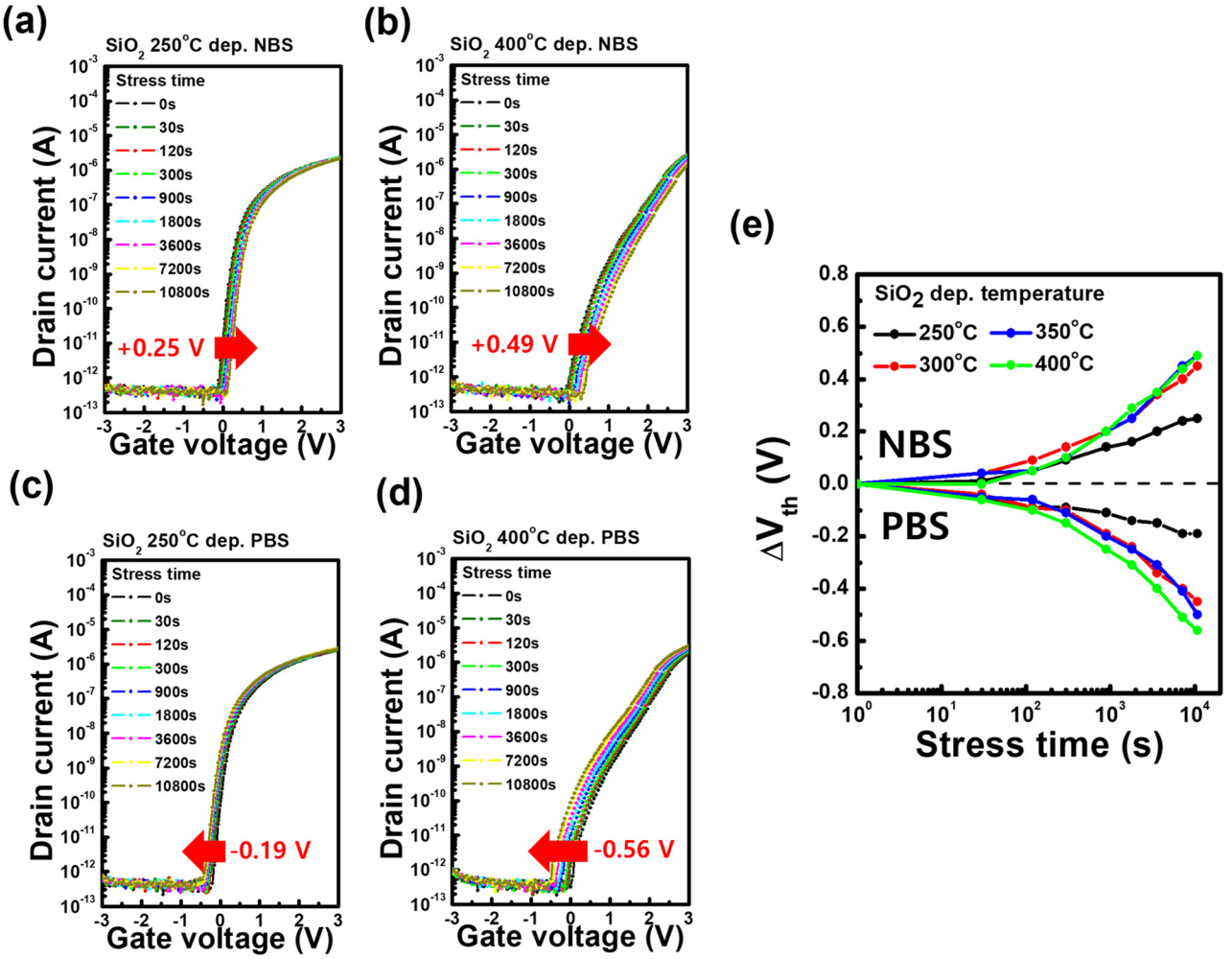

Fig. 7 Transfer characteristics and V_{th} shift values during the P(N)BS reliability tests for the (a) and (c) 250 and (b) and (d) 400 °C SiO_2 deposited FETs. (e) V_{th} shift values according to the SiO_2 deposition temperature and stress time.

effect of each layer, such as channel and GI, is more significant than considering the properties of a single layer itself.

4. Experimental

4.1. Thin-film fabrication and characterization

The IGZO active layer and SiO_2 gate electric films were deposited *via* ALD using ozone with a 200 g m^{-3} density as the reactant. The deposition temperature of the IGZO was 250 °C. (3-Dimethylaminopropyl)dimethyl indium (DADI) heated to 45 °C, trimethylgallium (TMGa), and diethylzinc (DEZ) were used as the indium, gallium, and zinc precursors, respectively. The super-cycle of the IGZO cations was 1 : 1 : 1. The SiO_2 deposition temperature was varied from 200 to 400 °C in 50 °C intervals, and BTBAS was used as a silicon source. The purge gas was argon and the working pressure was maintained at 1.2 mTorr using a throttle valve. The thickness and refractive index (RI) of the films were measured using a spectroscopic ellipsometer (Elli-SE(UV)-FM8, Ellipso Technology). X-ray photoelectron spectroscopy (XPS, K-Alpha$^+$, Thermo Fisher Scientific) was used to investigate the presence of carbon, nitrogen, potassium, and sodium impurities and the ratio of the metal and oxygen bonding states within the film. The film density was evaluated by X-ray reflectance (XRR; Smartlab, RIGAKU). To investigate the variations in the O and H signals in the SiO_2/IGZO stacked films as a function of the SiO_2 deposition temperature and post-annealing process, dynamic secondary ion mass spectrometry (D-SIMS; IMS-7 F_Auto, CAMECA, UK) was conducted using a cesium ion source at 6 keV. The hydrogen concentration of SiO_2 films was calculated using the reference sample (Evans Analytical Group). The hydrogen atomic density was calculated using Rutherford back scattering spectroscopy (RBS) and elastic recoil detection (ERD) analyses (NEC, National Electrostatics Corporation).

4.2. Device fabrication

A staggered TG FET was fabricated on a 100-nm thick thermally grown SiO_2 substrate. The 100-nm thick indium tin oxide (ITO) layer was deposited as the source and drain electrodes using radio-frequency magnetron sputtering. The IGZO active layers

were deposited at a thickness of 10 nm. Next, a 10-nm thick SiO_2 gate dielectric was deposited at various temperatures ranging from 250 to 400 °C. Finally, a 100-nm thick ITO layer was deposited as the gate electrode. Photolithography patterning and wet etching were used to define the electrodes, channels, and dielectric layers. After FET fabrication, the post-annealing process was conducted at 400, 500, and 600 °C in an Ar atmosphere for 1 h. The channel length and width of the FET were 40 and 20 μm, respectively. The overlapped area of ITO electrodes was designated as 400 μm^2 regardless of the misalignment of a photolithography process.

4.3. Device evaluation and characterization

All devices were evaluated using a Keithley 4200 semiconductor analyzer. The gate-source voltage (V_{gs}) was swept from −3 to 3 V (positive bias) and 3 to −3 V (negative bias) at the drain–source voltage (V_{DS}) = 0.1 and 1.1 V to measure the transfer characteristics. The output characteristics were measured under the following conditions: V_{gs} was increased from 0 to 5 V in 1 V intervals and V_{DS} was swept from 0 to 5 V. The μ_{FE} of the FET was extracted from the linear transfer characteristics, given by $\mu_{FE} = L_{gm(max)}/(WC_{ox}V_{ds})$ at a V_{DS} of 0.1 and 1.1 V. Here, $g_{m(max)}$ is the maximum transconductance, W is the channel width of the transistor, and C_{ox} is the oxide capacitance of the GI. The threshold voltage (V_{th}) was calculated using the linear extrapolation method.[48] Hysteresis is the difference in V_{th} between the positive- and negative-bias gate voltage sweeps. The sub-threshold swing (S. S.) is the lowest value calculated using the following equation: S. S. = $dV_{gs}/d\log(I_d)$, where V_{gs} is the gate voltage and I_d is the drain current density. The electrical property values of TG FETs were extracted at 0.1 V of V_{DS}. Capacitance–voltage (C–V) characteristics were measured using an LCR meter (HP 4284A). The mobile ionic charge density was extracted from the C–V results using a charge-pumping technique with bias-temperature stress (BTS) in the MOS structure. The BTS condition was ±1 MV cm^{-1} at 200 °C for 2 min.

Author contributions

Su-Hwan Choi: methodology, investigation, writing – original Draft. Dong-Gyu Kim: methodology, investigation, writing – original draft. Jae-Hyeok Kwag: methodology, investigation. Ki-Cheol Song: methodology, investigation. Yeonhee Lee: methodology, investigation. Chang-Kyun Park: funding acquisition. Jin-Seong Park: conceptualization, supervision, writing – review & editing. S.-H. Choi and D.-G. Kim contributed equally to this study.

Data availability

The authors declare that all data supporting the results reported in this study are available within the paper and the ESI.† Additional data used for the study are available from the corresponding author upon reasonable request.

Conflicts of interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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