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Microfluidic memristive oscillators as universal logic gates for neuromorphic computing

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Conical microfluidic channels filled with electrolytes exhibit volatile memristive behavior, offering a promising platform for energy-efficient, neuromorphic computing. Here, we integrate theoretical models of these iontronic channels as additional nonlinear elements in nonlinear Shinriki-inspired oscillators and demonstrate in simulations that they exhibit alternating chaotic and non-chaotic dynamics across a broad frequency range. Exploiting this behavior, we construct XOR and NAND gates by coupling three "Memriki" oscillators, and we further realize the full set of standard logic gates through combinations of NAND gates. Our results establish a new paradigm for iontronic computing and open avenues for scalable, low-power logical operations in microfluidic and bio-inspired systems.

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I. Introduction

The era we live in has been proposed the silicon age,[1] defined by semiconductor transistors that have revolutionized data processing, accelerating it by several orders of magnitude. This technological advancement has enabled groundbreaking inventions, including computers, the internet, and, more recently, artificial intelligence (AI).

However, advancements in AI are rapidly approaching a critical power bottleneck.[2] A key factor driving this challenge is the high energy cost caused by Ohmic losses of frequent data transfer between physically separated processing and information storage units in conventional computing architectures, a limitation known as the von Neumann bottleneck.[3] AI power consumption is currently doubling every four to six months,[4] which would surpass global energy production by the 2030s. This trend highlights the pressing need for novel computing paradigms. To enhance energy efficiency and meet the increasing demands for computing power in the era of AI and big data, a fundamentally different approach is required.[5]

Inspired by the most energy-efficient computer known – the biological brain – the field of neuromorphic computing emerged.[6] The human brain, an intricate biological neural network comprising approximately 10^{11} neurons and 10^{15} synapses, operates with a remarkable efficiency at just 20 W of power. A key subfield of neuromorphic computing focuses on developing devices that mimic the computational functions of the brain. One such device is the memristor, first theoretically proposed by Chua in 1971 as the fourth basic circuit element.[7] Memristors act as memory elements, with a resistance that depends on past voltage or current, allowing them to retain information. In 2008, Strukov *et al.* experimentally demonstrated a solid-state memristor, paving the way for its use as an artificial synapse in neuromorphic systems,[8] with present-day applications in for instance crossbar arrays.[9,10] However, silicon-based technologies typically rely on a single type of information carrier: electrons (or their absence (holes)). In contrast, the biological brain utilizes ions dissolved in water as information carriers, allowing for a diverse range of soluble information carriers, such as various species of ions and small molecules. A key distinction between solid-state electronics and ion-mediated biological systems lies in their energy efficiency, with biological systems operating orders of magnitude more efficiently, albeit at much lower clock frequencies.

This contrast has led to the emergence of iontronics, a subfield of neuromorphic computing focused on developing electronic circuit elements where ions dissolved in water serve as information carriers.[11] Just as solid-state memristors have been widely explored, researchers have pursued iontronic analogs.[12] Memristive effects in charged conical nanopores were first observed in 2010 and 2012,[13,14] paving the way for the development of diverse nanofluidic memristors based on various mechanisms. These include electric double layer polarization,[14–17] salinity gradients yielding negative differential resistance behavior,[18] electro-wetting,[19,20] structural and conformational changes of nanopores,[21,22] the ionic analogue[23] of electronic Coulomb blockade,[24] mixtures of and interfaces between ionic liquids and water,[25,26] and specific polyelectrolyte–ion interactions.[27]

The next step towards neuromorphic computing is integrating iontronic devices into electric circuits. Key questions

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include: can these networks emulate neural functions, perform Boolean logic operations, or execute simple machine learning tasks?[28] While the use of iontronic elements in large-scale networks is still in its infancy, initial progress has been made in implementing basic logic gates such as AND, OR,[29,30] NAND and NOR,[31] and material implication IMP[16] gates. A combination of currents and pH as inputs have been used to realize a set of logic gates,[32,33] requiring expensive pH changes, when switching inputs to the gate. Nanofluidic carbon nanotubes have been used to realize nanofluidic transistors which can be used for logic gates.[34] However, a complete set of logic gates based on (memristive) iontronics purely based on electronic inputs has yet to be realized.

In this work, we bridge iontronics and memristive computing by constructing logic gates using microfluidic memristors.[35] In addition to microfluidic memristors, we base our logic gates on Shinriki-inspired oscillators.[36] Shinriki oscillators are simple electric circuits, first studied by Shinriki *et al.*, that can show chaotic behavior depending on the exact system parameters. As the human brain operates at the edge of chaos,[37,38] we designed our circuits to inherit this property. Furthermore, we exploit noise during our computations, which has been deemed essential for achieving power-efficient computing in soft-matter systems.[5]

We first provide a brief introduction to volatile microfluidic memristors as described in ref. 35, and then explore their integration into electric circuits that form Shinriki-inspired (non-linear) oscillators.[36] Finally, we demonstrate how these oscillators can be combined to realize the full set of logic gates, thereby advancing the use of iontronics for neuromorphic and Boolean logic applications.

II. Microfluidic iontronic memristor

In this study, we focus on volatile microfluidic memristors as presented in ref. 35 and illustrated in Fig. 1(a). This conical channel of length L has a wide opening of base radius R_b at $x = 0$ and a narrow tip of radius $R_t < R_b$ at $x = L$, and connects two reservoirs of an aqueous 1 : 1 electrolyte at a total bulk ion concentration $2\rho_b$ at room temperature. The channel can carry an ionic electric current when driven by an applied potential difference between the two reservoirs. The combination of the conical channel geometry and a negative surface charge $e\sigma$ on the channel walls results in current rectification when a static voltage drop U is applied.[39] This phenomenon was theoretically explained in terms of a nontrivial U-dependent steady-state salt concentration profile $\rho_s(x;U)$ for $x \in [0,L]$ that build up within the channel.[40] This concentration profile is caused by the much stronger electric field near the tip compared to the base and leads to ionic depletion or accumulation depending on the polarity of the potential. Consequently, the steady-state electric conductance $g_\infty(U)$ depends non-trivially on U and exhibits a hysteresis loop in the current–voltage relation when a time-dependent oscillating potential $U(t)$ is applied with a period on the order of the build-up time τ of the ionic concentration profile.[35] The time-dependent conductance $g(t)$ of such a

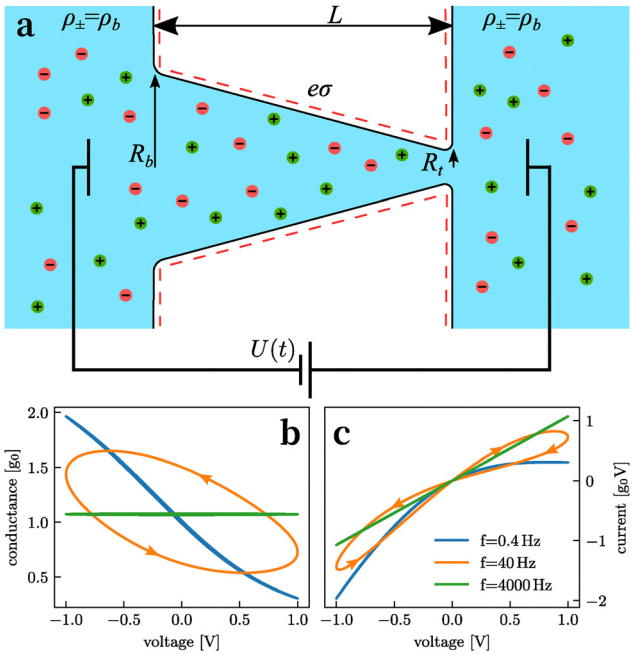

Fig. 1 (a) Schematic of a conical channel filled with an aqueous 1 : 1 electrolyte (cations in green, anions in red) with length L, base radius R_b, tip radius R_t, bulk ion concentrations $\rho_\pm = \rho_b$ in the reservoirs, and surface charge $e\sigma$. A time-dependent voltage $U(t)$ is applied across the channel. (b) Limit cycles of the conductance–voltage relation for three different driving frequencies f = 0.4 Hz (blue), f = 40 Hz (orange), and f = 4000 Hz (green) of a sinusoidal potential with an amplitude of 1 Volt. (c) Limit cycles of the current–voltage relation for the same frequencies and parameters as in (b).

memristive channel was calculated from numerical solutions of the Poisson–Nernst–Planck–Stokes (partial differential) equations for the coupled transport of charge, water, and ions,[35] and subsequently experimentally verified.[15] In a large parameter regime $g(t)$ was also found to be accurately approximated by the following (ordinary differential) equation of motion[41]

$$\tau\dot{g}(t) = g_\infty(U(t)) - g(t) \tag{1}$$

with

$$g_\infty(U) = g_0\int_0^L \frac{\rho_s(x,U)}{2\rho_b L}\mathrm{d}x, \tag{2}$$

where the functional form of the static conductance $g_\infty(U)$ is determined by the channel geometry and the electrolyte properties, that we keep fixed here however such that its numerical evaluation for different U is straightforward. The parameter g_0 represents the zero-field conductance, which we use as the unit of conductance below. Throughout this work we will use the (physically realistic) set of system parameters of ref. 35, which are all given, together with detailed expressions for $g_\infty(U)$, in Section A. Of particular importance is the characteristic time scale $\tau \approx 5$ ms of our parameter set, which is the memory retention time of the microfluidic memristor. We note, however, that the dynamic response of the conical channel is

qualitatively independent of the details of the system parameters.

We consider a sinusoidal voltage $U(t) = U_0 \sin(2\pi ft)$ with fixed amplitude $U_0 = 1$ V and several frequencies f applied over the microfluidic channel to analyze its frequency-dependent dynamic response resulting from numerical solutions of eqn (1). Focusing on the limit cycle in which all transients have decayed, we present in Fig. 1 parametric plots for three different frequencies, $(U(t), g(t))$ in (b) and $(U(t), I(t))$ in (c), where the current is defined as $I(t) = g(t)U(t)$. Depending on the driving frequency, the electric response of the channel falls into one of three regimes: (i) at low frequencies $f \ll 1/\tau$, exemplified here by $f = 0.4$ Hz (blue), the conductance $g(U(t))$ closely follows the steady-state function $g_\infty(U(t))$ in (b), as the driving voltage changes slowly enough for the concentration profile to fully build up at all times. In this low-frequency regime, the electric current $I(t)$ in (c) shows strong rectification, approaching nearly full diodic behavior, with significantly higher current at negative voltages than at positive ones. (ii) At high frequencies $f \gg 1/\tau$, exemplified here by $f = 400$ Hz (green), the sinusoidal voltage oscillates too rapidly for the ionic concentration profile to develop, leaving it essentially spatially and temporally constant. As a result, the conductance is essentially Ohmic with constant $g(t) \approx 1.07 g_0$ in (b) and $I(t)$ linear in $U(t)$ in (c). One might have expected the conductance in this high-frequency regime to be exactly equal to g_0. However, the nonlinearity of $g_\infty(U)$ results in a nonzero difference between the static conductance at the time-averaged voltage g_0 and the time-averaged steady-state conductance for the time-dependent voltage, yielding $\langle g_\infty(U(t))\rangle \approx 1.07 g_0$. (iii) At intermediate frequencies $f \sim 1/\tau$, exemplified here by $f = 40$ Hz (orange), the driving voltage varies on a timescale comparable to the memory timescale of the channel. As a result, hysteresis emerges in both the conductance (b) and the current (c) since the ionic concentration profile can partially build up and break down but not fully equilibrate. This leads to a lower channel conductance when the potential was recently positive and a higher conductance when it was recently negative.

Recently, the behavior of such an iontronic device has been extensively tested experimentally using an easy-to-fabricate tapered microfluidic channel of uniform height, filled with colloidal particles and connected to two aqueous KCl electrolyte reservoirs. Both the diode-like behavior and the dynamic I–V curves show good agreement with theoretical predictions, similar to those presented in Fig. 1b and c,[15] thereby providing confidence that these microfluidic iontronic memristors can serve as reliable components in larger electric (or microfluidic) circuits.

In the remainder of this work, we measure all quantities relative to the steady-state conductance g_0 of the memristor at 0 V. We use volts (V) and seconds (s) as our units for potential and time, respectively. Specifically, resistance is expressed in g_0^{-1}, current in g_0V, capacitance in g_0s, and inductance in s/g_0. We solve the equations of motion for all circuits in this paper using the circuit simulation software ACME.jl based on.[42] For all simulations, we use a time step $\delta t = 10^{-5}$ s, except for the calculations in Fig. 1(b) and (c), where we use $\delta t = 10^{-5}/f$, to ensure sufficient resolution for the high frequency cases. The code for reproducing the simulations is provided in ref. 43.

III. Characterization of a single Memriki oscillator

To leverage the volatile behavior of the memristors of Section II, we incorporate two of them into a nonlinear electrical circuit with an intrinsic oscillatory timescale similar to that of the memristors. The circuit design, shown in Fig. 2, is heavily inspired by the well-known Shinriki-oscillator,[36] albeit with a slightly modified topology and with iontronic memristors M_1 and M_2 rather than diodes. We propose the name Memriki oscillator for this circuit. Later we will swap out the memristors

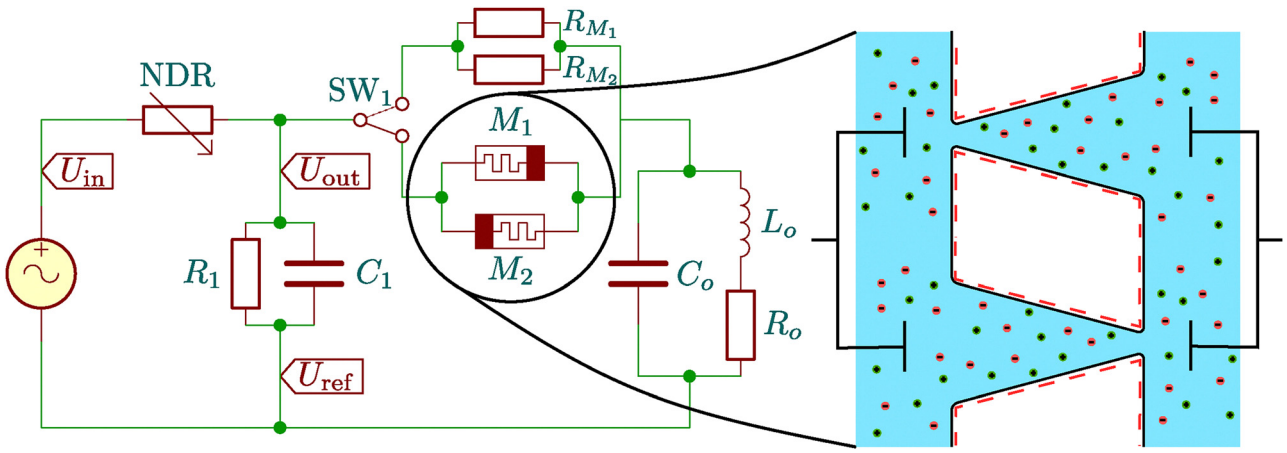

Fig. 2 Schematic of a single Memriki oscillator. The capacitor C_o, inductor L_o and resistor R_o together form a damped oscillator. The circuit is driven by the input voltage U_{in}, measured relative to the reference voltage U_{ref}. A negative differential resistance NDR introduces nonlinearity into the circuit. The output voltage U_{out} is measured, stabilized by C_1, and slowly relaxed towards U_{ref} by R_1. Two iontronic memristors M_1 and M_2 are added between U_{out} and the oscillatory section to introduce further nonlinearity. With the switch SW_1 the memristors can be replaced with ordinary resistors.

for conventional resistors to study the role of the memristors. In order to allow for this swapping, we introduced the switch SW_1 into the circuit, to either connect the resistors or the memristors. The circuit, driven by a sinusoidal source potential $U_{in} = U_0 \sin(2\pi ft)$ with amplitude U_0 and frequency f, consists of a negative differential resistance NDR, two anti-parallel memristors in series with a (weakly damped) LRC oscillator with eigen frequency $1/(2\pi\sqrt{L_o C_o})$, and a resistor R_1 and capacitor C_1 that are both parallel to the memristor-oscillator part. Based on the original work of Shinriki *et al.*,[36] the NDR is an active element with a characteristic function given by $R(U)\, g_0 = (U/\mathrm{V})^3 - 3U/\mathrm{V}$. In this work we restrict ourselves to this specific form of the NDR without exploring variations, which implies that it behaves as an active amplifier rather than a passive resistor within the ± 1 V voltage range around 0 V. The parallel resistor and capacitor, with $g_0 R_1$ of order unity and $C_1 = 10^{-4} g_0$s, respectively, can serve as tunable parameters that significantly alter the dynamics of the circuit. The electric specifications for the oscillatory part of the circuit read $C_o = 10^{-3} g_0$s, $L_o = 10^{-3}$ s/g_0 and $R_o = 10^{-3} {g_0}^{-1}$, ensuring that $R_o \ll R_1$. As a result, the eigen period of the weakly damped oscillator is approximately $2\pi\sqrt{L_o C_o} \approx 6$ ms, which is comparable to the memory time of the two memristors, $\tau \approx 5$ ms. While we describe and denote all circuit elements (except for the memristors) as conventional electrical components, we note that microfluidic counterparts exist for each of the elementary circuit components,[44,45] however, our work would additionally require iontronic NDRs and operational amplifiers. Because the essential building blocks for iontronic NDRs and operational amplifiers, namely iontronic transistors, have been experimentally realized,[46,47] we expect that a purely iontronic realization of the Memriki oscillator will be possible in the coming years.

The dynamic response of the Memriki oscillator varies dramatically depending on the precise values of the resistor R_1 and the driving frequency f. For three different combinations of R_1 and f (and for $U_0 = 0.25$ V and all other parameters fixed as in the text above) this parameter sensitivity of the response is illustrated in Fig. 3. Here the top row (a)–(c) shows the time-dependence of the driving voltage $U_{in}(t) = U_0 \sin(2\pi ft)$ (orange) with the resulting output voltage $U_{out}(t)$ (blue); the bottom row (d) and (e) shows the parametric plot $(U_{in}(t), U_{out}(t))$. Fig. 3 thus exhibits behaviors ranging from simple driven oscillations at $R_1 = 0.425 {g_0}^{-1}$ and $f = 120$ Hz in (a) and (d), to chaotic dynamics by increasing the frequency to $f = 400$ Hz in (b) and (e), and finally to subharmonic oscillations with frequency $f/3$ by subsequently increasing the resistance to $R_1 = 1.0 {g_0}^{-1}$ while maintaining $f = 400$ Hz in (c) and (f).

To quantify the complexity of the output voltage $U_{out}(t)$ in greater detail, we count the number of distinct output voltage values at discrete times $t = n/f$, where $n \in \mathbb{N}$, *i.e.* at time points corresponding to integer multiples of the input signal's periodicity. The number of recurrences of distinct output values is defined as $N_{rec} = |\{U_{out}(n/f) \quad \text{for } n \in \mathbb{N}\}|$, where $|\cdot|$ denotes the number of elements in the set. In practice, we consider two output values to be the same if their (absolute) difference is smaller than a typical tolerance, $\epsilon = 0.01$ V, to account for finite numerical precision. For example, this definition yields $N_{rec} = 1$ for the periodic oscillation in Fig. 3(a) and $N_{rec} = 3$ for the subharmonic oscillation in Fig. 3(c). Similarly, N_{rec} is a small integer for periodic output voltages $U_{out}(t)$ that are commensurate with the input signal $U_{in}(t)$. However, for incommensurate or chaotic output voltages, the number of distinct output values diverges, *i.e.* $N_{rec} \to \infty$. To ensure that the computation of N_{rec} remains numerically tractable, we first let the system equilibrate for 100 periods of the input signal and then analyze the next 100 periods. Thus, we restrict the analysis to $n \in [101, 200]$, which bounds $N_{rec} \in [1, 100]$. This approach gives, for instance, $N_{rec} = 61$ for the case of Fig. 3(b) that we would deem to be

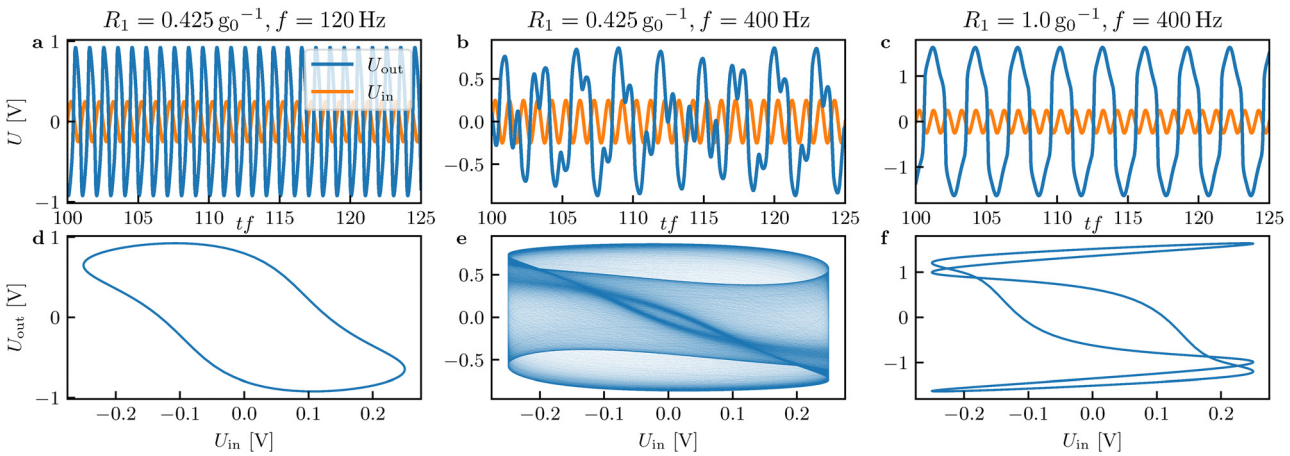

Fig. 3 Dynamics of the driven Memriki oscillator from Fig. 2 for three different combinations of resistor R_1 and driving frequency f, with all other circuit elements specified in the text. The top panels (a)–(c) show the time series of the input voltage $U_{in} = 0.25 \sin(2\pi ft)$ V (orange) and the output voltage U_{out} (blue) during 25 driving periods after 100 initial periods. The bottom panels (d)–(f) show the corresponding parametric plots of U_{out} *versus* U_{in} over 1000 driving periods, revealing stable periodic orbits in (d) and (f) separated by a chaotic, non-periodic regime in (e). Thus, in (a) and (d) the Memriki oscillator follows the input signal and oscillates at the driving frequency f, in (b) and (e) the response exhibits chaotic behavior, while in (c) and (f), the response is subharmonic with a threefold period at an oscillating frequency $f/3$.

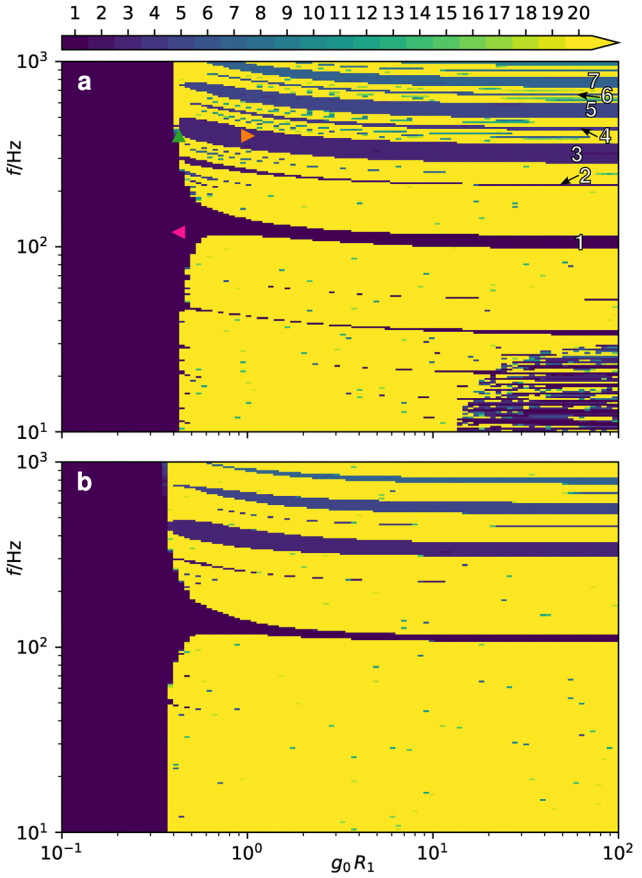

Fig. 4 Heat map of the number of recurrences N_{rec} of distinct output voltage values at times corresponding to integer periods of the input (see text), as a function of the driving frequency f and the resistance of R_1 in the circuit shown in Fig. 2. Results are shown for the two positions of the switch SW_1, which couples either (a) the memristors or (b) the ohmic resistors to the RCL oscillator. All other parameter values are provided in the text. Numbers in (a) indicate N_{rec} for the corresponding bands. Marked points show the state-points of Fig. 3. Pink left pointing triangle for Fig. 3 (a), green upwards pointing triangle for (b) and orange right pointing triangle for (c).

chaotic for all intents and purposes. In the analysis and figures below, we further simplify the presentation and only distinguish $N_{rec} \in [1, 20]$.

In Fig. 4(a) we show the heatmap of N_{rec} for the circuit of Fig. 2 as a function of R_1 and f, with the switch SW_1 in the "memristor state" and with all other parameters given in the text. We can clearly distinguish a (fully purple) low-resistor regime $g_0R_1 < 0.4$ where the oscillator is completely stable with $N_{rec} = 1$, regardless the driving frequency f. The high-resistor regime $g_0R_1 > 0.4$ shows a richer palette of behavior with large chaotic regimes (yellow) where $N_{rec} \geq 20$ and substantial stable bands (purple) with $N_{rec} = 1$ dispersed by tiny intermediate regimes (green). Several of the stable (purple) bands extend deep into the high-resistor regime, especially at high frequencies $f > 100$ Hz. Also, for $g_0R_1 > 10$ and low frequencies $f < 10^{1.5}$ Hz, a regime appears where chaos and stability are closely inter-dispersed. Furthermore, we note that the stable (purple) bands with subharmonic response are significantly wider when the response frequency is an odd multiple of the input frequency as compared to an even multiple.

In order to analyze (and appreciate) the role of the memristors, we show the heat map of N_{rec} again in Fig. 4(b), however now with the switch SW_1 set to the "resistor state" with two parallel Ohmic resistors replacing the two parallel memristors. The value $R_{M_{1,2}} = 0.25g_0^{-1}$ that we chose for the two resistors might seem a bit low at first sight, however this is justified because one of the two memristors in (a) is always in the low-resistance state due to their anti-parallel wiring. Comparing the Ohmic case of Fig. 4(b) with the memristor case of (a) reveals a similar low-resistance stability regime, however in the predominantly chaotic (yellow) regime at higher resistances much fewer stable (purple) bands appear and their (purple-yellow) interfaces appear to be sharper in (b) indicating fewer modes with intermediate harmonic periods of several driving periods. Moreover, the finely dispersed stable-and-chaotic regime found at low f and high R_1 in (a) has disappeared altogether in (b). In other words, the memristors increase the regime of predictability in the predominantly chaotic high-resistance regime, and therefore contribute to a circuit being at the edge of chaos. For this reason, we focus on circuits of Memriki oscillators below.

IV. Coupling Memriki oscillators

The most fundamental computations involve combining two inputs to produce a single output. To achieve this, we couple three Memriki oscillators, represented by the three "boxes" in the circuit diagrams of Fig. 5(a) and (c). Two oscillators serve as inputs, while the third acts as an output. In Fig. 5(a), we see that the outputs of the two input oscillators are capacitively connected to the input of the output oscillator, which prevents any DC current from flowing from the inputs to the output. When the circuit of Fig. 5(a) is driven by input voltages 0 and 1 V, representing low and high logic levels, along with Gaussian noise with a standard deviation of 0.003 V, the output of the circuit turns out to correspond to a logic XOR-like gate. For $R_1 = 0.4g_0^{-1}$, this is shown in the voltage time trace of Fig. 5(b), with blue and orange representing the four consecutive input combinations (10, 00, 01, 11) and green the output. That is, the circuit oscillates when the two inputs differ and remains quiescent when they are the same. This XOR-type behavior can be interpreted as performing a nonlinear classification task, one of the most fundamental classification tasks in machine learning.[48] For reasons that will become clear in the next section we refer to this as an XOR-pre-gate.

The NAND-gate is the primary objective when building logic gates, as all other gates can be constructed from combinations of NAND. We realize a NAND-pre-gate by inserting two additional operational amplifiers into the circuit as shown in Fig. 5(c). These amplifiers function as impedance changers, ensuring sustained oscillations in the third oscillator when both inputs are low. The resulting output voltage, shown in green in Fig. 5(d) for the same four input combinations

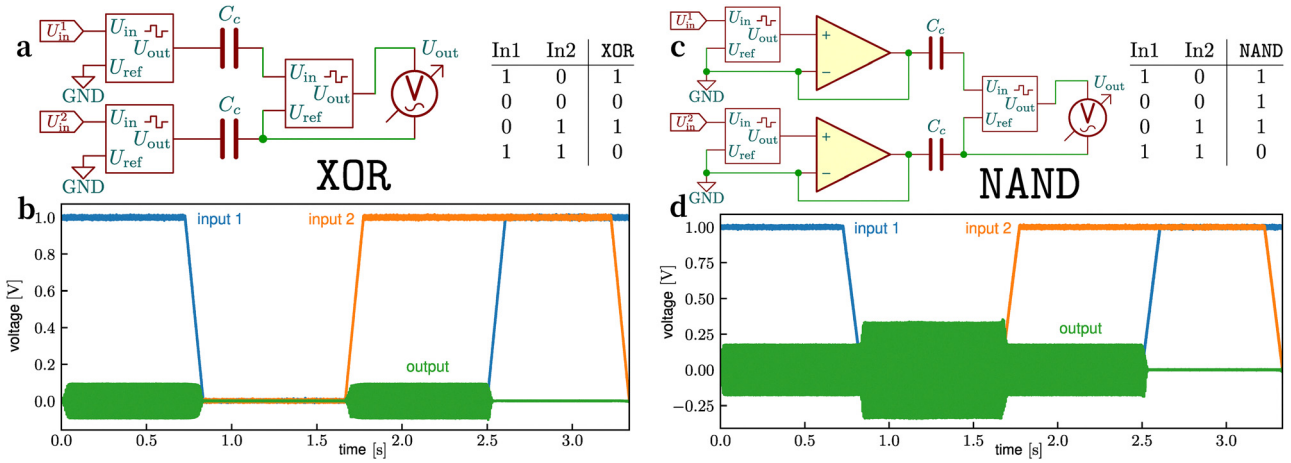

Fig. 5 Circuit diagrams of a XOR-pre-gate (a) and a NAND-pre-gate (c) constructed by combining three Memriki oscillators from Fig. 2 (represented here by the three boxes), either coupled solely *via* capacitors (a) or with the addition of two operational amplifiers (c). Time traces of the two input voltages (blue and orange) representing the four consecutive binary states 10, 00, 01, 11. The resulting quasi-binary output voltage (green), which is either quiescent or oscillating, is shown in (b) for circuit (a), revealing XOR behavior, and in (d) for circuit (c), exhibiting NAND behavior. The corresponding truth tables are shown next to the circuit diagrams.

(blue and orange) as in (b), oscillates with a frequency ≈ 55 Hz for the input states 10, 00, and 01, but remains quiescent for input 11. Therefore, we classify this circuit as a NAND-pre-gate. When testing the resilience of these pre-gates to noise we find that they remain stable under uniformly distributed noise with an amplitude of approximately 0.1 V, and under Gaussian noise with a standard deviation of roughly 0.1 V. We also note that the oscillation frequency of approximately 55 Hz provides for the present parameters an experimental selection criterion for feasible NDR elements and operational amplifiers, which should be able to respond to voltage changes on time scales faster than several milliseconds.

To use the output of one logic gate as the input for another, the output must be compatible with the input requirements, in this case static signals of 0 V and 1 V. To achieve a proper NAND gate, we must transform the oscillatory output of our NAND-pre-gate into a constant output of 1 V while its quiescent (0) output for the 11 input remains unaffected. This transformation is achieved by passing the output voltage of our NAND-pre-gate through the coupler shown in the circuit diagram of Fig. 6. In this coupler, the output voltage first passes through the operational amplifier OA_1, which strengthens the signal and prevents drawing any current from the input gates. The amplified signal is then passed through a full-wave bridge rectifier composed of four diodes, followed by time-averaging with a low-pass filter with time constant $R_{LP}C_{LP} = 0.5$ ms. Finally, the signal is amplified by OA_2 to achieve the desired 1 V logic level.

The two operational amplifiers used in the coupler convert the input voltage U_{in} into an output voltage given by

$$U_{out} = \Delta U \tanh\left(\frac{G U_{in}}{\Delta U}\right), \qquad (3)$$

where G is the gain factor (for small inputs), set to $G = 15$ for OA_1 and to $G = 35$ for OA_2. The parameter $\Delta U = U_+ - U_- = 1.0$ V defines the range of the amplifier, allowing amplification up to

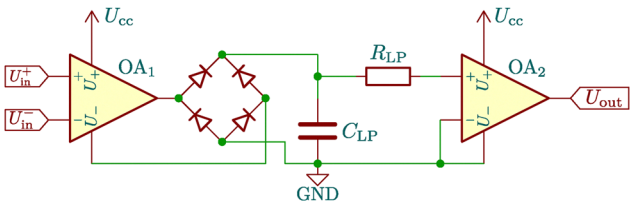

Fig. 6 Coupler for converting an oscillatory signal into constant logic levels. The oscillatory input voltage difference between U_{in}^+ and U_{in}^- is first amplified by the left operational amplifier OA_1. This amplified signal is then rectified by a full-wave bridge rectifier, consisting of four diodes. The rectified signal is subsequently smoothed by a low-pass filter consisting of R_{LP} and C_{LP} and finally amplified to the desired logic level by the right operational amplifier OA_2. The operational amplifiers in this circuit are modeled by eqn (3), with a maximum voltage of $U_+ = U_{cc} = 1$ V.

± 1 V. The low-pass RC filter consists of a resistance $R_{LP} = 10^{-2} {g_0}^{-1}$ and a capacitance $C_{LP} = 5 \times 10^{-2} g_0$s, while the diodes are modeled with a saturation current of $0.3 g_0$V and an emission factor $\eta = 1$.[49]

With the addition of this coupler circuit, the NAND-pre-gate becomes a true NAND gate.

V. Combining gates

The NAND gate is well known to be functionally complete, which means that any other logic gate can be constructed from it. In particular, an OR gate can be constructed using three NAND gates, as shown in Fig. 7(a). The Boolean logic for the OR gate follows $\overline{U_{in}{}^1 \cdot U_{in}{}^1} \cdot \overline{U_{in}{}^2 \cdot U_{in}{}^2} = \overline{\overline{U_{in}{}^1} \cdot \overline{U_{in}{}^2}} = \overline{\overline{U_{in}{}^1}} + \overline{\overline{U_{in}{}^2}} = U_{in}{}^1 + U_{in}{}^2$, where $\cdot$ denotes the logic AND, + the logic OR, and an overline indicates negation. In our circuits, each input signal $U_{in}{}^1$ and $U_{in}{}^2$ is passed through the combined gates twice to ensure independent noise sources for all our Memriki gates. If identical signals were used, the differential input to the final gate would cancel out,

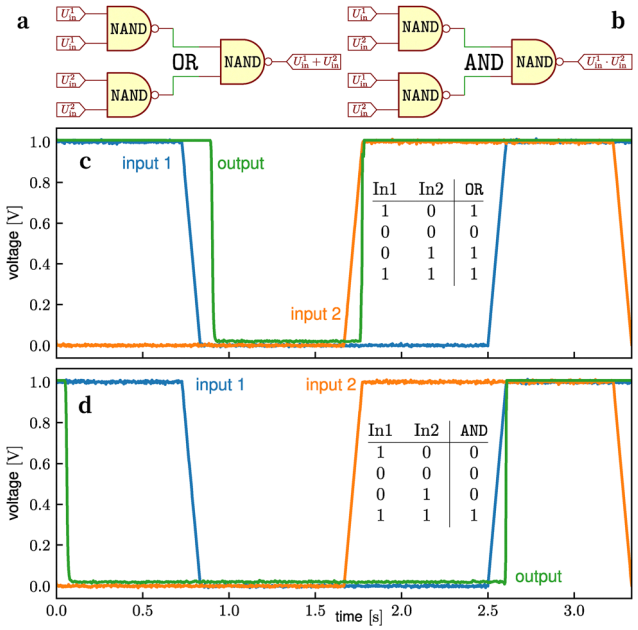

Fig. 7 Three combined NAND gates (see text) form (a) an OR gate and (b) an AND gate. Time traces of the input voltages (blue and orange), representing four consecutive binary states, and the corresponding output voltage (green) for (c) the OR gate and (d) the AND gate, along with the corresponding truth tables. The delay in the switching of the output signal after the inputs have changed originates from the low-pass filter in the coupling circuit in Fig. 6.

preventing the oscillations from self-exciting. To further aid self-excitation, we also add Gaussian noise with a standard deviation of 0.003 V to the inputs of the last gate.

The voltage time trace in Fig. 7(c) displays the output (green) of the OR gate for the same four consecutive input signals (blue and orange) used previously. This confirms that the gate functions correctly as a logic OR gate, processing weakly noisy static inputs. The response time of the gate is approximately 0.1 s for relatively slowly varying input signals.

As is well known, the circuit for the OR gate can be reused to realize an AND gate; only the inputs need to be rearranged such that both input gates now receive $U_{\mathrm{in}}{}^{1}$ and $U_{\mathrm{in}}{}^{2}$, as shown in Fig. 7(b). The logic for the AND gate is as follows: $\overline{\overline{U_{\mathrm{in}}{}^{1}\cdot U_{\mathrm{in}}{}^{2}}\cdot\overline{U_{\mathrm{in}}{}^{1}\cdot U_{\mathrm{in}}{}^{2}}}=\overline{\overline{U_{\mathrm{in}}{}^{1}\cdot U_{\mathrm{in}}{}^{2}}}+\overline{\overline{U_{\mathrm{in}}{}^{1}\cdot U_{\mathrm{in}}{}^{2}}}=U_{\mathrm{in}}{}^{1}\cdot U_{\mathrm{in}}{}^{2}$. The resulting input–output relation for this AND gate is shown in Fig. 7(d), confirming that it functions correctly as an AND gate. The dynamic response to slowly varying inputs is comparable to that of the OR gate.

To test the repeatability and reproducibility of the gates we need to verify whether they perform as expected over many cycles of the (weakly noisy) input and output sequences. For our continuous system, with output voltages spanning the full range between zero and one volt when the input signal switches, we need to define boundaries separating high- and low-level signals during specific time intervals. Here we set the time interval as the duration between the switching of the input signals and consider an output larger than 0.66 V as a digital 1 and below 0.33 V a digital 0. To evaluate the pre-gates, we connect them to the coupling circuit as described above to ensure they function as proper gates. Using these definitions, we tested 100 cycles of all possible input combinations and obtained the following accuracies. Individual XOR gates and NAND gates operate with an accuracy of $\geq$99%, the combined OR gate achieves also $\geq$99% accuracy, and the combined AND gate reaches an accuracy of $\geq$95%.

An exact power consumption analysis of our circuit depends on the implementation details of the negative differential resistance and the operational amplifiers. Therefore we solely focus on the Ohmic losses in the circuit. The power consumption of our NAND gate can then be estimated by the average voltages and resistances in the circuit, leading to $\langle P\rangle=\frac{1}{2}\langle U^2/R\rangle\approx 1 g_0 \mathrm{V}^2$. Given our experimentally realistic default value of a few pS for the zero-field conductance g_0 of the channel, this leads to an Ohmic power consumption of the order of pW, which may be reduced substantially by optimizing the dimensions and the surface chemistry of the channel. Given that the typical time scale for bit operations in our circuit is of the order of seconds, our pW estimate for the ohmic power consumption corresponds to an energy of the order of pJ per bit. However, we expect it will be challenging to find NDR elements and operational amplifiers that function reliably at currents in the pA–fA range, so higher currents and therefore higher power consumption will likely be required. Quantifying the actual power consumption of these circuits thus remains an important topic for future research.

VI. Conclusion

We designed models of microfluidic iontronic circuits, primarily combining volatile memristors with Shinriki-like oscillators, that can perform non-linear XOR classification and act as functional complete NAND logic gates. The theoretical description of the properties of the elements of the circuits are either standard or, in the case of the iontronic memristors, recently experimentally verified to be realistic.[15] We showed that these NAND gates are robust and can be combined to construct other logic gates, especially OR and AND. A key feature of these circuits is their exploitation of noise, here introduced at a level of 3 mV relative to a 1 V signal scale. This noise level enables the self-excitation of oscillators from a quiescent (0) to an oscillating (1) state, a feature that stems from the intrinsic non-linearity of the ''Memriki'' oscillators from which our circuits were composed. This self-excitation is fundamental to the operation of our circuits and enables the construction of logic gates such as NAND without requiring separate inverters. We hope our findings will inspire future experimental exploration of memristive iontronic devices. Although we have not yet assessed the energy efficiency of our circuits and logic gates in detail, we do not expect them to outperform present-day silicon-based technologies in this regard. In this sense, this work serves as a proof of concept for a potentially versatile iontronic computing platform, operating with the same aqueous electrolyte environment as mammalian brains.

Author contributions

N. C. X. S. designed the circuits, performed the simulations and analyzed the data. All authors discussed the results and contributed to the manuscript.

Conflicts of interest

There are no competing interests.

Code availability

The code to perform the simulations is provided in ref. 43.

Data availability

All data can be generated with the source-code provided in ref. 43. The raw data is also available in ref. 50.

Appendices A: model details

To evaluate the steady-state conductance of the conical channels, we use the parameters and expressions from ref. 35 for eqn (1). For a conical channel of length L = 10 μm, base radius R_b = 200 nm, tip radius R_t = 50 nm, and a radius profile $R(x) = R_t x/L + R_b(1 - x/L)$ for $x \in [0,L]$ running from base to tip, the static conductance $g_\infty(U)$ is given by

$$\frac{g_\infty(U)}{g_0} = 1 + \Delta g \int_0^L \left(\frac{xR_t}{LR(x)} - \frac{e^{\frac{x\mathrm{Pe}R_t^2}{LR_bR(x)}} - 1}{e^{\mathrm{Pe}\frac{R_t}{R_b}} - 1} \right) \frac{dx}{L}. \quad \text{(A1)}$$

Here, $g_0 \approx 4.2$ pS is the zero-field conductance, $\Delta g \approx -3.59$ is the asymmetry parameter, and Pe is the Peclet number, which varies linearly with the applied voltage U as $\mathrm{Pe}(U) \approx 16\ U/\mathrm{V}$ for our parameter set (exact expressions provided below). Using the short-hand notation $\Delta R = R_b - R_t$, and performing the integral, one obtains the explicit static channel conductance

$$g_\infty(U) = g_0 \left(1 + \Delta g \frac{R_t}{\Delta R} F(U) \right) \quad \text{(A2)}$$

$$F(U) = \frac{e^{\frac{-\mathrm{Pe}R_t^2}{\Delta R R_b}} A(U)}{e^{\mathrm{Pe}\frac{R_t}{R_b}} - 1} - \left(\frac{R_b}{\Delta R} \ln \frac{R_t}{R_b} + 1 \right) \quad \text{(A3)}$$

$$A(U) = e^{\frac{\mathrm{Pe}R_t}{\Delta R}} - \frac{R_b}{R_t} e^{\frac{\mathrm{Pe}R_t^2}{\Delta R R_b}} + \frac{\Delta R}{R_t} + B(U) \quad \text{(A4)}$$

$$B(U) = \frac{-\mathrm{Pe}R_t}{\Delta R} \left(\mathrm{Ei}\left(\frac{\mathrm{Pe}R_t}{\Delta R} \right) - \mathrm{Ei}\left(\frac{\mathrm{Pe}R_t^2}{\Delta R R_b} \right) \right), \quad \text{(A5)}$$

where $\mathrm{Ei}(x) = \int_{-\infty}^{x} e^{-t}/t\,dt$ is the exponential integral function.

We stress that this explicit expression for $g_\infty(U)$ stems from an (approximate) analytic solution to the fully microscopic Poisson–Nernst–Planck–Stokes equations in the long-channel limit. The dependence of the conductance on U is a direct consequence of electro-osmotic flow, characterized by the dimensionless parameter $\mathrm{Pe}(U)$. This effect relies on the presence of a nonzero surface charge $e\sigma$ (and hence a nonzero zeta potential ψ on the channel walls), as becomes explicit by the analytic relation $\mathrm{Pe}(U) = \frac{-eR_b}{k_B T R_t w} U$, where $w = \frac{eD\eta}{k_B T \varepsilon \psi} \approx -9.6$ represents the ratio of ionic mobility D/k_BT to osmotic mobility $\varepsilon\psi/(e\eta)$. Here D = 1.75 nm^2 ns^{-1} is the diffusion coefficient of the monovalent cations and anions in water, k_B denotes the Boltzmann constant, T = 293.15 K is the absolute temperature, and $\varepsilon = 80.2\epsilon_0 \approx 7.1 \times 10^{-8}$ F m^{-1}is the dielectric constant, and η = 1.01 mPa s is the shear viscosity of water. We define the steady zero-field conductance as $g_0 = \frac{\pi R_t R_b}{L} \frac{2\rho_b e^2 D}{k_B T}$, where ρ_b is the ionic bulk concentration, set to 10 mM. The asymmetry parameter is given by $\Delta g = \frac{-2w\Delta R}{R_b \mathrm{Du}} \approx -3.59$, where the Dukhin number is $\mathrm{Du} = \sigma/(2\rho_b R_t) \approx -0.25$, with $e\sigma = -0.0015e$ nm^{-2} the surface charge density on the channel walls. The corresponding zeta potential is $\psi = \frac{2k_BT}{e} \mathrm{asinh}(2\pi\lambda_D\lambda_B\sigma) \approx -10$ mV, where $\lambda_D = \sqrt{\varepsilon k_B T/(2e^2\rho_b)} \approx 30$ nm is the Debye length and $\lambda_B = e^2/(4\pi\varepsilon k_B T) \approx 0.71$ nm is the Bjerrum length.

The characteristic time scale of this conical channel, which is the time scale to build up (or break down) the static voltage-dependent salt concentration profile $\rho_s(x;U)$ in the channel, was derived to be the diffusion time $\tau = L^2/12D$, valid in the long-channel limit $L \gg R_b$. For the present parameters this leads to $\tau \approx 5$ ms.

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