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$MoTe_2$ synaptic transistor and its application to physical reservoir computing†

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In this study, we systematically analyzed the synaptic properties of an $MoTe_2$-based transistor and propose a physical reservoir computing system based on it. The device was fabricated as a back-gate structure using mechanically exfoliated $MoTe_2$ sheets on a SiO_2/Si substrate, which showed the characteristics of an n-type field effect transistor. It exhibited synaptic properties upon application of voltage pulses to the gate, such as excitatory post-synaptic currents or paired pulse facilitations. A long-term conductance modulation was achieved upon the application of a voltage pulse series, and its potential in hardware-based artificial neural networks was confirmed *via* a simulation study. Furthermore, we demonstrated physical reservoir computing using the device in a classification task involving gray-scale handwritten digits. The nonlinear response and fading memory characteristics of the device played critical roles in achieving good accuracy in physical reservoir computing. The $MoTe_2$-based synaptic transistor demonstrates the feasibility of two-dimensional materials in neuromorphic computing for energy efficient AI systems.

Introduction

The huge energy consumption by computing facilities for artificial intelligence (AI) is raising concerns in achieving sustainable development.[1] Despite the continuous scaling of silicon electronics for higher efficiency and performance, such efforts are approaching the physical limits of scaling.[2] As an alternative and ultimate solution, synaptic devices that emulate the principle of the synapse in neural networks of the human brain are being researched worldwide.[3–11] Synaptic devices can serve as building blocks for fully hardware-based neural networks that can accelerate AI computation with high energy efficiency, circumventing the von Neumann bottleneck in digital computation.

Synaptic devices can play significant roles not only in traditional neuromorphic computing but also in physical reservoir computing (PRC)—an alternative computing framework.[12–14] Here, the inherent physical dynamics in the device serve as a reservoir, mapping the temporal input into higher-dimensional states. Versatile nonlinear behaviors and fading memory characteristics of synaptic devices can readily be utilized in PRC.[15–21] Therefore, synaptic devices can provide a direct solution for energy-efficient AI, while a neuromorphic system remains a long-term goal.

Given the opportunities in synaptic device development, two-dimensional (2D) materials can provide synergetic advantages for synaptic devices, including scalability to the atomic range, excellent electronic performance, and good physical stability.[10,22] Among 2D materials, $MoTe_2$ has recently emerged as an attractive candidate because of its unique combination of high electron mobility, reversible conductivity tunability, and phase-change control properties, which are well-suited for synaptic applications.[23,24] Given their advantages, such materials are expected to enable the efficient development of PRC- and hardware-based artificial neural networks if they can be fabricated into synaptic devices.

Herein, we report the fabrication and characterization of an $MoTe_2$-based artificial synaptic transistor and its application in PRC. We investigated the synaptic characteristics of the transistor and its effectiveness in neural networks (simulation study). Importantly, we experimentally demonstrated PRC by classifying grayscale handwritten digits using the device. Results highlighted the potential of 2D-material-based artificial synapses in future energy-efficient AI systems.

Results and discussion

Device fabrication and electrical characteristics

An $MoTe_2$ synaptic transistor was fabricated using mechanically exfoliated multilayer $MoTe_2$ flakes. Fig. 1a illustrates the

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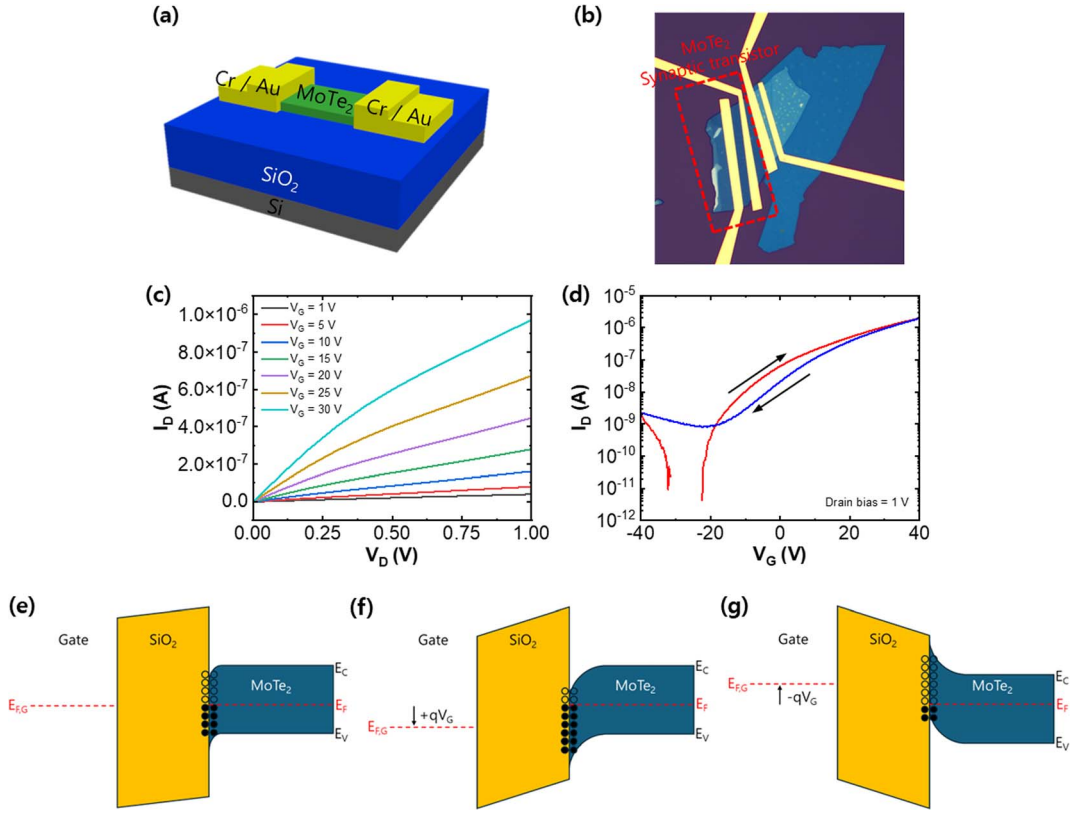

Fig. 1 (a) Schematic of the structure of the $MoTe_2$ synaptic transistor. (b) Optical image of the $MoTe_2$ synaptic transistor. (c) Output characteristics and (d) transfer characteristics of the $MoTe_2$ synaptic transistor. (e–g) Illustration of the band energy diagram of the device with trap sites at the $MoTe_2/SiO_2$ interface under different gate bias conditions: (e) neutral, (f) positive bias, and (g) negative bias.

structure of the device. We used the tape method to exfoliate and transfer a layer of $MoTe_2$ onto a SiO_2/Si substrate. Si served as a back-gate electrode, whereas the SiO_2 layer served as a gate dielectric layer. Using the pre-patterned alignment-assisting marks, we formed patterns for the source and drain electrodes *via* photolithography and deposited Cr/Au electrodes *via* e-beam evaporation followed by the lift-off process.

First, we evaluated the electrical characteristics of the device as a transistor. Fig. 1c shows the output characteristics for drain biases from 0 to 1 V, with the gate bias changing from 1 to 30 V. The current increased as the gate bias increased, indicating that the device is an n-type. The highly linear *I–V* curves at a small bias suggested the successful formation of ohmic junctions. The transfer characteristics in Fig. 1d show that the current could be modulated by the gate bias ranging from −40 to 40 V. The I_{max}/I_{min} ratio was approximately 10^4 in this range. Importantly, the device exhibited a hysteresis of approximately 10 V in this V_g sweep range. Although such hysteresis is not favorable for ordinary transistor applications, it plays a positive role in synaptic transistors.

The hysteresis of the device was mainly attributed to the traps in the channel/dielectric interface (Fig. 1e–g). We assumed that there exists a high density of traps at the $MoTe_2/SiO_2$ interface (Fig. 1e), as deduced from the hysteresis in the transfer characteristics. When a positive bias was applied at the gate, more electrons were captured by the trap sites (Fig. 1f), and these accumulated electrons shifted the threshold voltage positively. In contrast, when a negative bias was applied at the gate, the electron field emptied the electrons, resulting in a negatively shifted threshold voltage (Fig. 1g). These effects combined to yield the hysteresis.

Synaptic characteristics and short-term memory functions

Next, we evaluated the synaptic properties of our device, measuring the similarity with biological synapses. In a biological synapse, the action potential in a pre-neuron makes its axon terminals release the neurotransmitters. The post-neuron's dendrites capture the neurotransmitters, and depolarization is induced in the cell membrane. Once the depolarization exceeds a threshold, the post-neuron fires the action potential.[25] Similarly, in a synaptic transistor, a potential spike in the gate electrode induces electron release/trapping in the channel, which results in spikes in the drain current.

First, we measured the excitatory post-synaptic current (EPSC) of the device. We investigated how the EPSC changes as a function of amplitude and pulse duration. Fig. 2a shows the EPSC characteristics with different gate pulse amplitudes of −5, −10, −15, and −20 V and the same duration of 500 ms. Because the negative pulse to the gate extracts the trapped electrons, we observe a strong current response in the source–drain channel (*i.e.*, EPSC) after the pulse. The increased current (EPSC)

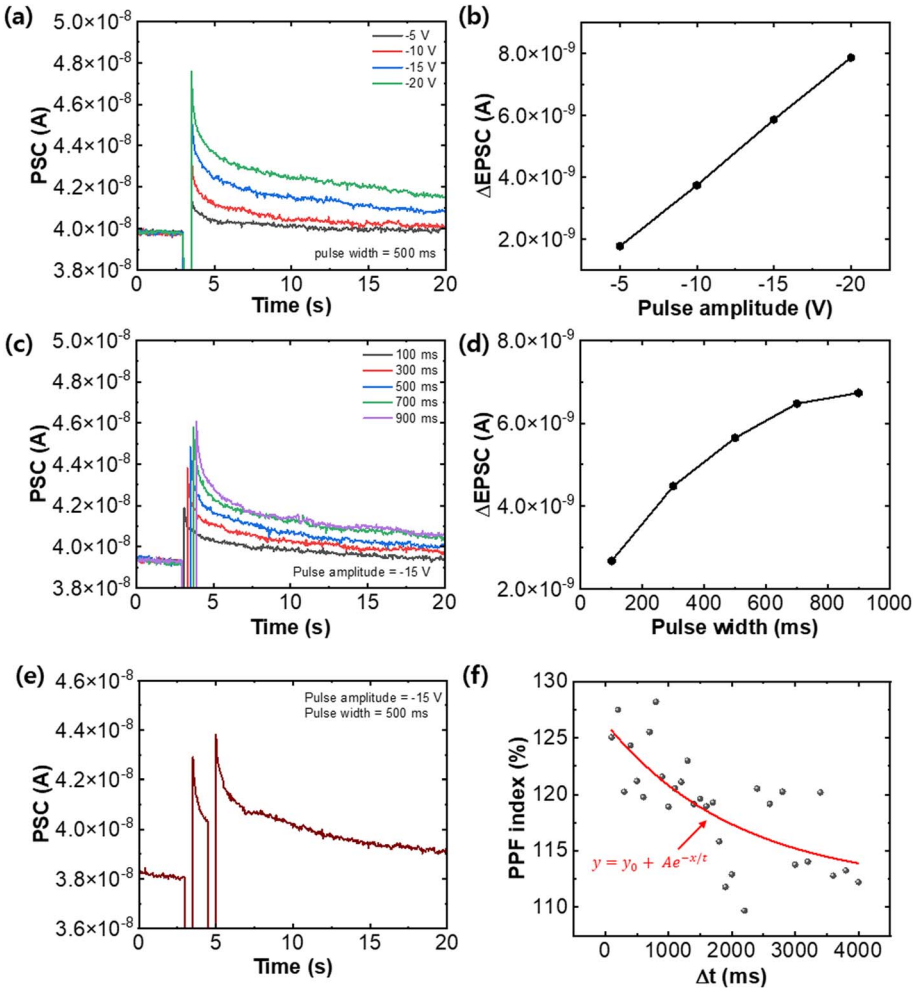

Fig. 2 Synaptic characteristics of the device. (a) and (c) EPSC response of the device for different voltage pulses: (a) for various pulse amplitudes with a fixed width and (c) for various pulse widths with a fixed amplitude. (b) and (d) EPSC index extracted from (a) and (c): (b) EPSC index for different pulse amplitudes from (a) and (d) EPSC index for different pulse widths from (c). (e) Paired pulse facilitation (PPF) characteristics of the device. (f) Change of the PPF index as a function of Δt.

decayed to its initial state because of the recapture of electrons in the trap sites. The EPSC index—defined as the maximum EPSC minus the initial current level—was proportional to the pulse amplitude (Fig. 2b). Similarly, the plots in Fig. 2c show the EPSC under different pulse durations of 100, 300, 500, 700, and 900 ms and a fixed amplitude of −15 V, revealing that the EPSC increases with greater pulse width. The EPSC index was proportional to the pulse width (Fig. 2d).

We evaluated the synaptic plasticity—the ability to change the synaptic strength to adapt to certain activity—by investigating the paired pulse facilitation (PPF) characteristics. PPF measures the change in synaptic strength upon two consecutive pulses. It represents the short-term change of the synaptic connection and can be related to the short-term memory function of the synaptic system.[26,27]

Fig. 2e shows the PPF plots upon two consecutive pulses, with an amplitude of −15 V, pulse width of 500 ms, and pulse-to-pulse separation of 1500 ms. The first pulse increased the current to A_1, and the current decayed within a period of Δt. After the second pulse, the current increases again, and the peak current was higher than the initial state (A_2). The overall increase divided by the first increase is called the PPF index, which is defined as $100\% \times A_2/A_1$. The PPF index shows how the consecutive pulse is effective in changing the synaptic strength. Fig. 2e shows that the application of a series of pulses can further facilitate the synaptic strength (conductivity), which can be maintained for a short period.

We investigated how the pulse-to-pulse delay affects the PPF index. Fig. 2f shows the distribution of the PPF index as a function of the pulse-to-pulse delay (Δt). Although the distribution showed some stochastic behavior, the overall trend was a decreasing PPF index with increasing delay, indicating that the frequency of the stimulus plays an important role in short-term memory. We fitted the trend using an exponential function:[28–33]

$$y = y_0 + Ae^{-x/t_1}$$

where y_0 and A are constants representing the initial facilitation magnitudes, and t is the characteristic relaxation time

corresponding to the decay.[34,35] The fitting yielded the following results: $y_0 = 111.7$, $A = 14.62$, and $t = 2100$ (unit: ms). We expect that appropriate engineering of the $MoTe_2/SiO_2$ interface can improve the stochastic nature of our device. It should be noted that even in biological synapses, the PPF behavior is often approximated using the single exponential decay.[36]

Long-term memory functions and simulation study for application in artificial neural network

Long-term memory (LTM) characteristics or potentiation-depression (PD) characteristics can be achieved by applying a train of multiple pulses.[37] Fig. 3a shows the PD behavior of the device when a series of 50 potentiating (−5 V) and depressing (+5 V) pulses were applied. The pulse series gradually modulated the conductivity of the device in an approximate range of 8.0 nA. Fig. 3b shows the reliability of the PD behavior during 70 PD cycles (7000 pulses). In addition, the current was uniformly modulated under extended pulse cycles (Fig. 3b), demonstrating the device's ability to reliably modulate pulse-induced current.

From the statistical information of the device's PD behavior, we performed a simulation to investigate the potential of the device for use in a fully hardware-based neural network. We used the CrossSim simulator in the present study.[38] During the simulation, all the connections in the neural network were implemented using the conductivity of the device, which was controlled by the application of electrical pulses. Fig. 3c shows a schematic of the setup. For the simulation, the statistical behavior of the device in potentiation/depression was modeled for the conductivity update (Fig. 3d). The plots represent the cumulative probability of the conductivity change (y-axis) for a given conductivity (x-axis) for potentiation (left) and depression (right). For the potentiation process, at a small conductance (30 nS), the expected ΔG was large and stochastic,

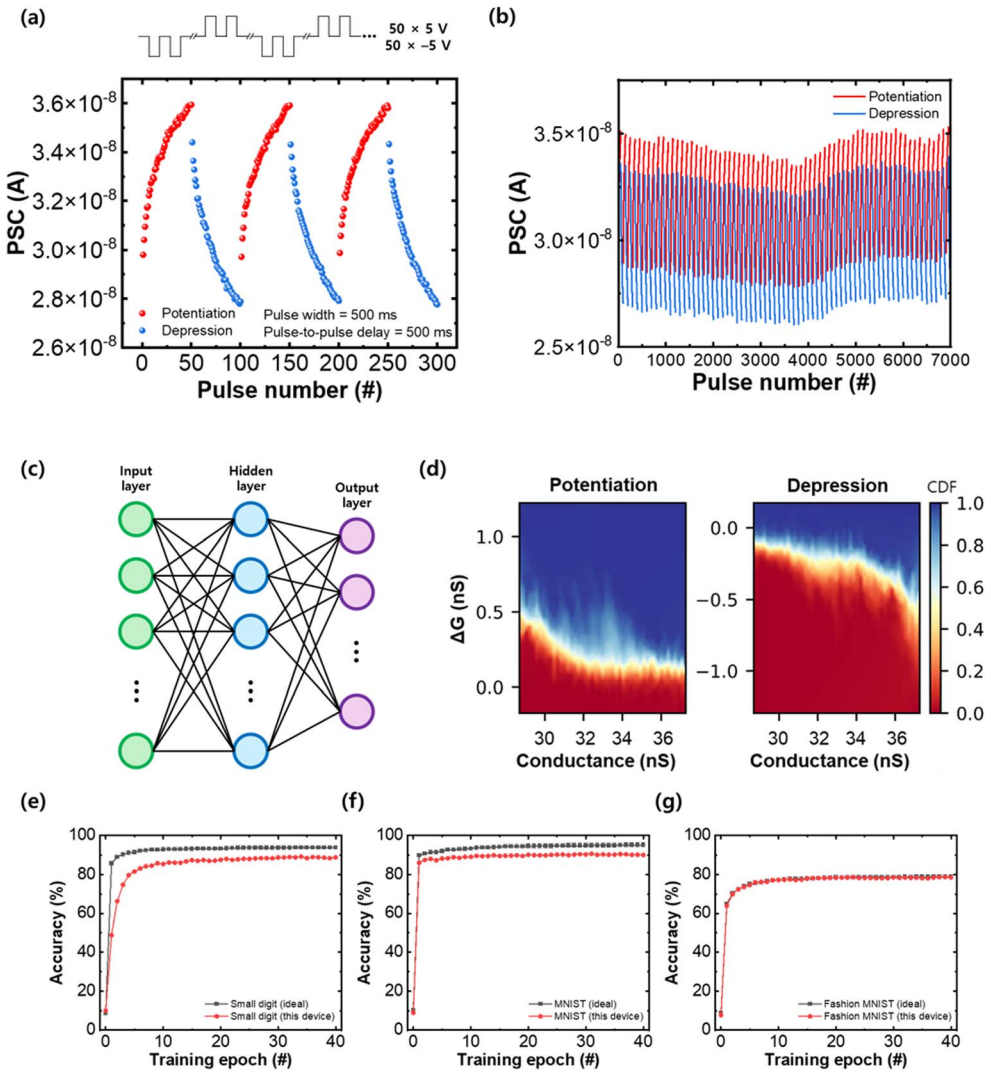

Fig. 3 (a) Potentiation–depression (PD) characteristics of the device for three cycles. (b) PD behavior measured for 7000 pulses (70 PD cycles). (c) Structure of the neural network used in the simulation. (d) Heatmap plots of the cumulative probability distribution of the conductance change in potentiation and depression. (e)–(g) Prediction accuracy of the simulated neural network with the number of training epochs. The black curves represent the results of the ideal numeric model, and the red curves show the simulation results for the device. (e) Small digits (8 × 8 pixels), (f) MNIST (28 × 28 pixels), and (g) Fashion-MNIST (28 × 28 pixels) are the datasets used in the simulation.

indicating that a single pulse can quickly potentiate the conductivity. Once the conductivity was greater than 32 nS, the expected ΔG was small and stable ($\sim$0.1 nS). For the depression process, the expected ΔG was highly negative for high conductance ($\sim$36 nS), indicating that a single pulse effectively lowered the conductivity when it was near the saturation value. For medium and small conductivities, the expected ΔG for a single pulse was uniformly distributed near -0.1 nS.

From this statistical data, we conducted a simulation to predict the accuracy of the hardware-based neural network. We carried out a classification task for three different datasets: small handwritten digits (small digits), the standard MNIST dataset, and the Fashion-MNIST dataset. The accuracy for each epoch is plotted in Fig. 3e (small digits), Fig. 3f (MNIST), and Fig. 3g (Fashion-MNIST).[39–41] For the small-digit case, the device achieved an accuracy greater than 88.9%, which was approximately 5% lower than the accuracy in the ideal numerical-calculation-based case. For MNIST, the achieved accuracy was 90.7%, which was approximately 5% lower than the ideal case. For the Fashion-MNIST dataset, both the ideal case and our device achieved relatively low accuracy (78.9% and 78.5%, respectively). Nevertheless, the accuracies of $\sim$90% for small-digit classification and $\sim$80% for the Fashion-MNIST dataset suggest that the $MoTe_2$ artificial electronic synapse has strong potential for use in future hardware-based neural networks.

Discussion on the origin of synaptic behavior

We hypothesized that the synaptic behavior of the $MoTe_2$ device mostly originated from the interfacial trap sites at the $MoTe_2$–SiO_2 interface. To further evaluate this hypothesis, we compared the synaptic behavior of the device with h-BN layers inserted at the $MoTe_2$–SiO_2 interface, where the $MoTe_2$ channel was employed from the same flake for fair comparison (Fig. S1†). Owing to their dangling bond-free surface, h-BN layers can reduce the interfacial trap sites when inserted at the $MoTe_2$–SiO_2 interface.[42] The overall synaptic behavior of the h-BN-inserted device is shown in the ESI (Fig. S1–S7).† The h-BN-inserted device exhibited similar *I–V* characteristics but with a reduced hysteresis range (Fig. S2†). The EPSC characteristics for different pulse amplitudes and pulse widths are plotted in Fig. S3.† The EPSC response is reduced and more stochastic compared with the device without h-BN (Fig. S3b and d†). We interpreted this as a result of the reduced trap sites at the $MoTe_2$–SiO_2 interface. The change in the PPF index as a function of time difference (Δt) is shown in Fig. S4,† indicating its decreasing behavior. Importantly, the PD behaviors (Fig. S5†), extracted conductance change behaviors (Fig. S6†), and the prediction accuracy in a simulated neural network (Fig. S7†) suggested that the h-BN-inserted device was less effective in terms of the artificial synapse.

A good ohmic contact is an important factor for achieving a reliable synaptic behavior. Another $MoTe_2$ device fabricated without h-BN layers exhibited Schottky barriers at source and drain junctions, as described in Fig. S8.† While the device exhibited similar synaptic behaviors, as summarized in Fig. S9,† the stochasticity in the synaptic behavior resulted in limited prediction accuracy (Fig. S10†). Thus, charges can be trapped or released at the source or drain junctions with a certain energy barrier, which can lead to randomness in the response, degrading the synaptic performance.

Application to physical reservoir computing

Most importantly, we demonstrated the application of our device to PRC by classifying 8 $\times$ 8 grayscale handwritten digits.[43] Fig. 4a illustrates PRC for digit classification. The image was processed into horizontal and vertical slices. Pixel intensity values of the 16 sequences (8 horizontal and 8 vertical slices) were converted into voltage sequences and then fed to the gate electrode of the device with a constant drain bias (1 V). We recorded the current response to these voltage-pulse sequences. Finally, the last values (after the 8th pulses, 16 values) or the middle and last values (after the 4th and 8th pulses, 32 values) of the recorded current plots were used as readout nodes, and the connection between the readout nodes and output nodes (0–9) was trained. Among 1100 images, 80% were used for training and 20% were used for the test. Notably, the information was preferably processed in parallel (*i.e.*, by applying 16 voltage sequences into 16 different devices). However, because of the limited number of available devices, we conducted pulse application and current recording in series from a single device.

Fig. 4b and c show the accuracy of the PRC using models with 16 and 32 readout nodes, respectively. The model with 16 readout nodes used the lowest number of connections (160 connections) for training/inference and exhibited moderate accuracy of 79.22% and 72.42% (left panel of Fig. 4b) for both the training and test data, respectively. The confusion matrix in the middle panel of Fig. 4b indicates that digits such as 1, 5, and 8 are difficult to distinguish. The weight of each connection to a single output "2" after 1000 epochs of training is shown in the right panel of Fig. 4b; only 16 connections are used for each digit (total of 160 connections for all outputs). When the model with 32 readout nodes was used (Fig. 4c, left), the accuracy for the training increased to 95.32%, and the accuracy for the test reached 92.42%. The confusion matrix (middle panel of Fig. 4c) shows that most digits are well recognized except digit 1. The weight distribution for the single digit (right panel of Fig. 4c) shows the strengths of connections from 32 readouts to output "2". We also performed the ideal case, where all of the values in the image were directly connected to the output (64 connections per output node, total of 640 connections). In this case, both the training and test accuracies reached 100% and 95.45%, respectively, indicating superior performance (data are not shown here). However, it should be noted that 640 connections were used for training and inference, thus consuming more computational resources than our PRC cases. For this PRC, the device described in the ESI (Fig. S8–S10)† was used.

Comparison with the state-of-the-art electronic artificial synapses using 2D materials

To compare the efficiency of the prepared device, we summarized the recent advances in the electronic synapses using 2D materials, as listed in Table 1.

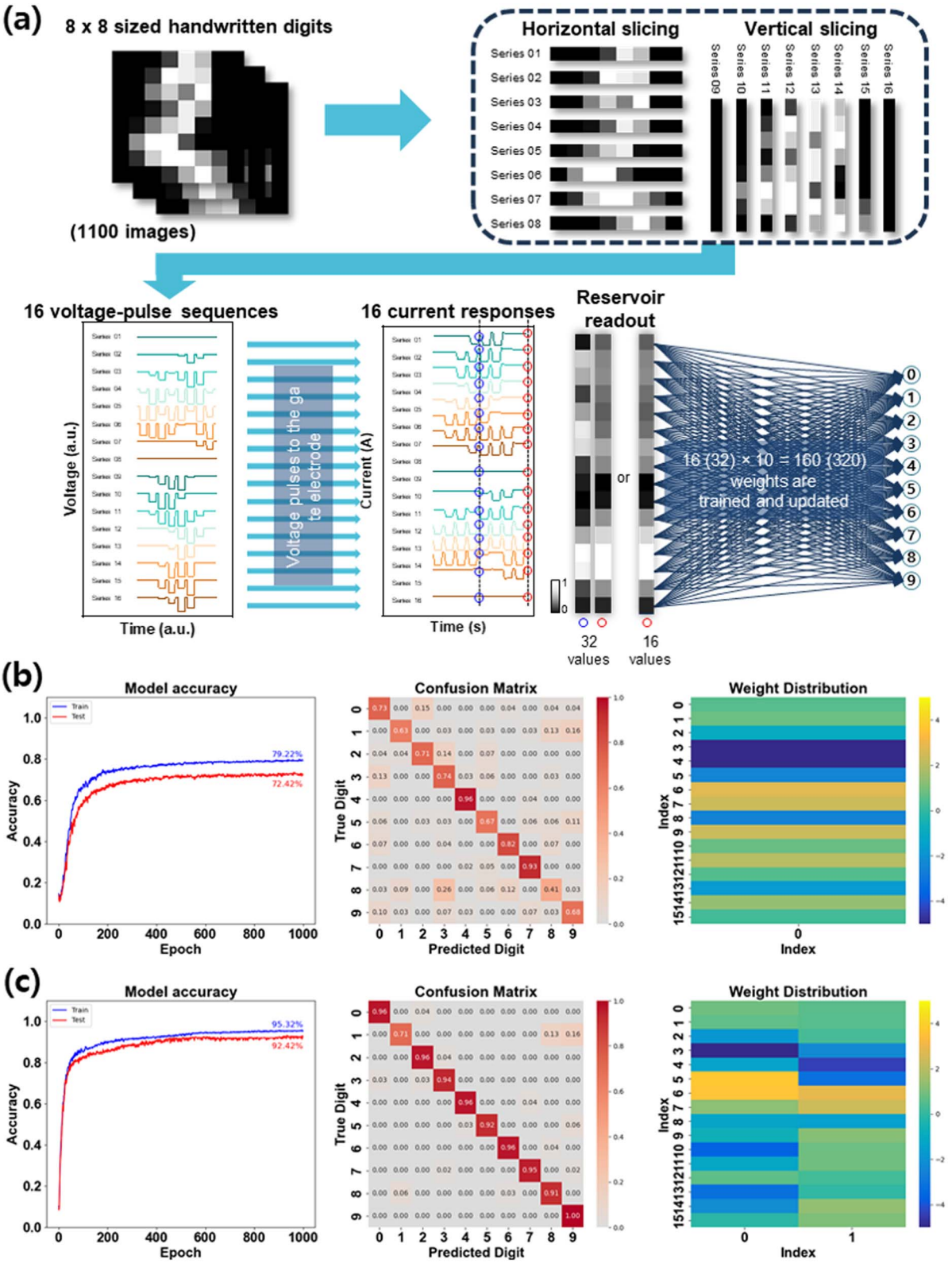

Fig. 4 Classification of handwritten digits using PRC. (a) Schematic of the processing pipeline for small (8 × 8 pixels) images of handwritten digits, where images are converted into pulse signals, readout values are obtained from the current responses, and connections between readout values and output nodes are trained. (b) and (c) Training and inference results of PRC, including classification accuracy plots over epochs for the training dataset (blue line) and test dataset (red line), confusion matrices, and weight distribution heatmaps for the digit "2". Results are shown for both 16-valued and 32-valued readout versions of PRC.

Table 1 Recent works on electronic artificial synapses using 2D materials

Device structure	Channel	Mechanism	Emulated synaptic functions	MNIST accuracy	Physical reservoir computing	Ref.
MoS_2/h-BN/FLG	MoS_2	Floating gate charge trapping	EPSC, IPSC, PD	97.7%	N/A	44
SnS_2/HZO	SnS_2	Ferroelectric gate switching	PPF, PD, STDP	94%	N/A	45
MoS_2/h-BN/graphene	MoS_2	Floating gate charge trapping	PPF, PD, STDP	N/A	N/A	46
MoS_2/SiO_2	V-doped MoS_2	Doping-induced trap	PD	N/A	N/A	47
h-BN/BLG/h-BN	BLG	Moiré-induced ferroelectricity	EPSC, PPF, PD	N/A	Binarized digit recognition	48
MoS_2/SiO_2	MoS_2	Interface charge trapping	PD	N/A	Binarized digit recognition	49
$MoTe_2$/SiO_2	$MoTe_2$	Interface charge trapping	EPSC, PPF, PD	90.7%	Gray scale digit (8 × 8) recognition	This work

Overall, our work articulated two important milestones in 2D-material based electronic artificial synapses. First, we showed that $MoTe_2$ with a semi-conducting phase can be utilized as artificial synapses in combination with charge trapping, confirming the potential of $MoTe_2$ for broader application in neuromorphic computing devices. Second, we demonstrated its more realistic example of physical reservoir computing. Moving forward from classifying the binarized, simplified digits, we showed that the concept of physical reservoir computing can be utilized in classifying general gray-scale images using the $MoTe_2$ artificial synaptic devices.

Conclusion

We fabricated $MoTe_2$-based artificial electronic synapses, characterized their synaptic behaviors, and used them in PRC for classifying grayscale handwritten digits. The fabricated device exhibited the features of an n-type field-effect transistor with hysteretic transfer characteristics. Because of this hysteresis, the device showed good synaptic properties, including good EPSC and PPF. The conductance of the device could be further modulated by applying multiple pulses, with moderate linearity. The simulation study conducted on the basis of these results suggested that the device can achieve good accuracy when integrated into a hardware-based neural network. Most importantly, on the basis of the device's fading memory characteristics, we conducted PRC to classify grayscale handwritten digits (8 × 8 resolution). By encoding the image into voltage pulse sequences that resemble horizontal and vertical slices of the image, feeding them into the device, and using the resultant current as readout nodes, we achieved good accuracy with reduced computation for training and inference. Overall, this research confirms the potential of 2D-material-based artificial synaptic devices for PRC and energy-efficient AI systems.

Experimental

Device fabrication

$MoTe_2$ flakes with a thickness of 10 nm were obtained through mechanical exfoliation and subsequently dry-transferred onto SiO_2 (300 nm)/Si substrates using polydimethylsiloxane (PDMS). Photolithography employing LOR 3B and AZ5214E photoresists was used to create the desired electrode patterns. Finally, Cr/Au (10/50 nm) layers were deposited by electron beam evaporation at a deposition rate of 0.2 Å s^{-1} under a vacuum of 10^{-6} torr.

Electrical characterization and neural network simulation

Electrical characterization was performed on a probe station using two source-meter units (Keithley 2450 source-meter unit, Tektronix). The source-meter units were controlled using homemade *I–V* measurement software written in Python.[50] Classification by neural network simulation was performed using CrossSim software, which utilizes open libraries such as scikit-learn, SciPy, TensorFlow, *etc.* The classification was performed using PD data obtained through electrical characteristic measurements.

Physical reservoir computing

For the PRC experiment (small MNIST numerical classification), we used homemade software written in Python. The voltage signal was generated by the software and passed to a 2450 source meter unit (Tektronix). Throughout the experiment, two separate source-meter units were used to impose defined drain and gate biases while simultaneously recording the corresponding current responses.

Data availability

Data for this article, including dataset and codes, are available at figshare at **https://doi.org/10.6084/m9.figshare.28642523**.

Conflicts of interest

The authors declare no competing interests.

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