RSC Advances

REVIEW

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Cite this: *RSC Adv.*, 2025, **15**, 14428

Quantum dot-based non-volatile memory: a comprehensive outlook

Abu Taher,[a] M. Atikur Rahman,[ab]* Rana Mia,[a] Nasir Uddin,[b] Mustavi Islam,[c] M. N. I. Khan,[d] M. Khurshed Alam[e] and Mohammad A. Alim*[a]

Received 22nd November 2024
Accepted 28th March 2025

DOI: 10.1039/d4ra08307e

rsc.li/rsc-advances

With the rise of digital technology, the use of memory devices is swiftly expanding, and this trend is expected to continue in the forthcoming years. Accordingly, researchers are exploring materials that surpass the performance of those used in traditional memory devices, and notably, there is a considerable interest in quantum dots (QDs). This is primarily due to the fact that quantum dots possess exceptional optical and electric properties. As a result, they have become appealing materials to enhance the performance of non-volatile memory devices. In this review, we outlined the various approaches employed for the synthesis of quantum dots as well as different types of quantum dots used for prototyping different non-volatile memory technologies and their current perspective. Additionally, we compared various key parameters, such as the ON/OFF ratio, retention time, memory window, charge trapping capacity, and multiple voltage levels, of these QD-based memories together with future outlook.

1. Introduction

With digitization expanding across various domains, from personal gadgets to automated industries, the demand for memory devices is increasing rapidly.[1–7] A crucial component of the majority of contemporary electronic devices is non-volatile memory (NVM) devices. Computer memory that keeps recorded information even when the power is turned off belongs to NVM systems. NVM is utilized for long-term data storage in a variety of applications, such as firmware, embedded systems, and mass storage devices, such as USB flash drives and solid-state drives (SSDs), in contrast to volatile memory, such as random access memory (RAM), which needs constant power to preserve data. Non-volatile memory technologies have undergone substantial advancements over time. Initially, the foundation of NVM was floating gate MOS transistors, which facilitated the development of NAND flash memory. NAND flash is extensively used owing to its increased density and economical cost. Nevertheless, when technology progressed beyond the 20 nm node, conventional NAND flash faced significant constraints, including scaling challenges, high power consumption, and restricted durability.[8] Alternatively, various emerging NVM technologies, including all-optical switching, magnetic tunnel junction (MTJ), resistive random access memory (ReRAM), phase change memory (PCM), spin–orbit torque magnetic random-access memory (SOT-MRAM), and spin-transfer torque magnetic random-access memory (STT-MRAM), offer retention periods exceeding 10 years while improving the memory endurance capability. Endurance of approximately 10^5 cycles has been reported for CdSe QD-based resistive memory.[9] The latency for read and write operations in these memories falls within the range of 1 to 7 ns, demonstrating a significant improvement over flash memory and other charge-based memory, such as dynamic random access memory (DRAM) and electrically erasable programmable read-only memory (EEPROM).[10]

In the last few years, there has been significant interest in quantum dots (QDs) in the fields of electrical engineering, materials science, and physics.[11] Quantum dots (QDs) are inorganic semiconductor nanoparticles characterized by a radius smaller than that of Bohr excitons.[12–14] The nanoscale size (typically 2–10 nm) and quantum confinement of these nanocrystals result in unique optical and electrical properties. These are crystalline materials whose nanoscale dimensions can be considered negligible. Owing to the confinement of excitons in all three spatial directions, these nanocrystals have quantum mechanical characteristics.[15–17]

The pursuit of devices characterized by high speed, scalability, and reliability has led to extensive investigations into memory devices based on QDs in recent times. The scientific

[a]*Department of Electrical and Electronic Engineering, University of Chittagong, Chittagong-4331, Bangladesh. E-mail: atikursomon1@gmail.com; mohammadabdulalim@cu.ac.bd*

[b]*Department of Electrical and Computer Engineering, University of Missouri Kansas City, Missouri, USA*

[c]*Department of Computer Science, University of Missouri Kansas City, Missouri, USA*

[d]*Material Science Division, Bangladesh Atomic Energy Commission, Dhaka-1000, Bangladesh*

[e]*Department of Physics, Bangladesh University of Engineering and Technology, Dhaka-1000, Bangladesh*

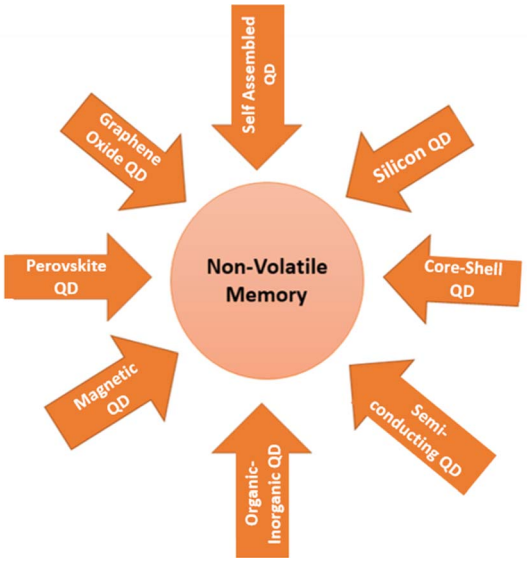

Fig. 1 Various quantum dots used in non-volatile memory.

community is experimenting with various quantum dots such as perovskite quantum dots (PQDs), self-assembled quantum dots (SAQDs), magnetic quantum dots (MQDs), core–shell quantum dots (CSQDs), metal oxide quantum dots (MOQDs), metal alloy quantum dots (MAQDs), graphene oxide quantum dots (GOQDs), graphene quantum dots (GQDs), and silicon quantum dots (SiQDs) for application in non-volatile memory.[18–32]

Quantum dots possess an adjustable bandgap, allowing precise control of their electrical and optical characteristics *via* size adjustment. This tunability facilitates the tailoring of quantum dots for particular memory applications, hence improving their performance and efficiency.[33] The characteristics of quantum dots, including charge storage capacity and energy levels, are significantly influenced by their dimensions. This size dependence facilitates the construction of memory devices with customized attributes, such as multi-level storage, which may substantially enhance the data storage density.[34] Quantum dot materials possess many exceptional qualities, including scalability,[33] compatibility with semiconductor production,[33,34] enhanced charge retention, and stability.[34] Besides, QD-based memories have superior retention times, enhanced ON/OFF ratios, increased charge trapping capacity, multiple storage voltages, low power consumption, and tunable bandgaps, making them very attractive candidates for non-volatile memory applications. These attributes also make quantum dots promising materials for data storage. Fig. 1 illustrates various types of quantum dots and their applications in non-volatile memory device prototyping. Different types of QDs can bring unique advantages towards NVM systems. For examples, self-assembled quantum dots have improved chemical stability and charge retention capacity, enabling longevity and fast read/write operation of NVM.[11] Core–shell quantum dots show improved quantum yield (QY) and faster carrier transfer, reducing the excitation recombination losses. Also, they can be integrated with other semiconductors during the fabrication process. These crucial properties make CSQDs another promising agent for NVM.[35] Graphene oxide quantum dots also exhibit fast read/write operation for (ReRAM) applications.[20,36,37] Graphene-based quantum dots have high electrical conductivity, extensive surface area, minimal operating voltage, rapid switching speed, and enhanced quantum confinement, making them promising materials for non-volatile memory systems.[29–31]

The major goal of this review is to determine how various types of quantum dots may be used to improve the performance of non-volatile memory systems. We summarize their synthesis processes, working mechanisms, switching properties, ON/OFF ratios, multiple levels and overall potential as transformational materials in the realm of data storage. By analyzing the benefits and drawbacks of each form of quantum dots, we aim to give insights into the future orientations of non-volatile memory technology and the role of quantum dots in its evolution.

2. Prospects and challenges of QDs in NVM technology

Quantum dots show excellent charge transfer capacity due to their unique electronic structure and ultra-low energy consumption. This enables more efficient data storage and retrieval in NVM cells.[15,38] In addition, the optical tuning capabilities of QDs are opening new horizons for the creation of photonic memories, where it is possible to control memory devices using light. Quantum dots (QDs) offer several advantages for non-volatile memory (NVM) devices over conventional material across various aspects.

2.1 Scalability

Quantum dots (QDs) significantly enhance the scalability of non-volatile memory (NVM) devices. The electronic properties of QDs are size-dependent, allowing precise control of their behavior by adjusting their size. This is crucial for scaling down memory devices, given that smaller QDs can be used to create more densely packed memory cells. In conventional floating-gate (FG) MOSFETs, the floating gate is a continuous layer that stores charge. As the device scales down, the gate dielectric thickness must also decrease, leading to reliability issues such as charge leakage and dielectric breakdown. Alternatively, QDs act as discrete charge storage nodes. This discrete nature reduces the risk of charge leakage and improves the reliability of the memory device. The tunnel oxide in FG MOSFETs becomes less resistant to defect formation as it scales down, which can cause data loss. In QD-based NVMs, the tunnel oxide can be thicker, while still allowing efficient charge trapping and de-trapping due to the quantum confinement effect. This improves the reliability and endurance of the memory device.

2.2 Power consumption

The quantum confinement effect in QDs enables them to operate at lower voltages compared to bulk materials. This is because the energy levels in QDs are quantized, allowing more

Table 1 Comparison of QD-based NVM with conventional materials

Aspect	Quantum dots (QDs)	Conventional bulk materials
Scalability	-Better scaling	-Limited by gate dielectric thickness and reliability issues
Power consumption	-Lower operating voltages due to efficient charge trapping and de-trapping -Reduced leakage currents due to discrete charge storage nodes	-Higher power consumption due to continuous floating gate -Significant leakage currents, especially at smaller scales
Endurance	-Improved endurance with discrete and isolated charge storage nodes -Reduced defect formation in thicker tunnel oxide	-Higher risk of charge leakage and degradation over time -Tunnel oxide more prone to defects and charge loss
Retention	-Enhanced retention -GeO_x cladding provides electrical and physical isolation	-Lower retention for higher charge leakage -Continuous floating gate more susceptible to charge loss

precise control of their charge states, which allows efficient charge trapping and de-trapping. This efficiency reduces the energy required to write and erase data. In conventional floating-gate (FG) MOSFETs, the continuous floating gate requires higher voltages to move charges in and out, leading to higher power consumption. As a result, QD-based NVMs can achieve the same functionality as conventional devices but with significantly lower power requirements.[39] Another concern related to power consumption is the leakage current. In conventional NVM devices, leakage currents can significantly contribute to the power consumption, especially as the device scales down. As mentioned, discrete and isolated charge storage nodes also reduce the likelihood of charge leakage. This isolation helps maintain the stored charge without a continuous power supply, thereby reducing the static power consumption.

2.3 Endurance/retention

Endurance refers to the ability of a memory device to withstand numerous program/erase cycles without degradation. QD-based NVMs exhibit improved endurance due to several factors. As an example, the aforementioned fact of reduced charge leakage minimizes the wear and tear on the tunnel oxide layer, which is a common issue in conventional floating-gate transistor memory. The tunnel oxide in QD-based NVMs can be thicker compared to the conventional NVMs, which improves its resistance to defect formation. This reduces the likelihood of charge loss and enhances the endurance of the memory device. The thicker tunnel oxide in QD-based NVMs not only improves the endurance but also enhances the retention by reducing the likelihood of charge leakage through defects. Retention refers to the ability of a memory device to retain stored data over time. QD-based NVMs exhibit enhanced retention due to their quantized energy levels, which makes it more difficult for the trapped charge to escape. In some QD-based NVMs, QDs are clad with materials such as germanium oxide (GeO_x). This cladding provides electrical and physical isolation, preventing lateral dot-to-dot conduction and reducing charge leakage.[33] Also, controlling the solvent or ligand can control the interatomic distance, which will be discussed in the next section. These facts favor QD high-speed operation in memory devices. For example, GeO_x-cladded Ge QDs have shown a negligible shift in threshold voltage over a period of one year (Table 1).[40]

2.4 Optimizing the performance of ligand-assisted QDs

The use of insulating ligands during the synthesis of quantum dots (QDs) can significantly impact the performance of non-

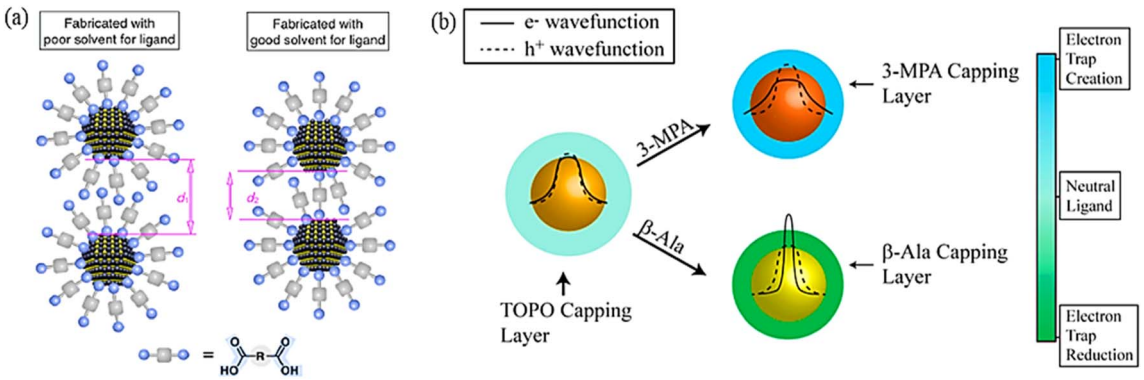

Fig. 2 (a) Effect of solvent on atomic distance. (b) Capping layer effect of 3-MPA and β-Ala on transport properties. Reproduced from ref. 41 with permission from RSC. Copyright 2013, RSC.

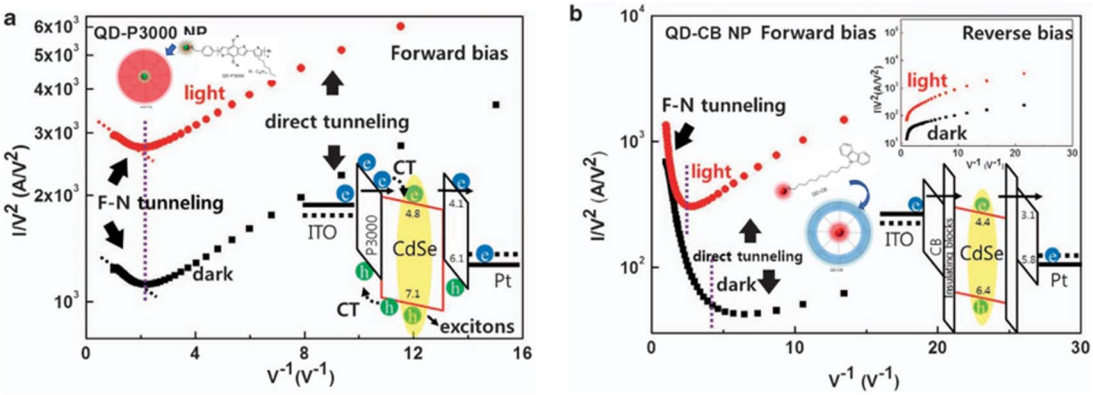

Fig. 3 Fowler–Nordheim (F–N) and direct tunneling models under dark and light conditions with (a) forward conditions of QD-P300 and (b) reverse bias of QD-CB NPs. Energy diagram is shown in the inset. Reproduced from ref. 42 with permission from Springer-Nature.

volatile memory (NVM) devices. These ligands, often long-chain organic molecules such as oleic acid, stabilize the QDs but also hinder charge transport between them. This can reduce the efficiency of NVM devices by limiting the movement of charge carriers, which is crucial for device operation. Thus, to address this issue, researchers often employ ligand exchange techniques to replace these long, insulating ligands with shorter, more conductive ligands. This improves the electronic coupling between QDs, enhancing the charge transport and overall device performance. In this case, sometimes the choice of solvent affects ligand-assisted QDs. Fig. 2(a) shows that employing an appropriate solvent, the interatomic distance can be controlled for the better functionalization of QDs.

When QDs are capped with long, insulating ligands, the distance between the QDs is relatively large, and the electronic wavefunctions of the QDs do not overlap significantly. This results in weak electronic coupling and poor charge transport. Thus, by replacing long, insulating ligands with shorter, more conductive ligands, the distance between QDs can be reduced, allowing their electronic wavefunctions to overlap more. This stronger overlap enhances the electronic coupling, facilitating more efficient charge transfer between QDs. This is because the overlapping electronic wavefunctions create pathways for charge carriers to hop or tunnel from one QD to another in non-volatile memory networks. Hines *et al.*[41] explained the effects of various ligands on the surface of QDs and their influence on the electron wavefunction, as shown in Fig. 2(b). TOPO is a common ligand employed for the synthesis of CdSe QDs, which stabilizes the QDs and protects their surface. In the presence of this ligand, the wavefunctions of electrons and holes are confined to the core of the QDs. The TOPO ligand does not create trap states on the surface of the QDs, and thus the wavefunctions of electrons and holes are generally confined to the core of the QDs. 3-Mercaptopropionic acid (3-MPA) is a thiol-based ligand that creates trap states on the surface of QDs. In the presence of this ligand, the electron wave function is extended towards the surface of QDs, as the thiol group creates electron trap states on the surface of QDs. These trap states prevent electron–hole pair separation and slow down the electron transfer process. β-Alanine (β-Ala) is an amino acid ligand that fills the trap states on the surface of QDs. The amino group of this ligand fills the electron trap states on the surface of QDs and confines the electron wavefunction towards the core of the QDs. In the presence of the β-Ala ligand, the electron–hole pair separation improves and the electron transfer rate increases. Conjugated ligands can also induce changes in the tunneling mechanism of QDs. Fig. 3(a and b) show the analysis of the photoresponsive *I–V* characteristics of polythiophene conjugated CdSe QD (QD-P3000) and carbazole conjugated QD-CB nanoparticles (NPs) based on the Fowler–Nordheim (F–N) tunneling and direct tunneling models, respectively.

Fig. 3(a) shows the *I–V* characteristics of QD-P3000 NPs. At a high forward bias, F–N tunneling behavior is observed, indicating photo-induced charge transport. At a low bias voltage, direct tunneling occurs, where the charge flows across the triangular barrier. Fig. 3(b) shows the *I–V* characteristics of QD-CB NPs, where F–N tunneling occurs at a high bias and direct tunneling occurs at a low bias. However, compared to QD-P3000 NPs, the photo-induced charge transfer in QD-CB NPs is much weaker because of the insulating molecular block in the CB molecule. This image was used to analyze the photoresponsive charge transport, which showed that QD-P3000 exhibits more efficient charge transfer and photo-responsiveness, whereas QD-CB NP shows a poor charge transport performance. QD-P3000 has a direct n–p junction, which allows efficient energy and charge transfer. The QD-CB has an n-ins-p junction, where an insulating molecular block limits the charge transfer. In this case, ligand-assisted QDs can be optimized through engineering for efficient transport operation in memory devices.

3. Synthesis perspective of quantum dots

3.1 Bottom-up approach

3.1.1 Hydrothermal method. Core–shell quantum dots can be flexibly and cost-effectively prepared *via* hydrothermal synthesis.[43–46] The primary stages in this process are core preparation and shell development. Initially, stabilizing ligands

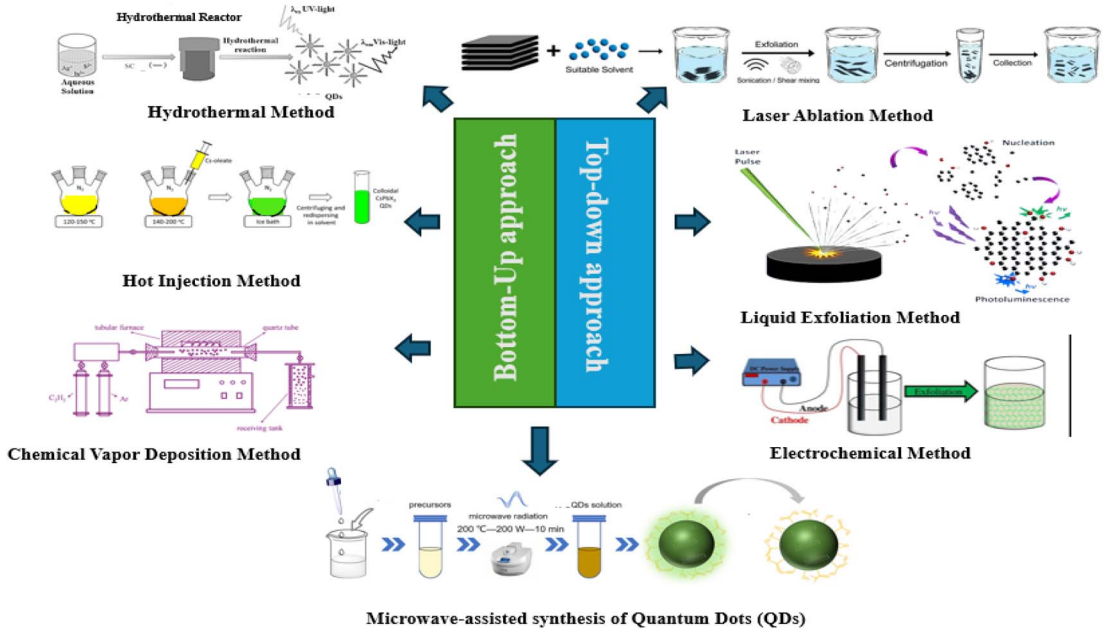

Fig. 4 Different synthesis approaches for quantum dots.

and a precursor for the core material, often a metal salt, are solubilized in a solvent such as ethanol and water. Researchers can control the dimensions and characteristics of core nanoparticles by adjusting variables such as temperature, reaction duration, and precursor ratios. These core particles are isolated during purification using methods such as centrifugation. The cleaned cores are re-dispersed in a new solvent in the shell development stage. Then, the shell precursor is dissolved in the same solvent as an additional stabilizing agent. Under carefully regulated stirring and temperature conditions, this shell precursor solution is gradually introduced in the core nanoparticle dispersion. To get a shell layer with the appropriate thickness and characteristics, careful control of the reaction time and temperature is essential. Lastly, centrifugation or precipitation is performed to separate the core–shell quantum dots from the unreacted components, similar to the core purification step. The purified core–shell QDs can be dried using methods such as rotary evaporation for storage, or they can be re-dispersed in an appropriate solvent depending on the desired usage. Hydrothermal synthesis enables the accurate regulation of the dimensions and morphology of core–shell quantum dots. Furthermore, structures with good regularity and great crystallinity are frequently produced by this approach. Also, it is regarded as an environmentally benign practice, especially compared to some other approaches. Nevertheless, there are drawbacks, such as scalability issues and trouble attaining incredibly fine control of the shell thickness. Further post-treatment procedures may occasionally be required to maximize the surface characteristics of the core–shell quantum dots.[47–49] Due to its overall affordability, strong degree of control of the final nanostructures, and relative simplicity, hydrothermal synthesis is still a useful technique for researchers (Fig. 4).[50–52]

3.1.2 Solvothermal method. One effective method for producing quantum dots (QDs), which are extraordinary nanoparticles with special characteristics based on light, is solvothermal synthesis. With the help of this approach, researchers can accurately regulate the composition, size, and shape of these tiny materials, which opens up a wide range of uses.[53,54] In this method, a small pot is used to develop a unique type of formulation. Precursors, the fundamental components of QDs, are one of the constituents (mainly metal salts or organometallic compounds). High-boiling-point solvents, such as ethylene glycol, are combined with the precursors to serve as the reaction medium in the presence of heat and pressure. Additionally, unique molecules known as ligands or stabilizers are introduced to regulate the development process and avoid undesired clumping. At this point, the formulation becomes intriguing. The mixture is heated to a precise temperature, often as high as 300 °C, while sealed inside a sturdy cylinder known as an autoclave. Similar to a pressure cooker, this heated and pressurized environment speeds up the reaction and encourages the creation of QDs. New QDs are formed when the precursors degrade and the ions that are left behind are guided to form small crystals by the ligands. Given that it dictates the final size of these nanoparticles, the reaction time is quite important. After cooking, the autoclave gradually cools down. After that, the mixture is cleaned, often using solvents or centrifugation, to get rid of any remaining components and separate the produced QDs.

Solvothermal synthesis is elegant because of its adaptability. Researchers can produce QDs with precise sizes, forms (ranging from spheres to rods), and even compositions by varying the types and quantities of components, reaction temperature, and reaction time. The light absorption and emission characteristics of these QDs can be further optimized by doping them with

additional components. There are various benefits to this approach. It works with a range of QD materials, is easily scaled up for larger volumes, and permits exact control of the features of QDs. Additionally, QDs with great uniformity in size and characteristics are frequently produced by solvothermal synthesis. However, to withstand the tremendous pressure and temperature involved, specific equipment is also needed. Furthermore, some solvents and precursors may be dangerous, necessitating cautious handling and appropriate waste disposal. Notwithstanding these drawbacks, solvothermal synthesis is still a vital method for producing functioning, high-quality quantum dots.[55–57] Scientists may unleash the enormous potential of these adaptable nanomaterials by carefully selecting the formulation and reaction conditions, opening the door to breakthroughs in solar cells, LEDs, bioimaging, and many other areas.[50,58]

3.1.3 Hot injection method. The hot injection method is a widely utilized technique for the synthesis of quantum dots (QDs).[59] This process relies on the rapid injection of a heated precursor solution to initiate the production of light-emitting nanoparticles, in contrast to the gradual heating characteristic of solvothermal synthesis. In this case, a pair of hot beakers is used, each containing one the required components. A heated precursor solution, often containing a metal salt such as cadmium selenide dissolved in a high boiling point solvent, is placed in one beaker, while a mixture of stabilizing ligands and a hot solvent is contained in the other beaker. These ligands, which are usually long-chain organic compounds or thiols, are essential for regulating the development of QDs and averting their unintended aggregation. The rapid introduction of the hot precursor solution into the ligand mixture results in significant changes. The significant rise in temperature acts as a catalyst for the rapid nucleation and growth of quantum dot crystals. The ultimate dimensions and morphology of the quantum dots are dictated by the controlled growth conditions established by the heated solvent and ligands. In this context, the reaction speed is essential, given that extended durations lead to an increase in the size of the quantum dots (QDs). The reaction mixture is usually quenched by quickly cooling it after the injection. The process of quenching aids in stopping the growth of the QDs at the target size and keeps them from aggregating. Ultimately, any unreacted precursors or byproducts are eliminated from the produced QDs by isolating them using purification methods including centrifugation and precipitation. The hot injection technique has several benefits. It is a relatively fast and simple procedure that not only allows considerable control of the dimensions and distribution of the QDs, but is also relatively rapid and easy in comparison to other methods. Furthermore, QDs with excellent optical characteristics and great crystallinity are frequently produced using the quick injection procedure. However, this approach also has drawbacks. The achievement of the intended QD properties depends on exact control of the injection temperature and time. Furthermore, the quality of the QDs may be impacted by the sensitivity of the hot injection process to air exposure. Hot injection synthesis is still the preferred method for researchers because of its simplicity, rapidity, and capacity to generate high-quality quantum dots despite of these drawbacks.[60–63] Through precise manipulation of temperature, time, and ingredient selection, scientists can utilize this technology to produce QDs with targeted properties for use in solar cells, displays, and bioimaging.[50]

3.1.4 Simple one-pot method. The one-pot method for the synthesis of QDs typically involves the use of a single reaction vessel, where all the necessary reagents are combined and heated under controlled conditions. This method removes the necessity for numerous purification stages and decreases the total synthesis duration. Appropriate precursors need to be chosen for the desired QDs. The common precursors include metal salts (*e.g.*, cadmium chloride and zinc acetate) and sulfur or selenium sources (*e.g.*, sodium sulfide and sodium selenide), respectively. A suitable solvent should be selected that can dissolve the precursors and maintain a stable reaction environment. The common solvents include organic compounds such as trioctylphosphine oxide (TOPO) and octadecylamine (ODA). A surfactant is added to stabilize the growing QD particles and prevent their aggregation. The common surfactants include TOPO and ODA. The prepared reagents should be placed in a reaction vessel, such as a three-necked flask. The reaction mixture must be heated to a specific temperature, typically between 200 °C and 300 °C. This temperature range is crucial for the nucleation and growth of QD particles. Maintenance of an inert atmosphere for synthesis (*e.g.*, nitrogen or argon) is an important step to prevent the oxidation of the reagents and QD particles. At an elevated temperature, the precursors react to form nuclei, which serve as starting points for the growth of the QDs. The nuclei expand by incorporating further atoms from the reaction mixture. The growth rate can be modified through the adjustment of variables such as temperature, precursor concentration, and reaction duration. Upon achieving the target quantum dot size, the reaction mixture is gradually cooled to ambient temperature. The cooling process stabilizes the QD particles and inhibits their additional growth. In certain instances, the synthesized quantum dots may necessitate purification to eliminate impurities and byproducts. This can be accomplished *via* precipitation utilizing a solvent that is incompatible with the quantum dots (QDs). The precipitated quantum dots can be isolated from the supernatant through centrifugation.[64–66] The one-pot method eliminates the need for multiple purification steps, making it a more straightforward process. By combining all the reaction steps in a single vessel, the overall synthesis time can be significantly reduced. This method can be scaled up to produce larger quantities of QDs, making it suitable for industrial applications.[50]

3.1.5 Chemical vapor deposition (CVD). Chemical vapor deposition (CVD) is a multifaceted method used for the synthesis of several materials, including quantum dots.[67,68] This technique utilizes the deposition of a thin layer onto a substrate by the chemical reaction of gaseous precursors. A suitable substrate, such as a sapphire wafer, is cleaned and prepared to provide a smooth surface for deposition. Gaseous precursors containing the desired elements for the formation of quantum dots are introduced into the reaction chamber. The common

precursors for quantum dot synthesis include organometallic compounds and hydrogen sulfide. The precursors are subjected to elevated temperatures and pressures, causing them to decompose and react to form quantum dots. The quantum dots that are made start to form and grow on the surface of the medium. The rate of growth and dimensions of the quantum dots can be regulated by modifying many factors, including temperature, pressure, precursor flow rate, and the type of carrier gas used. Firstly, the sample is deposited, and then it is cooled down to room temperature. It is possible to perform annealing to enhance the crystallinity of the quantum dots and strengthen their optical characteristics. CVD allows meticulous control of the dimensions, morphology, and composition of quantum dots. This technique may provide high-quality quantum dots characterized by narrow size distributions and superior optical characteristics. This technology is scalable for the extensive manufacturing of quantum dots, making it appropriate for commercial applications. Furthermore, it can be used with other production techniques, including as lithography and etching, to produce intricate quantum dot-based devices. However, the overall system can be complex and expensive, requiring specialized equipment and expertise. Furthermore, the precursors used in CVD can be toxic or hazardous, requiring careful handling and disposal. The selection of substrate may affect the growth kinetics and characteristics of the quantum dots.[50,69–71]

3.1.6 Microwave-assisted synthesis of quantum dots (QDs). The microwave-assisted synthesis of quantum dots (QDs) is a cutting-edge technique, which involves the use of microwave radiation to achieve the rapid and uniform heating of the reaction mixture. This method significantly reduces the synthesis time compared to traditional heating methods, which rely on convection and conduction. The microwaves penetrate the reaction medium, causing dielectric heating, which leads to a more homogeneous temperature distribution. This uniform heating is crucial for the controlled nucleation and growth of QDs, resulting in particles with narrow size distributions and high crystallinity. The ability to quickly reach and maintain the desired reaction temperature also minimizes the formation of defects and impurities, enhancing the optical and electronic properties of the QDs.[72–76]

One of the major advantages of microwave-assisted synthesis is its versatility. It can be applied to a wide range of precursor materials and solvents, both aqueous and organic. This flexibility allows the synthesis of various types of QDs, such as CdSe, ZnS, and other semiconductor nanocrystals. Additionally, this method is compatible with environmentally friendly solvents and lower reaction temperatures, making it a greener alternative to some conventional synthesis techniques. The rapid heating and cooling cycles enabled by microwave irradiation also facilitate the synthesis of QDs with complex core–shell structures, which are essential for applications requiring specific optical properties.[77–80] However, despite its many advantages, microwave-assisted synthesis has some limitations. The scalability of this method can be challenging, given that the uniformity of microwave heating may decrease with larger reaction volumes. Also, specialized microwave reactors are required to ensure consistent and reproducible results, which can be costly and require careful calibration. Moreover, the penetration depth of microwaves can be limited by the dielectric properties of the reaction medium, potentially affecting the synthesis of certain types of QDs. Nevertheless, ongoing advancements in microwave reactor design and process optimization continue to expand the potential of this technique, making it a promising approach for the efficient and sustainable production of high-quality QDs.[81–83]

3.2 Top-down approach

3.2.1 Laser ablation method. Using the accuracy and power of laser pulses, laser ablation is an advanced method for producing quantum dots and nanoparticles with special characteristics. The procedure starts with a high-energy laser beam pointed at a target substance, usually in a liquid or gaseous state, under regulated conditions. A plasma plume is formed when the target is struck by laser pulses, which quickly heat and evaporate the material. A mixture of atoms, ions, and clusters that are expelled from the target surface is contained in this plume. The vaporized material experiences nucleation and growth as the plasma plume extends and cools, resulting in the production of nanoparticles, including quantum dots. The wavelength, pulse duration, energy, and other factors of the laser, together with the characteristics of the surrounding medium, may all be precisely adjusted to regulate the size and dispersion of these quantum dots. For example, greater energy and shorter laser pulses typically result in smaller quantum dots with narrower size distributions.[84–87]

The capacity of laser ablation to generate high-purity quantum dots is one of its main benefits. The quick quenching of the vaporized material minimizes contamination and enables the creation of nanoparticles with well-defined characteristics. This technique is extremely flexible and may be applied to a variety of materials, such as metals, carbon-based compounds such as graphene and carbon quantum dots, semiconductors such as Ge and Si, and others.[84–88] Because of their nanoscale size, the quantum dots created by laser ablation have special optical and electrical properties, making them useful for a variety of applications, including solar cells, photodetectors, and light-emitting diodes (LEDs) in optoelectronics.[44,89,90] Also, their intense and stable fluorescence makes them perfect for marking and tracking biological molecules in the field of bioimaging. Additionally, because of their excellent sensitivity and selectivity, quantum dots are used in sensors to identify chemical and biological substances.[86,91,92] Laser ablation is a strong and adaptable technique for creating quantum dots, providing exact control of their size and characteristics, excellent purity, and suitability for a variety of materials and uses.[87]

3.2.2 Electrochemical method. Utilizing electrochemical processes, the electrochemical synthesis of quantum dots is a highly effective and eco-friendly technique that yields nanoparticles with exact control of their size and characteristics. Two electrodes submerged in an electrolyte solution containing the precursor ingredients are usually used in this procedure.

Table 2 Comparison of methods for the synthesis of quantum dots

Method	Type	Advantages	Disadvantages	Examples	Ref.
Hot injection	Bottom-up	High-quality, monodisperse QDs, precise size control	Requires high temperature, complex setup	CdSe, PbS	105 and 106
Solvothermal	Bottom-up	Simple setup, scalable, high crystallinity	Long reaction time, high pressure	ZnS, CdTe	107–109
Hydrothermal	Bottom-up	Environmentally friendly, low cost	Limited to water-soluble precursors	CdS, ZnO	110–112
Microwave-assisted	Bottom-up	Rapid synthesis, uniform heating, energy-efficient	Limited scalability, specialized equipment	CdSe, ZnS	113 and 114
Laser ablation	Top-down	No chemical precursors needed, high purity	Expensive equipment, low yield	Si, Ge	88 and 115
Liquid-phase exfoliation	Top-down	Simple, scalable, no need for high temperature	Produces QDs with wide size distribution	Graphene QDs	116 and 117
Electrochemical	Top-down	Precise control over size and composition	Requires conductive substrates, complex setup	CdSe, ZnO	118 and 119
Soft-template	Bottom-up	High surface area, tunable pore size	Template removal can be challenging	ZnS, SiO_2, TiO_2, C, graphene	90, 120 and 121
Pyrolysis	Bottom-up	High yield, continuous production possible	High temperature required, potential for toxic by-products	CdSe, InP	122 and 123
Chemical vapor deposition	Bottom-up	High purity, good control over thickness and composition	Requires high temperature, expensive equipment	Si, Ge	124–126

Quantum dots are created when a voltage is applied between the electrodes, causing redox processes in the precursor materials. The capacity of the electrochemical method to precisely control the size and surface characteristics of quantum dots through manipulation of the electrochemical parameters, including applied voltage, current density, and electrolyte composition, is one of its main advantages. One way to improve the solubility and compatibility of quantum dots in diverse settings is by introducing different functional groups on their surface using different electrolytes.[93]

There are various steps in the electrochemical synthesis process. Firstly, the electrolyte solution dissolves the precursor components. Metal or semiconductor nanoparticles are formed at the cathode when the voltage is applied because the precursor ions are reduced there. Depending on the specific circumstances and materials utilized, these nanoparticles may experience additional oxidation or other surface alterations. When graphite electrodes are utilized in the production of carbon-based quantum dots, such as graphene quantum dots, this approach works especially well. The electrolyte in these cases usually consists of a mixture of bases and acids.[94,95] The resulting quantum dots, with their nanoscale dimensions and quantum confinement effects, display distinctive optical and electrical features. Their characteristics make them appropriate for an extensive array of applications, including bioimaging, medication administration, sensing, and optoelectronic devices. Also, because it typically requires gentler temperatures and generates less byproducts than conventional chemical synthesis methods, the electrochemical method is regarded as a green synthesis route.[96] Overall, the electrochemical method for the synthesis of quantum dots is a useful technique in nanotechnology and materials research given that it provides a flexible and sustainable way to produce high-quality nanoparticles with customized features.[95,97]

3.2.3 Liquid-phase exfoliation. One popular technique for creating quantum dots is liquid-phase exfoliation, especially for layered substances such as graphene. Using mechanical forces to exfoliate bulk layered materials, such as like graphite, into nanoscale sheets and quantum dots, this process involves distributing the materials in a solution. To accomplish the exfoliation, this method usually employs high-shear mixing or sonication.[98,99]

The bulk material is initially dispersed in an appropriate solvent in liquid-phase exfoliation. The stability of the resultant quantum dots and the effectiveness of exfoliation are both impacted by the choice of solvent, which is critical. Water, ethanol, and organic solvents such as dimethylformamide (DMF) and *N*-methyl-2-pyrrolidone (NMP) are examples of the common solvents. After the material is distributed, thin nanosheets and quantum dots are created using high shear pressures or ultrasonic waves to break the van der Waals forces keeping their layers together. Numerous variables, including the length and force of sonication, the material concentration in the solvent, and the solvent type, can be changed to regulate the size and quality of the generated quantum dots. For example, smaller and more homogeneous quantum dots can be achieved with increased power and longer sonication durations.

In order to maintain a stable dispersion of quantum dots, surfactants or stabilizers in the solvent can also aid in preventing the re-aggregation of the exfoliated layers.[100–102] Because liquid-phase exfoliation is easy to use, scalable, and economical, it is very beneficial. It is suitable for large-scale production

because it doesn't require high temperatures or sophisticated equipment. Additionally, this process is eco-friendly, particularly when water or other green solvents are used. Excellent optical and electrical properties render the quantum dots generated *via* liquid-phase exfoliation useful for a multitude of applications, such as bioimaging, sensors, and optoelectronics. In general, liquid-phase exfoliation is a scalable, ecologically benign, and very effective technique for producing high-quality quantum dots. It provides exact control over the size and characteristics of the dots.[103,104] Table 2 illustrates the different quantum dot synthesis techniques, highlighting their respective benefits and drawbacks.

4. Different quantum dots in non-volatile memory systems

4.1 Perovskite quantum dots (PQDs)

Perovskites are a common class of materials with the general formula ABX_3. In this configuration, 'A' and 'B' represent two cations with markedly different sizes, while 'X' denotes an anion that establishes bonds with both cations.[38] These nano-sized crystals are a product of perovskite materials, initially defined as metal oxides possessing an octahedral crystal structure similar to that of natural calcium titanate ($CaTiO_3$). Perovskite quantum dots (PQDs) merge the distinctive semiconductor properties of bulk perovskite structures with the precise exciton dynamics made possible by the quantum confinement effect.[127,128] This suggests that the semiconductor traits of PQDs can be adjusted through quantum size and surface engineering.[17,129,130] Perovskites have been utilized in non-volatile memory devices because of their exceptional electronic properties and the flexibility offered by dimensionality engineering.[16,131] There is a considerable relationship between the dimensions of perovskite materials and the operational efficiency of these memory devices.[16,18,132]

4.1.1 Ionic/vacancy migration mechanism of PQDs. PQDs exhibit unique ionic and vacancy migration mechanisms, which significantly impact their structural stability and performance in memory devices. This process can be influenced by external stimuli such as light illumination or an electric field. The migration of ions creates vacancies, which can move through the lattice. These vacancies can act as charge traps, affecting the electronic transport properties. Xu *et al.*[133] studied a write once read many (WORM) NVM memory device with ternary states based on $CsPbI_3$ PQDs, which can give an idea of the migration mechanism in PQDs. They found four distinct states of operation in the fabricated memory device. They proposed two pathways to explain the ternary states observed in their resistive switching devices, as depicted in Fig. 5. Thermal annealing of the PQDs facilitates the detachment of their surface ligands, resulting in the formation of iodine vacancies, which are predominantly situated at grain boundaries (GBs). This process led to the creation of a limited number of conductive filaments (CFs), which contributed to the establishment of the initial low resistance state (iLRS), as shown in Fig. 5(a). Throughout the RESET process in memory function, the substantial current passing through the CF produces considerable Joule heat, which aids in the lateral diffusion of iodine vacancies and the annihilation of the CF, leading to the transition of the device from the iLRS to high resistance state (HRS), as shown in Fig. 5(b). As the next set process starts, more iodine gaps are created, which move up and down when a positive bias is applied to the Ag electrode. Because VIs have less energy to form and move at the grain boundaries (GBs) compared to grain interiors (GIs), CFs mostly form and grow at GBs, and then move into the GIs at a larger bias. This causes a series of changes to IRS and the final low resistance state (fLRS), as shown in Fig. 5(c and d).

4.1.1.1 Write operation. The 'write' operation in PQD-based NVMs is usually accomplished by transferring an external electric field, which causes halide vacancies (such as iodine and bromine vacancies) to migrate within the PQD lattice. As a result of this migration, conductive filaments (CFs) grow between the electrodes of the device, turning it from a high-resistance (HRS) to a low-resistance (LRS) state and decreasing its resistance. The 'SET' operation describes this procedure.[133]

4.1.1.2 Read operation. The 'read' function in these devices entails supplying a reduced voltage that is inadequate to modify the existing conductive pathways. The resistance state (HRS or LRS) of the device can be ascertained by measuring the resultant current, which corresponds to the stored data bits ('0' or '1').[133]

4.1.2 Applications of PQDs in memory devices

4.1.2.1 Resistance switching memory. Resistance switching memory, often referred to as resistive memory or memristor, represents innovative non-volatile memory technology. It

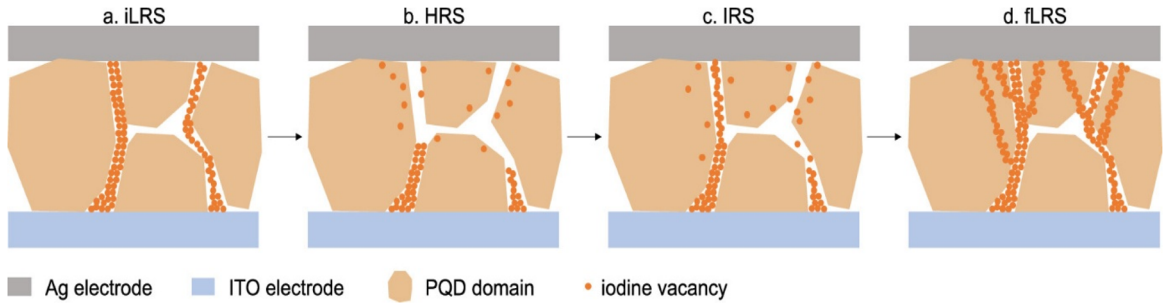

Fig. 5 Schematic of CF formation and annihilation in $CsPbI_3$ PQD-based device across various states: (a) iLRS; (b) HRS; (c) IRS; and (d) fLRS. Reproduced from ref. 133 with permission from ACS. Copyright 2024, ACS.

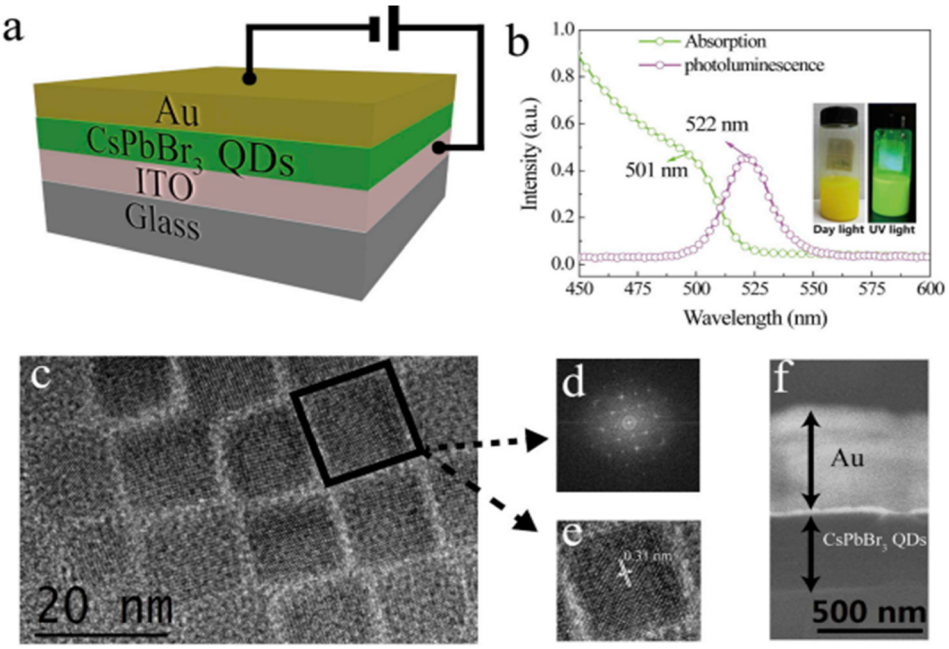

Fig. 6 (a) $CsPbBr_3$ QD-based WORM setup. (b) Photoluminescence and absorbance of $CsPbBr_3$ QDs. Daylight and UV light images of $CsPbBr_3$ QD solution are in the inset. (c–e) TEM images of $CsPbBr_3$ (f) SEM cross-sectional image of $CsPbBr_3$ QD-based resistive switching device. Reproduced from ref. 18 with permission from Elsevier. Copyright 2019, Elsevier.

operates by altering the electrical resistance of a material between a low resistance state (LRS) and a high resistance state (HRS) when an adequate electric voltage is applied. This mechanism functions similarly to a switch that relies on varying resistance levels, enabling data storage without requiring continuous power to preserve the information.[134] A conductive filament is formed within the material when a voltage pulse is applied, resulting in a substantial decrease in resistance (LRS). The filament can be broken by reversing the voltage polarity, which will restore the resistance to a high state (HRS).[135] Z. Chen *et al.*[18] synthesized $CsPbBr_3$, an inorganic perovskite quantum dot, and experimentally proved that it exhibits a highly favourable response for use in non-volatile memory cells.[18] They used a sandwich model sample (depicted in Fig. 6(a)), which consisted of Au (gold), $CsPbBr_3$, ITO and glass.

Fig. 6(b) presents the UV-vis absorption and PL spectra of the synthesized $CsPbBr_3$ quantum dots. The inset highlights how the $CsPbBr_3$ QD solution appears under daylight and UV light. The strong exciton absorption peak and well-defined PL spectra suggest a uniform size distribution for the $CsPbBr_3$ quantum dots. Fig. 6(c–e) display the TEM images of these QDs. The cubic perovskite structure, with an average edge length of about 10 nm, exhibits excellent crystalline properties in the $CsPbBr_3$ QDs. Fig. 6(f) shows a cross-sectional SEM image of the memory device unit. The $CsPbBr_3$ quantum dot layer has a thickness of around 350 nm, and the current–voltage properties of the quantum dot were observed.

They observed different voltage sweeps in a sequence of 0 V, −4 V, 0 V, 3 V and 0 V. Initially, the memory device was in a state referred to as HRS or OFF. Fig. 7(a) delineates the sweep voltage and current characteristics. In sweep 1, the initial voltage was 0 V. As the negative voltage increased in sweep 2 from 0 V to −4 V the current increased gradually. Upon reaching −1.1 V for the sweep voltage, there was a sharp rise in current, from approximately 10^{-4} mA to 1 mA, signifying the shift in the device status from HRS to LRS or ON, which indicates an ON/OFF ratio of approximately 10^4. The electrical transition occurring in a memory device while shifting from the high resistance state (HRS) to the low resistance state (LRS) is termed the "writing" process, with a voltage threshold of −1.1 V designated as the "writing" voltage. Throughout the subsequent negative sweep (sweep 2) and the positive sweeps (sweeps 3 and 4), the device maintained stability in the ON state. Thus, thus device revealed a WORM-type memory effect.[136]

Fig. 7(b) shows the memory device capacity for retention. The values of the LRS and HRS remained nearly constant over a duration of 1000 s. Although there were slight fluctuations in the LRS and HRS values, the ON/OFF ratio remained unchanged. Fig. 7(c) depicts the entire procedure of the "writing" process, commencing at 0 V, transitioning to −4 V, and subsequently returning to 0 V. In the high-resistance state (HRS), as shown in Fig. 7(d), the voltage varied from 0 V to −0.96 V, with the experimental data conforming to a linear fit, exhibiting a slope near 1. This indicates that the primary mechanism entails charge injection across the energy barrier separating ITO and $CsPbBr_3$ quantum dots. As depicted in Fig. 7(e), the slope of the fitted line increased from 1 to 2 in the applied negative voltage range of −0.96 V to −1.1 V. This suggests a gradual filling of traps by carriers, leading to the closure of the active material band gap. This area is recognized as the space charge-limited conduction (SCLC) region that is saturated with traps. Upon reaching a negative bias voltage of

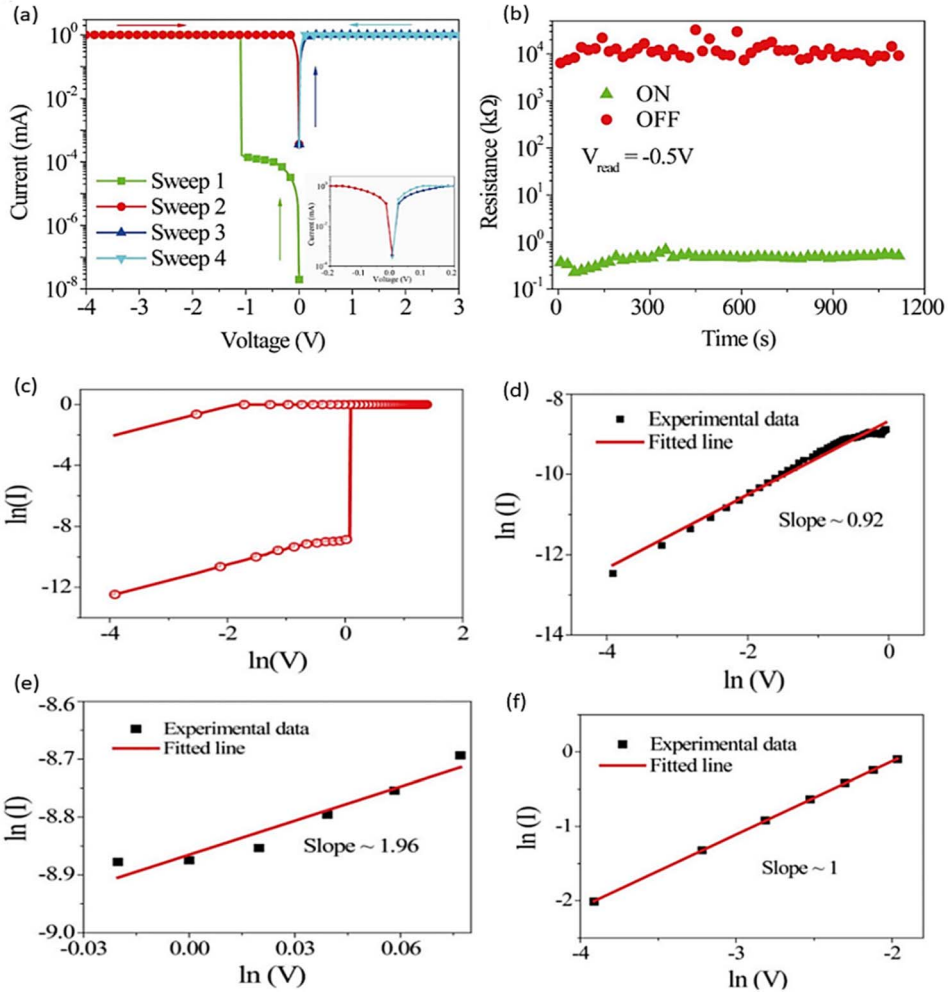

Fig. 7 (a) Compliance current of 1 mA applied during the voltage sweep to avoid hard breakdown of the device. The detailed view, particularly near 0 V bias, is shown with an enlarged scale. (b) Retention properties of the low-resistance state (LRS) and high-resistance state (HRS) measured using a reading voltage of −0.5 V across all resistive states. (c) *I*–*V* curves for the "writing" process, (d) and (e) *I*–*V* characteristic curves for the HRS (both are measured and fitted), and (f) *I*–*V* characteristic curves for the LRS (both measured and fitted). Reproduced from ref. 18 with permission from Elsevier. Copyright 2019, Elsevier.

−1.1 V, nearly all traps become filled with carriers. Subsequently, the injected electrons can move freely *via* trap-to-trap hopping, forming conductive pathways. As a result, the device shifts from a high-resistance state (HRS) to a low-resistance state (LRS). In the LRS, as depicted in Fig. 7(f), the current follows ohmic conduction. After the "writing" process, the device exhibits a write-once-read-many (WORM)-type memory effect. This behavior is primarily attributed to the considerable height of the space charge layer within the $CsPbBr_3$ quantum dots, which effectively counteracts the applied electric field.[18]

4.1.2.2 Floating gate transistor memory. A floating gate transistor memory is memory technology that stores data by trapping electrical charges on a specially designed floating gate within a transistor. This gate is electrically isolated and retains the charge even when power is removed, resulting in a non-volatile memory solution frequently utilized in flash memory devices such as USB drives and SSDs[137] Jin *et al.*[138] studied a floating gate transistor-based memory device using inorganic halide perovskite $CsPbBr_3$ quantum dots. The floating gates, as shown in Fig. 8(a), were fabricated using composite layers including inorganic perovskite quantum dots placed inside a polystyrene (PS) matrix. This architecture enabled higher-quality memory features including tiered data storage and extended retention length. The composite layer of the floating gate consisted of inorganic perovskite QDs embedded in a polystyrene (PS) matrix. Improved memory properties, such as layered data storage and prolonged retention duration, were made possible by this structure.

The QD-embedded PS layer improved the stability and charge trapping, leading to higher on/off ratios and a wider memory window.[138] In the past two decades, non-volatile memory based on organic field-effect transistors (OFETs) has attracted considerable attention due to its benefits such as non-destructive read-out, lightweight construction, simple processing, low production costs, and strong compatibility with current integrated circuit technologies.[139–141] Jin *et al.*[138] synthesized

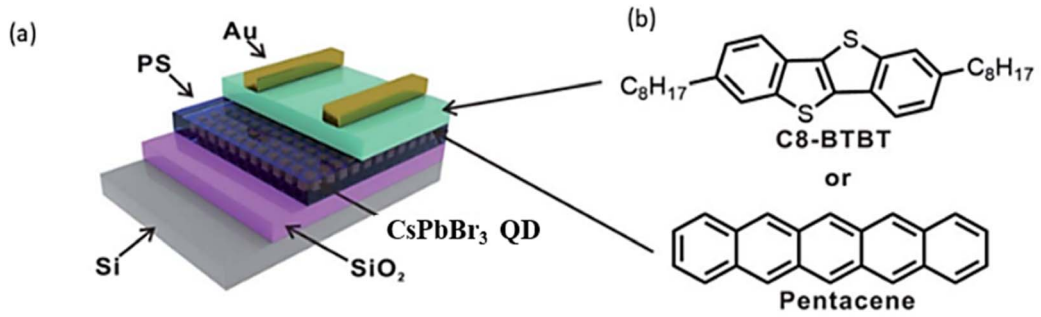

Fig. 8 (a) Diagram showing the structure of $CsPbBr_3$ quantum dots (QDs) combined with a polystyrene (PS) composite film in field-effect transistor memory devices (FGOFETMs). (b) Molecular structures of pentacene and C8-BTBT. Reproduced from ref. 138 with permission from RSC. Copyright 2020, RSC.

$CsPbBr_3$ QD using the method established by L. Protesescu *et al.*[142] and proceeded to form and characterize a floating gate transistor flash memory system. They used Si and SiO_2 as the substrate and top of the substrate $CsPbBr_3$ QD layer, PS and pentacene layer, and organic semiconductor 2,7-dioctyl[1] benzothieno[3,2-b][1]benzothiophene (C8-BTBT) layer, respectively, and finally on the top of two Au plates, as shown in Fig. 8(a and b). The molecular structures of pentacene and C8-BTBT are shown in Fig. 8(b). They achieved a large memory window, ultra-high ON/OFF ratio (10^7), and a retention time of 10 years (3.16×10^8 s). Consequently, C8-BTBT-based floating-gate organic field-effect transistor memories (FGOFETMs) have great potential to achieve multilevel data storage.[143,144] These devices impressively offer the ability to store data across four distinct levels, showcasing their multilevel storage capability. Additionally, they incorporate a photoinduced-reset function, which innovatively allows the erasure of stored data through light exposure instead of traditional electrical methods as an energy saving operation. The $CsPbBr_3$ QDs absorb photons in the presence of white light, producing photoexcited electron–hole pairs (excitons). The internal electric field (E_{in}) created by the stored holes causes these excitons to split. The charge storage is neutralized when the photogenerated electrons recombine with the holes that were stored in the QDs. The

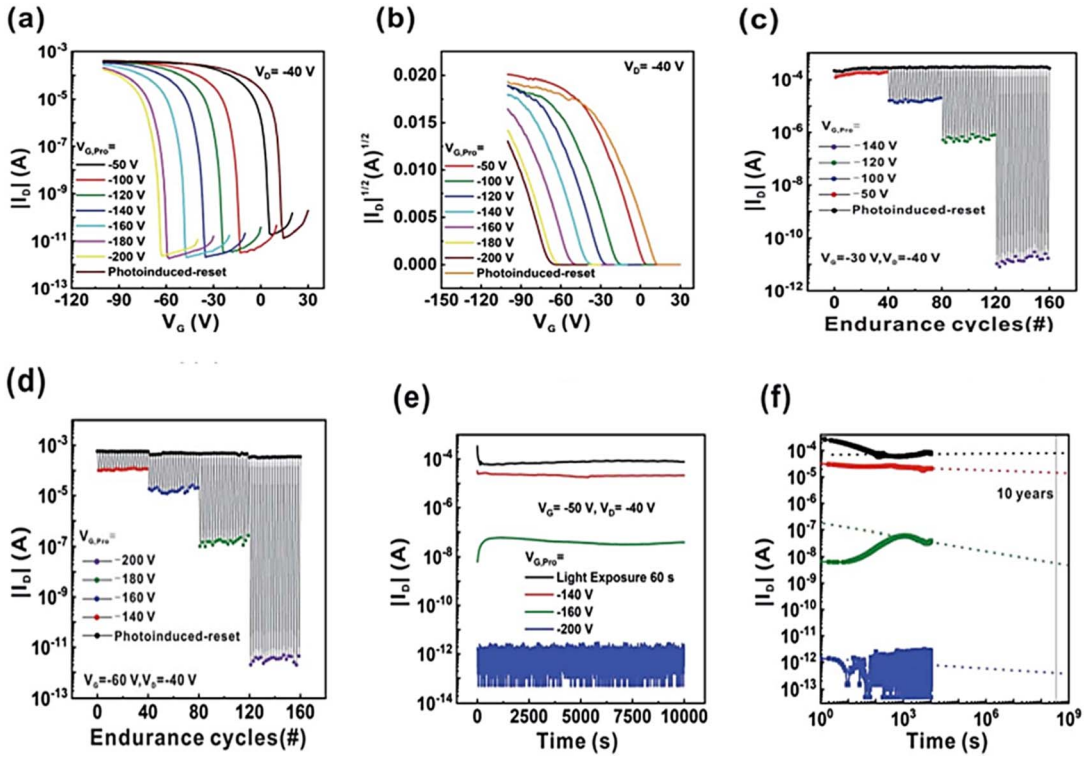

Fig. 9 (a) I–V curves and (b) $\sqrt{I}$–V curves for devices featuring C8-BTBT with a $CsPbBr_3$ QD/PS composite floating-gate layer. (c) Program/erase cycling across 20 iterations at $V_G = -30$ V, $V_D = -40$ V, and (d) at $V_G = -60$ V, $V_D = -40$ V. (e) Retention behavior for various current levels following programming at $V_G = -140$, -160, and -200 V, along with the photoinduced reset process. (f) Retention time derived from the extrapolation of the on- and off-state data. Reproduced from ref. 138 with permission from RSC. Copyright 2020, RSC.

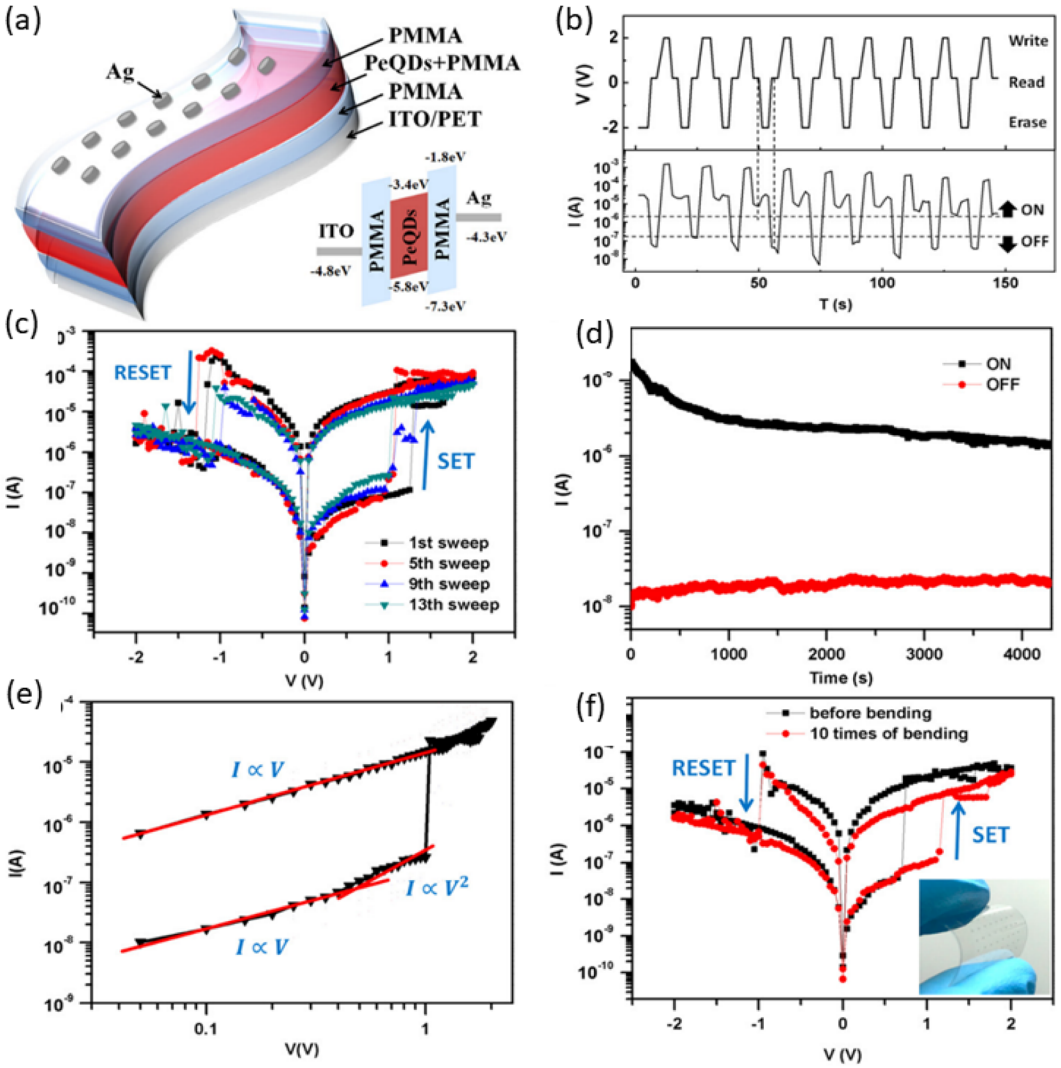

Fig. 10 (a) Schematic of the flexible PeQD memory device, featuring a PET/ITO/PMMA/PeQDs:PMMA/PMMA/Ag structure. Inset: depiction of the energy band diagram for the PeQD memory device. (b) Typical *I*–*V* characteristics for the PeQD memory device through repeated testing. (c) Results of fitting a typical *I*–*V* curve with a log–log scale. (d) Outcome of the erase-read-write-read sequence test conducted on the PeQD memory device. (e) Data retention characteristics observed for ON and OFF states. (f) *I*–*V* characteristics of the flexible memory device before and after undergoing 10 cycles of bending. Inset: photograph of the as-fabricated flexible PeQD memory device subjected to bending. Reproduced from ref. 132 with permission from AIP. Copyright 2017, AIP.

initial charge balance is restored when photo-generated holes return to the organic semiconductor layer at the same time. This causes the device to enter a reset mode, where it regains its original threshold voltage and erases recorded data without causing any electrical stress. After light exposure for the erase operation, the transfer curve is shown in Fig. 9(a) with a range of programming voltages ($V_{G,Pro} = -50$, -100, -120, -140, -160, -180, and -200 V). Fig. 9(b) delineates the corresponding $\sqrt{I_D}$ *vs.* V_G characteristics.

The cycling tests conducted during the repeated programming and erasing operations, as illustrated in Fig. 9(c) and (d), reveal a consistent and repeatable pattern of current cycles, highlighting the reliability of the devices. The retention test of the four current states in FGOFETMs utilizing C8-BTBT, as illustrated in Fig. 9(e), demonstrated that these states remained stable even after 10 000 s, showing no significant degradation. The multilevel FGOFETM charge storage stability stands out, with $CsPbBr_3$ QDs demonstrating impressive quasi-permanent retention for more than a decade, as illustrated in Fig. 9(f). This highlights the impressive long-term reliability of the device.

4.1.3 Hybrid ($CH_3NH_3PbBr_3$) perovskite quantum dots. Yang *et al.*[132] synthesized $CH_3NH_3PbBr_3$ using a straightforward one-step method involving ultrasonic vibration and an organic capping ligand. They experimentally validated its advantageous properties for integration into resistive random-access memory (ReRAM), highlighting its potential as a candidate for next-generation non-volatile memory systems. To elucidate the resistive switching (RS) phenomenon in devices incorporating dielectric switching materials, researchers have proposed

various conduction mechanisms. These mechanisms include ohmic conduction, hopping conduction, Schottky emission, Poole–Frenkel (PF) conduction, and trap-controlled space-charge-limited conduction (SCLC).[145] Notably, the trap-controlled SCLC mechanism stands out, given that it is intricately linked to the trapping or de-trapping of charge carriers.[146] This mechanism has been proven to be suitable for explaining the RS phenomenon observed in this case, particularly in the context of quantum dots embedded within the dielectric matrix. The PeQDs can function as traps due to their energy level falling within the range of the lowest unoccupied molecular orbital (LUMO) and highest occupied molecular orbital (HOMO) levels of PMMA, as illustrated in the inset of Fig. 10(a).[147] Fig. 10(b) illustrates that the transition between the high resistance state (HRS) and the low resistance state (LRS) is controllable, with an ON/OFF current ratio above 10^3, therefore substantially reducing the likelihood of misreading.[132,148,149]

To provide a more in-depth interpretation of the conduction mechanism, Yang *et al.* represented the *I–V* curve on a log–log scale, as demonstrated in Fig. 10(c). Within the high-resistance state (HRS) region, the fitting result predominantly encompasses two regions characterized by distinct slopes of 1 and 2. In the range of 0 to 0.5 V, the *I–V* curve exhibits linearity, adhering to Ohm's law (I/V). In the range of 0.5 V to 1 V, the *I–V* curve adheres to Child's law (I/V^2), indicating a characteristic feature of space charge-limited conduction (SCLC).[27,42] With a substantial increase in the number of injected carriers induced by the high electric field, the traps within the PeQDs layer undergo continuous filling with these injected carriers. To showcase the switching characteristics of the memory, they conducted an "erase-read-write-read" sequence test. The applied voltage pulse was cycled through a sequence of "−2 V, 0.2 V, 2 V, 0.2 V" with each pulse lasting for 1 s per step, as depicted in Fig. 10(d). The write voltage was configured at 2 V to transition the device into the ON state (low-resistance state, LRS), whereas the erase voltage was set to −2 V to revert the device back to the OFF state (high-resistance state, HRS). Subsequently, the "read" voltage was configured at 0.2 V to discern between the ON state and OFF state. In each cycle, the application of the setting pulse induced a transition from the OFF state to the ON state, resulting in a high recorded current during the subsequent reading period. Conversely, a low current was recorded in the subsequent reading period after the application of the resetting pulse. This confirmed that switching the memory device by a voltage pulse is feasible, where Fig. 10(d) shows that the switching procedure is repeatable from cycle to cycle. The memory device data retention characteristics for both the ON and OFF states were evaluated by applying a reading bias of 0.2 V. This assessment served to demonstrate the electrical reliability of the memory device. As depicted in Fig. 10(e), the ON and OFF states persisted for a duration of up to 4000 s, exhibiting only a marginal reduction from approximately 10^3 to 10^2. Although there was a slight decrease, it remained significant to distinguish between the ON and OFF states.

The findings presented above collectively affirm the commendable reproducibility and reliability of PeQD memory devices, underscoring their suitability for practical applications.

Table 3 Comparison of the ON/OFF ratio and retention time of various organic and organic–inorganic PQD based non-volatile memory

Materials	Type	ON/OFF ratio	Retention time (s)	Ref.
$CH_3NH_3PbBr_3$ QD	Hybrid	10^3	4×10^3	132
$CH_3NH_3PbI_3$ QD	Hybrid	10	10^4	150
$CsPbBr_3$ QD	Inorganic	1.86×10^5	10^3	151
$CsPbBr_3$ APQD	Inorganic	10^7	10^3	152
$CsPbBr_3$ QD	Inorganic	10^7	3.16×10^8	138
$CsPbBr_3$	Inorganic	10^4	10^3	18
$CsPbI_3$ QD	Inorganic	10^3	10^4	133

The flexibility of the PeQD memory device was showcased, demonstrating its viability for application in flexible electronics. The bending test involved subjecting the flexible device to bending with a curvature radius of 7 mm, as illustrated in Fig. 10(f). Following 10 instances of bending, the ON/OFF current ratio of the device experienced a modest reduction from 10^3 to approximately 10^2. This suggests its commendable flexibility under conditions of sharp bending.

4.1.4 Comparison of inorganic *vs.* hybrid PQDs for NVM applications. The research conducted by Z. Chen *et al.*[18] and Jin *et al.*[138] indicates that the floating gate transistor memory model exhibits superior characteristics compared to the resistive switching memory model, despite both being constructed from the same quantum dots (QD). Inorganic perovskite quantum dots clearly demonstrate a superior ON/OFF ratio and enhanced retention time compared to their organic counterparts for non-volatile memory applications. Inorganic $CsPbBr_3$ PeQDs[138] demonstrate an ON/OFF ratio of 10^7 and a retention time of 3.16×10^8 s, while $CH_3NH_3PbBr_3$, organic–inorganic PeQDs,[132] show an ON/OFF ratio and retention time of 10^3 and 4×10^3 s, respectively. Table 3 presents a comparative analysis of the organic–inorganic and inorganic perovskite quantum dots, focusing on their ON/OFF ratio and retention time. Therefore, inorganic perovskite quantum dots demonstrate superiority over organic perovskite quantum dots considering non-volatile memory applications.

4.2 Self-assembled quantum dots

Self-assembled quantum dots (SAQDs) are semiconductor formations capable of trapping charge carriers at a scale comparable to their de Broglie wavelength. These structures are often called "artificial atoms" because their quantum confinement effects limit the motion of electrons and holes in all three dimensions, resulting in discrete energy levels similar to that found in atoms.[153] This formation arises from the release of strain energy in epitaxial systems, where the deposited material has a significantly larger lattice parameter compared to the substrate material. This self-assembly technique can significantly increase the mobility and stability of QDs. In the realm of non-volatile memory applications, self-assembled quantum dots (SAQDs) present intriguing possibilities given that they exhibit discrete energy levels, charge trapping and retention characteristics.[150,153–155]

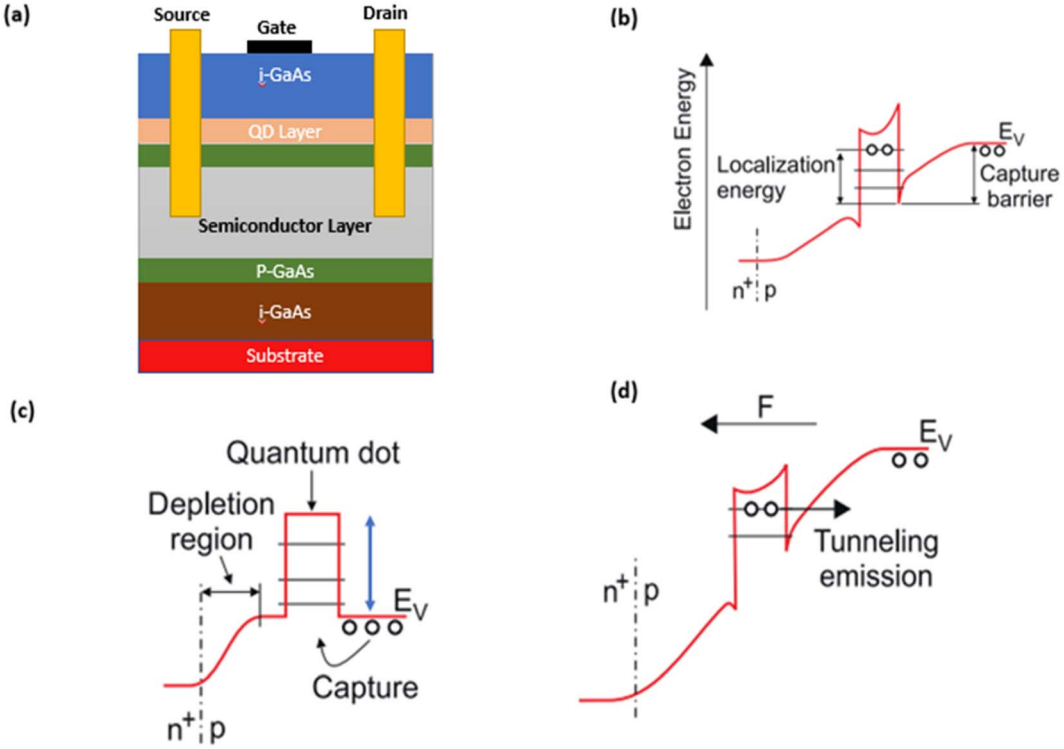

Fig. 11 Schematic of (a) device architecture and mechanisms of (b) charge carrier storage, (c) writing and (d) erase processes in the proposed quantum dot-based flash memory using hole storage. Reproduced from ref. 157 with permission from Elsevier. Copyright 2009, Elsevier.

4.2.1 Operation of SAQDs in NVM systems. The fundamental architecture of an SAQD-based NVM device includes a control gate, a quantum dot layer, and a source/channel-drain current.[156] The quantum confinement effect is the foundation of the operation of SAQDs in NVM. The effect is defined by the fact that the production of different energy levels, made possible by the microscopic size of quantum dots, allows the efficient storage and maintenance of charges.[154] Marent *et al.*[157] incorporated flash memory using self-assembled InAs/GaAs QDs. The device architecture is illustrated in Fig. 11(a). The mechanisms of charge carrier storage and the write/erase operations are schematically illustrated in Fig. 11b–d, respectively. The detailed prototype structure of the SAQD-based memory studied by the same author is also briefly discussed in Section 4.2.2.

In terms of hole storage, the doping concentration and the positioning of the quantum dots within the structure are meticulously calibrated at zero bias to ensure that the quantum dots reside within the depletion region. This illustrates the storage scenario, as shown in Fig. 11(b). An external bias can effectively alter the width of the depletion region. The application of forward bias effectively decreases the width, positioning the quantum dots outside the depletion region, as illustrated in Fig. 11(c). In contrast to the traditional flash memory concept, which relies on a fixed SiO_2 barrier height, this approach eliminates the capture barrier, allowing remarkably fast capture in the quantum dot states. A high reverse bias is applied to the diode to erase the information, as illustrated in Fig. 11(d).

4.2.1.1 Charge trapping. When a voltage is applied across the device, such as from the control gate, electrons or holes are injected into the quantum dots through the process of injection. Quantum confinement results in the restriction of charges within the SAQDs, which serve as nodes for the storage of floating charges.[154]

4.2.1.2 Data retention. The trapped charges in quantum dots can indicate a binary state of 0 or 1, depending on the device configuration. A quantum dot is analogous to a floating gate in quantum physics; its presence indicates one logic state (such as "1") and its absence another (such as "0").[154]

4.2.1.3 Read operation. During the read process, a reduced voltage is applied to the gate to examine whether there is any charge present in the quantum dots of the memory cell. The trapping of charges within the quantum dots alters the threshold voltage of the memory cell, leading to a variation in the observed current through the channel, indicating a "1." Conversely, if no charges are trapped, the channel current reaches a different value, representing a "0."[154]

4.2.1.4 Write operation. To write data to the quantum dots, a higher voltage is applied to the control gate, which activates the tunneling oxide layer. This allows electrons or holes to travel from the channel into the quantum dots. The dielectric material surrounding the quantum dots creates potential barriers, confining the electrons within the quantum dots.[154]

4.2.1.5 Erase operation. Typically, erasing data requires applying a negative voltage or reverse voltage to the control gate. This procedure resets the memory cell by releasing the quantum

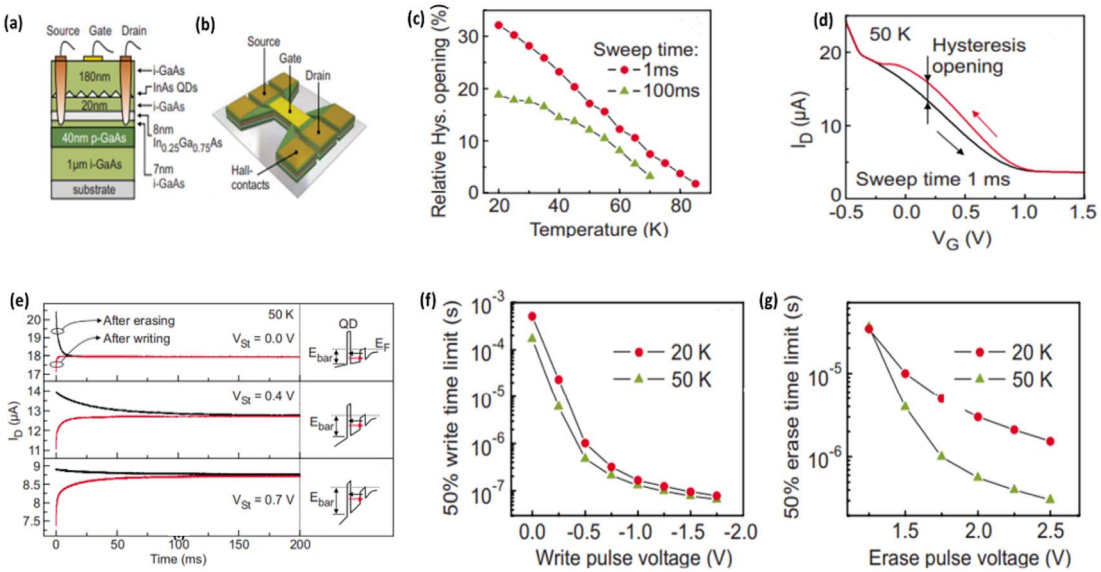

Fig. 12 (a) Cross-sectional schematic showing the layer structure. (b) Diagram of the QD-flash prototype. (c) Hysteresis at 50 K. (d) Temperature dependence of hysteresis width for sweeps at 50 K with 1 ms and 100 ms intervals. (e) Changes in drain current at 0 V, 0.4 V, and 0.7 V, with the valence band profile at the respective voltage shown in the inset. (f) Write times and (g) erase times, demonstrating their relationship with pulse voltage in the QD-flash prototype. Reproduced from ref. 21 with permission from AIP. Copyright 2009, AIP.

dot trapped charges and forcing them to return to the channel *via* the oxide layers.[154]

4.2.2 InAs/GaAs SAQDs. In a recent study by A. Marent *et al.*,[21] they found that SAQDs acted as a prominent agent for non-volatile memory applications. They created an InAs/GaAs prototype that employs holes rather than electrons as a charge carriers. They substituted the typically used electron channels with a two-dimensional hole gas (2DHG) and positioned it beneath the quantum dot layer for examination. Fig. 12(a) presents the schematic cross-section and Fig. 12(b) the memory prototype.

They observed the valence band for three functionalities such as store, write and erase for the discussed prototype. The binding potential of holes in the QD at the storage site serves as the emission barrier required to store a logic "1". To store a logic "0," or an empty QD, a capture barrier must be formed, which is achieved through band-bending at the Schottky contact. The retention time for both logic states is determined by the emission and capture mechanisms associated with the QDs.[158,159] In their prototype, the processes of charging and discharging are initiated by the use of thermally assisted tunneling over the emission and capture barriers.[160,161] The rates of emission and capture depend factors such as barrier height (localization energy and capture barrier height), temperature, and electric field. Applying a negative bias to the gate was employed to write a logic "1". This action entirely removed the capture barrier formed by the band-bending, facilitating rapid write times in the order of nanoseconds.[162] The QD-flash approach efficiently addresses the limitations of flash SiO_2 barriers by using a significant barrier height, which may be practically reduced to zero during the writing process. This method makes it possible to achieve write times comparable to or perhaps shorter than that of DRAMs. To erase information, the electric field at the quantum dot site is intensified by applying a positive bias, which induces tunnel emission. Stored information is retrieved *via* the 2DHG located underneath the QD layer.

This study investigated the influence of stored holes in QDs on the conductance of the 2DHG by measuring the drain current (I_D) as a function of gate voltage (V_G) without light exposure. The experiments maintained a constant drain-source voltage of 100 mV. Fig. 12(c) depicts the characteristic graph of drain current against time in ms after erasing and writing for a saturated voltage of 0 V at a temperature of 50 K. As can be seen in Fig. 12(d), the measurement cycle starts with a 10 millisecond charging pulse ($V_G = -1$ V), which drives the QD states below the Fermi level. After that, the QD states are charged with holes from the two-dimensional hole gas (2DHG). When the gate voltage is increased to 1.5 V, a decrease in drain current occurs, eventually resulting in the pinching off of the 2DHG, which typically happens around 1.1 V for 2DHG.[163,164] Moreover, there was an expectation that the transference of holes within QDs would lead to a reduction in the carrier density within the 2DHG following Gauss' law.

During the downward voltage sweep, the quantum dots (QDs) remain occupied as long as the duration of the sweep is shorter than the time the holes are held within the QDs. Acting as Coulomb scattering centers, the charged QDs reduce the charge carrier mobility. This dual effect, encompassing both a diminished charge carrier density and lower mobility, contributes to a decrease in conductance during the downward sweep. Consequently, this manifests in a current trace lower than that observed during the upward sweep.[165,166] Because of the decreased mobility and lower charge carrier density, the

Table 4 Comparison of the parameters of various SAQD-based non-volatile memory

SAQD name	Composition	Dot size (nm)	Hole localization energy (eV)	Charge storage time (Years)	Strain	Ref.
InGaSb/AlP	InGaSb/AlP	4–4.5	1.35–1.50	10	Yes	154
GaSbP/AlP	GaSbP/AlP	4–4.5	1.35–1.50	10	Yes	154
InSb/AlP	InSb/AlP	4–4.5	1.65–1.70	10	No	167
InAs/GaAs	InAs/GaAs	2–5	1.0–1.20	5	Yes	157
InAs/AlGaAs	InAs/AlGaAs	3–6	1.20–1.40	7	Yes	168
CdSe/ZnS	CdSe/ZnS	3–5	1.40–1.60	6	Yes	169
Ge/Si	Ge/Si	2–3	1.30–1.50	9	Yes	26

conductance is reduced during the downward sweep. This results in a lower current trace as opposed to an upward sweep. In Fig. 12(d), the maximum hysteresis opening concerning the upward sweep is presented as a temperature-dependent function, considering two distinct sweep durations. Employing a sweep time of 1 ms, the hysteresis opening decreased from 32% at 20 K to nearly zero at 85 K. The decrease originates from the decreasing charge carrier storage time in the QDs at high temperatures. Stated differently, more holes are released during a declining sweep at greater temperatures. For the purpose of analyzing the QD-flash prototype memory performance, time-resolved measurements of the drain current at varying storage voltage (V_{st}) was obtained. Experiments such as this one make use of QDs that are either originally populated or blank. QDs are charged or discharged in accordance with the gate voltage, which may be either 0.8 V or 2 V. The gate voltage is quickly adjusted to the storage voltage after the initialization for either "1" or "0," and the drain current is continually checked to ensure that it remains constant. There are three distinct storage voltages (0, 0.4, and 0.7 V), and Fig. 12(e) provides a thorough perspective of the transients that occur at 50 K for each of these voltages. Hole capture into originally empty QDs is shown by increased transients. This results in a reduction in the conductance of the two-dimensional high-gain material, which in turn leads to a decrease in the drain current. Alternatively, lower transients indicate hole emission from QDs that are entirely occupied, which causes the drain current to increase until it reaches the equilibrium level. Fig. 12(e) illustrates that a change in the storage voltage from 0 to 0.4 V, and subsequently to 0.7 V had different impacts. Both transients showed an increase in the time constants; however, the amplitude of the capture transient decreased, while the amplitude of the emission transient increased. The obtained findings are attributed to the alterations in the capture and emission processes induced by the application of a positive storage voltage to the structure.

The valence band profiles corresponding to the three storage voltages elucidate these variations, as illustrated on the right side of Fig. 12(e). The transient amplitude is related to the quantity of transferred holes and the levels situated below the Fermi level for emission, as well as those above the Fermi level for capture. The Fermi level shifts towards the ground state of a QD with increasing positive storage voltages. Consequently, fluctuations in amplitudes occur due to the increase in the release of holes and decrease in their capture rate. The extension of the time constants is associated with the shift in the Fermi level, resulting in an increase in both capture and emission barrier heights (E_{bar} in Fig. 12(e)). They measured the write and erase times of the memory structure. A technique was employed to investigate emission from or capture into QDs across a broad range of time constants, facilitating the determination of the write and erase times. Following the application of write/erase pulses with progressively reduced pulse widths, down to 10 ns, the hysteresis opening at a storage position of 0.4 V was recorded. The hysteresis opening vanished if the pulse width was inadequate to charge or discharge the QDs.[21]

The pulse width corresponding to a 50% reduction in the maximum hysteresis opening was utilized to characterize the write/erase time. The write time at 20 and 50 K is shown as a function of the write pulse voltage in Fig. 12(f). An exponential decrease in write time is the outcome of a more negative write pulse, which lowers the capture barrier during the writing process. The saturation effect in write time is activated by write pulses over 0.5 V, achieving a minimum of 80 ns for a write pulse of 1.75 V. Fig. 12(g) illustrates the erase times clearly. At a capacity of 50 K, the results show that a minimum erase time of 350 ns was achieved with an erase pulse of 2.5 V. The observed increase in thermal capture and emission rates at elevated temperatures is clearly evident in the temperature sensitivity of both write and erase durations.[158] Table 4 provides information on several SAQDs including their composition, size, hole localization energy, charge storage duration, and strain condition.

4.3 Core–shell quantum dots (CSQDs)

CSQDs are fascinating nanoscale semiconductor particles, characterized by a core material enveloped by a shell of another substance.[170,171] Their unique structure offers intriguing possibilities in various applications. This class of nanoparticles stands out due to its distinctive optical properties, including enhanced photo-stability, broad absorption range, and narrow emission spectrum characteristic of quantum dots. The optical features of core/shell quantum dots are enhanced and intensified compared to regular quantum dots, owing to their unique structure. By further optimizing the structural composition QDs, we can achieve core/shell quantum dots.[172–174] QDs that have been coated with appropriate materials to form core/shell structures have enhanced stability and quantum yields

compared to QDs with only a core structure. Specifically, this is due to the fact that the growth of the shell restricts the excitation to the core and safeguards it from oxidation and chemical deterioration.[175–177] Composite quantum dots, which have a core–shell structure, exhibit unique properties that make them attractive for both experimental and practical purposes.[175] Core/shell-structured CdSe nanoparticles have attracted significant attention due to their fascinating potential in future nonvolatile flash memory systems, which are noted for their low power consumption and ultrahigh-density components.[178,179]

4.3.1 Brief operation of CSQDs in NVM systems

4.3.1.1 Charge trapping/detrapping. This technique depends on the capacity of memory cells to hold and release electrical charges. Here, core–shell quantum dots are important. Charges can occasionally become trapped in defect states either in the core itself or at the interface where the materials of the shell and core meet. A voltage can be applied to modify the distribution of these trapped charges, which indicates a shift in the memory state (often a '0' or '1'). Then, the memory state can be reset by applying a different voltage later on, which will free the trapped charges.[180–182] Z. Sun *et al.*[183] fabricated nonvolatile memory with a floating gate structure using ZnSe@ZnS core–shell quantum dots as discrete charge-trapping and tunneling centers. ZnSe quantum dots (QDs) were used as the charge storage centers in four types of FGT nonvolatile memories.

The FGT nonvolatile memory utilizing the ZnSe/ZnS core–shell quantum dots demonstrated a significant memory window, impressive endurance, and stable retention. Also, oleic acid (OA) was used as a capping agent. The working mechanism of their fabricated device is depicted in Fig. 13. The ZnS shell forms a type-I core–shell structure, while the OA ligand acts as a dielectric layer because of its low conductivity. Trapped electrons pass across these layers during the writing process using a gate pulse (V_G) of 130 V for 100 ms in the ZnSe QDs. The ZnS shell and OA ligand must both be present for some trapped electrons to spontaneously return to the conductive channel when the gate pulse, V_G, is withdrawn. ZnSe@ZnS-OA QDs have the best charge-holding capacity given that they have both a ZnS shell and OA ligand, but ZnSe-MPA QDs have the maximum recovery because they do not have blocking layers. In the case of ZnSe@ZnS-OA QDs, this led to the widest memory window despite their lower QD density. To restore a neutral state, the trapped electrons can be erased with a negative gate pulse of −50 V/100 ms. The trapped electron equilibrium state is ranked according to charge-holding capacity, where the charge-holding capacity has a greater influence than the QD density.

4.3.1.2 Nordheim and fowler tunneling in core–shell QDs. This process includes controlling the passage of electrons through a tiny layer of insulating material. The shell usually serves as the insulator in core–shell quantum dots made for this purpose. Electrons may be "tunneled" through this thin shell with a high voltage, changing the conductivity of the device. The stored data is represented by this change in conductivity. To keep the memory state, lowering the voltage usually prevents electrons from passing back through the barrier.[180–182] These are only two instances; the precise method may differ based on the components and design of the gadget. Nonetheless, the fundamental idea is the same, controlling the electrical characteristics of the device by deliberate charge manipulation to encode and store data.

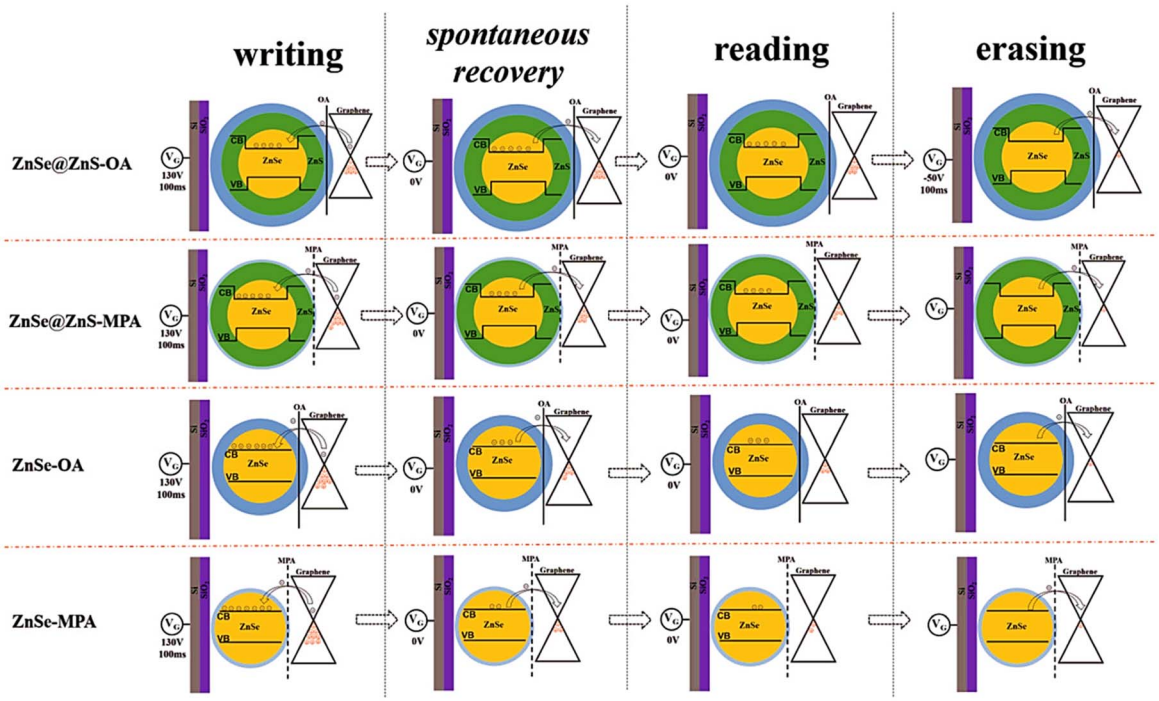

Fig. 13 Mechanism of charge trapping-detrapping in core–shell and non-core–shell QDs and retain process in each of the four quantum dots with the associated devices of writing, reading, and erasing. Reproduced from ref. 183 with permission from Wiley. Copyright 2019, Wiley.

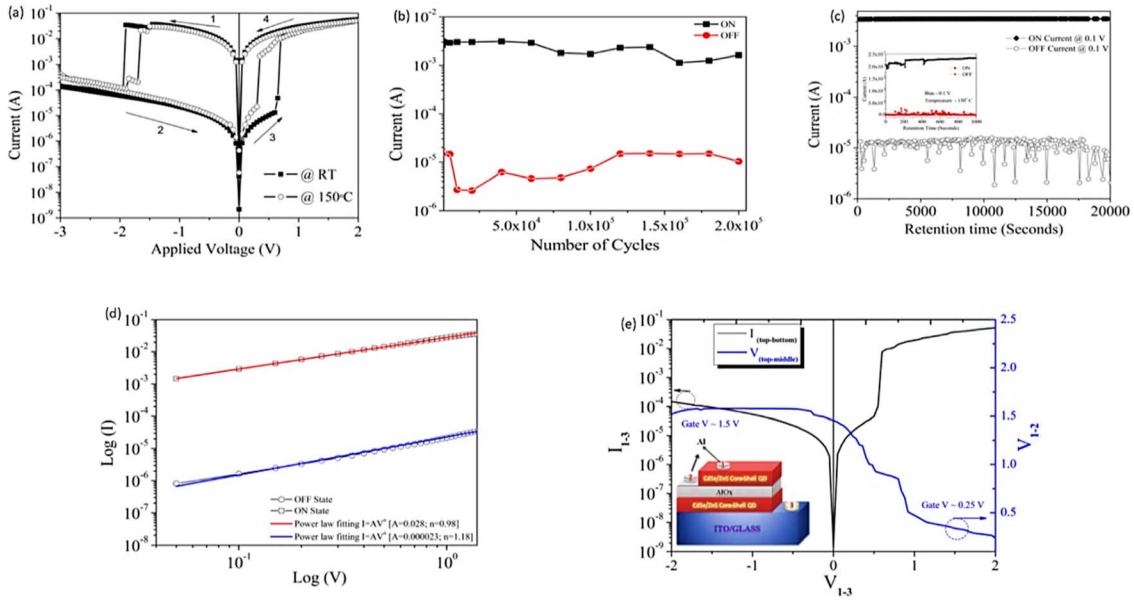

Fig. 14 (a) *I–V* switching behavior of the ITO/CdSe–ZnS core–shell quantum dot/Al device at room temperature and 150 °C, with arrows showing the switching direction. (b) Endurance performance for core–shell quantum dot memory devices over 200 000 switching cycles. (c) Retention data at 0.1 V for 20 000 seconds, with an inset showing a 150 °C retention test for 1000 seconds. (d) Log *I vs.* log *V* plot for *V* < turn-off voltage in both ON and OFF states. (e) *I–V* characteristics of a three-terminal device, with current through top and bottom electrodes on the left *y*-axis, and potential drop between top and middle electrodes on the right *y*-axis. The inset shows the device schematic with three leads. Reproduced from ref. 181 with permission from RSC. Copyright 2013, RSC.

4.3.2 CdSe/ZnS CSQDs for nonvolatile memory. The study conducted by V. Kannan *et al.*[19] showcased the use of quantum dot nanoparticles with a CdSe/ZnS core/shell structure, measuring around 5.2 nm in diameter. These nanoparticles were synthesized on a glass substrate that was coated with indium tin oxide (ITO). They fabricated the memory device with the CdSe/ZnS quantum dots sandwiched between 120 nm aluminum electrodes (diameter in the range of 1 mm to 0.3 mm) using spin coating, thermal evaporation, and shadow masking techniques. The thickness of the quantum dot layer was measured to be approximately 60 nm. The devices showcased reliable bipolar non-volatile resistive memory features throughout their performance. In Fig. 14(a), it can be observed that the ON state is achieved by applying a forward voltage sweep, while the OFF state is reached through the application of a reverse voltage sweep. The device exhibited a notable increase in injection current of around 0.6 V, indicating its shift from a low-conductivity state (OFF-state) to a high-conductivity state (ON-state), commonly known as the 'writing' process.

Conversely, at approximately −2 V, the device reverts from the ON state back to the OFF state, a process referred to as 'erase'. The process of reading is executed by scanning to +0.1 V, which is employed to discern the two different 'ON' and 'OFF' states. The device showcases a fascinating characteristic where two conducting states occur at the same voltage, illustrating a bi-stable behavior that is quite noteworthy. The device status endured even after removing the applied bias. Therefore, a demonstration of non-volatile resistive memory with bi-stable behavior was presented. The conductivity ratio achieved between the two states was 10^3. The device demonstrated a reliable and consistent switching process between its ON and OFF states. The voltages applied for writing, erasing, and reading were 2 V, −3 V, and 0.1 V, respectively.[19] The endurance results from a multi-cycle measurement are presented in Fig. 14(b). The resistance values remained stable in both the ON and OFF states throughout 200 000 switching cycles. To assess the retention time of the memory devices in these states, a constant low voltage of 0.1 V was applied across the top and bottom electrodes, with current measurements taken at regular intervals of 10 s, as shown in Fig. 13(c). The current in the ON state was nearly three orders of magnitude higher than that in the OFF state. Fig. 14(c) indicates that there was minimal degradation in the device during the 20 000 s stress test for both states, confirming their stability. Although the ON-state current maintained a steady profile, the OFF-state current exhibited some fluctuations, which is likely due to charge storage in the QDs/AlO_x nanoclusters. The retention tests conducted at 150 °C for both states at 0.1 V over 1000 s showed that the device remained stable. Furthermore, after six months post-fabrication, there was no significant decline in performance. The memory device also demonstrated a consistent distribution of set and reset voltages, with averages of approximately 0.7 V and −1.7 V, respectively, for a single device.[19] Fig. 14(d) illustrates the log-scale *I–V* characteristics for both the ON and OFF states when the voltage is below the turn-off threshold. In this region, the ON state follows a power–law relationship described by $I = AV^n$, where n is the exponent factor (with $n = 1$ indicating ideal ohmic conduction) and A is a coefficient related to the resistance state. The ON state shows an exponent factor (n) close

Table 5 Comparison of the parameters of various CSQD-based non-volatile memory systems

Core–shell QD	Core material	Shell material	Retention time (s)	ON/OFF ratio	Ref.
CdSe/ZnS	CdSe	ZnS	2×10^4	10^3	181
CdSe/ZnS	CdSe	ZnS	2.88×10^5	1.43×10^6	184
CdSe/ZnS	CdSe	ZnS	7.2×10^5	3.78×10^5	185
CdTe	CdTe	—	10^4	—	186
CdSe/CdS	CdSe	CdS	—	13.4	5
Ti–TiO_x/CdSe–ZnS	Ti–TiO_x	CdSe–ZnS	1.5×10^3	100	182
CdTe/CdSe	CdTe	CdSe	$>10^3$	$>10^3$	187
CdSe/ZnSe	CdSe	ZnSe	8×10^3	2.7×10^3	188
CdSe/AlO_x	CdSe	AlO_x	4×10^3	$>10^4$	9

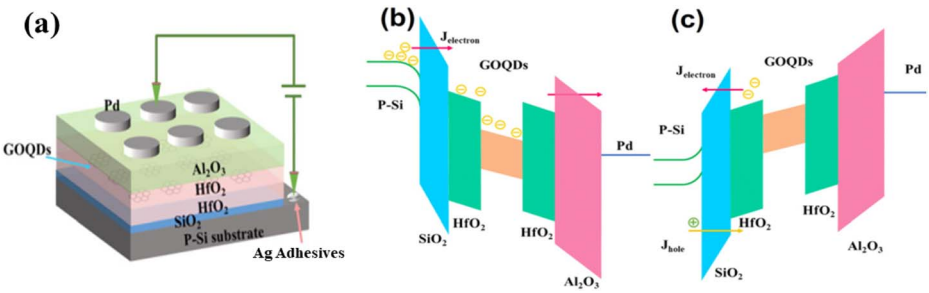

Fig. 15 (a) Pd/Al_2O_3/HfO_2/GOQDs/HfO_2/SiO_2/Si charge trapping memory device, (b) programmed state and (c) erased state. Reproduced from ref. 31 with permission from AIP. Copyright 2020, AIP.

to 1, suggesting that it behaves according to ohmic conduction. In contrast, the OFF state curve exhibits a slightly exponential trend with n greater than 1, which points to more complex transport mechanisms at play. They developed a three-terminal memory device with the structure Al/CdSe–ZnS core–shell QD/AlO_x/CdSe–ZnS core–shell QD/ITO/glass. The middle Al/AlO_x layer served as the third terminal, as shown in the inset of Fig. 13(e). The aluminum contact for the third terminal was created using the previously mentioned shadow mask. The transition between the two conducting states is attributed to the trapping and de-trapping of charges in the CdSe/ZnS core–shell quantum dots embedded in the AlO_x matrix. A bias was supplied between the top and bottom electrodes, as shown in Fig. 14(e), which depicts the voltage sweep in the range of −2 to +2 V. The right Y-axis of the graph shows a representation of the bias-dependent potential drop that occurs on the top section of a three-terminal memory device (between 1 and 2 of the voltage range). In addition, it displays the measured device current *via* 1 and 3 (on the left Y-axis). The bulk of the negative voltage bias occurs when the device is in the OFF state, and the potential drop V_{1-2} is about 1.5 V during the majority of the bias. A comparison of the characteristics of various core–shell QDs in non-volatile memory systems is displayed in Table 5. There is a significant decrease in V_{1-2} at the switch ON voltage, which is around 0.6 V. Subsequently, V_{1-2} stabilizes at 0.25 V as the positive voltage bias ends. Similarly, when the memory device transitions from the ON state to the OFF state at roughly −1.5 V, there is a dramatic increase in voltage 1–2. This occurs during the reverse voltage sweep.[19]

4.4 Graphene oxide quantum dots

Graphene oxide quantum dots are nanocrystal particles derived from graphene oxide with a diameter typically less than 10 nm. They have special characteristics including effective photo-induced electron transfer, high solubility, adjustable photo-luminescence, minimal toxicity, and biocompatibility. Because of these features, GOQDs are well suited for a wide range of uses, including non-volatile memory.[189,190] GOQDs are placed in high-k materials such as HfO_2 charge trapping layer for use in non-volatile memory applications. With a wider memory window and less gradual charge depletion, this integration improves the memory properties.[31] Because GOQDs are less susceptible to local tunnelling oxide defects, lateral charge transfer is less likely to occur, improving the data retention and density.[191] Because of these qualities, GOQDs are materials that holds great promise for creating high-performing non-volatile memory devices.[20,189]

4.4.1 Brief operation of GOQDs in NVM systems. The majority of non-volatile memory devices based on GOQDs use either charge trapping or resistive switching to function.[20,191] This increases the ability of electrons to be trapped, and thus information is stored for a long time. Yang *et al.*[31] conducted a study to enhance charge trapping memory through the use of graphene oxide quantum dots. The fabricated memory prototype is presented in Fig. 15(a), while the programmed and erased states are depicted in Fig. 15(b) and (c), respectively. When the applied voltage (V_G) reached a high positive value (programmed state), electrons could traverse the 4 nm-thick SiO_2 barrier *via* Fowler–Nordheim tunneling.[192] During the

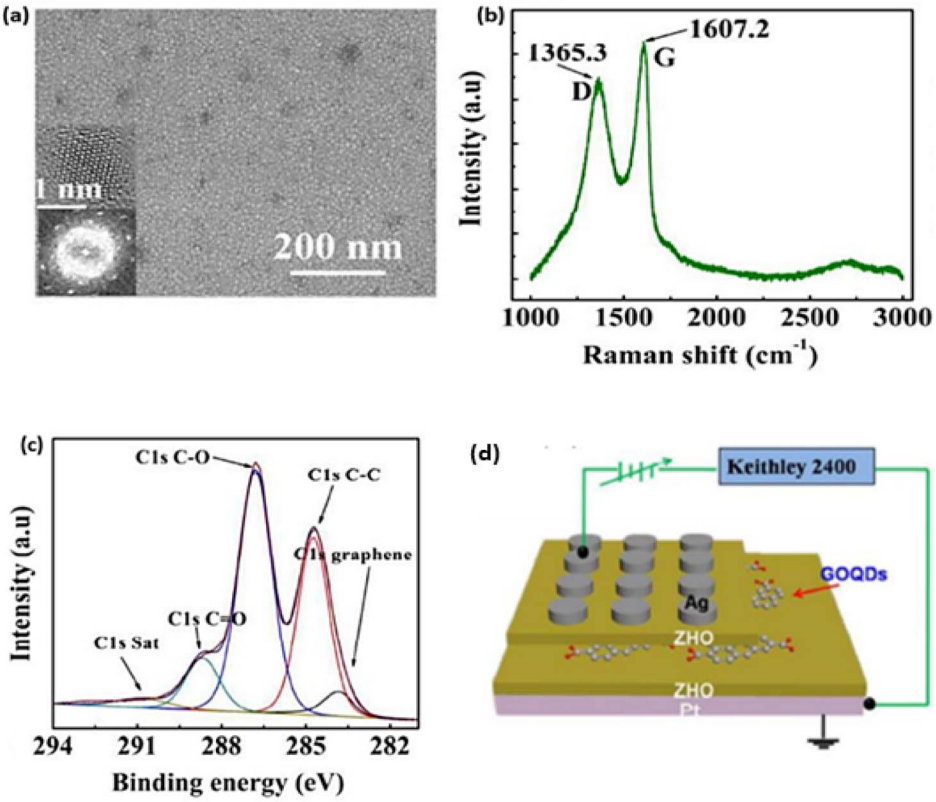

Fig. 16 Properties of graphene oxide quantum dots (GOQDs). (a) Scanning electron microscope (SEM) images showing GOQDs on ZHO films, with high-resolution transmission electron microscope (TEM) images and their corresponding two-dimensional fast Fourier transform (2D FFT) images displayed in the bottom-left corner. (b) Raman spectrum illustrating GOQDs on mica. (c) X-ray photoelectron spectroscopy (XPS) characterization of GOQDs on ZHO films. (d) Schematic of memory prototype. Reproduced from ref. 20 with permission from RSC. Copyright 2017, RSC.

programming process, the application of a positive voltage to the Pd electrode facilitates electron tunneling through the SiO_2 triangular energy barrier from the Si substrate. Subsequently, these electrons are driven by the strong electric field into the conduction band of HfO_2, and then into the conduction band of the GOQDs, as illustrated in Fig. 15(b). Then, numerous electrons penetrate the HfO_2 layer beneath the GOQDs. During the erasing process, applying a negative voltage to the Pd electrode facilitates the transfer of electrons trapped in the quantum well of GOQDs and defects in HfO_2 from the charge layer back to the substrate. Concurrently, holes traverse the barrier and are directed by the strong electric field into the valence band of HfO_2, subsequently entering the valence band of the GOQDs and the underlying HfO_2, resulting in a shift in the flat-band voltage in the negative direction, as illustrated in Fig. 15(c).

4.4.1.1 Write operation. A higher voltage pulse is used to inject charges into the GOQDs during the writing process. One possible binary '1' state is the result of the trapped charges changing the electrical conductivity of the device.[20,191]

4.4.1.2 Erase operation. The erase operation returns the conductivity to its initial state, which represents a binary '0', by releasing the trapped charges with a reverse or lower voltage pulse.[20,191]

4.4.2 GOQD in resistivity-based memory applications. Generally, ReRAM denotes the electrical transition between various resistance states observed in various metal oxides (such as NiO_x, HfO_x, TiO_x, TaO_x, and $Pr_xCa_{1-x}MnO_3$). However, a similar effect has also been documented in non-oxide materials, including silicon, sulfides, and chalcogenides.[193] A solid-electrolyte insulator can be used in resistor random-access memory (ReRAM) to make it more useful in nonvolatile memory, analog circuits, and neuromorphic synapse systems. However, improving the performance of ReRAM is still challenging because the switching factors are not always the same. This is because the nucleation and conductive filament (CF) generation process is not always reliable. Thus, to overcome these obstacles, Xiaobing Yan *et al.*[20] incorporated GOQDs into $Zr_{0.5}Hf_{0.5}O_2$ (ZHO) oxide films and observed an improved result. They performed several experiments and obtained the expected results. In Fig. 16(a), the scanning electron microscopy (SEM) image illustrates the presence of GOQDs on the ZHO films, suggesting the relatively uniform distribution of GOQDs. Fig. 16(b and c) show the Raman spectra and XPS response of the GOQD, respectively. GOQDs typically have dimensions in the range of 30 to 50 nm.

The lower left corner of Fig. 16(a) displays the high-resolution TEM images of GOQDs, together with their

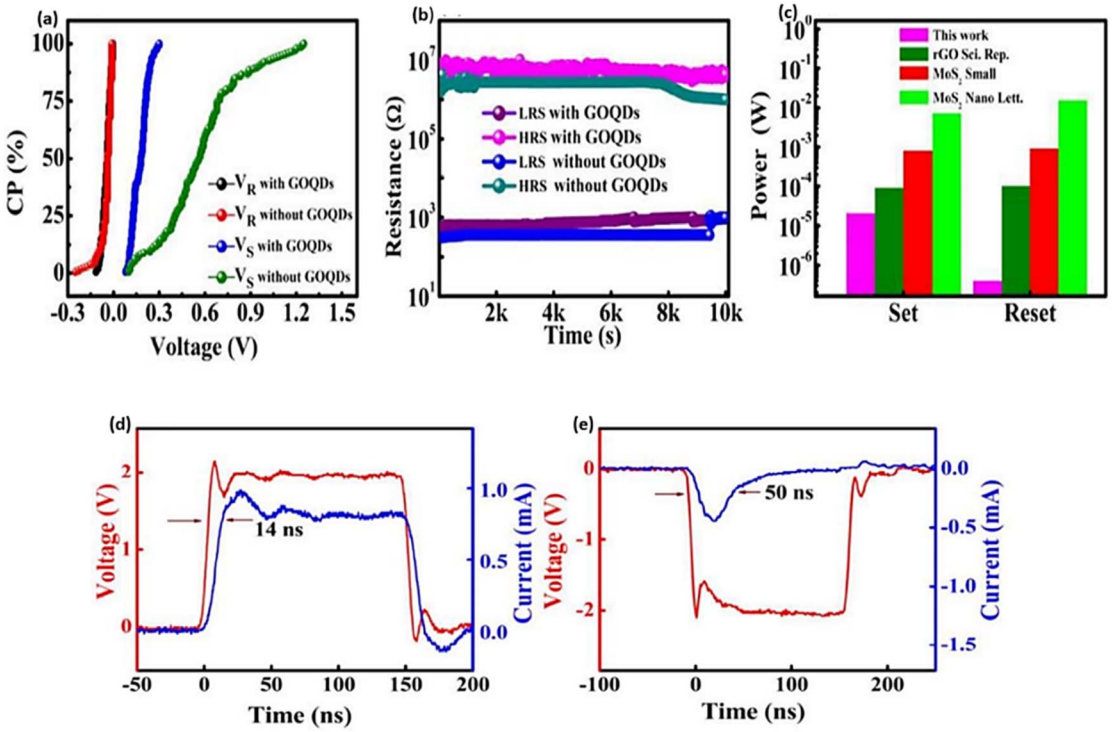

Fig. 17 (a) Statistical distribution of threshold voltage in ZHO-based devices with and without GOQDs. Cumulative probability is abbreviated as CP. (b) Retention behavior of ZHO-based devices with and without GOQDs. (c) Graph with magenta bars depicting the power consumption of the device with GOQDs, while the green, red, and olive bars representing the power consumption reported in ref. 194–196 for other devices. (d) Configuration of input pulse (depicted in red) and the resulting conducting current output (depicted in blue) during the SET operation. (e) Configuration of input pulse (depicted in red) and the resulting conducting current output (depicted in blue) during the RESET operation. Reproduced from ref. 20 with permission from RSC. Copyright 2017, RSC.

corresponding 2D fast Fourier transform (FFT) images. Both the TEM image and FFT pattern reveal a highly crystalline structure with a lattice spacing of approximately 0.24 nm. The AFM analysis of the GOQDs on ZHO films indicated that their height is roughly 1 nm. The Raman spectroscopy data for GOQDs, as shown in Fig. 16(b), revealed the disordered (D) band at 1365.3 cm^{-1} and crystalline (G) band at 1607.2 cm^{-1}. The intensity ratio of the D band to the G band (I_D/I_G) is 0.92.

The XPS data, as shown in Fig. 16(c), were used to determine the composition of the GOQDs. The GOQDs display a sp^2 C 1s peak at 284.5 eV, accounting for 30.14%, an sp^3 carbon peak, which includes hydroxyl groups, at 287.24 eV (50.62%), and a carboxyl peak at 289.5 eV (16.24%). These peaks correspond to C═C/C–C in the aromatic rings, C–O (epoxy and alkoxy), C═O (carbonyl), and COOH (carboxylic) groups, respectively. The dominant peak at 287.24 eV is attributed to sp^3 carbons, particularly the hydroxyl group. Fig. 16(d) depicts the prototype of the memory, where grey balls represent carbon atoms and red balls represent oxygen atoms.

To demonstrate the enhanced stability of the device using GOQDs, a 200 loop test of two types of devices was statistically examined. Fig. 17(a) depicts the statistical threshold distribution of the ZHO-based device with and without GOQDs. In the case of the GOQD device, the values of V_S and V_R were limited in a 200-times continuous RS cycle measurement to the range of 0.08 V to 0.3 V and −0.14 V to −0.01 V, respectively. However, in the device without GOQDs, the values of V_R and V_S were in the range of 0.08 to 1.25 V and −0.01 to −0.25 V, respectively. According to the comparison of the results for the two types of ZHO-based devices, the Ag/ZHO/GOQDs/ZHO/Pt memory device has a smaller distribution of V_S and V_R than the device without GOQDs. This enhanced the precision of programming voltage control during set and reset operations, making the device more suitable for practical use.

Based on the test results, it is evident that incorporating GOQDs led to performance improvements, particularly in achieving better uniformity. Fig. 17(b) illustrates the retention characteristics of devices with and without GOQDs. Notably, in the absence of GOQDs, the resistance of HRS and LRS began to fluctuate after 1×10^4 s,[197] whereas the device containing GOQDs maintained stable resistance levels. Furthermore, given the current data trend, the stored information in this structure appeared to remain intact for an extended period, demonstrating the reliability of the bipolar RS effect. As a result, the device integrated with GOQDs exhibited a superior retention performance compared to its counterpart without GOQDs. The power consumption for the set and reset processes of the device using GOQDs is around 2×10^{-5} W and 3.9×10^{-7} W, respectively ($P_{Set} \times R_{Off} = V_{SET2}$, $P_{Reset} \times R_{On} = V_{Reset2}$). This is lower than the power requirements of the devices made from graphene oxide (GO) or MoS_2 materials, as shown in Fig. 17(c).[194–196] A pulse of 2 V and a −2 V negative pulse, each

Table 6 Comparison of the parameters of graphene oxide quantum dot in non-volatile memory system

Functional layer	Trapped charge density (cm^{-2})	Gate voltage (V)	Memory window (V)	Retention time (s)	Ref.
SiO_2/GOQDs/ZHO/SiO	1.21×10^{14}	±3	1.67	1.08×10^4	200
SiO_2/ZHO/SiO_2	7.45×10^{13}	±5	1.67	1.08×10^4	200
ZnO/GOQDs/ZnO	1.57×10^{11}	±4	1.86	10^4	201
Al_2O_3/HfO_2/GOQDs/HfO_2	3.7×10^{12}	±3.5	1.57	1.2×10^4	31
GOQDs/PS/pentacene	7.2×10^{12}	>±12	>12	10^4	202
ALD–Al_2O_3	7.2×10^{12}	±5	3.27	3.1536×10^8	203
h-BN/MoS_2/h-BN	—	±5	>12	10^5	204

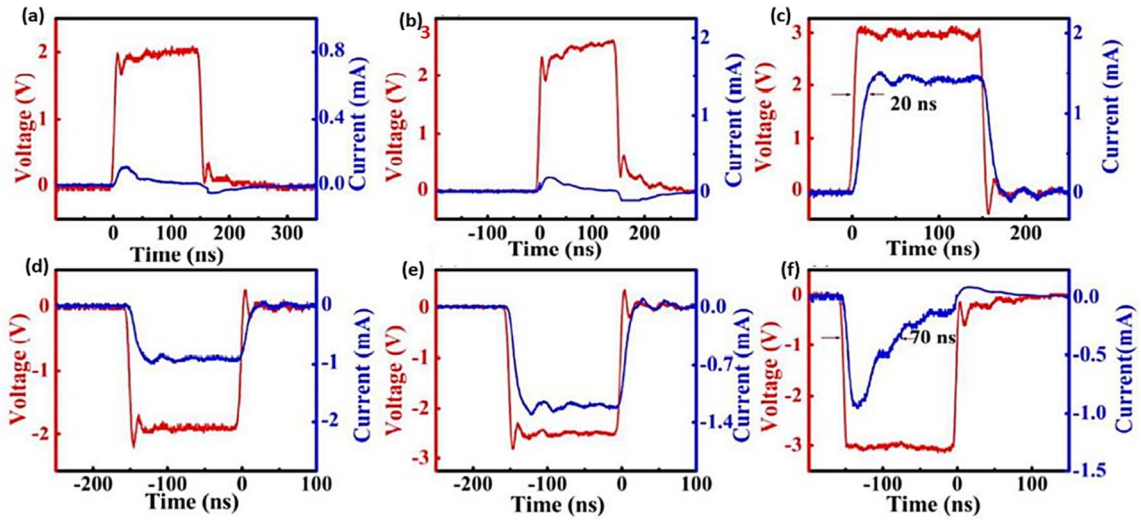

Fig. 18 Results of the switching-speed measurement for the ReRAM device lacking GOQDs. Illustrations include input pulse shapes in red and corresponding output conducting current shapes in blue. The input pulses have amplitudes/widths of (a) 2 V/150 ns, (b) 2.5 V/150 ns, (c) 3 V/150 ns, (d) −2 V/150 ns, (e) −2.5 V/150 ns, and (f) −3 V/150 ns. Reproduced from ref. 20 with permission from RSC. Copyright 2017, RSC.

lasting 150 ns, were used to activate and deactivate the device, as shown in Fig. 17(d and e), respectively. All devices operated successfully. The device could be programmed to a low resistance state (LRS) in just 14 ns and to a high resistance state (HRS) within 50 ns during programming, showcasing faster switching speeds compared to traditional ReRAM devices.[198,199] Table 6 illustrates a comparative analysis of several functional layers of GOQDs in terms of trapped charge density, gate voltage, memory window, and retention time for non-volatile memory applications. Fig. 18(a–c) show that pulses with amplitudes of 2 V/150 ns and 2.5 V/150 ns are insufficient to switch the device from a high resistance state (HRS) to a low resistance state (LRS).

However, when the pulse amplitude was increased to 3 V, the device was successfully activated. During the reset process, as shown in Fig. 18(d–f), pulses of −2 V/150 ns and −2.5 V/150 ns were ineffective at deactivating the device, which remained off until a 3 V pulse lasting 150 ns was applied. The device response times for activation and deactivation were approximately 20 ns and 70 ns, respectively.

4.4.3 Potential of GQDs in emerging ReRAM. Graphene-based materials, known for their exceptional electrical and structural properties, have been explored extensively for ReRAM devices. Ren *et al.*[205] found that incorporating graphene quantum dots (GQDs) significantly improved the resistive and magnetic switching performance of Ag/GQD:GO/ITO devices, achieving a resistance switching (RS) ratio nearly 20 times greater than that of the devices without GQDs. Fig. 19(a) illustrates the RS performance, showing a forming-free bipolar RS behavior ideal for low power consumption.[206] The device transitions from a high-resistance state (HRS) to a low-resistance state (LRS) at −0.43 V (SET voltage) and resets at 0.43 V (RESET voltage), both about 65% lower than comparable devices. The histograms in Fig. 19(b) depict stable V_{SET} and V_{RESET} values (0.06 V and 0.04 V), respectively, signifying improved voltage uniformity. Over 500 cycles, the Ag/GQD:GO/ITO device maintained a high RS ratio (>10^3), with minimal deviation in resistance states (~41 kΩ HRS, ~40 Ω LRS), outperforming the Ag/GO/ITO devices.[207,208] After 28 days, its RS ratio remained above 10^3, highlighting its excellent endurance and retention, as shown in Fig. 19(c) and (d), respectively.

The reliability tests on 36 randomly selected memory cells, as shown in Fig. 20(a and b), show an 89% functional yield, with minimal variation. Fig. 20(c) confirms the stable bi-stable resistance states, while Fig. 20(d) demonstrates the centralized operating voltages (~0.05 V), ensuring high reliability.

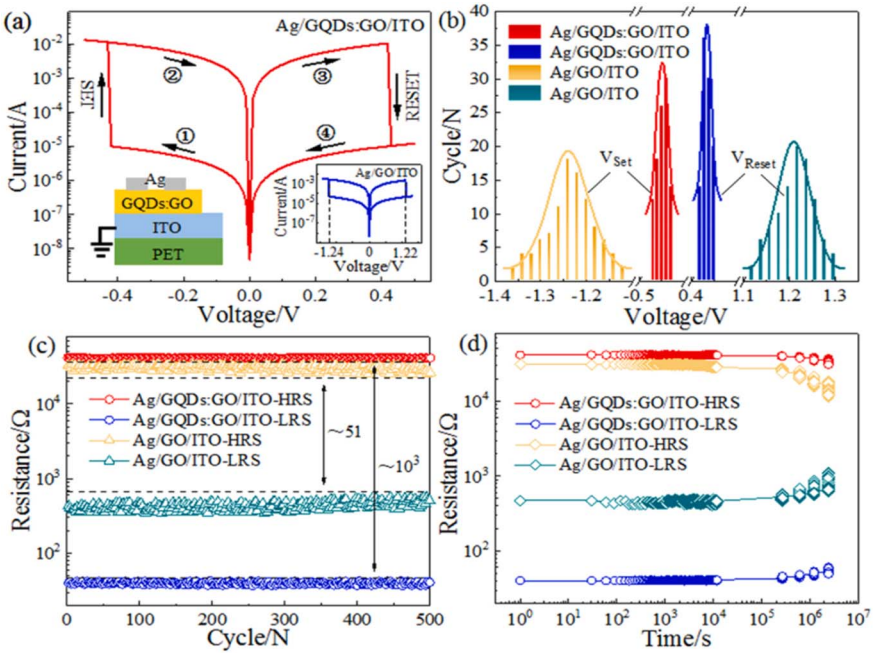

Fig. 19 RS performance comparison of Ag/GQDs:GO/ITO and Ag/GO/ITO devices. (a) *I*–*V* characteristics of the Ag/GQD:GO/ITO device, with arrows indicating the voltage sweeping directions. The left inset provides a schematic of the Ag/GQD:GO/ITO device structure, while the right inset displays the *I*–*V* characteristics of the Ag/GO/ITO device. (b) Distribution of VSET and VRESET over 100 switching cycles. (c) Endurance performance and (d) retention capability of both Ag/GQD:GO/ITO and Ag/GO/ITO devices, with HRS and LRS measured at −0.02 V. Reproduced from ref. 205 with permission from Elsevier. Copyright 2021, Elsevier.

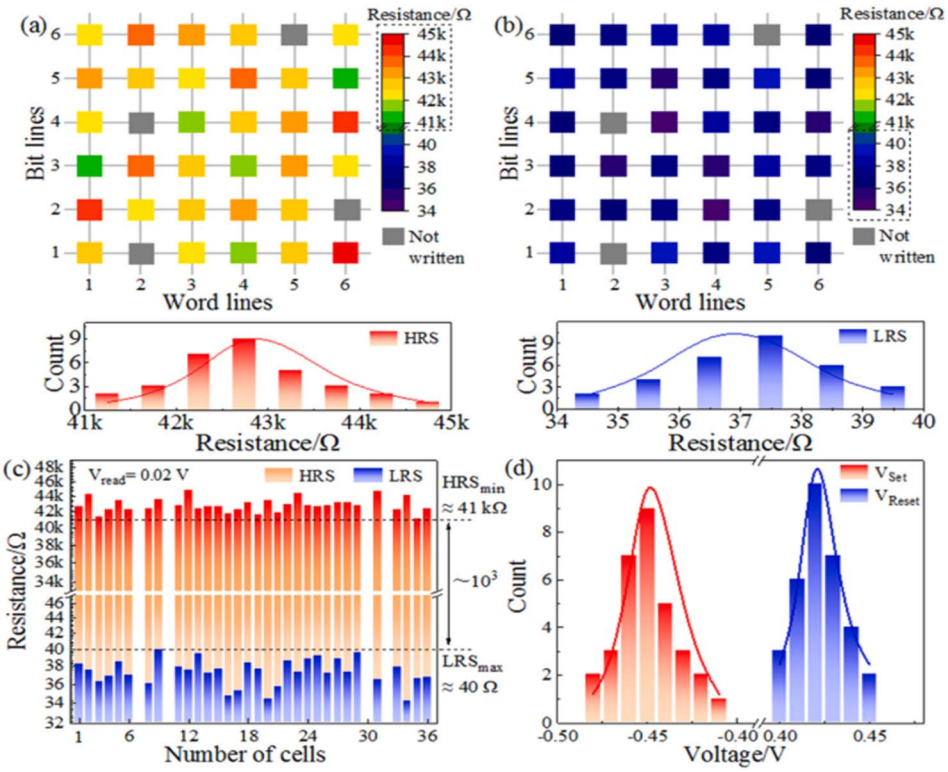

Fig. 20 Color-coded resistance map of 36 memory cells in (a) HRS and (b) LRS states. Unwritten cells are shown in grey. The resistance values, represented by the color scale bar on the right, are mapped accordingly. The resistance distributions for each memory cell in the HRS (red) and LRS (blue) are illustrated in histograms at the bottom. (c) Resistance values of HRS (red) and LRS (blue) plotted for each memory cell, with blank spaces indicating unwritten cells. The minimum HRS value and maximum LRS value are highlighted on the right. (d) V_{SET} and V_{RESET} distributions across 32 standard memory cells. Reproduced from ref. 205 with permission from Elsevier. Copyright 2021, Elsevier.

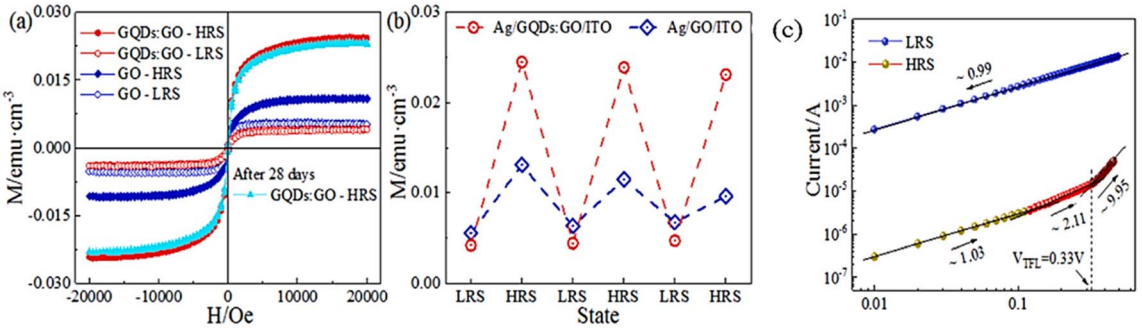

Fig. 21 GQD:GO hybrid film and GO film room-temperature LRS and HRS magnetism. (a) *M*–*H* curve. (b) RS behaviour causes reversible magnetic moment shifts. (c) Linear fitting of Ag/GQD:GO/ITO device *I*–*V* curve on log–log scale. Reproduced from ref. 205 with permission from Elsevier. Copyright 2021, Elsevier.

Table 7 Comparison of the non-volatile memory properties of different quantum dots

Materials	ON/OFF ratio	Retention time (s)	Multilevel	Ref.
$CsPbBr_3$ QD	1.86×10^5	10^3	6	151
$CsPbBr_3$ QD	10^7	3.16×10^8	4	138
$CsPbBr_3$ QD	10^4	10^3	2	18
$CsPbBr_3$ APQD	10^7	10^3	3	152
$CsPbBr_3$ QD	1.6×10^5	>100	2	211
$CsPbI_3$	10^3	10^4	—	133
CdSe	10^4	$>3.6 \times 10^3$	3	19
$CH_3NH_3PbBr_3$ QD	10^3	4×10^3	3	132
$CH_3NH_3PbI_3$ QD	10	10^4	—	150
GO QD	—	1.08×10^4	3	200
GO QD	10^4	10^4	4	20
GO QD	3×10^3	10^4	3	212
GO QD	—	1.08×10^4	6	200
GO QD	10^3	10^4	3	37
GO QD	10	10^2	2	213
Graphene QD	10^6	2×10^4	5	214
Graphene QD	10^5	10^4	2	215
Graphene QD	10^6	200	2	216
Graphene QD	10^4	10^4	2	217
ITO-free graphene QD	10^4	10^4	2	218
Graphene QD	10^4	10^4	4	219
Ti–CdSe/Ti–TiO_x–CdSe	100	10^4	2	220
Ti–TiO_x/CdSe–ZnS QD	100	1.5×10^2	2	182
CdSe QD	10^5	10^4	2	221
CdSe	6.1×10^4	Long	4	222
CdSe/ZnS QD	6.9×10^4	10^4	7	141
CdSe/ZnS QD	10^4	10^4	2	223
Si QD	10^7	10^5	2	224
Fe_2O_3 QD	10^7	10^5	2	26
InP QD	—	10^5	2	225
InAs QD	10^3	—	2	226
Carbon QD	10^4	7×10^6	5	227
$CuInS_2$ QD	10^5	1.5×10^3	2	180
Al/CdSe–ZnS QD	10^3	2×10^4	2	181
Black P QD	$>10^4$	10^4	2	228
CdTe QD	—	10^4	2	186
ZnO QD	5×10^4	10^5	2	229
InO_x QD	100	5×10^3	2	230
MoS_2 QD	10^7	10^4	2	231
MoS_2 QD	$>10^4$	2×10^3	3	232
MoS_2 QD	10^2	10^4	—	233
MoS_2 QD	10^5	Long	4	234
WS_2	10^4	Long	3	235
WSe_2 QD	100	7×10^3	4	236
MXene QD	100	1.2×10^4	4	237
Ag–In–Zn–S QD	10^5	10^4	—	28

Fig. 21(a) presents the *M–H* curves for graphene oxide and hybrid GQD films in HRS and LRS switching, while Fig. 21(b) reveals the enhanced magnetic switching in the GQDs:GO hybrid films compared to GO films. The hybrid film exhibited a higher saturation magnetization (M_s) in HRS (2.45×10^{-2} emu cm^{-3}) than in LRS (4.18×10^{-3} emu cm^{-3}), with a magnetic change ratio (MHRS/MLRS) of 5.86, which is substantially greater than that of GO of 2.01. After 28 days, the hybrid film retained over 95% of its magnetization, showing superior magnetic stability. Additionally, it maintained magnetic properties over three RS cycles, unlike the GO films, which degraded to 71% of their initial ratio.

The *I–V* slope in Fig. 21(c), plotted on a log–log scale, indicates that at low bias, the HRS follows linear (slope = 1.03) and quadratic (slope = 2.11) behavior, while at high bias, the slope increases to ~9.95, confirming space-charge-limited conduction (SCLC).[209,210] The linear relationship (slope ~0.99) of the *I–V* curve over the whole voltage sweep range in the LRS validated the ohmic conduction behaviour, indicating that high conductivity was a localized filamentary effect in the LRS.[209] The calculated trapped charge density in the high resistance state (HRS) is approximately 4.508×10^{16} cm^{-3}, which significantly decreased to approximately 0 in the low resistance state (LRS). These findings indicate that the trap densities, primarily associated with oxygen groups in graphene oxide (GO), can be substantially reduced by applying a negative electric field to the device in the low resistance state (LRS). A comparison of the data of various QD-based NVMs is presented in Table 7.

5. Challenges and future scope

QD-based NVM devices face several significant challenges that impede their practical application. A primary concern is charge retention; QDs are prone to charge leakage due to quantum tunneling and interface defects, leading to decreased data stability over time.[238] Additionally, the variability in the size and distribution of QDs affects the memory uniformity and performance, complicating large-scale manufacturing. Scalability is another issue, given that maintaining consistent characteristics across an array of memory cells is challenging.[239]

Integrating QD-based memory with existing semiconductor technologies, particularly CMOS, involves overcoming material compatibility and fabrication complexities.[240] Furthermore, QD memories require precise control voltages to prevent unintended charge loss or disturbances, resulting in increased power consumption.[241] The reliability of QD-based memory under varying temperature and environmental conditions is also a significant obstacle, given that the charge trapping and de-trapping behaviors change with external factors. Despite these challenges, research continues to explore novel materials, improved fabrication methods, and optimized device architectures to enhance the memory performance and feasibility of QDs for commercial applications.[239] QD-based non-volatile memory devices hold significant promise for future technological advancements. One potential development is the integration of QDs with memristor-based systems, which can enable scalable cryogenic quantum dot biasing, enhancing the performance in quantum computing applications.[240] Additionally, the use of III–V self-assembled quantum dots as floating gates in non-volatile memories is being explored to achieve long charge storage times, aiming for data retention of up to 10 years. Furthermore, the energy-efficient manipulation of topologically protected states in QD-based devices offers the potential for ultrafast switching speeds and low power consumption, which are crucial for high-performance computing applications. Advancements in QD synthesis methods, material properties, and device architectures are expected to overcome current limitations, paving the way for the practical implementation of QD-based non-volatile memory in various applications.[167]

6. Conclusions

The latest developments in information and technology have led to an increase in the need for non-volatile memory that is both efficient and effective. In the field of non-volatile memory, quantum dots are innovative technology that have the potential to totally transform the available technology for data storage. Within the scope of our investigation, we explored the potential role that quantum dots may play in the implementation of non-volatile memory. In comparison to conventional non-volatile memory, quantum dot-based non-volatile memory demonstrates a greater ON/OFF ratio, a longer retention period, and a greater number of sweep voltages. Because of these enhanced qualities, quantum dots have emerged as potential raw materials for the development of non-volatile memory systems. An examination of the comparative analysis shown in the tables illustrates the varied performance of quantum dots across a variety of parameters. Although quantum dots have huge promise for non-volatile memory, there are still several difficulties that have not been addressed, including their scalability, stability, and integration with available technology. The resolution of these challenges, as well as the investigation of innovative materials and manufacturing procedures that have the potential to increase the effectiveness and reliability of quantum dot-based memory systems, should be the primary subjects of study in the future.

Data availability

No primary research results, software or code have been included and no new data were generated or analyzed as part of this review.

Conflicts of interest

There are no conflicts to declare.

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