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Integration of the evaporable spin-crossover complex [Fe(HB(1,2,4-triazol-1-yl)$_3$)$_2$] into organic field-effect transistors: towards multifunctional OFET devices†

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Integrating stimuli-responsive molecular switches into organic electronic devices opens interesting perspectives to achieve unprecedented functionalities. However, significant challenges arise in maintaining device functionalities and ensuring synergy with the molecular properties. Here, we described three different ways of incorporating thin films of the molecular spin crossover (SCO) complex [Fe(HB(1,2,4-triazol-1-yl)$_3$)$_2$] into an organic field-effect transistor (OFET) device. The fabrication of high-quality films was enabled by the use of vacuum thermal evaporation, which permitted the deposition of the SCO compound either on the surface of the organic semiconductor or at the semiconductor/dielectric interface. In device configurations where the SCO layer was not in contact with the conduction channel, changes in the drain-source current were observed near the spin crossover temperature, suggesting a potential synergistic effect. These results provide valuable guidance for the design and integration of bistable-material-based functional devices.

Introduction

In an era where information technologies are rapidly advancing, microelectronics have greatly enhanced daily life. Field-effect transistors (FETs) are fundamental yet important components in various electronic devices, such as computers, mobile phones, televisions and cameras. Traditional FETs are built on the basis of inorganic semiconductors, most commonly silicon. However, several alternative material platforms have also been developed. In particular, the fast development of novel organic semiconductors (OSCs) has opened the era of organic electronics, including organic light-emitting diodes (OLEDs), organic photovoltaics (OPV) and organic field-effect transistors (OFETs), among others. The main advantages of OFETs are as follows:[1] (1) a wide range of materials is available through synthetic chemistry, allowing the synthesis of various compounds tailored to meet end user requirements for different performance characteristics. (2) Various thin-film deposition technologies and device architectures can be used, including both conventional (*e.g.* vacuum evaporation) and non-conventional (*e.g.* printing, spraying) methods. (3) The materials are lightweight and can be used in flexible devices, such as displays (*e.g.* electronic paper) and integrated circuits (*e.g.* microcontrollers). (4) The size of the device can be reduced to the nanoscale, potentially reaching the single-molecule level.[2] (5) Perhaps most importantly, OFETs offer more versatile application possibilities than traditional FETs. (6) Finally, it is widely acknowledged that even minor disturbances in the conduction channel can significantly alter device performance.[3] These multifunctional devices not only leverage the exceptional optoelectronic and sensing capabilities of organic materials but also utilize the three-terminal design for effective amplification of external signals. For example, they have been used in physicochemical and biological sensors (including pH, temperature, pressure, glucose, DNA and enzyme sensing) as well as in flexible flat-panel displays.[4,5] As such, developing new functions and incorporating various functional materials into OFETs is an important area of research.[6]

Among these materials, the integration of photochromic molecular switches (*e.g.* azobenzene, spiropyran) into organic electronic devices, particularly OFETs, is already in an advanced stage. Various photo-isomerizable molecules (*e.g.* diarylethenes,

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spiropyrans, azobenzene) have been integrated into organic transistors with the aim of using light irradiation to either tune transistor properties or achieve novel functionalities (*e.g.* non-volatile memory or light-emitting OFETs).[7–10] Switching between the two isomers of such photochromic molecules can modify the OFET performance owing to their switchable properties: change in dipole moment, steric conformation, frontier orbital energies and so forth. Importantly, to take maximum advantage of these properties, it is vital to integrate molecules at various parts of the OFET, including the OSC surface, gate dielectrics, OSC/electrode or OSC/dielectric interfaces, and even in the OSC layer, either as a blend or as the channel layer itself.[7] Consequently, photochromic molecules allowed for the modulation of transport, trapping, scattering, injection and accumulation of charge carriers within the device.

This study on functional OFETs with photochromic molecules can be extended to other switchable molecules. Among the most attractive molecular switches, we are interested in spin crossover (SCO) complexes of transition metal ions, which exhibit bistability between the low spin (LS) and high spin (HS) electronic configurations of the central metal ion.[11–13] Various external stimuli can be used to change the spin states (temperature, pressure, light irradiation, *etc.*), but the most common and convenient method is to use temperature. As a consequence of changing the spin states, the physical properties (dielectric permittivity, HOMO–LUMO energy levels, molecular volume, *etc.*) also change, leading to increasing interest in achieving multifunctional devices using SCO materials. From a technological viewpoint, SCO materials have been proposed for numerous applications, such as displays, memory devices, pressure and temperature sensors, gas sensors, nanothermometers, optoelectronic devices and mechanical actuators.[14,15] Recently, SCO-based transistors have also gained increasing attention,[16–23] either as a means to detect the spin state switching event[16] or to achieve novel transistor functionalities.[17] It is important to note that at present, owing to the low conductivity of SCO compounds,[24,25] they cannot be directly used as conducting channels in transistors. However, the performance of OFETs is strongly related to various physical phenomena occurring at the interfaces (metal/semiconductor and dielectric/semiconductor), which provide numerous possibilities for the effective integration of SCO molecules. Indeed, dielectric and mechanical property changes associated with the SCO phenomenon have already been considered in the context of three-terminal devices based on either graphene[16,19,20,22,26–28] or ferroelectric materials.[17,18] In another approach, our team reported the integration of a PVP:SCO/P3HT bilayer heterostructure (PVP = polyvinylpyrrolidone, P3HT = poly(3-hexylthiophene)) into a solution-processed OFET device.[23] It was observed that the drain-source current across the P3HT conduction channel can be modulated by 50–70% through spin state switching. Capacitance measurements and finite element analysis enabled the identification of the mechanical stress induced by the spin transition as the source of the current change. This represents the first instance of current modulation by SCO materials in an OFET configuration achieved by strain coupling. However, it is important to mention that the solution process used for the fabrication of this SCO-OFET device considerably restricts the degree of freedom in device engineering. In particular, the roughness of spin-coated SCO films does not enable their integration between the gate and the conducting channel.

Motivated by the idea of enlarging the scope of the integration of SCO molecules into OFET devices, in this study, we investigate an SCO-OFET (Fig. 1a), where both the organic semiconducting material[29] and the SCO complex[30] are deposited by vacuum evaporation. Note that only few SCO complexes are evaporable[31] and none of them have been integrated into OFET devices to the best of our knowledge. Importantly, the vacuum thermal evaporation technique allows us to (1) deposit a smooth, dense and homogeneous SCO thin film either before or after the deposition of the OSC film, (2) easily pattern the deposited layers using an evaporation mask, and (3) precisely control their thickness.

Experimental

Heavily doped n-type ($\rho \sim 10^{-3}$ Ω m) silicon substrates were used with a 225 nm thick SiO_2 top layer, which serves as gate dielectric. The main steps of cleaning are as follows. First, we place the substrates (either with or without pre-patterned source and drain electrodes, *vide infra*) in a Teflon rack and sonicate them with acetone (VLSI, 99.5%) and ethanol (VLSI, 99.9%) for 10 min, respectively, followed by a 5 min H_2O_2 : H_2SO_4 (1 : 1 by volume) treatment, finally rinsed them in deionized water and dried them with nitrogen. The preparation

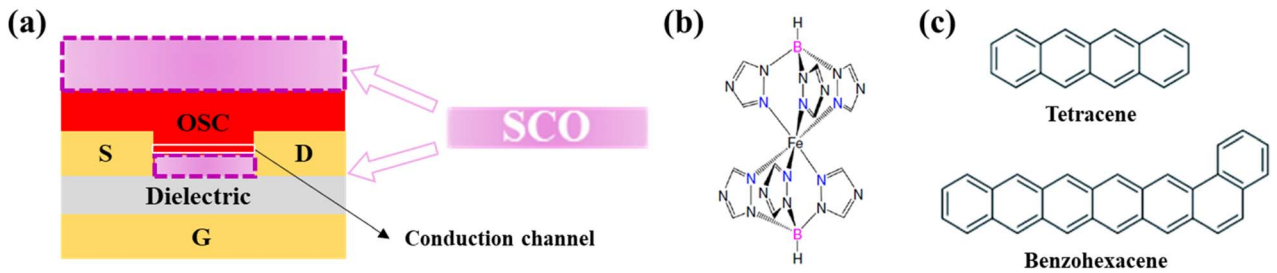

Fig. 1 (a) Schematic of different SCO-OFET configurations using a BG/BC OFET as an example. Molecular structure of (b) the SCO compound [Fe(HB(1,2,4-triazol-1-yl)$_3$)$_2$] (note that the formal charges of the iron and boron atoms are +2 and −1, respectively) and (c) the OSC compounds (tetracene and benzohexacene) used in this study.

of source and drain electrodes includes either conventional photolithography or the evaporation mask method. In the former case, we used a 5 μm negative NLOF 2035 resist purchased from MicroChemicals, whereas in the latter case, a high-resolution nickel mask was used. In both cases, gold (50 nm) was deposited through the mask openings by thermal evaporation. To ensure the good adhesion of gold, a thin layer of Cr (10 nm) was intercalated between the SiO_2 substrate and the electrodes. Both approaches allowed us to obtain devices with channel lengths (L) of 10, 30, 50, 70 and 110 μm and channel widths (W) of 0.5, 1.0 and 1.5 mm.

The SCO compound $[Fe(HB(tz)_3)_2]$, with tz = 1,2,4-triazol-1-yl (see Fig. 1b), was synthesized as described in ref. 32. The molecular structures of the organic semiconductors tetracene and benzohexacene are shown in Fig. 1c. Their synthesis and characterization in OFETs (mobility, *etc.*) were reported in a previous work.[29] The OSC layer (50 nm, except otherwise mentioned) and SCO film (50 nm, except otherwise mentioned) were both deposited by vacuum thermal evaporation in a Plassys system at a base vacuum of *ca.* 2×10^{-7} torr, as described in ref. 29 and 30, respectively. After depositing the SCO film, a water vapor annealing treatment was carried out to increase its crystallinity.[30] Finally, the device was encapsulated by a glass slide using epoxy glue inside a glove box (O_2/H_2O < 3 ppm), flanked to the thermal evaporator system.

For electrical measurements, three gold-coated tungsten tips were placed in contact with the extension of drain/source/gate electrodes with the chip placed on a heating–cooling stage (Linkam Scientific, HFS600EV-PB4). The measurements were conducted either in an ambient environment or under a primary vacuum (10^{-2} mbar). We used two measurement setups: either an Agilent 4142B source-meter unit (SMU) associated with a probe station (Karl Suss PA200 or Cascade Summit 12000) or a combination of two SMUs (Keithley 6430 and 2420).

Results and discussion

The transistors studied here have a bottom gate (BG) configuration with either bottom contact (BC) or top contact (TC) source-drain electrodes. Two possible SCO-OFET device configurations are shown schematically in Fig. 1a based on the example of a BG/BC OFET architecture. As shown in this figure, the conduction channel is at the gate dielectric/OSC interface and has a typical thickness of a few nm. By modulating the gate voltage bias, the charges generated within the conduction channel are impacted. In this work, the challenge is to incorporate the SCO layer into the device architecture at the dielectric/OSC interface to enable additional modulation of charge transport in the OFET channel as a function of the spin state of the SCO layer. This could occur (1) owing to the alteration of dielectric permittivity between the HS and LS states and/or (2) owing to the change in interface interactions (trap sites) upon the SCO phenomenon. Alternatively, the SCO layer can be integrated at a distance from the conduction channel (on top of the OSC layer), where long-range interactions *via* mechanical stress[21] and/or electrostatic effects[19] can occur, modifying the charge transport in the conduction channel. Among the few known evaporable SCO complexes,[31] we used the compound $[Fe(HB(tz)_3)_2]$ (see Fig. 1b), which displays a highly reproducible SCO above room temperature.[33] To gain initial insight into the potential of SCO-based evaporable OFET devices, tetracene (see Fig. 1c) was selected as the OSC material. This choice was influenced by the ease with which it can be integrated with high-mobility transistors, its relatively high charge mobility in the transistor channel, and its demonstrated capability for strain sensing.[34] Three different OFET devices were designed and fabricated in either BG/BC or BG/TC configurations. The fabrication process differs from one configuration to another.

The so-called "Device A" is a BG/BC OFET, whose fabrication is shown in Fig. 2a. On top of the cleaned Si/SiO_2 substrate with pre-patterned source and drain electrodes, the $[Fe(HB(tz)_3)_2]$ film was first deposited (with variable thicknesses between 2 and 30 nm), followed by the deposition of a tetracene layer (with variable thicknesses between 20 and 100 nm). In this configuration, the SCO layer acts as a gate dielectric, together with the SiO_2 layer. To verify its insulating nature as well as the capacitance switching at the SCO phenomenon, impedance spectroscopy measurements were conducted on an ITO/

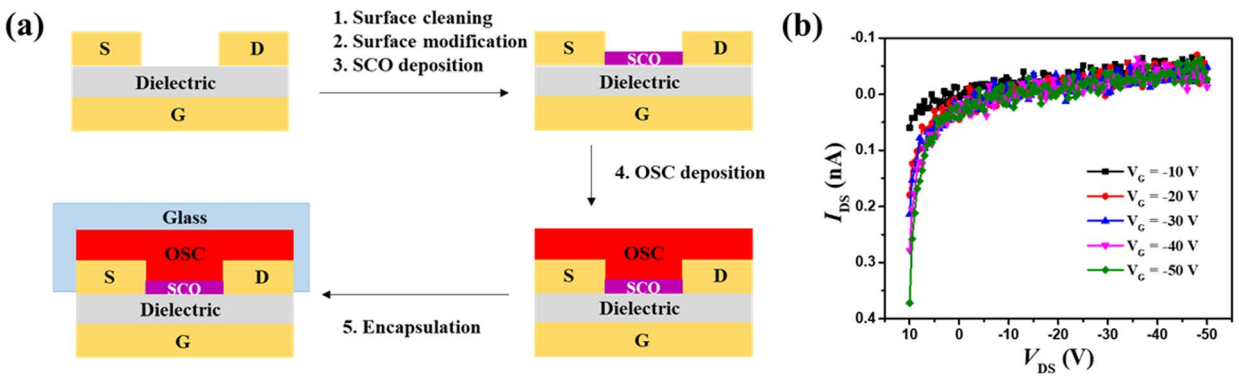

Fig. 2 (a) Process scheme of the BG/BC OFET with the SCO layer between the OSC and the gate dielectric (device A). (b) Representative output characteristics (V_G = −10, −20, −30, −40 and −50 V) of device A (see the transfer characteristic of the same device in Fig. S2a†). Channel width W = 50 μm, channel length L = 1500 μm, OSC thickness = 50 nm, and SCO thickness = 30 nm.

$[Fe(HB(tz)_3)_2]$/Al junction as a function of temperature. As shown in Fig. S1 in the ESI,† the conductivity of the SCO film appears extremely low (see also ref. 35). Equally important for our work is the fact that the capacitance of the junction shows a drop at the spin transition temperature. The change is relatively small in contrast to some other SCO compounds[24,25] but very clear and reversible. This capacitance change provides the scope for the modulation of the transistor characteristics *via* the SCO phenomenon. Nevertheless, in this configuration, one might also expect that the SCO phenomenon could modify the OSC/dielectric interfacial properties (*e.g.* charge trapping). Fig. 2b depicts the representative output characteristics of a device with an SCO thickness of 30 nm. The source-drain current (I_{DS}) is, however, extremely low ($<10^{-10}$ A) and displays no gating effect, indicating that the channel is not conducting. This failure of device A should be either linked to (1) the presence of an SCO 'interlayer' between the source and drain electrodes and the tetracene thin film, and/or (2) the poor quality of the SCO/OSC interface. As shown in Fig. S2b in the ESI,† in this fabrication protocol, the SCO layer inevitably covers the 'wall' of the source/drain electrodes owing to an angle between the effusion cell (used for the evaporation of the SCO material) and the substrate. Hence, during the thermal evaporation, SCO molecules are deposited in every corner on the 'wall' of the gold electrodes. Unfortunately, even the thinnest SCO layer (2 nm) appears to be an efficient injection barrier that impedes the current flowing in the transistor channel.

In the next step, to avoid this charge injection problem, we designed another device where we deposited drain/source electrodes on top of the OSC layer in the last step of fabrication. The procedure for fabricating this BG/TC SCO-OFET (device B) is shown in Fig. 3a. It is important to note that for device B, we used benzohexacene as an OSC instead of tetracene. The reason for this change is that we did not succeed in depositing top contact electrodes on tetracene owing to the greater roughness of the tetracene films.[29] The output and transfer characteristics of device B are shown in Fig. 3. As we can observe in Fig. 3b, the output characteristic of this device shows a characteristic saturation of I_{DS} as the drain-source voltage (V_{DS}) increases negatively at a fixed gate voltage (V_G) typical for a p-type OFET device. In addition, one can observe a clear gate voltage modulation of the drain-source current. However, we also note that the current intensity in device B is reduced by *ca.* 2 orders of magnitude with respect to the 'blank device' without the SCO film (see Fig. S3 in the ESI†). This can be most likely attributed to the reduced quality of the SCO/OSC interface in comparison with the SiO_2/OSC interface. The reduced quality can be linked either to the relatively rough surface of the $[Fe(HB(tz)_3)_2]$ film[29] (in comparison with SiO_2) and/or to the fact that the SCO thin film may unfavorably influence the growth of the benzohexacene film (in terms of crystallinity, morphology, *etc.*). One can also note a hysteresis[36] in the transfer characteristics (Fig. 3c), probably denoting the presence of charge traps.

In the next step, temperature-dependent measurements were carried out both on device B and on a 'blank device' (*i.e.* the same device, but without the SCO film). The temperature dependence of the drain-source current extracted from the transfer characteristics is shown in Fig. 4 for both devices. All temperature-dependent data exhibit thermal activation. For the 'blank device', this dependence is nearly linear in the investigated temperature range (30–70 °C) and for all combinations of V_{DS}–V_G. Note that we limited the device characterization to this range because above 70 °C, the reproducibility of the measurements seriously degraded. See the ESI† for further discussion about the thermal stability and its impact on the characterization of the devices. Note also that measurements were conducted with relatively large temperature steps (5 °C) to

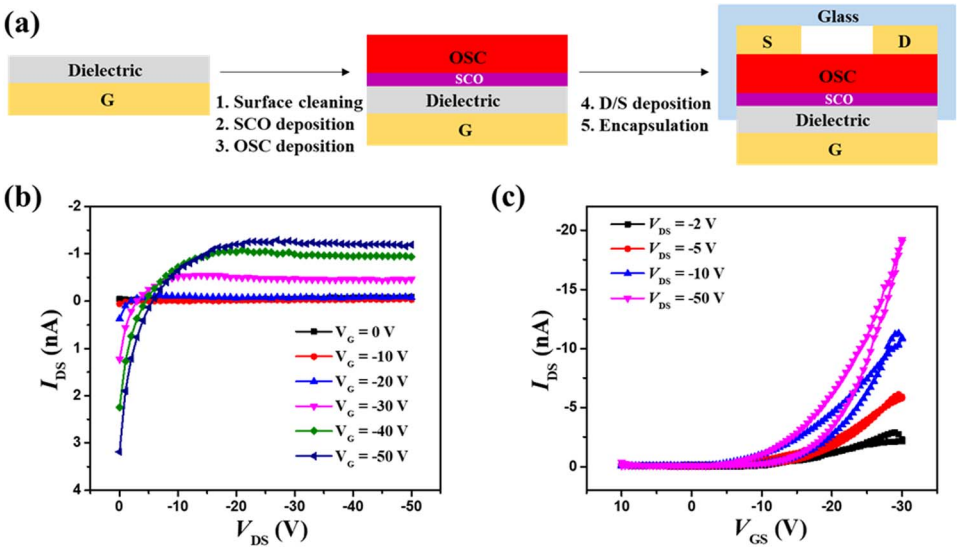

Fig. 3 (a) Process scheme of the BG/TC OFET with the SCO layer positioned between the OSC and the gate dielectric (device B). (b) Output characteristics (V_G = 0, −10, −20, −30, −40 and −50 V) and (c) transfer characteristics (V_{DS} = −2, −5, −10 and −50 V) of device B measured at 45 °C. Channel width W = 70 μm, channel length L = 1000 μm, OSC thickness = 50 nm, and SCO thickness = 50 nm.

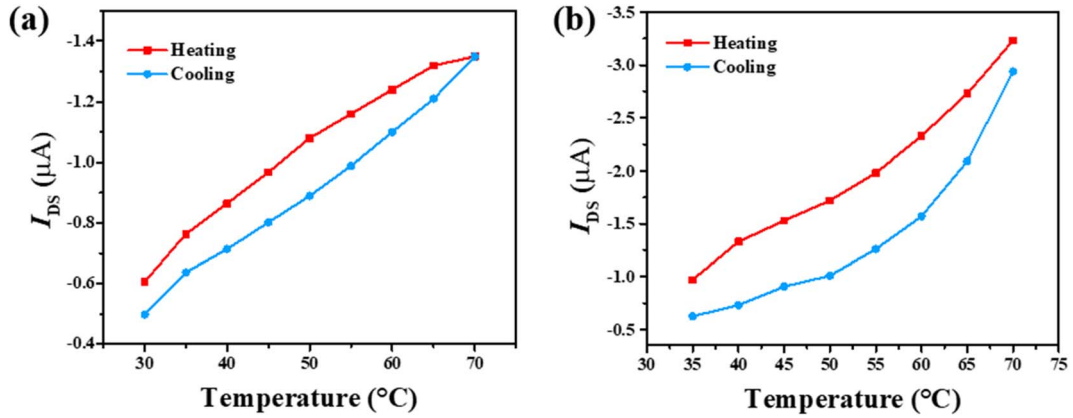

Fig. 4 Temperature dependence of the drain-source current for a 'blank device' (a) and for device B (b) extracted from transfer curves at $V_G = -30$ V and $V_{DS} = -10$ V. Channel width $W = 50$ μm, channel length $L = 1000$ μm, OSC thickness = 50 nm, and SCO thickness = 50 nm.

avoid long exposure of the device to high temperatures under electrical bias. Remarkably, for the SCO-OFET device, the I_{DS} *vs.* T curves deviate from a linear behaviour, and an apparent change in slope occurs around 60 °C, close to the SCO temperature of the $[Fe(HB(tz)_3)_2]$ film.[30] It would thus be tempting to correlate the shape of the I–T curves with the thermal SCO event, even if we cannot discard other reasons. At this point, it is important to underline that these differences are real and not related to device degradation. This robustness of the devices (and of our measurement protocol) is clearly illustrated in Fig. S4 in the ESI,† which shows the output characteristics of device B recorded near ambient temperature (35 °C) before the thermal cycles and after the first and second heating–cooling cycles. One can observe that the first cycle leads to a small increase in the output current, which might be related to thermally activated charge detrapping in the transistor channel. However, the output characteristics recorded after the first and second cycles are closely comparable.

In a different approach, we fabricated a second type of BG/BC device, but this time the SCO layer was deposited on top of the OSC layer (Fig. 5a). In this configuration, which we call device C, a 75 nm thick tetracene film was first deposited on the pre-patterned substrate, which was followed by the deposition of a 150 nm thick $[Fe(HB(tz)_3)_2]$ film in the last step of the device

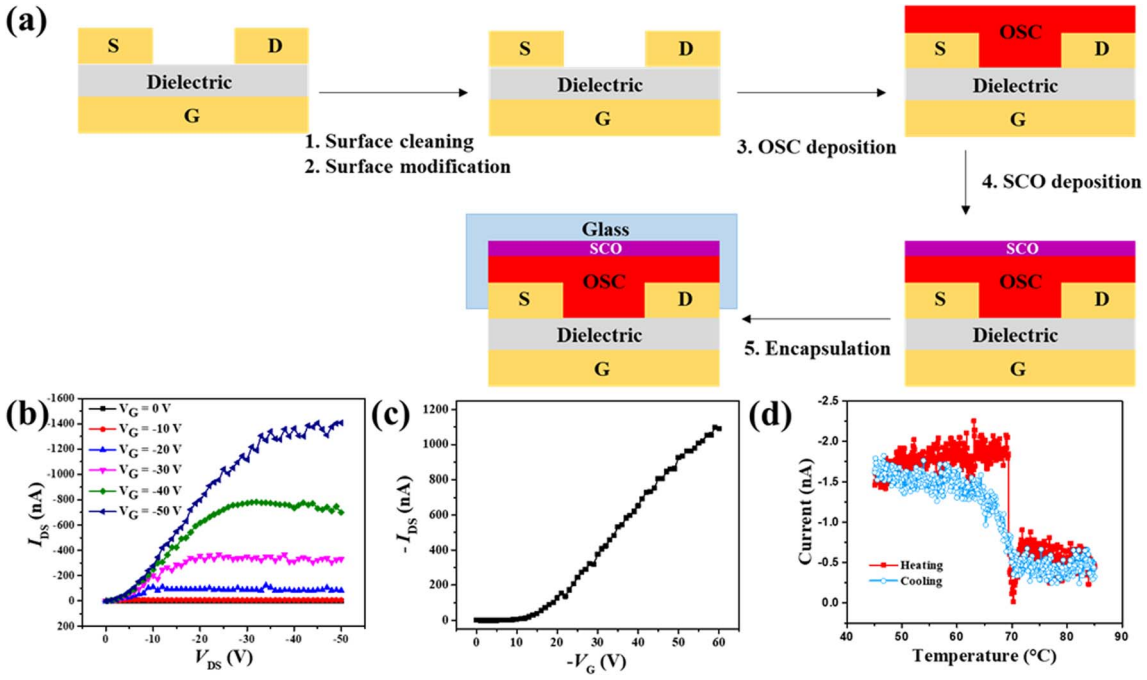

Fig. 5 (a) Process scheme of the BG/BC OFETs with the SCO layer on top of the OSC film (device C). Representative (b) output characteristics ($V_G = 0$, −10, −20, −30, −40 and −50 V) and (c) transfer ($V_{DS} = -30$ V) characteristics of device C. Channel width $W = 50$ μm, channel length $L = 1000$ μm, OSC thickness = 75 nm, and SCO thickness = 150 nm. (d) Temperature dependence of I_{DS} for device C upon heating and cooling ($V_G = -10$ V, $V_{DS} = -30$ V, $dT/dt = 5$ °C min^{-1}).

fabrication. It may be worth noting that this architecture is similar to our previously reported solution-processed SCO-OFET device.[23] Fig. 5b and c depict the representative output and transfer characteristics of device C, respectively. The output characteristics are significantly improved in comparison with devices A and B, with current intensities on the order of μA and with a significant gating effect, indicating that the transistor is working properly. As shown in Fig. 4b, the I_{DS} has increasingly negative values when changing the gate voltage from 0 to −50 V, in line with the p-type characteristics. Both the linear and saturated regimes are clearly depicted in this figure. From Fig. 5c, we can infer a threshold voltage of *ca.* −12 V and an ON/OFF ratio of *ca.* 3 orders of magnitude for this transistor.

In the next step, we examined the temperature-dependent behaviour of device C to assess the effect of the SCO phenomenon on the device properties. A constant gate voltage of −10 V and drain-source voltage of −30 V were applied to this transistor, and the drain-source current was recorded during successive thermal cycles in the range of 45–85 °C (ramping rate of 5 °C min^{-1}). A current–temperature curve, which might be related to the SCO phenomenon, was observed in the first cycle (Fig. 5d). Unfortunately, the thermal stability of the device was rather low, and the initial device characteristic could not be reproduced after the first thermal cycle, leaving considerable doubt on the origin of the thermal behaviour of device C.

Conclusions

In summary, we demonstrated the integration of thermally evaporable $[Fe(HB(tz)_3)_2]$ thin films into different OFET configurations, with the objective of modulating the OFET output current *via* different synergistic effects with the SCO phenomenon. When the SCO layer was inserted between the OSC and dielectric layer in a bottom gate/bottom contact-type device, it failed to operate as a proper transistor. This failure was considered owing to the insulating SCO layer deposited on the drain and source electrodes, which could hinder charge injection. To avoid this, two other OFET configurations were designed. A bottom gate/top contact device was fabricated, which exhibited modest but unambiguous field-effect characteristics. In the third series of devices, the SCO layer was placed at a considerable distance from the conduction channel, which afforded superior transistor output and transfer characteristics. Unfortunately, the devices were rather sensitive to elevated temperatures, particularly under voltage bias, which is attributed to the temperature sensitivity of the organic semiconductors used. Consequently, further research should focus on enhancing the reliability of the device to facilitate robust coupling between the transistor performance and the SCO phenomenon. Two primary research directions are identified for future work. The first is the use of a more resilient, evaporable organic semiconductor that can withstand elevated temperatures. The second is the development of an evaporable SCO material that exhibits spin transition with hysteresis near room temperature, accompanied by a notable alteration in dielectric permittivity and/or molecular volume. These characteristics could enhance device stability and facilitate the development of a non-volatile memory effect.

Data availability

The data supporting this article are included as part of the ESI.†

Author contributions

Conceptualization (I. Sé., A. R., G. M.), sample synthesis (L. S.), device fabrication (Y. Z., I. Sé.), device characterization (Y. Z., I. So.), data analysis (Y. Z., I. Sé., G. M.), original draft (Y. Z., G. M.), review (I. Sé., H. Y., L. S., G. M., A. R., A. B.), project supervision (I. Sé., G. M., A. B.) and funding acquisition (G. M., I. Sé.). The manuscript was read and approved by all the authors.

Conflicts of interest

The authors declare no conflict of interest.

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