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Optically/electrically controlled Ag^+ metallization in solution-processed oxide memtransistors for neuromorphic computing

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In this work, a solution-processable oxide-based memtransistor is designed for neuromorphic computing, incorporating $LiInSnO_4$ as the gate dielectric, SnO_2 as the semiconducting channel, and Ag^+-exchanged LiV_3O_8 as the resistive switching medium. The device demonstrates dual tunability in its channel conductance through both gate voltage and light modulation, enabling precise control over its switching characteristics. Operating at low voltages, the memtransistor achieves an LRS/HRS ratio of up to 10^3, with stable performance across 10^3 switching cycles, over 10^6 pulse cycles, and retention up to 10^5 seconds. The device effectively replicates essential synaptic functions such as paired-pulse facilitation and short- and long-term plasticity, with ultra-low energy consumption: 193 pJ (0.1 fJ μm^{-2}) optically and 540 pJ (0.3 fJ μm^{-2}) electrically. It also shows low non-linearity in potentiation/depression events, 0.49/3.47 (optical) and 0.03/5.67 (electrical), facilitating accurate synaptic weight modulation. Light-driven logic operations and cognitive functions, learning, forgetting, and relearning are successfully demonstrated, along with Pavlovian classical conditioning. Neural network simulations confirm 98% and 95% recognition accuracy for optical and electrical synapses, while autoencoder-based denoising and data reconstruction further validate the applicability of the device in brain-inspired computing.

1. Introduction

The implementation of artificial intelligence (AI) to solve complex tasks and understand cognitive abilities has put considerable pressure on the traditional Von Neumann computer architecture. This is mainly due to its inherent inefficiencies in computing and power usage. The separation of memory and processing units creates fundamental constraints on data rate and energy efficiency, leading to a pressing need for a faster computing architecture that integrates memory and computation in a single unit. In response, researchers have turned their attention to the human brain, which can perform complex simulations, store vast amounts of data, and conduct parallel processing simultaneously. This capability has inspired the development of an artificial brain. However, replicating the human brain is an immense challenge due to its complexity, comprising millions of interconnected neurons and synapses. To address this, scientists advocate for a gradual approach, beginning with the creation of a functional artificial synapse.

Numerous non-volatile memory (NVM) structures for memory and synaptic functions, involving both two- and three-terminal device architectures, have been extensively studied.[1,2] These include flash memory,[3,4] memristors,[5–7] FeFETs,[8,9] FeTFTs,[10,11] and more. Researchers have also explored a variety of novel materials such as organic compounds,[12,13] two-dimensional materials,[14,15] inorganic substances,[16,17] transition metal dichalcogenides (TMDCs),[18,19] quantum dots,[20] and perovskites.[21,22] Recently, oxide materials have gained significant attention due to their ease of use, environmental stability and potential applications in various fields of study such as photoconductors, phototransistors, smart windows and many more.[23–27] Besides, oxide-based NVMs have demonstrated high-performance capabilities for various neuromorphic applications.[28,29] Among these devices, memristors are resistive switching devices that commonly work on the principle of thermal, electrical or ion-migration-induced switching mechanisms. The ion-migration mechanisms are coupled to redox processes in a reversible way, which causes cyclic variations in resistance. Particularly, Ag^+ migration shows very high endurance and fast on/off switching of the

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devices.[30,31] Besides, these devices have very simple structures that offer high-density integration. However, the lack of current modulation limits their application. To address this, the third terminal (gate) of the transistor can be utilized for gaining control over the switching voltage of a memristor, commonly called a memtransistor. This memtransistor[32,33] is a hybrid integration of a memristor and transistor and combines the resistive switching mechanism of the memristor with the gated control of the transistor within a single device architecture. This integration solves the existing issues of area efficiency and current modulation. In a memtransistor, resistive switching behavior is observed as variations in drain voltage are programmed by gate voltage, forming a field-effect transistor structure. While this three-terminal device faces challenges with complex fabrication and reliability of appropriate control, the fabrication technique devised in the work is relatively easier. These memtransistor devices have predominantly been realized using 2D materials like MoS_2 and WS_2, with limited exploration using oxide materials.[34,35]

This research presents an innovative approach towards resistive switching using a solution-processed oxide memtransistor device with LiV_3O_8. The use of high-κ dielectric $LiInSnO_4$ enables the device to operate in a low-voltage regime. $LiInSnO_4$ has been selected as the high-κ dielectric due to its large dielectric constant ($\kappa \approx 23$, where C = 325 nF cm^{-2}),[36] wide bandgap, and chemical stability, which help in suppressing leakage current and enabling efficient charge modulation at reduced voltages. Its solution-processability further offers compatibility with low-cost and low-temperature fabrication compared to conventional vacuum-based methods.

The Equivalent Oxide Thickness (EOT) of this dielectric thin film, which has a dielectric constant of 23 and is defined w.r.t the SiO_2 dielectric, is estimated to be ~11 nm (SI, P-3), which is consistent with the requirements for low-voltage operation.[37,38] The channel of this memtransistor is made of a SnO_2/LiV_3O_8 bilayer thin film. Furthermore, Li^+ of LiV_3O_8 has been replaced by Ag^+ through an ion-exchange process, which is responsible for resistive switching by virtue of reversible conductive nanofilament formation, while SnO_2 works as a semiconducting channel. The fabricated memtransistor displays a low-resistance state/high-resistance state (LRS/HRS) ratio of 10^3 orders, high device endurance over 1000 cycles, pulse endurance of 10^6 cycles and memory retention ability of up to 10^5 seconds while maintaining an ON/OFF state ratio of 10^2 orders. Synaptic plasticity is observed under optical and electrical stimuli with various fundamental measurements, including short-term and long-term plasticity, paired-pulse facilitation, and variations in post-synaptic signals with both optical and electrical inputs. The device successfully mimics learning–relearning behavior, logic gate operations, and the classical conditioning demonstrated in Pavlov's dog experiment, offering insights into the complexities of the human brain. The memtransistor device showcases exceptional power consumption of just 193 pJ or 0.1 fJ μm^{-2} (optical synapse) and 540 pJ or 0.3 fJ μm^{-2} (electrical synapse), which is notably low among reported oxide-based memtransistors in a solution-processed approach. Artificial neural network simulations indicate a high pattern recognition accuracy of 98% and 95% for optical and electrical modulation, respectively. Moreover, the use of the autoencoder algorithm for denoising and data reconstruction highlights the device's capabilities in neural network simulations.

2. Results and discussion

Assessment of the chemical state using X-ray photoemission spectroscopy

The synthesized thin film with the structure p^+-Si/SnO_2 (100 mM)/(Ag/Ag^+)-V_2O_3 has been analyzed using X-ray photoemission spectroscopy to examine the chemical state, particularly in the (Ag/Ag^+)-V_2O_3 layer. Before this analysis, the X-ray diffraction pattern was successfully confirmed through GIXRD, as depicted in Fig. S1. Additionally, UV-visible spectroscopy is conducted to obtain the absorption spectra, which are then used to determine the bandgap of the material. The bandgap values are 5.0 eV for LITO, 3.6 eV for SN, and approximately 2.7 eV for both LV and Ag-LV, with the Ag-LV layer showing a slightly lower bandgap at 2.6 eV. Detailed findings are presented in Fig. S2. The data of XRD and UV-Vis are consistent with the existing reports.[36,39–42]

Fig. 1 presents the XPS spectra for Ag 3d, V 2p and O 1s, respectively. In Fig. 1(a), two prominent peaks are observed at 367.8 and 373.8 eV, corresponding to the binding energies of Ag $3d_{5/2}$ and Ag $3d_{3/2}$, respectively. Additionally, deconvolution of the XPS spectra reveals four distinct peaks. The metallic Ag^0 peak for Ag $3d_{5/2}$ is observed at around 367.9 eV, while a peak at around 374.3 eV is detected for Ag $3d_{3/2}$ after deconvolution. The peaks at approximately 367.5 and 373.7 eV are associated with Ag^+, given that the intensity of the Ag^+ peak is significantly higher than that of Ag^0 for Ag $3d_{5/2}$. These data infer that the majority of the layer consists of Ag^+, with a small amount of Ag^0 likely present on the surface due to atmospheric oxidation.[43,44] Fig. 1(b) shows the XPS peak for V 2p with two peaks of V $2p_{3/2}$ and V $2p_{1/2}$ at binding energies corresponding to 516.3 and 523.3 eV, respectively. By deconvolution of these peaks, the observed valency of vanadium is +3 confirming the formation of (Ag/Ag^+)-V_2O_3.[45]

The deconvolution of the O 1s spectrum yields three peaks with binding energies of around 530.1 eV, 529.3 eV, and 531.7 eV, corresponding to lattice oxygen, Ag_2O, and oxygen vacancies, respectively (Fig. 1(c)). The positions of these peaks are consistent with previously published reports.[46,47] Therefore, the XPS analysis of this sample provides further evidence supporting the successful synthesis of the thin film with (Ag/Ag^+)-V_2O_3. Cross-sectional SEM is performed to determine the thickness of each respective layer, as shown in Fig. S3. The data indicate that the thicknesses of LITO, SnO_2, and (Ag/Ag^+)-V_2O_3 (100 mM) are approximately 63, 30 and 83 nm, respectively. Equating with the concept in thin film analysis, a 12.5 mM precursor concentration of (Ag/Ag^+)-V_2O_3 is expected to produce a thickness of ~10 nm, within which Ag

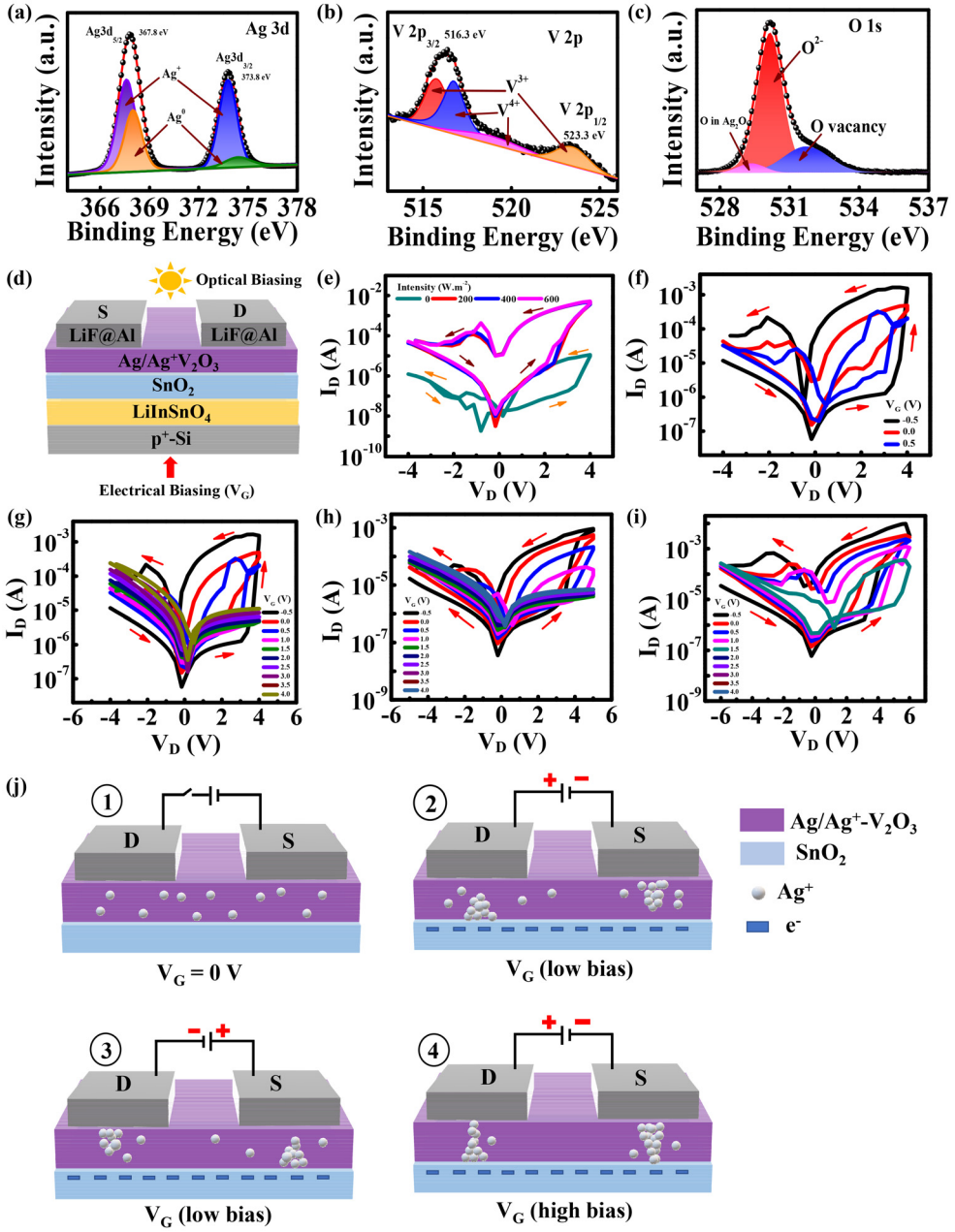

Fig. 1 XPS study of the dielectric layer (Ag/Ag$^+$)-V_2O_3 showing (a) Ag 3d, (b) V 2p and (c) O 1s, respectively; (d) device schematic under optical/electrical bias for the configuration p$^+$-Si/LiInSnO$_4$/SnO$_2$/(Ag/Ag$^+$)/LiF@Al; memtransistor behaviour in device-2 (e) under white light illumination and (f) under electrical gate bias; memtransistor behaviour shown in a drain bias range of (g) −4 V to 4 V; (h) −5 V to 5 V and (i) −6 V to 6 V in a gate bias range of −0.5 V to 4 V, respectively; and (j) schematic diagram illustrating resistive switching in a memtransistor under different bias conditions.

filament formation occurs. The surface topographies of thin films with configurations p$^+$-Si/LiInSnO$_4$/SnO$_2$/LiV$_3$O$_8$ and p$^+$-Si/LiInSnO$_4$/SnO$_2$/(Ag/Ag$^+$)-V_2O_3 are analyzed using atomic force microscopy (Fig. S4) with a root mean square roughness (R_{RMS}) of 1.09 nm for the former, while the p$^+$-Si/LiInSnO$_4$/SnO$_2$/(Ag/Ag$^+$)-V_2O_3 film has an R_{RMS} value of approximately 1.54 nm. The minimal variation in R_{RMS} values suggests that the ion-exchange mechanism does not significantly affect the surface morphology of the thin films.

Memtransistor characterization

Ambient atmosphere electrical characterization studies have been performed to analyze the memtransistor behavior of these devices. Schematic presentation of the reference device and memtransistor is shown in Fig. S5, referred to as device-1 and device-2. The transistor characteristics, including output (I_D *vs.* V_D) and transfer (I_D *vs.* V_G), are evaluated and illustrated in Fig. S6. Upon observation, device-2 exhibits better TFT be-

havior than device-1. Additionally, the DC current measurement of device configuration p^+-Si/LiInSnO$_4$/SnO$_2$/LiV$_3$O$_8$ and p^+-Si/LiInSnO$_4$/SnO$_2$/(Ag/Ag$^+$)-V$_2$O$_3$ are investigated to realize the insulating nature between gate and drain electrodes. In this analysis, device-2 demonstrates lower DC current up to two orders of magnitude (6.8×10^{-7} A cm^{-2} at 0.2 MV cm^{-1}) compared to device-1 (5.1×10^{-5} A cm^{-2} at 0.2 MV cm^{-1}), as observed in Fig. S7(a). Besides, gate leakage currents (I_G *vs.* V_G) of device-1 and device-2 are studied, as shown in Fig. S7(b) and S7(c), respectively. A comparison table is provided in Table S1 to evaluate the key figures of merit for the devices.

The memtransistor behavior is studied in device-1 and device-2 by sweeping V_D in a closed loop. This measurement has been performed, either under white light illumination with different intensities or with different gate voltages ranging from −0.5 V to 4 V, as depicted in the schematic diagram in Fig. 1(d). The *I*–*V* characteristic of device-1 does not show any resistive switching (RS) behavior neither on light illumination nor under gate bias, while a clear systematic variation has been observed in device-2. Fig. 1(e) shows a clearer RS behavior of device-2 even under dark conditions, while this amplitude increases with light intensities and does not change much when light intensities vary from 200 to 600 W m^{-2}. During gate voltage variation of device-2, the drain voltage in the output characteristics is varied across three different ranges for three sets of characterization studies. The characteristics with drain voltage range from −4 V to 4 V, −5 V to 5 V and −6 V to 6 V are shown in Fig. 1(g), (h) and (i), respectively, whereas a simplified version of Fig. 1(g) is portrayed in Fig. 1(f) to show the RS nature. Fig. 1(f) shows that the RS of device-2 is starting from V_G = −0.5 V, which gradually decreases with increasing gate bias (Fig. 1(f)) and ultimately diminishes at V_G = 4 V (Fig. 1(g)). At V_G = −0.5 V, a positive scan of V_D towards higher bias switches the device from a high resistance state (HRS) to a low resistance state (LRS). The device maintains the LRS state when reversing the bias to V_D = 0 V. Meanwhile, an HRS state can be achieved with a negative bias sweep of the drain voltage, and this state is maintained from V_D = −4 V to 0 V. The search for RS behavior in device-1 continues by varying the same drain voltage ranges, like from −4 V to 4 V, −5 V to 5 V and from −6 V to 6 V, which are shown in Fig. S8(a), S8(b) and S8(c), respectively, but no such RS behavior is observed. In contrast, device-2 shows an increase in the LRS to HRS state ratio with an increase in V_D as shown in Fig. 1(h) and (i), respectively. A comparative table for this is presented in Table S2. The device-to-device variation for up to 10 devices is displayed in Fig. S9. This figure also displays the average device-to-device variation over 10 separate batches, with each batch containing 5 devices.

The resistive switching mechanism in the fabricated memtransistor is depicted in Fig. 1(j). Diagram 1 shows the state when neither gate nor source–drain (S–D) bias is applied, with Ag$^+$ dispersed throughout the (Ag/Ag$^+$)-V$_2$O$_3$ layer. When a low gate and S–D bias are introduced, the Ag$^+$ begin to form a nanofilament (Diagram 2), creating a temporary conducting path through the semiconducting SnO$_2$. Reversing the S–D bias causes the nanofilament to rupture, and a new conducting path forms in the reverse direction shown in Diagram 3, enabling SET and RESET switching of the device. As the gate bias increases, the temporary nanofilament transforms into a permanent one, resulting in a continuous conducting path within the (Ag/Ag$^+$)-V$_2$O$_3$ layer regardless of S–D polarity, thus eliminating resistive switching in the device, as illustrated in Diagram 4. A similar phenomenon happens when white or UV light is illuminated on top of the device that enhances free carrier concentration in the channel by several orders of magnitude and acts equivalently to the gate bias. This process of nanofilament formation and rupture governs the switching behavior of the memtransistor. To understand the carriers and photogenerated charge transport behaviour in the heterojunction structure, Mott–Schottky analyses of ITO/SnO$_2$/(Ag/Ag$^+$)-V$_2$O$_3$ and ITO/SnO$_2$/LiV$_3$O$_8$ thin films are performed and described in section 1 Fig. S10. A comparative chart of Mott Schottky potentials under dark and light conditions is given in Table S3.

To gain a broader understanding of resistive switching, a simple experiment has been designed. By fixing the gate bias at −0.5 V and varying the drain bias at 2 V, 3.7 V, 3.9 V, 4 V, and 4.1 V, the time response of the device is analyzed. The data clearly show that at a lower drain bias of 2 V, the current saturates around 10^{-7} A, corresponding to the high-resistance state (HRS). As the drain bias approaches the switching voltage (4 V), the current gradually increases over time, indicating the formation of a filamentary pathway (Fig. S11). These data serve as indirect evidence of the switching behavior in our device through filament formation.

To further investigate the resistive switching behavior, the memristive properties of device-2 are studied by fixing the gate voltage at −0.5 V (where the highest memtransistor behavior is observed) and performing an I_D *vs.* V_D measurement. The studies reveal appropriate bipolar switching behavior with device stability over 1000 cycles of continuous measurement. The endurance plot also shows the device's consistency in maintaining the LRS to HRS ratio for 1000 cycles. In addition, pulse endurance measurement has been performed by applying electrical pulses (5 V–3 V; 20 ms) with the device demonstrating 10^6 cycles of endurance with no device degradation. All these observations are illustrated in Fig. S12. The memory capabilities of device-1 and device-2 are tested by allowing the devices to switch between HRS and LRS, and recording the current *vs.* time measurements in each state, as shown in Fig. 2. Device-1 does not exhibit any recognizable memory retention, which is expected since it does not display any switching behavior. On the other hand, device-2 shows memory retention lasting up to 10^5 seconds, and projections indicate that it maintains a significant On state to Off state (LRS to HRS) ratio of 10^2 orders for 30 days. Thus, device-2 demonstrates better retention ability compared to device-1.

The Resistive Random-Access Memory (ReRAM) property of the device is also shown in Fig. S13. To investigate this, a series of voltage pulses, specifically 2.5 V, −0.5 V, −2.5 V, and

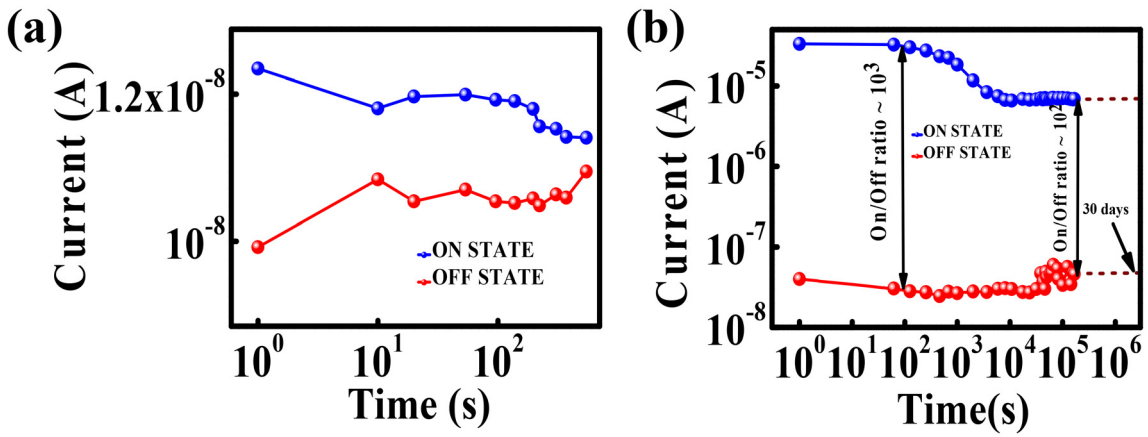

Fig. 2 Retention time measurement for the device configurations: (a) p^+-Si/LiInSnO$_4$/SnO$_2$/LiV$_3$O$_8$ and (b) p^+-Si/LiInSnO$_4$/SnO$_2$/(Ag/Ag$^+$)-V$_2$O$_3$, respectively.

−0.5 V, have been systematically applied to the top electrode in an iterative manner. The corresponding currents have been measured at each step. Following the application of a 2.5 V pulse, the device transitions into the high-resistance state (HRS), and subsequent current measurements are taken at −0.5 V, called "read after erase". Similarly, upon the application of a −2.5 V pulse, the device shifts to the low-resistance state (LRS), and subsequent current measurements are obtained again at −0.5 V. This investigation has been performed for ∼10 consecutive pulses, indicating its distinct ReRAM behavior.

Emulation of synaptic plasticity in a memtransistor

Optical synapse. Fig. 3(a) depicts a schematic representation of a biological synapse, where the flow of neurotransmitters from the presynaptic neuron to the postsynaptic neuron is influenced by a modulating neuron. This biological synapse's equivalent circuit is replicated by the memtransistor device (device-2) also shown in Fig. 3(a). In this setup, the gate electrode and optical stimulus act as the modulating neuron, while the source–drain terminals correspond to the pre-and post-synaptic neuron terminals. When an optical stimulus is applied, the postsynaptic response, known as the excitatory post-synaptic current (EPSC), spikes and then gradually decays after the light is removed. This phenomenon is primarily due to the gradual slow release of the trapped charge carriers resulting from the electron–hole pair generation under light exposure. A detailed study is provided in section 2 Fig. S14.

Fig. 3(b) illustrates the EPSC *versus* time graph when a single pulse of white light, with an intensity of 700 W m^{-2}, is applied to the device for 3 seconds while maintaining V_{DS} = 10 mV. The data reveal that upon the application of light, the EPSC reaches a peak value of 6.5 nA. Once the light is removed, the current decays but remains sustained for an extended period (up to 45 seconds), highlighting the long-term plasticity of the device. From the graph, the minimum energy consumption per synaptic event is calculated using the following formula:[48]

$$E = I_{peak} \times T_d \times V_{DS} \quad (1)$$

where I_{peak} is the maximum EPSC value reached when an optical pulse is applied, T_d is the duration for which the light is illuminated, and V_{DS} is the source–drain voltage. With the values I_{peak} = 6.5 nA, T_d = 3 s, and V_{DS} = 10 mV, the calculated minimum energy consumption is 193 pJ, which when divided by an effective electrode area of 1.7 mm^2, gives an energy consumption per area of around 0.1 fJ μm^{-2}. This value is considerably lower than that of other reported oxide memtransistors. A comparison chart for different oxide based memtransistors is shown in Table S3.

Paired-Pulse Facilitation (PPF) is a type of short-term plasticity where two consecutive white light pulses, each with a pulse width of 2 seconds and a pulse interval of 4 seconds, are applied successively to the device. The resulting signal exhibits a higher EPSC value for the second pulse. This phenomenon is analogous to a biological synapse, where the second signal increases neurotransmitter release, resulting in an enhanced action potential that triggers a greater concentration of Ca^{2+}. Fig. 3(c) illustrates the PPF index for two consecutive white light pulses. The PPF index is calculated using the equation:[49]

$$PPF_{index} = \frac{A_2}{A_1} \times 100\% \quad (2)$$

where A_1 and A_2 are the amplitudes of the EPSC generated by the first and second optical signals, respectively. Fig. 3(d) illustrates the PPF index as a function of the pulse interval (ΔT). The interval is varied from 4 seconds to 20 seconds, and the corresponding PPF index is calculated and plotted. The graph demonstrates an exponential behavior, with the maximum PPF value reaching 129% at 4 seconds, which decays to 123% at 20 seconds. This decaying trend is attributed to the combined photoconductive–photovoltaic effect of the device resulting

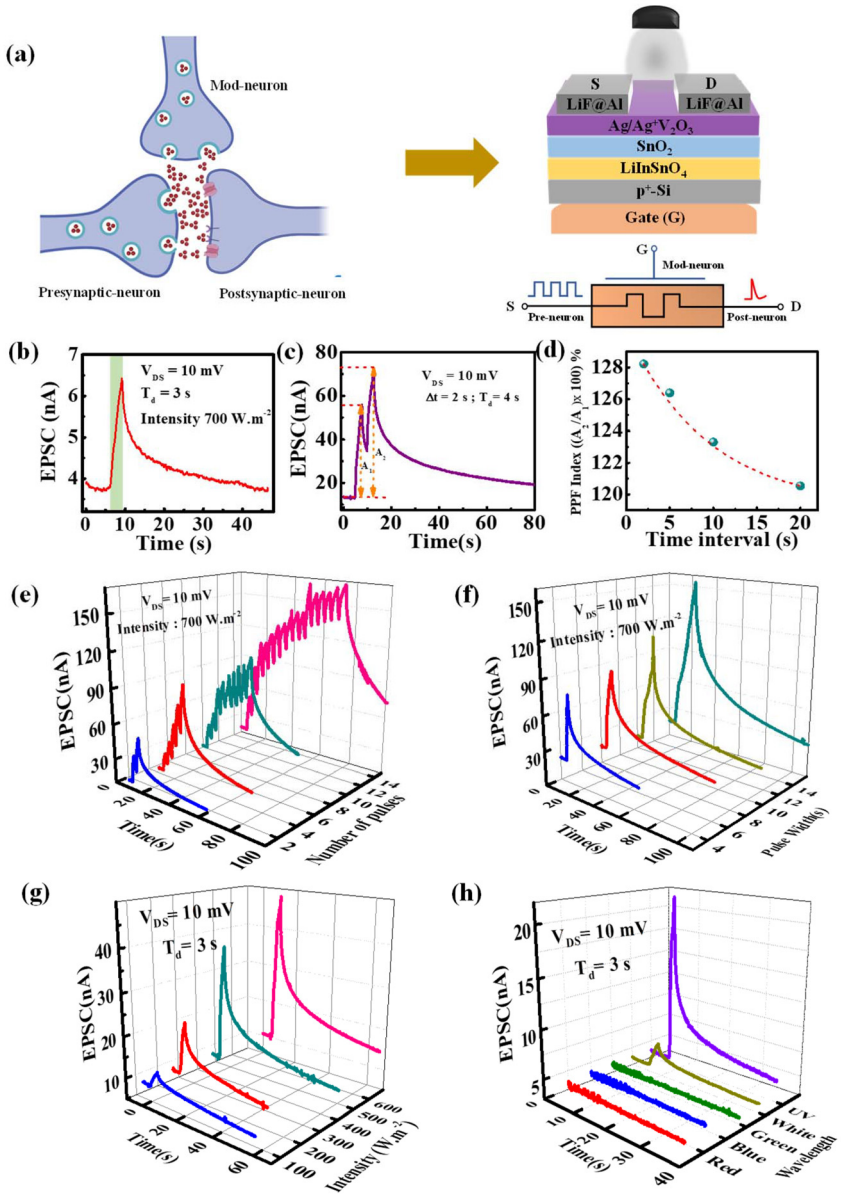

Fig. 3 (a) Biological synapse where the neurotransmitters between pre-synaptic and post-synaptic neurons are modulated by modulating the neuron and its equivalent memtransistor device configuration of p^+-Si/LiInSnO$_4$/SnO$_2$/(Ag/Ag$^+$)-V$_2$O$_5$; (b) EPSC *vs.* time for a single optical pulse; (c) PPF index for two consecutive light pulses; (d) PPF variation with different pulse intervals of two consecutive pulses; EPSC *vs.* time for (e) varying number of optical pulses; (f) varying white light pulse duration; (g) varying white light intensity and (h) different wavelengths of optical pulses.

from optical illumination. The curve is fitted with a double-exponential function described by the following equation:

$$y = y_0 + B_1 \exp\left(-\frac{x}{t_1}\right) + B_2 \exp\left(-\frac{x}{t_2}\right) \quad (3)$$

where B_1 (55%) and B_2 (56%) are the rapid and slow phase facilitation magnitudes, and t_1 (9 ms) and t_2 (10 ms) are the characteristic relaxation times of their respective phases, y_0 is the resting magnitude and x is the pulse interval.

Fig. 3(e) shows the EPSC (excitatory post-synaptic current) *versus* time graph by varying the duration of the optical pulse, while Fig. 3(f) illustrates how the EPSC changes with the number of white light pulses. In both scenarios, there is a noticeable increase in the EPSC value, indicating a shift from short-term plasticity (STP) of the device to long-term plasticity (LTP). This transition from STP to LTP is attributed to an increase in charge carriers, leading to the entrapment of photogenerated electrons at the source (or drain)/SnO$_2$ interface, resulting in a slow recombination process after turning off the light that causes a longer decay time (Fig. S13).

Additionally, the EPSC *vs.* time graph has been tested with white light of different intensities, as shown in Fig. 3(g). Here, a similar behavior is observed, where the EPSC value increases

with the intensity of the light. Fig. 3(h) presents the variation of EPSC with time for different wavelengths of light. Although there is no significant observable spike in EPSC within the visible light range, a sharp change, greater than that of white light, is detected for ultraviolet (UV) light. This indicates that the device is highly sensitive to UV signals. Despite this sensitivity, white light has been chosen as the primary optical signal to minimize energy consumption. This can be attributed to the increased sensitivity of the device, resulting from the wide band-gap SnO_2 layer. To have a clear distinction between the STP to LTP transition as observed in Fig. 3(e)–(h), the decay has been fitted with two phase exponential decay function and the respective decay time constants are obtained. The decay time constants are given in Table S5.

In a synapse, the connection between two neurons can be strengthened or weakened through changes in the action potential, a process known as potentiation and depression. This dynamic adjustment of synaptic strength is fundamental to learning and memory in both biological and artificial neural networks. Fig. 4(a) illustrates the potentiation–depression curve measured over a single cycle. Potentiation is achieved by exposing the system to continuous white light pulses with a 4 s pulse interval, while a voltage pulse with an amplitude of 2 V is applied to the gate terminal to induce the depression event. This process is repeated for 3 cycles, as shown in Fig. 4(b). One of the critical parameters derived from this curve is the non-linearity factor, shown in Fig. 4(c), which measures how the synaptic response deviates from a simple linear relationship during potentiation and depression. The non-linearity factors obtained for potentiation and depression events are 0.49 and 0.03, respectively. This factor is essential for creating a highly functional neural network because it directly influences the network's ability to learn complex patterns and behaviors. A high linear response enables the synapse to mimic the intricate adjustments seen in biological systems, allowing for more sophisticated information processing and memory retention.

In practical terms, the non-linearity factor plays a vital role in determining the efficiency and effectiveness of synaptic plasticity. By quantifying the degree of non-linearity, researchers can optimize synaptic behavior to achieve desired learning dynamics, thereby enhancing the overall performance of neuromorphic systems. The non-linearity factors for potentiation and depression events are calculated using the following equations:[50,51]

For potentiation:

$$G = G_1(1 - e^{-\nu P}) + G_{min} \quad (4)$$

For depression:

$$G = G_{max} - G_1(1 - e^{-\nu(1-P)}) \quad (5)$$

where $G_1 = \frac{G_{max} - G_{min}}{1 - e^{-\nu}}$

G_{min} ($EPSC_{min}$) is the minimum conductance, G_{max} ($EPSC_{max}$) is the maximum conductance, P is the number of pulses and ν is the parameter characterizing the nonlinearity. Understanding and controlling this factor is crucial for advancing neuromorphic engineering and achieving more realistic and capable artificial neural networks.

Several key synaptic functionalities, including "associative learning", "learning-forgetting-relearning" and the "emulation of logic gates" using optical pulses, have been successfully replicated and are detailed in section 3 Fig. S15, section 4 Fig. S16 and section 5 Fig. S17, respectively.

Electrical synapse. Fig. 5(a) presents the variation of EPSC with time upon applying a single electrical pulse with a width of 20 ms and an amplitude of 1 V, applied at the drain electrode. Based on this, the minimum power consumption is calculated to be 540 pJ, corresponding to 0.3 fJ μm^{-2}. The effect of varying pulse width parameters has also been investigated, as shown in Fig. 5(b), and the resulting energy consumption trend is plotted in Fig. 5(c). The data exhibit an almost linear increase in energy consumption per spike with increasing pulse width. Furthermore, the paired-pulse facilitation (PPF) index for a 20 ms pulse and its variation with pulse interval have been measured, shown in Fig. 5(d) and (e), respectively. An increase in pulse amplitude results in a higher EPSC, as

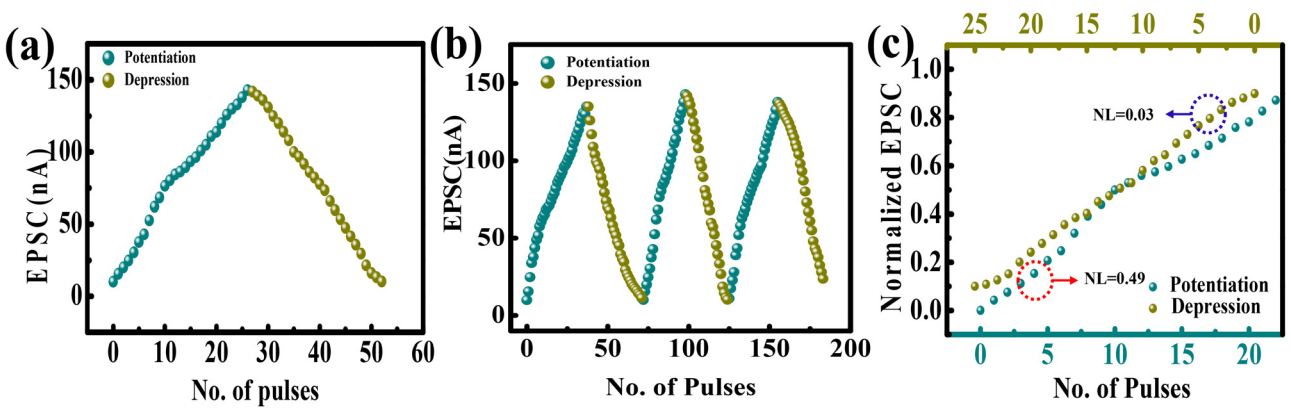

Fig. 4 Potentiation and depression curve for (a) single cycle and (b) three cycles of measurement; and (c) non-linearity factor obtained from the potentiation–depression curve.

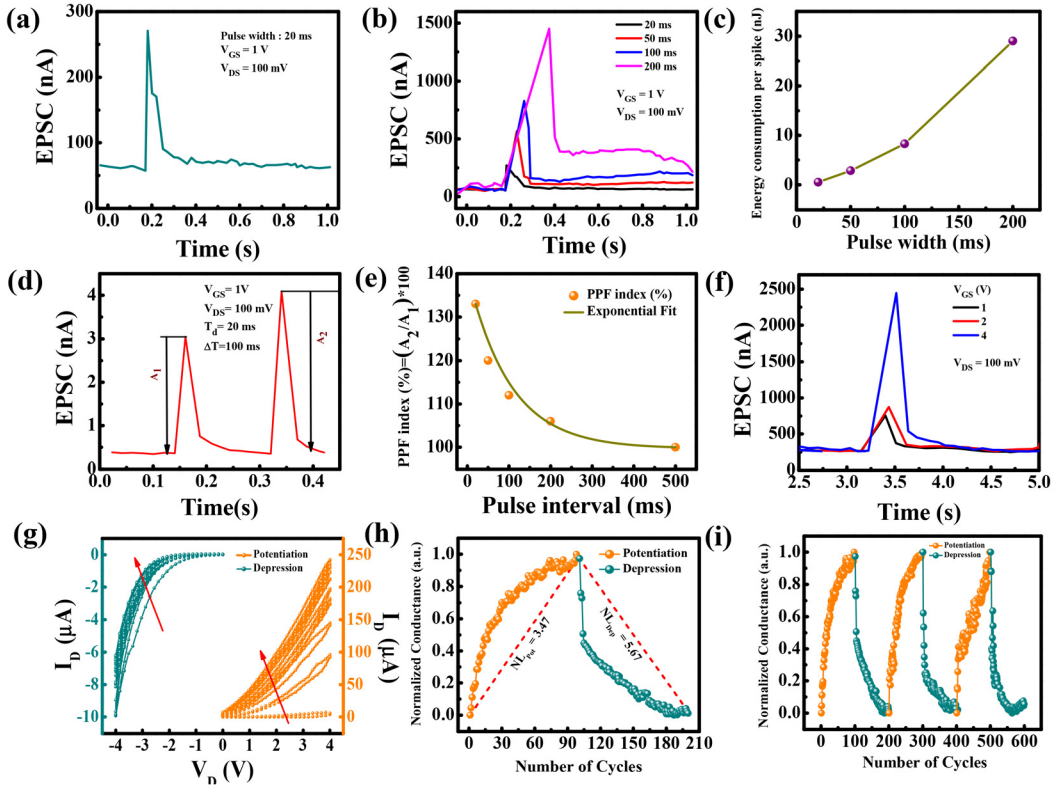

Fig. 5 (a) EPSC *vs.* time curve for a single electrical pulse (pulse width: 20 ms; pulse amplitude: 100 mV); (b) EPSC *vs.* pulse width variation; (c) energy consumption per spike *vs.* pulse width variation; (d) PPF index for two consecutive electrical pulses; (e) PPF variation with pulse interval; (f) EPSC *vs.* pulse amplitude variation; (g) potentiation and depression cycles at a fixed gate bias of −0.5 V for 100 cycles at 10 cycle intervals; and normalized conductance *vs.* the number of pulses for (h) a single cycle with non-linearity factors of 3.47 and 5.67 for the potentiation–depression curve and (i) 3 cycles.

depicted in Fig. 5(f), indicating that higher amplitudes lead to greater energy consumption.

Since the optimal resistive switching behavior is observed at a gate bias of −0.5 V, the output characteristics were recorded under this fixed bias over 100 cycles, using both positive (0 to 4 V) and negative (0 to −4 V) drain biases, as illustrated in Fig. 5(g). The collected data demonstrate clear potentiation and depression behaviors through the corresponding increases and decreases in the channel current. The normalized conductance profile for a single potentiation–depression cycle is provided in Fig. 5(h), also highlighting the nonlinearity factors of 3.47 and 5.67 for potentiation and depression, respectively. The repeatability of this behavior over three cycles is presented in Fig. 5(i).

Pattern reconstruction and denoising using an autoencoder

Fig. 6(a) illustrates the schematic of the autoencoder, with the input, latent, and output layers distinctly highlighted. Fig. 6(b) presents the pattern reconstruction achieved with the autoencoder, where the first layer displays the original pattern and the second layer shows the reconstructed pattern. The results indicate that the neural network effectively reconstructs the data, as demonstrated in the figure. When noise was added to the pattern '7' with factors of 1.0, 0.5, and 0.3, the autoencoder denoised the pattern with recognition accuracies of 82%, 84%, and 90%, respectively, as shown in Fig. 6(c). Thus, leveraging the synaptic weights obtained, the autoencoder has accomplished both data reconstruction and pattern denoising. The details of the autoencoder algorithm are described in section 6 of the SI.

Pattern recognition using a convolutional neural network

Using the data of optoelectronic and electrical synaptic weights, a convolutional neural network is trained for 20 epochs, achieving a recognition accuracy of nearly 98% (for optical synaptic weights) and ~95% for electrical weights, a validation accuracy of 98.5% with a mean loss of 0.005 and 0.02, respectively, as shown in Fig. 7(a–c). This result demonstrates the high effectiveness of the neural network model, optimized using synaptic weights from the potentiation-depression curve. This represents the highest accuracy reported to date for a solution-processable oxide memtransistor device in this category. Fig. 7(d) shows the confusion matrix comparing true *versus* predicted values for MNIST digits 0 to 9 after training for 1, 10, and 20 epochs. The matrix reveals an increasing alignment between true and predicted values with each training iteration. These findings highlight the potential of integrating the fabricated device into complex

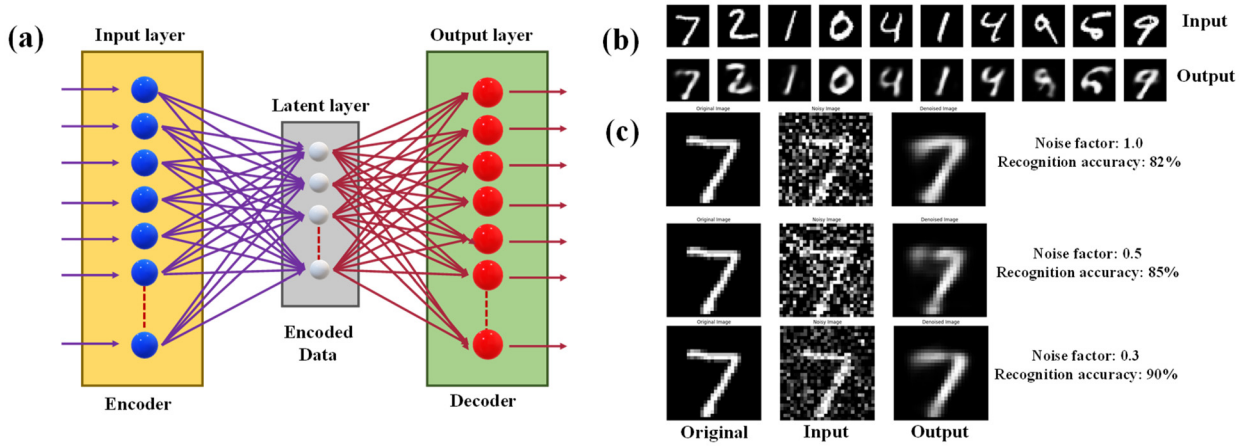

Fig. 6 (a) Schematic diagram of a simple autoencoder circuit, (b) pattern reconstruction where the 1st layer shows the original pattern and the 2nd layer displays the reconstructed pattern, and (c) denoising a pattern with noise factors of 1.0, 0.5 and 0.3, respectively.

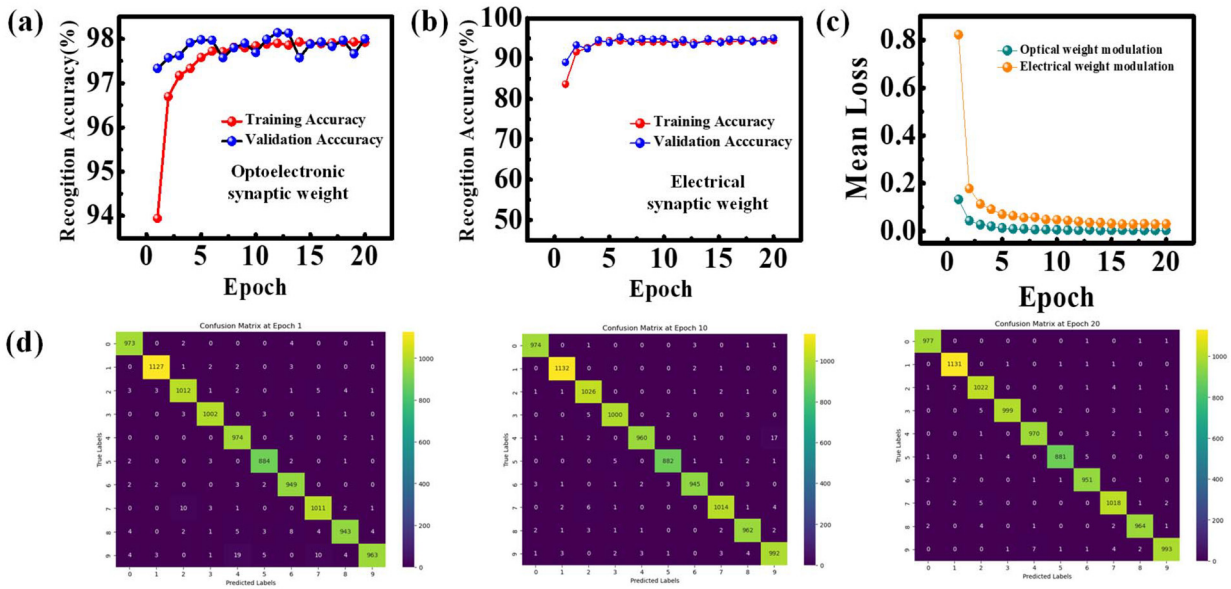

Fig. 7 Recognition accuracy *vs*. epoch using (a) optoelectronic synaptic weights and (b) electrical synaptic weights, (c) mean loss *vs*. epoch and (d) confusion matrix for digit recognition after 1, 10 and 20 epochs, respectively.

systems to emulate highly functional neuromorphic devices. The detailed analysis of the CNN model is described in section 7 of the SI.

3. Conclusion

This work presents a new method for developing a memtransistor by employing Ag ion-exchange and subsequent metallization of the Ag^+ mechanism in a SnO_2/LiV_3O_8 bilayer thin film transistor. In this process, Li^+ of the top LiV_3O_8 layer is substituted with Ag^+ to form a switching layer. This substitution is crucial as it allows Ag^+ to form temporary conductive nanofilaments when selectively biased, resulting in memristor behavior. The fabricated device, with a structure of p^+-Si/$LiInSnO_4/SnO_2/(Ag/Ag^+)$-$V_2O_3$, demonstrates optical and gate bias dependent memtransistor (memT) characteristics with an LRS/HRS ratio of $\sim 10^2$ to 10^3 in a low operating voltage region. Additionally, the device showcases impressive endurance (1000 cycles), pulse endurance (10^6 cycles) with memory retention up to 10^5 s. Moreover, the memT device successfully replicates optical signal-based synaptic plasticity, including both short-term and long-term plasticity, which are fundamental for mimicking neural behaviors. The energy consumption of this device is remarkably low, with a minimum energy usage of nearly 193 pJ or 0.1 fJ μm^{-2} (for optical) and 540 pJ or 0.3 fJ μm^{-2} (for electrical), making it the most energy-efficient among existing oxide memtransistors. Besides, it replicates

PPF and demonstrates EPSC variations with the pulse duration, the number of pulses, and the intensity and wavelength of light. Potentiation and depression events, achieved through the application of optical and electrical pulses, have been realized over three cycles. These events were employed in a pattern recognition study using a convolutional neural network model, achieving a learning accuracy of 98% and 95% under optical/electrical synaptic modulation, along with investigations using an autoencoder model for pattern reconstruction and denoising. Furthermore, the learning–forgetting–relearning model is demonstrated, effectively simulating human-like knowledge acquisition processes. Associative learning is exemplified through Pavlov's dog experiment, where classical conditioning is used to transform an unconditioned response into a conditioned response. Additionally, the memT device is capable of performing basic logic gate operations such as 'OR' and 'AND' using selective intensities of UV and white light. Overall, this work paves the way for a cost-effective and straightforward method of fabricating memtransistors with synaptic capabilities. Altogether, these results not only offer insights into the creation of more efficient memtransistors but also provide a blueprint for future innovations in neuromorphic engineering and cognitive computing technologies.

4. Experimental

Preparation of precursor materials

To function as a dielectric layer, lithium indium tin oxide [LITO] ($LiInSnO_4$) has been synthesized using three different precursors: lithium acetate [$C_2H_3LiO_2$] (TCI, >98.0% purity), anhydrous indium chloride [$InCl_3$] (Alfa Aesar, >99.99% purity), and tin chloride [$SnCl_2$] (Sigma–Aldrich, >99.99% purity). At first, a 200 mM solution of $InCl_3$ is prepared by dissolving it in widely used 2-methoxyethanol (2-MEA) and stirring for 24 hours. It is then stabilized for another 24 hours. The remaining precursor salts are then mixed separately in 2-MEA and stirred for 1 hour. Subsequently, the solutions are combined in a 1 : 1 : 1 molar ratio and stirred for an additional hour at room temperature under ambient conditions to produce a clear, transparent homogeneous solution.

Lithium trivanadate (LiV_3O_8) has been synthesized using solution-processing techniques with two different salts as precursor materials: lithium acetate dihydrate (Alfa Aesar, >99% purity) and ammonium metavanadate (99% purity, obtained from Sigma). For this synthesis, 12.5 mM solutions of lithium acetate and ammonium metavanadate are prepared separately in 2-methoxyethanol, and each solution is stirred for one hour. The two solutions are then mixed in a 1 : 3 molar ratio of lithium acetate to ammonium metavanadate, followed by the addition of 10 μL of HNO_3. The mixture is stirred constantly at 60 °C for one hour to obtain a clear solution. Before spin coating, both LITO and LiV_3O_8 precursor solutions are filtered through a 0.45 μm PVDF filter to improve film quality. Following previous studies, a SnO_2 semiconductor precursor solution at a concentration of 100 mM is prepared using tin(II) chloride salt (99.99% purity, obtained from Sigma Aldrich).

Thin film device fabrication

For the analysis of memtransistor behaviour, two devices have been prepared following the top-contact bottom-gated staggered transistor architecture. For the choice of substrate, highly boron-doped silicon (p^+-Si) of dimension 16 mm × 16 mm and possessing a sheet resistance of 0.01–0.02 Ω $\square^{-1}$ has been used. Initially, the substrates are cleaned following the widely recognized three-solution cleaning method. At first, the substrates are subject to cleaning with an Extran solution (50% Extran & 50% distilled water) followed by ultrasonication for 15 minutes with distilled water (DI), acetone and isopropanol (IPA), each separately. The substrates are then dried, followed by an oxygen plasma treatment (20 W, 10 minutes). The plasma treatment ensures hydrophilicity and pin-hole free precursor thin film formation. The LITO dielectric is then spin-coated on the cleaned substrates at 3000 rpm for 40 seconds followed by a heat treatment at 350 °C for 30 minutes. This process has been repeated twice with the final heat treatment at 550 °C for 1 hour. The semiconducting SnO_2 is then spin coated at 4000 rpm for 40 seconds and annealed at 500 °C for 30 minutes. For the development of the switching layer, LiV_3O_8 is spin coated at 5000 rpm for 50 seconds with a final heat treatment at 500 °C for 1 hour.

For the reference device, the channel is made up of SnO_2 with a LiV_3O_8 bilayer thin film, whereas for the memtransistor, the bilayer film is treated with $AgNO_3$ solution for the ion-exchange process. During this ion-exchange process, the Li^+ of the LiV_3O_8 layer gets replaced with Ag^+. This Ag^+ forms a temporary conductive nanofilament upon the application of external bias showing the resistive switching mechanism. The final device has a device configuration of p^+-Si/$LiInSnO_4$/SnO_2/(Ag/Ag^+)-V_2O_3. For metallization, LiF/Al has been used as an electrode with a thickness of nearly 104 nm (LiF = 4.2 nm; Al = 100 nm) using the thermal evaporation method. The electrodes are patterned using shadow masks having a channel width to length (W/L) ratio of 19 (W = 1900 μm; L = 100 μm).

Memtransistor and synaptic functionality tests

For the structural analysis of the prepared thin films, grazing incidence X-ray diffraction (GIXRD) is performed using a Rigaku SmartLab system with Cu-K_α radiation (λ = 0.15405 nm). The scan covers a range of 10°–70° with a scan rate of 3° min^{-1}. For optical studies, UV-visible spectroscopy is conducted on thin films deposited on a quartz substrate (JGS2, Vritratech Technologies) using a JASCO V-650 UV-Vis spectrophotometer. Atomic force microscopy (AFM) (Agilent 5500 AFM/SPM microscope) studies are carried out to examine the surface topography of the thin films. For identification of the chemical state, X-ray photoemission spectroscopy (XPS) has been employed using an Al K_α monochromatic X-ray source (1486.6 eV) and a high-resolution hemispherical analyzer (K-Alpha XPS system) for the detection of excited electrons. Cross-sectional scanning electron microscopy (SEM) (EVO 60,

Carl Zeiss, Germany) is employed to study the thickness of each layer. Electrical characterization studies are performed with a Keysight B1500A semiconductor parameter analyzer. Standard TFT measurements are conducted by varying the gate voltage (V_G) and source–drain voltage (V_D). Synaptic studies are conducted using a Tektronix AFG31052 function generator, with a UV (395 nm) and white light source, in conjunction with a mechanical chopper. Mott–Schottky analysis is conducted using an Autolab MetroOhm system.

Author contributions

R. C., H. S. and B. N. P. designed the experiments. R. C., S. P. and H. S. synthesized the samples, performed electrical and optical measurements, and analyzed the data. R. G. performed the cross-sectional SEM experiment. R. C. and H. S. carried out the simulations. R. C., H. S., A. K. Y., U. P. and B. N. P. wrote the manuscript. All the authors discussed the results and contributed to finalizing the manuscript.

Conflicts of interest

The authors declare no competing conflicts of interest.

Data availability

Data for this article are available at https://drive.google.com/drive/folders/1B9InD7lI3x5UnKXSlM6pkUswHX-lSWuH?usp=sharing.

Supplementary information (SI): Grazing incidence X-ray diffraction studies of each layer are illustrated in Fig. S1. UV-Vis spectra and Tauc plots for each thin film layer are given in Fig. S2. Fig. S3 shows the cross-sectional SEM image of the device configuration p^+-Si/LiInSnO$_4$/SnO$_2$/(Ag/Ag$^+$)-V$_2$O$_3$. The AFM micrographs for device-1 and device-2 are illustrated in Fig. S4. Schematic configuration of device-1 and device-2 is shown in Fig. S5. The output and transfer characteristics of device-1 and device-2 are presented in Fig. S6. DC current measurement and gate leakage current are plotted in Fig. S7. The memtransistor behaviour of device-1 is displayed in Fig. S8. Device-to-device variation of important parameters is presented in Fig. S9. The absorbance *vs.* exposure time curve for device-2 and Mott–Schottky plots of various thin films under dark and light are given in Fig. S10. The temporal response of device-2 is studied in Fig. S11 to gain an understanding of RS. The memristive behaviour of device-2 is depicted in Fig. S12. Fig. S13 shows the ReRAM property in device-2. The band diagram mechanism for synaptic response is illustrated in Fig. S14. Pavlov's dog experiment is given in Fig. S15. Fig. S16 illustrates the learning–forgetting–relearning behaviour of the device. Emulation of logic gate operation is shown in Fig. S17. The schematic for the CNN model is displayed in Fig. S18. Table S1 shows the key device figure of merit of device-1 and device-2. The parameters of memT behaviour at different ranges of V_D are tabulated in Table S2. Table S3 presents a comparative chart for Mott–Schottky potentials for various thin films under dark and light. A comparative chart of different oxide memtransistors is given in Table S4. The decay time constants are shown in Table S5. Section 1 provides the details of Mott–Schottky analysis. Section 2 gives an explanation of synaptic behaviour in the device. The learning–relearning behaviour and logic gates are described in Section 3 and Section 4, respectively. Section 5 deals with the classical conditioning experiment. The autoencoder circuit is described in Section 6, whereas Section 7 elucidates the CNN architecture. See DOI: https://doi.org/10.1039/d5nr03811a.

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