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Dual-mode switching of a bidirectional self-rectifying Ti/HfO_2/Ti device for bipolar and electronic complementary resistive switching

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This study explores the dual-mode switching behavior of bidirectional self-rectifying Ti/HfO_2/Ti (THT) memristors to address the growing demand for efficient in-memory computing. The device operates in electronic bipolar resistive switching (eBRS) and electronic complementary resistive switching (eCRS) modes with bidirectional self-rectifying properties, differing from conventional unidirectional self-rectifying devices. The device achieves stable dual-mode switching by utilizing electronic trapping/detrapping at oxide layers formed at the top and bottom interfaces, while the HfO_2 layer in the middle serves as a blocking layer. The characteristic bidirectional dual-mode self-rectifying switching offers efficient parity bit generation through in-memory parity generation, minimizing overhead and potential errors during data delivery. When the THT memristors are integrated into a 1 × *n* line cell configuration, the eBRS mode device as a 1-bit encoded memory cell and the eCRS mode device as a 1-bit parity cell within the given interconnect line enable the desired in-memory parity generation.

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New concepts

In this study, we propose a Ti/HfO_2/Ti (THT) memristor to achieve bidirectional self-rectifying (bSR) behavior and in-memory parity generation for error detection within crossbar arrays (CBAs). Unlike conventional self-rectifying devices that allow switching only in a single direction, the THT device forms trap layers at both the top and bottom interfaces by employing Ti electrodes on both sides. This configuration enables bidirectional self-rectifying characteristics and allows electronic complementary resistive switching (eCRS) behavior. The proposed THT memristor maintains the selector-free characteristic of self-rectifying switching while addressing the low retention caused by electronic detrapping using an integrated error-checking system. In addition, when the THT device is implemented in a 1 × *n* line cell configuration, the eBRS mode functions as a 1-bit memory cell, while the eCRS mode serves as a 1-bit parity cell. This dual-mode operation enables in-memory parity bit generation using the same memristor. We experimentally demonstrate XNOR-based operations utilizing the eCRS mode, verifying its use for error detection. Furthermore, the proposed scheme improves energy efficiency and uniformity compared to filament-based CRS devices, suggesting its scalability for larger arrays using parallel operations.

Cheol Seong Hwang

Cheol Seong Hwang has been a Professor in the Department of Materials Science and Engineering at Seoul National University, Korea, since 1998, and has been a university Distinguished Professor since 2020. His research interests include semiconductor memory materials and devices, as well as neuromorphic computing with memristors. He is the author or coauthor of over 750 peer-reviewed papers, including one selected for Nanoscale Horizons' 10th anniversary Regional Spotlight Collection: Asia-Pacific. He also served as a Guest Editor with other colleagues for the 'Memristors and Neuromorphic Systems' collection of the journal. He is proud of the long-standing collaboration, which is set to continue.

Introduction

With the rapid development of artificial intelligence, the memory bottleneck issue, which refers to the critical burden of handling enormous data transfer between the memory and the processor, has become increasingly problematic. In response, alternative computing architectures, such as near-memory and in-memory computing, have emerged, benefiting from shorter or eliminated data paths between memory and computing

units. Resistive switching random-access memory (RRAM) has attracted significant attention for these applications due to its nonvolatile memory functionality, low power consumption, fast switching speed, and high scalability due to the simple two-terminal structure and stackable design.[1–3] However, the passive nature of the memory introduces sneak-current issues in a cross-bar array (CBA) structure, thereby undermining the reliability of circuit operation due to interference from adjacent cells, which limits large-scale integration and adversely affects logic operations.[4] Furthermore, the risk of data corruption is higher due to more limited endurance than the complementary metal–oxide–semiconductor (CMOS) transistor.[5,6]

Various solutions have been proposed to address sneak-current issues. For instance, embedding selector devices (*e.g.*, diodes, transistors, and threshold switches) into RRAM has been proposed.[7,8] However, the additional selectors induce higher operation voltages, increased variation, and integration complexity. Alternatively, self-rectifying RRAM that utilizes band alignment using one (*i.e.*, top) electrode with a higher work function than the other (*i.e.*, bottom) electrode can resolve sneak-current issues without using selectors.[4] The switching mechanism of reported self-rectifying RRAM typically relies on switching between electronic trapping/detrapping within the trap-rich layer. This approach offers higher endurance than the conductive filament formation/rupture mechanism, but lower retention at high temperatures and slower operation speeds.[9] Consequently, adopting an error-checking system to account for data degradation is crucial.

Recent works have demonstrated the detection and correction of various errors using XOR operations with parity bits in RRAM.[10–14] A single RRAM with complementary resistive switching (CRS) behavior can implement XOR operations within a single cycle, achieving the smallest chip area and high switching speed.[15] Nevertheless, no work has reported bidirectional self-rectifying (bSR) memristors with CRS behavior to simultaneously solve the sneak current and data reliability issues.

In this study, a low-power and high-reliability Ti/HfO_2/Ti (THT) device is reported that exhibits electronic complementary resistive switching (eCRS) with bSR behavior. Ti is generally used as an active electrode due to its strong affinity for oxygen, allowing it to react with oxygen ions in the resistive switching (RS) layer.[16,17] In particular, the interfacial TiO_x/HfO_x structure, formed through oxygen scavenging by Ti from HfO_2, contributes significantly to the switching behavior by providing a defect-rich environment and acting as a reservoir for oxygen vacancies. Previous studies demonstrated that engineering the Ti/HfO_2 interface to form TiO_x can improve the RRAM switching characteristics.[18,19] In most RRAM devices, an active electrode is paired with an inert electrode to control oxygen vacancies in the RS layer and adjust the barrier height at the interface. However, this work used Ti thin films for both electrodes to form two distinct vacancy-rich RS layers, enabling the eCRS mode with bSR behavior. Structural analyses based on transmission electron microscopy (TEM), X-ray photoelectron spectroscopy (XPS), and electrical analyses through current–voltage (*I–V*) measurements were conducted to understand the underlying origin of the bSR behavior. While many studies have reported electronic bipolar resistive switching (eBRS) based on an electron trapping/detrapping mechanism, this work introduces eCRS with bSR behavior, which can be utilized for in-memory parity generation in a CBA. Using the eCRS with bSR behavior, where the SET operation occurs in both the positive and negative bias regions, two distinctive low-resistance states (LRS) can be achieved in a single directional bias sweep. Consequently, eCRS behavior with bSR was demonstrated by setting the initial state to a LRS, followed by RESET (switching from a LRS to a high-resistance state (HRS)), and subsequent SET (switching from a HRS to another LRS). A single memory cell string with three THT devices was fabricated to demonstrate the 1-bit parity generation. Furthermore, the extension of the demonstrated parity generation to larger array sizes is proposed, along with its potential application in Hamming code-based error correction. Lastly, eCRS with bSR was compared with conventional CRS devices, demonstrating improved power efficiency and operation.

Results and discussion

Structural and electrical analysis of the Ti/TiO_{2-x1}/HfO_y/TiO_{2-x2}/Ti structure

The THT memristor was examined through structural and electrical analysis. First, the crystal structure, suboxide formation, and chemical composition were analyzed using TEM and XPS. Fig. 1(a) shows a cross-section TEM image of the THT memristor, where an easily distinguishable layer structure with metallic Ti at the top and bottom, amorphous 10-nm-thick HfO_2 in the middle, and amorphous TiO_{2-x1} and TiO_{2-x2} ($x1$, $x2 < 2$) at the upper and lower Ti/HfO_2 interfaces could be recognized. The thickness of the upper TiO_{2-x1} layer ($\sim$2 nm) appears thinner than the lower TiO_{2-x2} layer ($\sim$5 nm). Fig. S1 shows the chemical composition mapping results for Hf and Ti, obtained using energy-dispersive X-ray spectroscopy (EDS), indicating the well-defined 10-nm-thick HfO_2, thinner TiO_{2-x1} and thicker TiO_{2-x2}, consistent with the TEM image. The difference in the suboxides is related to the film growth process. The lower TiO_{2-x2} layer is formed in two steps. First, the Ti bottom electrode surface is exposed to air, forming a native oxide. It is then further oxidized by active oxygen atoms during the plasma-enhanced atomic layer deposition (PEALD) of HfO_2 film at a substrate temperature of 200 °C, with O_2 plasma as the oxygen source.[20,21] In contrast, the upper TiO_{2-x1} layer is formed when the Ti top electrode is deposited by electron-beam evaporation, where Ti interacts with the underlying HfO_2 layer and absorbs oxygen ions from the top portion of HfO_2 at room temperature, resulting in fewer Ti–O interactions compared to the lower layer of TiO_{2-x2}.

XPS analysis was subsequently used to confirm the influence of the formation of TiO_{2-x1} and TiO_{2-x2} on the HfO_2 layer. Fig. 1(b) shows the XPS depth profile results from the Hf 4f peak for the 10-nm-thick HfO_2 layer. The Hf 4f peaks could be

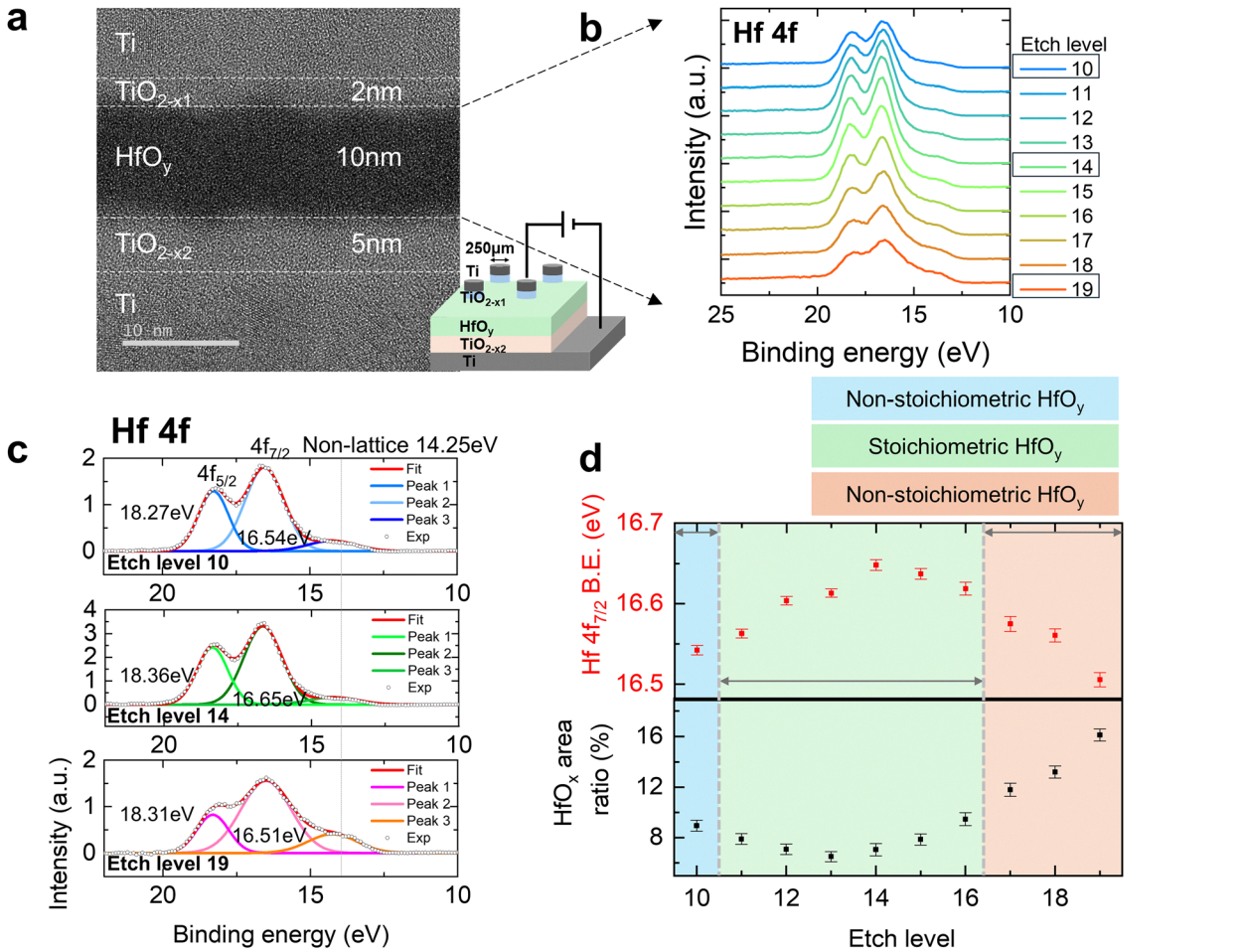


Fig. 1 (a) A cross-sectional TEM image of the Ti/TiO_{2-x1}/HfO_y/TiO_{2-x2}/Ti structure. (b) XPS spectra of the Hf 4f region for a depth profile of the HfO_y layer. (c) Deconvolution of the Hf 4f peaks at etching levels of 10, 14, and 19. (d) Binding energy (upper panel) and HfO_x area ratio (lower panel) shift analysis.

deconvoluted into a Hf $4f_{5/2}$ peak, $4f_{7/2}$ peak, and non-lattice HfO_x ($x < 2$) peak, with the binding energy of the non-lattice peak fixed at 14.25 eV. Fig. 1(c) shows the deconvoluted spectra from etch levels of 10 (upper HfO_2), 14 (middle HfO_2), and 19 (lower HfO_2). The upper panel in Fig. 1(d) shows the clear shifting tendency of the binding energy of the Hf $4f_{7/2}$ peak, which increases from 16.54 eV to 16.65 eV at depths of about 1 nm to 5 nm (etch level from 10 to 14), then decreases from 16.65 eV to 16.51 eV at depths of about 5 nm to 10 nm (etch level from 14 to 19). Based on the binding energy of the Hf $4f_{7/2}$ peak of 16.7 eV for stoichiometric HfO_2,[22] the shifts in the Hf $4f_{7/2}$ binding energy suggest that the HfO_2 layer in the THT memristor has a stoichiometric composition in the middle. In contrast, the composition is nonstoichiometric (oxygen deficient) at the top and bottom interfaces. The lower panel of Fig. 1(d) shows the non-lattice HfO_x ($x < 2$) peak area ratio variation, which is consistent with the shifts in Hf $4f_{7/2}$. For the upper TiO_{2-x1}/HfO_2 interface, the area ratio of non-lattice HfO_x was 9%, which then decreased to 6% in the middle and then increased to 16% for the lower HfO_2/TiO_{2-x2} interface. Fig. S2 shows the XPS depth profiles of the O 1s and Ti 2p peaks, where both the binding energy shift and non-lattice oxygen (or oxygen ions near oxygen vacancies (V_O)) area ratio follow the same trend observed in Hf 4f analysis, confirming Ti oxidation at both interfaces of the 10-nm-thick HfO_2 layer and supporting the identification of the TiO_{2-x1} and TiO_{2-x2} interfacial layers. The XPS results confirmed that the 10-nm-thick HfO_2 layer contained a high concentration of V_O formed at both interfaces compared to the relatively stoichiometric composition in the middle, resulting in a HfO_y ($y \leq 2$) layer composition. Therefore, it can be concluded that the fabricated sample coincides with a Ti/TiO_{2-x1}/HfO_y/TiO_{2-x2}/Ti structure. It was reported that electronic switching requires a trap-rich layer (TL) to capture and release the carriers through electron trapping and detrapping mechanisms.[23] Therefore, TL1—comprising TiO_{2-x1} and the adjacent upper portion of HfO_y—and TL2—consisting of the lower portion of HfO_y and TiO_{2-x2}—as confirmed by TEM and XPS analyses, are both expected to contribute to resistive switching behaviour in the THT memristor. The structural difference between the upper and lower interfaces, considered a key factor in asymmetric switching behavior, will be discussed below.

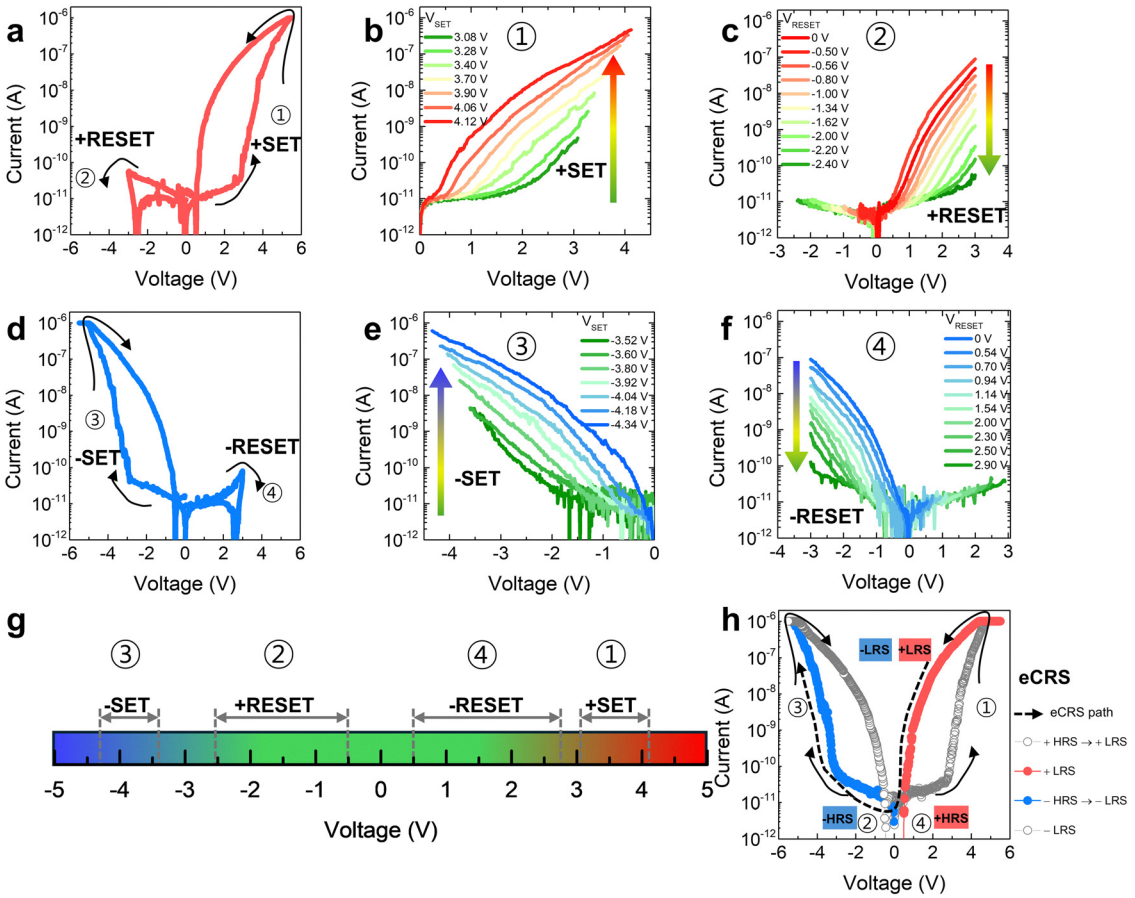


Fig. 2 (a) Positive eBRS operation of the THT device with a +SET voltage of 5 V, a compliance current of 1 μA and a +RESET voltage of −3 V. (b) Gradual SET switching from +HRS to +LRS with different set sweep voltages (3.08 V to 4.12 V). (c) Rectifying RESET switching from +LRS to +HRS with different reset sweep voltages from −0.50 V to −2.40 V, confirmed by a 3.0 V single sweep after each reset sweep. (d) Negative eBRS operation of the THT device. (e) Gradual −SET switching from −HRS to −LRS with different set sweep voltages (−3.52 V to −4.34 V). (f) Rectifying −RESET switching from −LRS to −HRS with different reset sweep voltages (from 0.54 V to 2.90 V) confirmed by a −3.0 V single sweep after each reset sweep. (g) A schematic diagram showing the THT device operation voltages with positive eBRS and negative eBRS. (h) eCRS with bSR operation obtained by the consecutive operation of positive eBRS and negative eBRS: switching from +HRS to +LRS, then resetting to −HRS, and back to −LRS.

Fig. 2 shows the two self-rectifying eBRS switchings of a pristine dot-type THT memristor with a top-electrode diameter of 250 μm. Fig. 2(a) shows a positive eBRS, having two transitions, with +SET (+HRS → +LRS) in the positive bias region and +RESET (+LRS → +HRS) in the negative bias region. Fig. 2(b) and (c) show the gradual SET and RESET operations with an increase in maximum sweep voltages from 3.08 V to 4.12 V and from −0.5 V to −2.4 V, respectively. The sign of the RESET operation is defined based on the polarity of the corresponding SET operation. For clarity, the HRS in the positive bias region is denoted as +HRS, while the HRS in the negative bias region is referred to as −HRS. Fig. 2(d) shows a negative eBRS, having two transitions, with −SET (−HRS → −LRS) and −RESET (−LRS → −HRS) operations. Similar to positive eBRS, Fig. 2(e) and (f) show the gradual −SET and −RESET operations from −3.52 V to −4.34 V and from 0.54 V to 2.90 V, respectively.

Fig. 2(g) summarizes the voltage ranges for the two eBRS switchings, where the two eBRS switchings can be combined for eCRS, as there is no overlapping of the voltage regions. Fig. S3 shows the dependence of the non-overlapping behavior on HfO_2 thickness. THT devices with 4-nm- and 7-nm-thick HfO_2 layers exhibit overlapping voltage regions and unstable switching, while the 10-nm-thick HfO_2 device provides well-separated windows suitable for stable eCRS operation. Fig. 2(h) shows eCRS with bSR operation, where the THT memristor transitions from +LRS to −HRS and from −HRS to −LRS. The two resistive switchings (RSs) are possible as the THT device has naturally formed anti-serial RS layers of TiO_{2-x1} and TiO_{2-x2}. In other words, CRS operation is also possible in eBRS operations as the RS in two anti-serial BRS devices is equivalent to CRS operation.[24] Thus, the proposed THT device can perform eBRS and eCRS operations, which are defined as dual-mode switching.

Fig. 3 shows the uniformity of the dual-mode switching in dot-type THT memristors with a diameter of 250 μm. Fig. 3(a) shows the positive eBRS curves acquired from 15 devices, each subjected to 10 cycles under a compliance current of 1 μA, confirming the high switching uniformity. Fig. 3(b) shows the cumulative probabilities of cycle-to-cycle variation in the resistance values of positive eBRS over 50 cycles of DC *I–V* sweeps at

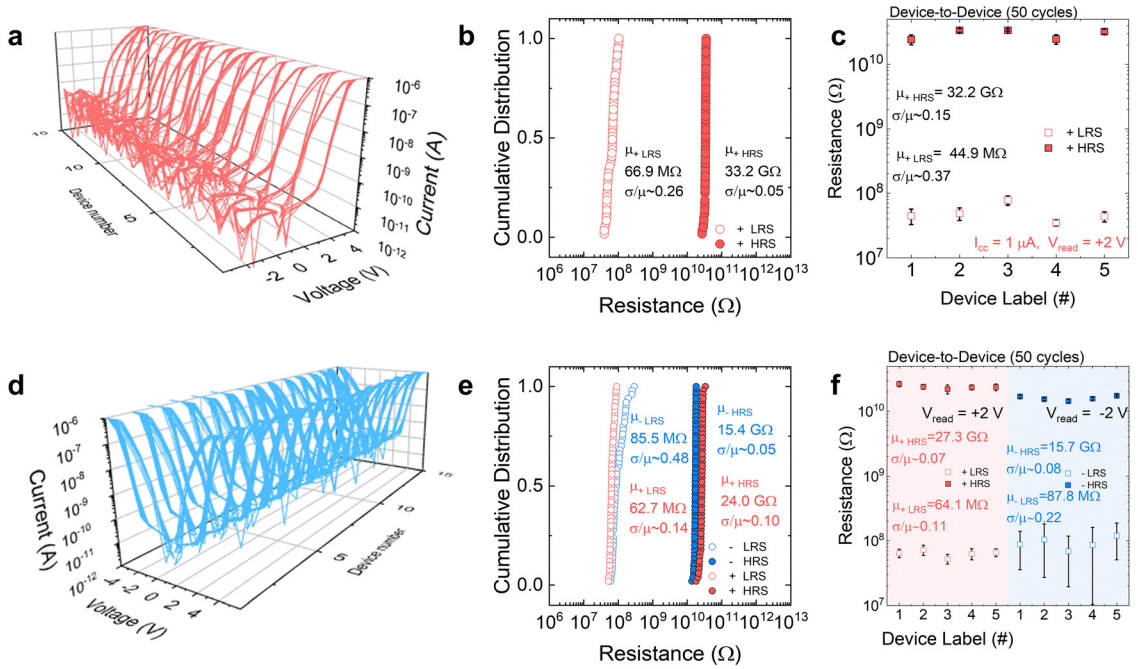


Fig. 3 (a) DC *I*–*V* switching cycles of positive eBRS for 15 devices, each measured over 10 cycles. (b) Cycle-to-cycle variation of positive eBRS over 50 cycles. (c) Device-to-device variation of positive eBRS for 5 devices over 50 cycles. (d) DC *I*–*V* switching cycles of eCRS for 15 devices, each measured over 10 cycles. (e) Cycle-to-cycle variation of eCRS over 50 cycles. (f) Device-to-device variation of eCRS for 5 devices over 50 cycles.

a reading voltage of 2 V. In this work, the read margin is defined as the difference between the voltages at which the HRS and LRS reach 0.1 nA, which were ~3 V and 0.5 V, respectively.[25] Therefore, the read voltage must be selected between these two voltage values. A read voltage of 2 V resulted in the lowest resistance value variations, while maintaining a sufficiently high on/off current ratio (~500). Therefore, 2 V was selected as the read voltage. The coefficients of variation (CV), which are defined as the standard deviation divided by the mean for positive eBRS, were 0.26 for +LRS and 0.05 for +HRS. Fig. 3(c) shows the median values of R_{+LRS} and R_{+HRS} acquired from five devices over 50 DC cycles to verify the device-to-device characteristics. The CVs for the +LRS and +HRS resistances were measured as 0.37 and 0.15, respectively. Likewise, Fig. 3(d) shows the eCRS curves from 15 different devices, each subjected to 10 cycles under a compliance current of 1 μA for both polarities, showing the bSR properties. Fig. 3(e) shows the cumulative probabilities of cycle-to-cycle variation for eCRS over 50 cycles, obtained at a read voltage of ±2 V. The evaluations included +LRS, +HRS, −LRS, and −HRS, and the corresponding CVs were 0.14 for +LRS, 0.10 for +HRS, 0.48 for −LRS, and 0.05 for −HRS. The observed difference in CV values between +LRS and −LRS is attributed to the Pre-SET process. Fig. S4 shows that positive eBRS operates in a forming-free fashion due to the higher defect density at the HfO_y/TiO_{2-x2} interface, whereas negative eBRS requires a Pre-SET process to induce switching at the opposite interface (TiO_{2-x1}/HfO_y), indicating that the active switching layer shifts depending on the bias polarity. Fig. 3(f) shows the median values of R_{+LRS}, R_{+HRS}, R_{-LRS}, and R_{-HRS} of eCRS at a read voltage of ±2 V, acquired from device-to-device assessment over 50 cycles for five devices. The CVs were measured as 0.11 for +LRS and 0.07 for +HRS in the positive region, and 0.22 for −LRS and 0.08 for −HRS in the negative region. These results demonstrate the high uniformity and reliability of dual-mode switching in the THT memristor.

Mechanism of the THT memristor eCRS operation

The mechanism of eCRS with bSR behavior in the THT memristor is further investigated by measuring the *I*–*V* curves of dot-type devices with a diameter of 250 μm at temperatures from 313 K to 373 K (40–100 °C). These curves were analyzed according to various conduction mechanisms, including Schottky emission, hopping conduction, Fowler–Nordheim (F–N) tunneling, Poole–Frenkel (P–F) emission, ohmic conduction, direct tunneling, and space-charge-limited conduction (SCLC). The electric field for fitting was calculated by dividing the voltage across 2-nm TiO_{2-x1}, 10-nm HfO_y, and 5-nm TiO_{2-x2}, using a dielectric constant of 25 for amorphous HfO_y and 30 for the mixed amorphous and anatase phase in TiO_{2-x1} and TiO_{2-x2}.[26,27] The phases of the layers were confirmed using TEM and XRD, with detailed and additional capacitance–frequency curve results shown in Fig. S5.[28,29] In the low voltage range of the positive region (LVR, 0.6 V to 1.2 V), electron charge injection from the Ti bottom electrode to TiO_{2-x2} proceeded smoothly due to the quasi-ohmic contact at the TiO_{2-x2}/Ti interface. In contrast, charge injection from TiO_{2-x2} to HfO_y was hindered due to the high energy barrier.[30,31] Therefore, the electric field of HfO_y was used to fit the *I*–*V* curves at each temperature. The linear relationship seen in the

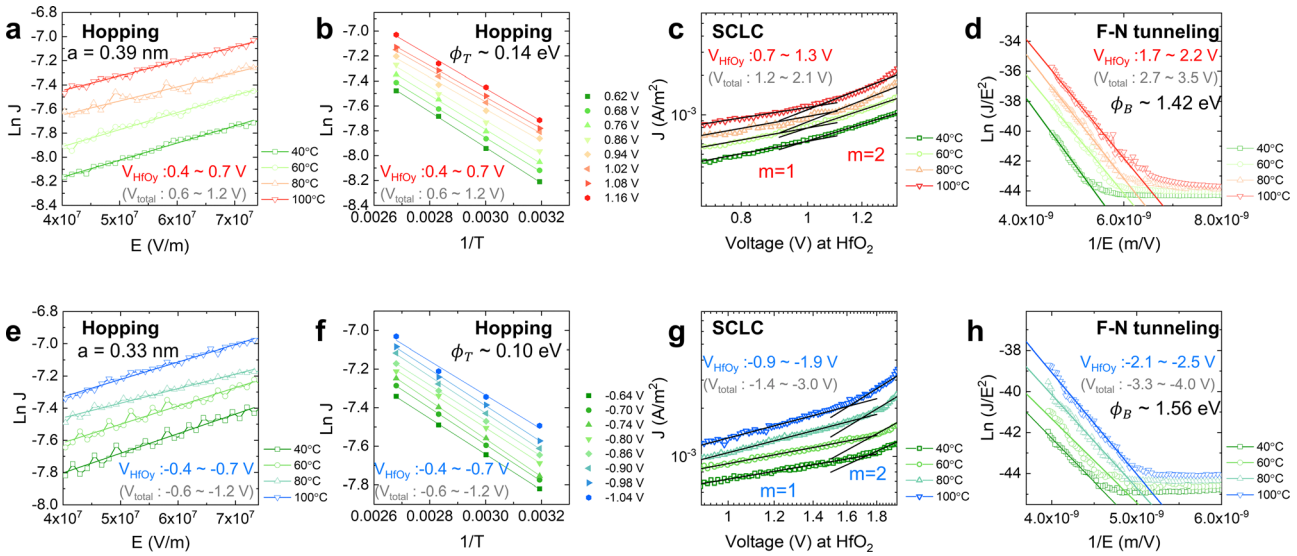


Fig. 4 (a) Hopping conduction in the HfO_y layer (0.6 V to 1.2 V). (b) Arrhenius plots for the HfO_y layer. (c) Double logarithmic I–V curves of the THT memristor in the positive region, showing ohmic (m = 1) and space-charge-limited conduction (m = 2) behavior (1.2 V to 2.1 V). (d) F–N tunneling in the HfO_y layer (2.7 V to 3.5 V). (e) Hopping conduction in the HfO_y layer (−0.6 V to −1.2 V). (f) Arrhenius plots for the HfO_y layer. (g) Double logarithmic I–V curves of the THT memristor in the negative region (−1.4 V to −3.0 V). (h) F–N tunneling in the HfO_y layer (−3.3 V to −4.0 V).

ln$J$ *versus* E plot at each temperature, as shown in Fig. 4(a), suggests that current conduction in the positive LVR is governed by hopping conduction, as described by eqn (1):

$$J = qan\nu \exp\left[\frac{qaE}{kT} - \frac{E_a}{kT}\right] \quad (1)$$

where a, n, ν, E_a, and k are the mean hopping distance, electron concentration at the conduction band, frequency of thermal vibrations of the trap site, activation energy, and Boltzmann constant, respectively.[32]

The hopping distance of 0.39 nm was calculated from the slopes of best-fit linear plots. Fig. 4(b) shows the ln$J$ *versus* $1/T$ plots at different voltages. Following the hopping mechanism, a zero-field trap energy level (ϕ_T) of 0.14 eV was extracted from the slopes of the best-linear-fit plots and their extrapolation to zero voltage. The low current level of +HRS observed in the I–V curve indicates that only a few excited electrons could transport through hopping in this region. In the intermediate voltage range (IVR, 1.2 V to 2.1 V), the voltage drop across the HfO_y layer was used for analysis. Fig. 4(c) shows the double logarithmic I–V curves, where the conduction behavior is consistent with SCLC. In these regions, slope values of 1 and 2 were observed, corresponding to ohmic conduction and SCLC, respectively.[33,34] In the high voltage range of the positive region (HVR, 2.7 V to 3.5 V), the electric field of HfO_y was again adopted, considering that while some excited electrons conduct through hopping conduction, the majority of carrier transport is limited by the insulating properties of the HfO_y layer. Fig. 4(d) shows the ln(J/E^2) *versus* $1/E$ plot, which exhibits a linear relationship, indicating that conduction in HfO_y in the HVR is governed by F–N tunneling, as described by eqn (2):

$$J = \frac{q^3E^2}{8\pi hq\phi_B} \exp\left[\frac{-8\pi(2qm_T^*)^{1/2}}{3hE}\phi_B^{3/2}\right] \quad (2)$$

where m_T^* is the tunneling effective mass in the dielectric layer, h is the Planck constant, and ϕ_B is the barrier height. The F–N tunneling barrier height (ϕ_B) extracted from the slope in the HVR was 1.42 eV, and the tunneling effective mass was given as 0.17 m_0, which was taken from the literature.[35]

The current transport properties in the negative bias region were similarly analyzed using hopping conduction in the low voltage range of the negative region (−0.6 V to −1.2 V), SCLC in the intermediate voltage range (−1.4 V to −3.0 V) and F–N tunneling in the highly negative bias region (−3.3 V to −4.0 V). Fig. 4(e) and (f) show the fitting results for the LVR, confirming that hopping conduction dominates the conduction in HfO_y, similar to the conduction in the LVR of the positive region. The similarly extracted hopping distance and ϕ_T values were ~0.33 nm and 0.10 eV, respectively. Fig. 4(g) shows the double logarithmic I–V curves, where the conduction behavior is consistent with SCLC. In these regions, slope values of 1 and 2 were again observed, corresponding to ohmic conduction and SCLC, respectively. Fig. 4(h) shows the ln(J/E^2) *versus* $1/E$ plot. The ϕ_B value for the F–N tunneling mechanism extracted from the slope in the HVR was 1.56 eV, similar to the value in the positive bias region. Therefore, these findings indicate that the trap-rich layer of TL1 or TL2 is filled with electrons in the LVR, depending on the polarity, with a few electrons crossing the middle HfO_y through hopping. In the HVR, the electrons accumulated in TL1 or TL2 can be transported through the middle HfO_y by F–N tunneling, switching +HRS to +LRS or −HRS to −LRS.

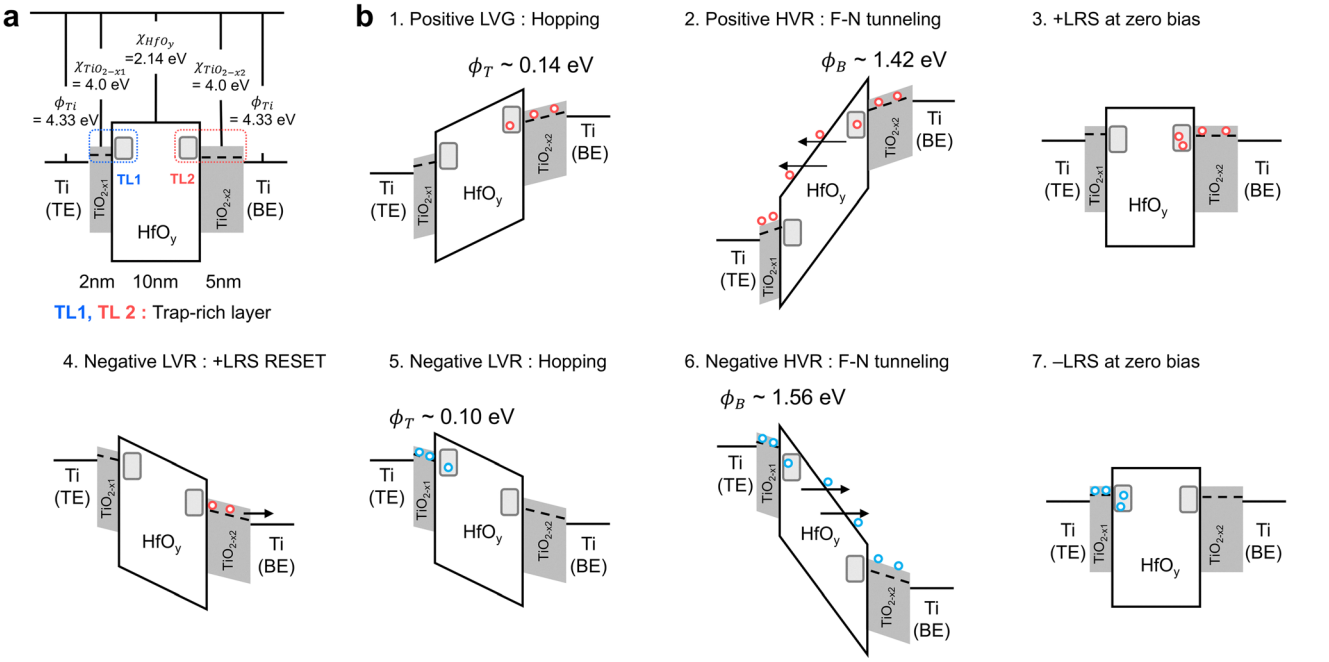


Fig. 5 (a) A schematic band diagram of the THT memristor under zero bias conditions. (b) Schematic band diagrams showing the +SET (steps 1 to 3), +RESET (step 4), and −SET (steps 5 to 7) mechanisms based on charge trapping/detrapping.

Additional analysis, including the overall *I–V* curve and poor fitting based on Schottky and P–F emission, is given in Fig. S6.

A switching model for eCRS in the THT memristor was established based on the structural and electrical test results. Fig. 5(a) shows an energy band diagram of the THT memristor. The work function (Φ) of the Ti electrode is assumed to be 4.33 eV, and the electron affinity (χ) values of TiO_{2-x1}, HfO_y, and TiO_{2-x2} are taken from the reference values (4.0 eV for TiO_{2-x1}, 2.14 eV for HfO_y, and 4.0 eV for TiO_{2-x2}).[36,37] Step 1 in Fig. 5(b) shows the positive LVR of the THT device. When a positive bias is applied to the Ti top electrode, electrons rapidly fill TL2—comprising TiO_{2-x2} and the lower HfO_y layer—owing to the quasi-ohmic contact between TiO_{2-x2} and the bottom Ti electrode. However, the movement of electrons to the top electrode is hindered by an energy barrier between HfO_y and TiO_{2-x2}, and only a few excited electrons can flow to the top electrode *via* hopping conduction. Step 2 shows F–N tunneling in the positive HVR, where electrons in TL2 tunnel through the thin potential barrier of HfO_y. After tunneling through the HfO_y layer, the electrons readily move through TiO_{2-x1} and reach the Ti top electrode due to the electron affinity difference between HfO_y and TiO_{2-x1}. Therefore, HfO_y acts as a blocking layer in response to low electric fields and a tunneling path under high electric fields. Step 3 shows the +LRS at zero bias, where electrons remain trapped in the TL2 trap sites even after the voltage is removed. In this state, the traps in TL2 are filled, decreasing the energy barrier at the HfO_y and TiO_{2-x2} interface and allowing efficient electron transport when a positive bias is subsequently applied. Fig. S7 shows the endurance of eCRS over 10^3 cycles and the retention of +LRS for over 30 000 s at room temperature, with gradual decay. Such stable retention in electronic switching devices can be attributed to the absence of an internal field, which is induced by the identical work functions of the electrodes; this can hardly be achieved when two electrodes with different work functions (*e.g.*, Pt and Ti (or TiN)) are adopted.[31,38] Step 4 shows the de-trapping of electrons from TL2 to the Ti bottom electrode under a negative bias at the Ti top electrode. In step 5, electrons are rapidly injected from the Ti top electrode to TL1, consisting of TiO_{2-x1} and upper HfO_y, due to Ti/TiO_{2-x1} quasi-ohmic contact. Conduction is dominated by hopping, as a few excited electrons move through HfO_y while the energy barrier at the HfO_y and TiO_{2-x1} interface restricts others. Step 6 shows that at a sufficiently high negative bias, HfO_y becomes thin enough for the electrons from TL1 to transit through F–N tunneling and reach the Ti bottom electrode, switching to −LRS. Similarly, step 7 shows that under zero-bias conditions, electrons remain trapped at the TL1 trap sites, indicating −LRS. From step 1 to step 7, HfO_y serves as a blocking and switching layer. As a blocking layer, the middle part of HfO_y prevents electrons injected at low voltage from moving to the opposite electrode, enabling rectifying behavior. As a switching layer, HfO_y at both interfaces, along with TiO_{2-x1} and TiO_{2-x2}, provides trap sites. Therefore, the dual-mode switching of the THT memristor can be understood from the structure, where two serially connected TL1 and TL2 layers are formed at both interfaces, separated by the middle part of the HfO_y layer, trapping and detrapping electrons depending on the polarity.

The *I–V* characteristics of MIM stacks with a 10-nm-thick HfO_2 layer and electrodes with different work functions and oxygen reactivities (Pt, TiN, and Ti) were examined to verify the effects of electrodes. Fig. 6(a)–(c) show the *I–V* characteristics of

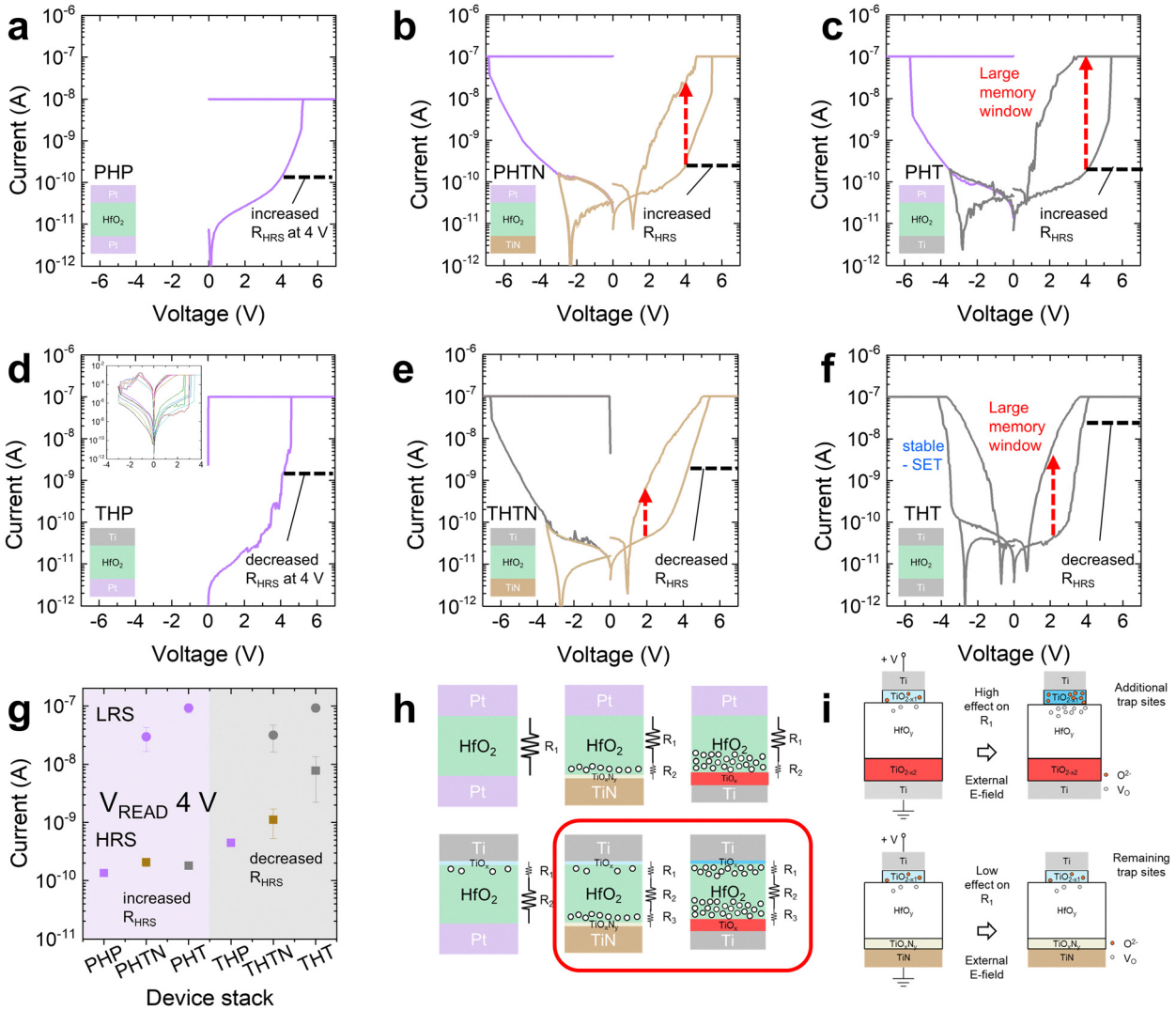


Fig. 6 Resistive switching *I*–*V* curves of (a) Pt/10-nm-thick HfO_2/Pt, (b) Pt/10-nm-thick HfO_2/TiN, (c) Pt/10-nm-thick HfO_2/Ti, (d) Ti/10-nm-thick HfO_2/Pt, (e) Ti/10-nm-thick HfO_2/TiN, and (f) Ti/10-nm-thick HfO_2/Ti devices. (g) LRS/HRS current distributions for different stacked devices. (h) Schematic diagrams of devices with different electrodes containing an HfO_2 layer and corresponding interface oxide layers; each layer is represented as a series resistance component (R_1 to R_3). (i) The formation of additional trap sites depending on differences in the external electric field distribution at the top interface (R_1), in the HfO_2 bulk layer (R_2), and at the bottom interface (R_3) for THTN and THT.

Pt/HfO_2/Pt (PHP), Pt/HfO_2/TiN (PHTN), and Pt/HfO_2/Ti (PHT). The inert top Pt electrode is invariant in these configurations, while the bottom electrode is varied. None of the three devices exhibited stable −SET behavior. The PHP device exhibited a breakdown at a compliance current of 10 nA. This failure is attributed to the Schottky barrier between HfO_2 and Pt, as well as the low oxygen vacancy density at the interface due to the low reactivity of Pt. However, when the bottom electrode was changed to TiN or Ti, self-rectifying behavior was observed due to their relatively low work functions (Φ_{TiN} = 4.5 eV; Φ_{Ti} = 4.3 eV) and high oxygen reactivity compared to Pt (Φ_{Pt} = 5.3 eV).[39,40] In particular, the PHT device exhibited an increased switching memory window compared to PHTN, which is attributed to a more V_O-rich interface at the Ti interface than at the TiN interface. Fig. 6(d)–(f) show devices where the Pt top electrode was replaced with a Ti top electrode. The configurations include Ti/HfO_2/Pt (THP), Ti/HfO_2/TiN (THTN), and Ti/HfO_2/Ti (THT). Stable eCRS with bSR behavior was observed only in the THT configuration. The breakdown of the THP device implies that +SET behavior is associated with the bottom interface. The THTN and THT devices exhibited switching windows comparable to PHTN and PHT but with decreased R_{HRS} values due to Ti's low work function and high oxygen affinity. However, THTN did not exhibit SET behavior in the negative bias region, indicating that the -SET behavior is not solely governed by the top interface. Fig. 6(g) shows the current distribution for each stack acquired from six devices over 10 *I*–*V* cycles at a read voltage of 4 V. R_{HRS} decreased when the top electrode was changed from Pt to Ti, while R_{LRS} was barely affected. This finding suggests that while the entire RS layer influences the HRS state, the bottom layer, where electron injection occurs, plays a more significant role in determining R_{LRS}. This finding

is consistent with the observation that the LRS current increased when the bottom electrode was changed from TiN (PHTN and THTN) to Ti (PHT and THT), considering the higher trap-site density in the bottom layer. Fig. 6(h) shows a schematic representation where each layer in a stack composed of the HfO_2 layer and interface layers is treated as a single resistance component connected in series, explaining the differences in switching behavior depending on the top/bottom electrode. The PHP device has no V_O-rich interface on either side, resulting in the highest R_{HRS}. In contrast, HfO_2 with TiN or Ti shows V_O-rich interfaces, with the Ti interface having a higher V_O concentration than the TiN interface. Based on the electrode materials, the relative resistance in the HRS state can be deduced as following the order: $R_{PHP} > R_{PHTN} > R_{THP} > R_{PHT} > R_{THTN} > R_{THT}$. This relationship matches the median value of HRS current measured at 4 V in Fig. 6(g), except for the PHT and THP devices. The lower HRS current in PHT compared to THP can be attributed to breakdown events. As expected, the HRS current at 2 V is lower in THP than in PHT. Consequently, the series resistance, composed of the HfO_2 bulk layer and the interface layers, is associated with the switching characteristics of each device. Compared to other configurations, the stable negative SET behavior observed in THT originates from the electric field distribution determined by the composition of the series resistance. Both THTN and THT exhibit the lowest overall resistance among all configurations, and they consist of a top interface (R_1), the HfO_2 bulk layer (R_2), and a bottom interface (R_3). In THTN, the bottom interface has a relatively low V_O concentration, leading to most of the electric field being distributed across R_2 and R_3. In contrast, in THT, the bottom interface with a high V_O concentration decreases R_3, which allows the electric field to also be applied to R_1. This results in the highest electric field existing at the top interface in THT, promoting additional reactions between Ti and HfO_2, generating more V_O, and enabling stable negative SET behavior, as shown in Fig. 6(i). Overall, the suppressed negative eBRS behavior observed in both Pt and TiN devices suggests that the formation of the top interfacial TiO_x layer is more likely driven by chemical interactions rather than deposition-induced effects.

Implementation of an XNOR logic gate and in-memory parity bit generation

XOR/XNOR gates are building blocks for various applications, such as encryption, arithmetic operations, and error handling. It was reported that the CRS can implement these functionalities in a sequential logic array; therefore, the eCRS described above can also be used for the same applications.[14] However, as discussed here, eCRS can offer additional merit for error correction by generating an in-memory parity bit.

Three THT memristors are fabricated with a common bit line (BL) connected to a load resistor for demonstration.

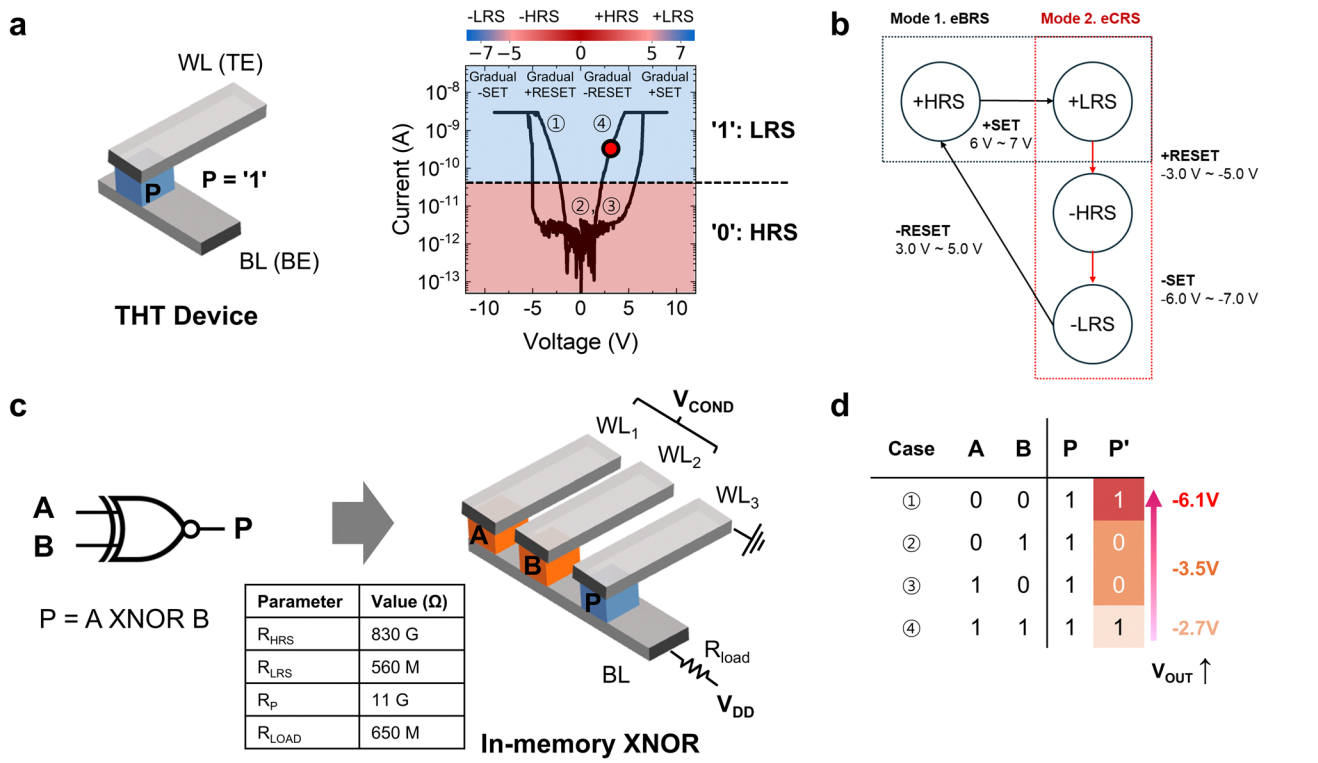


Fig. 7 An in-memory XNOR gate composed of three THT memristors connected in parallel with a common BL connected to a load resistor. (a) Electrical characteristics of the crosspoint THT memristor. (b) A state transition diagram for the THT memristor representing the required applied bias for eBRS and eCRS. (c) Implementation of the XNOR gate in 1 × 3 memristors. The WLs of the input and output memristors are connected to V_{COND} and GND, respectively. (d) The truth table of the XNOR gate. As the number of '1's in the input memristors decreases, the higher the voltage drop across the output memristor.

An XNOR logic gate can be implemented by representing the logical states '1' and '0' using the ±LRS and ±HRS of a memristor, respectively. Fig. 7(a) shows a single THT memristor initialized to +LRS. The bias conditions for eCRS and eBRS of the crosspoint THT memristor are summarized in the state transition diagram shown in Fig. 7(b). Depending on the magnitude of the applied negative bias, eCRS occurs from +LRS to −HRS or −LRS. Fig. 7(c) illustrates an in-memory XNOR gate based on two-input memristors, A and B. This operation is achieved by applying a conditional voltage (V_{COND}) to the word lines (WLs) of A and B, GND to the WL of the output memristor P, and a driving voltage (V_{DD}) to the BL through the load resistance (R_{load}). As the number of '1's in the input cells increases, the applied voltage across the P memristor decreases due to the voltage divider effect, as described by eqn (3) and (4):

$$V_{OUT,P} = \frac{R_P R_{eq}}{R^*} V_{DD} + \frac{R_{load} R_P}{R^*} V_{COND} \quad (3)$$

$$R^* = R_{eq}R_{load} + R_{load}R_P + R_{eq}R_P \quad (4)$$

where R_P, R_{eq}, and R^* are the resistance of the P memristor, the equivalent resistance, and the proportional resistance, respectively. Fig. 7(d) shows the truth table of the XNOR gate, where P and P′ represent the initial and final states of the P memristor, respectively. When both A and B are '1' (case 4), the P memristor remains in a +LRS state as the lowest $V_{OUT,P}$ is applied, as described in eqn (3). Cases 2 and 3 have the same number of '1's and a higher voltage drop than case 4, so the P memristor undergoes +RESET at ∼−3.5 V, resulting in −HRS. Case 1 has the highest $V_{OUT,P}$, resulting in the −LRS state. The load resistor and the resistance of the P memristor are set to 650 MΩ and 11 GΩ, respectively, to prevent resistance changes in the input memristors. Fig. S8 explains the input stability.

Fig. 8(a) shows an SEM image of the 1 × 3 arrangement of THT memristors, each with a switching area of 10 × 10 μm^2, used for the experimental demonstration of the XNOR logic operation. The optimal bias conditions for the conditional switching of the P memristor are selected based on the resistance states of the THT memristors, as described by eqn (3) and (4). V_{DD} and V_{COND} are set to −6.5 V and −1 V, respectively. Fig. 8(b) shows heatmaps representing the voltage drop across each memristor for each input case's initial and final states. Fig. 8(c) shows 15 cycles of XNOR operation with an average CV of 0.42. Logical '1' and '0' were determined based on whether the read current was $>5 \times 10^{-11}$ A or $<5 \times 10^{-11}$ A. A read voltage of 4 V was applied to the BL when the common node voltage of the bias controller exceeded −6.1 V and to the WL when it was lower to preserve the output state during the sensing step after the XNOR operation. Although the sensing operation is required after each logic cycle when a single XNOR

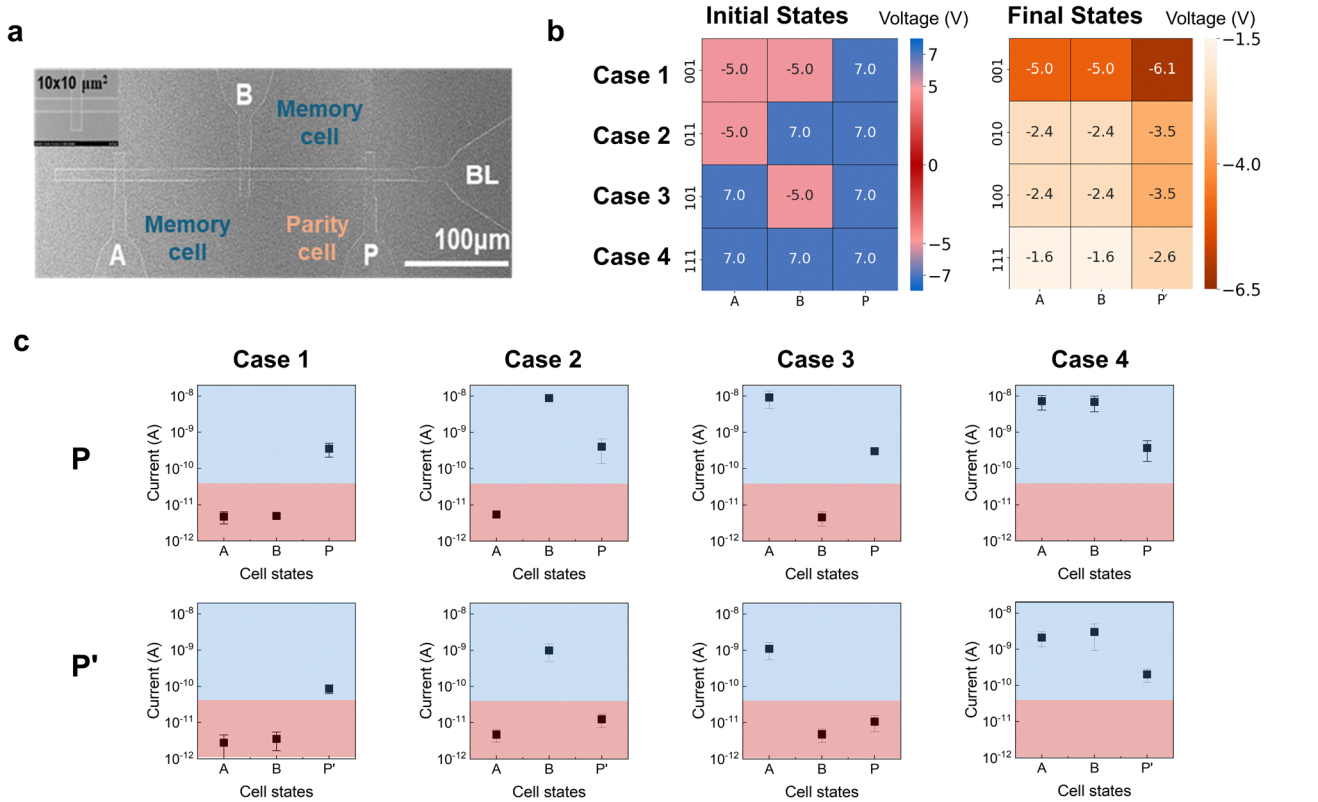


Fig. 8 Experimental demonstration of an XNOR logic gate. (a) A top-view SEM image of the 1 × 3 THT memristor consisting of two input cells and an output cell. (b) The voltage drop across each memristor in the initial and final states for each XNOR logic gate input case. (c) The results from 15 cycles of the XNOR gate.

operation is performed, the cost is negligible when the readout is conducted only after multiple logic operations are completed, such as in Hamming code applications.

Accordingly, given that error detection and correction using the Hamming code rely on XOR or XNOR logic gates, a parallel in-memory error handling method for three data bits per BL is proposed using the two-input XNOR logic gate. Fig. 9 shows the parallel error detection method for three-input data bits in 2 × 5 memristors. When the initial data is stored in the memory array, the first parity bit is generated and stored in the P_{15} cell using the two XNOR logic gates. Fig. 9(a) shows a 2 × 5 array of memristors for handling three data bits (D_{11}, D_{12}, D_{13}: '010') in BL_1 and (D_{21}, D_{22}, D_{23}: '011') in BL_2. The parity bit for the first and second bits is generated and stored in the 4th positions (P_{14} and P_{24}) by applying V_{COND} to WL_1 and WL_2, GND to WL_4, and V_{DD} to BL_1 and BL_2. Then, the three-input parity bits are generated using the XNOR logic operation and stored in the 5th positions (P_{15} and P_{25}). The two XNOR logic gates are equivalent to the three-input XNOR gate described in eqn (5) and (6):

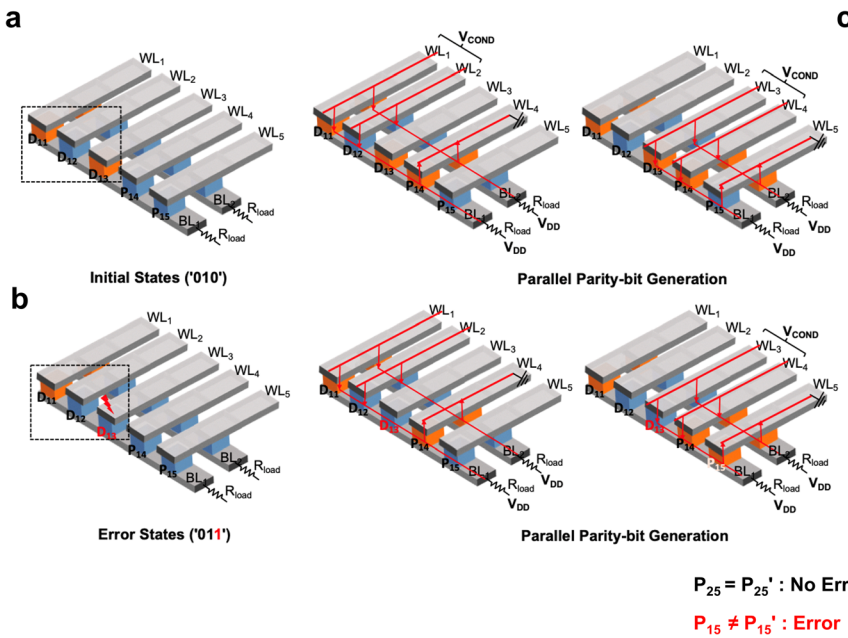
$$P_{14} = \overline{D_{11} \oplus D_{12}} \quad (5)$$

$$P_{15} = \overline{D_{11} \oplus D_{12} \oplus D_{13}} = \overline{P_{14} \oplus D_{13}} \quad (6)$$

Once a single-bit error occurs in the data, error detection can be performed by regenerating the parity bit. Fig. 9(b) shows an example of the error case where the D_{13} cell is flipped from '0' to '1' in BL_1 while the data bit in BL_2 remains unchanged. The error is detected when the regenerated parity bit, P'_{15}, differs from the previous parity bit, P_{15}. Fig. 9(c) summarizes the error detection process for all single-bit error cases. The proposed in-memory parity generation can be performed in parallel and extended to larger array sizes. Additionally, error detection and correction can be carried out using the Hamming code, as discussed in Fig. S9. Furthermore, the proposed THT memristor can be operated in eBRS or eCRS mode in the same array structure, depending on the initial state. As BRS and CRS operations in memristors can perform all 16 Boolean logic functions using logic cascading,[15,41] the proposed XNOR logic based on a THT memristor can be utilized in arithmetic operations to minimize costs.

Comparison of memristive CRS

The general mechanism for conventional CRS is based on the formation of an hourglass-shaped conductive filament (the SET operation) with the rupture of the conductive filament at the thinnest point due to the Joule heating effect.[42] Consequently, the high energy consumption and variation in CRS operation due to heat effects are inevitable, resulting in the memristor's low endurance. In contrast, the proposed THT memristor showed improved stability and power efficiency, with low fabrication cost, when performing CRS operation compared to other devices. Table 1 compares CRS operation in terms of ON/OFF ratio, retention, endurance, power, multilevel capabilities, variability, and cost. The high ON/OFF ratio is related to immunity to variation and multilevel performance. The proposed THT device has a high ON/OFF ratio due to the low HRS current from its self-rectifying characteristics. As the switching mechanism is related to electronic switching that does not involve the Joule heating effect, CRS can be operated with higher endurance than filamentary switching, while maintaining the lowest power consumption. In addition, the THT



Initial Data Bit			1-bit Error Case			Initial Check	
D11	D12	D13	D11'	D12'	D13'	P15	P15'
0	0	0	0	0	1	0	1
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	0	1	1	1	0
0	0	1	1	0	1	1	0
0	1	0	0	1	1	1	0
0	1	0	0	0	0	1	0
0	1	0	1	1	0	1	0
1	0	0	1	0	1	1	0
1	0	0	1	1	0	1	0
1	0	0	0	0	0	1	0
0	1	1	0	1	0	0	1
0	1	1	0	0	1	0	1
0	1	1	1	1	1	0	1
1	0	1	1	0	0	0	1
1	0	1	1	1	1	0	1
1	0	1	0	0	1	0	1
1	1	0	1	1	1	0	1
1	1	0	1	0	0	0	1
1	1	0	0	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	1	0	1	1	0
1	1	1	0	1	1	1	0

Fig. 9 Parallel error detection for three input data bits in 2 × 5 memristors. The XNOR logic gates can be operated in parallel along the BL. (a) Parity-bit generation using two XNOR logic gates (b) The 1-bit error detection process when the BL_1 data is flipped from '010' to '011'. (c) The parity bits for all possible 1-bit error cases for the three data bits.

Table 1 A comparison of various CRS device structures and their electrical characteristics

Ref.	Device structure	On/off ratio	Retention (s)	Endurance	Power (W cm^{-2})	Multilevel	Mechanism	Variability	Cost
43	Au/a-C/a-C:Cu/Au	10	—	10^4	7.5	No	Filamentary	1.5	High
44	ITO/GO/Au NPs/Al_2O_3/Al	10	4×10^3	150	0.03	No	Filamentary	0.3	High
45	TiN/HfO_2/Al_2O_3/TiO_x/IrO_x	10^2	10^4	10^3	—	Yes	Filamentary	1.6	Low
46	Ag/r-TiO_2/FTO	10	10^4	10^2	—	No	Filamentary	0.7	High
47	Pt/TiO_x/TiO_2/TiO_x/Pt	<10	10^6	10^5	700	No	Filamentary	0.3	High
48	Au/$SrFeO_x$/$SrRuO_3$	50	10^3	10^2	400	Yes	Filamentary	0.8	High
This work	Ti/HfO_2/Ti	10^3	3×10^4	10^3	0.006	Yes	Electronic switching	0.3	Low

device exhibited a low variability of 0.3, which is given by the following equation:

$$\frac{\max(I_{on}) - \min(I_{on})}{\text{median}(I_{on})} \quad (7)$$

where I_{on} is the current level of the LRS. In this work, the native oxidation of Ti electrodes reduces the fabrication costs without using noble metals or multiple layers. Therefore, the proposed THT memristor has the potential to be used in CRS applications with low power consumption and variability. Utilizing the multilevel characteristic can expand CRS operation from a 1-bit parity bit to multi-bit parity bit generation to process more data per operation.[13] Although this requires a sensing scheme with additional peripheral circuits, it can increase data reliability in in-memory computing.

Conclusions

In this work, a Ti/TiO_{2-x1}/HfO_y/TiO_{2-x2}/Ti memristor is proposed that exhibits dual-mode switching. The dual-mode switching mechanism is presented based on the anti-serial connection of TL1 and TL2, which act as RS layers, whereas the middle part of HfO_y acts as a blocking layer. The active Ti electrodes play a crucial role in forming the TiO_{2-x1} and TiO_{2-x2} layers and introducing nonstoichiometric interfaces with adjacent HfO_y, which reversibly trap or detrap electrons depending on the polarity. The proposed memristor shows advantages over conventional CRS devices by utilizing eBRS for the memory cell and eCRS for the parity cell during in-memory parity generation. In addition, trap-based eCRS outperforms reported CRS devices based on the filament mechanism in terms of low power consumption and uniformity. Consequently, the dual-mode switching of the proposed device can be utilized further for applications that require XOR operations, such as error correction codes and in-memory Hamming codes.

Methods

Device fabrication and structural analysis

Dot-type: the THT memristor was fabricated in dot-type with a 125 μm × 125 μm × π area. Using an electron-beam evaporator (SORONA, SRN-200), a 50-nm-thick Ti bottom electrode was deposited on a SiO_2/Si substrate. A 10-nm-thick HfO_2 switching layer was deposited *via* plasma-enhanced atomic layer deposition (CN-1, Atomic Premium plus 200) using tetrakis(ethylmethylamino)-hafnium and O_2 plasma as the Hf precursor and oxygen source, respectively, with an O_2 plasma power of 100 W at a substrate temperature of 200 °C. The PEALD sequence was as follows: a 0.5-s Hf-precursor pulse; a 15-s Ar purge; a 7-s O_2 plasma pulse; and a 15-s Ar purge. Then, a 50-nm-thick Ti top electrode was deposited using the e-beam evaporator, followed by lift-off.

1 × 3 THT memristor: a 50-nm-thick Ti layer was deposited on a SiO_2/Si substrate using an electron-beam evaporator (SORONA, SRN-200). Photolithography was performed using a maskless lithography system (NanoSystem Solutions, Inc., DL-1000 HP). A Ti common BL with a line width of 10 μm was formed by dry etching using an ICP etcher (Oxford, Plasma Pro System 100 Cobra). A 10-nm-thick HfO_2 switching layer was deposited under conditions identical to those used for the dot-type cell. Three Ti WLs with a line width of 10 μm were patterned by photolithography, followed by 50-nm-thick Ti layer deposition *via* electron-beam evaporation and subsequent lift-off. The pad-open process used an ICP etcher (Oxford, Plasma Pro system 100 Cobra) with Cl_2 and Ar plasma.

The X-ray photoelectron spectroscopy (XPS) data were acquired with Axis Supra (Kratos, UK) equipment using a monochromatic Al Kα source. The depth profiling was performed *in situ via* Ar^+ ion etching with an acceleration voltage of 5 kV in the XPS chamber. The binding energies were corrected relative to the C 1s signal at 284.5 eV. Transmission electron microscopy (TEM, JEOL, JEM-ARM200F) was used for structure analysis.

Characterization

The electrical properties were measured using a semiconductor parameter analyzer (Hewlett-Packard 4155A and 4155B). A direct current (DC) voltage bias was applied to the top Ti electrode while the bottom Ti electrode was grounded. All electrical measurements were conducted using a LabVIEW-based interface.

Author contributions

Hyun Young Kim designed and conducted the experiments and wrote the manuscript. Taegyun Park designed logic application. Néstor Ghenzi developed a LabVIEW-based measurement program for device characterization. Hyung Jun Park and Dong Hoon Shin contributed to data analysis and provided insightful advice. Dong Yun Kim, Tae Won Park, and Jea Min Cho assisted with data interpretation. Taegyun Park and Cheol Seong Hwang supervised the overall research and manuscript preparation.

Conflicts of interest

There are no conflicts to declare.

Data availability

Raw data are available from the corresponding author upon reasonable request.

All the data that support this study are included in this article and SI. See DOI: https://doi.org/10.1039/d5nh00256g

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