

COMMUNICATION

[View Article Online](#)
[View Journal](#) | [View Issue](#)



Cite this: *Nanoscale Adv.*, 2025, **7**, 7128

Received 6th July 2025
Accepted 8th September 2025

DOI: 10.1039/d5na00659g
rsc.li/nanoscale-advances

Ferroelectric (Fe) devices with 3D trench structures are highly promising to fulfill the demand for high-density and low-power memory applications. However, the potential effects of structure-induced strain on the Fe films' properties remain unclear. This work investigates the homogeneity of HfO_2 -based Fe trench capacitors across 2D planar to 3D trench structures. Systematic device characterization and temperature studies reveal consistent ferroelectric properties of the fabricated devices. Notably, the findings indicate that the large curvature of trench sidewalls minimally affects the ferroelectricity of HfZrO_2 (HZO) thin films, affirming their suitability for 3D structures. Meanwhile, the trench capacitors exhibit good reliability and retention characteristics, making them promising for high-density memory applications. This study provides valuable insights for 3D Fe capacitor development, emphasizing the potential of HfO_2 -based Fe materials to advance memory technology.

Introduction

The rapidly growing data size and data-intensive computing drive the advancement of emerging non-volatile memory devices.^{1–5} As a promising candidate, HfO_2 -based ferroelectric (Fe) RAM (FeRAM) with metal–ferroelectric–metal (MFM) capacitors is undergoing extensive development.^{6–13} By leveraging the doped HfO_2 thin films, the device not only offers remarkable memory characteristics but also demonstrates excellent compatibility with 3D structures like the trench capacitor for conventional DRAM.^{10,14–17} When implemented in FeRAM, the 3D capacitor structure enhances the immunity to parasitic effects and mitigates the device-to-device variation by enlarging the effective device area within the same footprint.¹⁶ With these advantages over the planar structure, stable memory operation was also successfully demonstrated in the large-scale high-density FeRAM array.¹⁷

Department of Electrical and Computer Engineering, National University of Singapore, 4 Engineering Drive 3, Singapore 117583, Singapore. E-mail: elegong@nus.edu.sg
† Z. Zheng and Z. Zhou contributed equally to this work.

Investigating the impact of 3D trench structures on HfO_2 -based ferroelectric capacitors

Zijie Zheng, † Zuopu Zhou, † Yue Chen, Xiaolin Wang, Leming Jiao, Dong Zhang, Yang Feng and Xiao Gong*

However, the ferroelectricity of the HfO_2 -based thin films could be sensitive to in-plane strain.^{18,19} Unlike the Fe layer of the planar capacitors, thin films deposited for the 3D capacitors may experience different strains induced by the sidewall curvature of the small trench structure. Although 3D Fe capacitors demonstrated previously still exhibit good ferroelectricity,¹⁷ and the slight curvature resulting from the flexible substrate does not significantly affect the film characteristics,²⁰ how the properties of the HfO_2 -based Fe capacitors are affected by the much larger curvature of the trench sidewall remains unclear (Fig. 1). Moreover, a previous study on perovskite ferroelectric materials has reported evident degradation of ferroelectricity in the Fe trench capacitors.²¹ Whether HfO_2 -based Fe capacitors suffer from the same issue is still unexplored. Additionally, the cylindrical surfaces not only affect the strain during the device fabrication but also induce strain when the operation temperature changes. This potential effect on the device operation requires further evaluation. In this context, a systematic investigation and comparison of the HfO_2 -based Fe capacitors with 3D trench structures are urgent to better understand the film properties and assist the development of high-density FeRAM. However, due to the small electrical signals falling below the noise margins of most measurement tools, conducting electrical measurements (e.g., P – V , C – V , endurance, and retention measurements) on a single ferroelectric trench capacitor with sub-micrometer dimensions is challenging.

In this work, we experimentally investigated the impact of 3D trench structures on the ferroelectricity of HfO_2 -based MFM Fe capacitors through extensive electrical characterization. To increase the electrical signals, a test structure was designed to parallelly connect a large number of small trenches. Additionally, a capacitance-based calibration method was developed to extract the planar area and effective trench area in the structure. On this test platform, the effects of strain induced by thermal expansion during both the annealing process and varying-temperature operation were considered and studied for the planar MFM capacitors and 3D trench capacitors with different



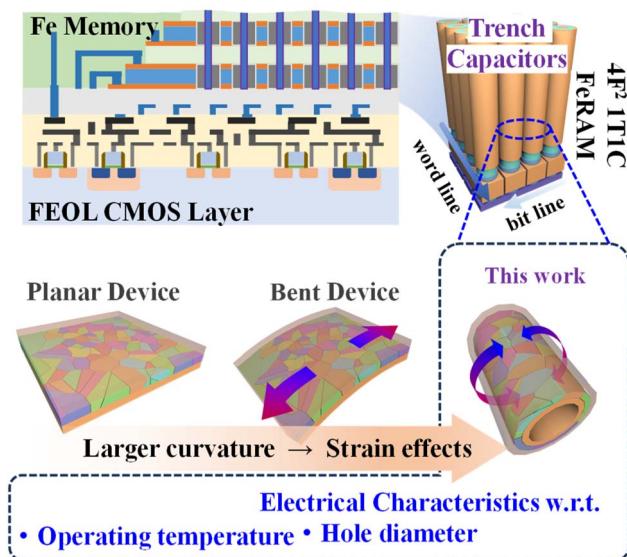


Fig. 1 Schematic of 4F² 1T1C FeRAM as a promising high-density embedded memory, where Fe 3D trench capacitors are implemented. Their electrical characteristics with varying hole diameters and at different operating temperatures are the highlights of this work.

hole diameters for the first time. By carefully evaluating the electrical characteristics of the fabricated devices, we confirm the consistent behavior of HfO₂-based ferroelectric films in both planar and trench structures, highlighting their potential for implementation in 3D architectures aimed at high-density integration.

Device fabrication

We have prepared four controlled splits of trench capacitor arrays with different hole diameters, denoted as D1 to D4. Fig. 2(a) shows the cross-sectional SEM images of individual

holes in each split, together with their approximate outer hole diameters (D) marked. The fabrication started with SiO₂ (500 nm) on a high-resistance Si substrate with acetone/IPA cleaning. First, the trench arrays were patterned using electron beam lithography (EBL) and then formed by a dry etching process, where the hole diameter was defined. During the dry etching, a Cr hard mask was adopted to improve the etch profile, which was defined and etched with a negative EBL resist AR-N 7520. On the developed structures of SiO₂, we further fabricated the MFM trench capacitors. Here, both TiN and Hf_{0.5}Zr_{0.5}O₂ (HZO) were deposited by atomic layer deposition (ALD) to ensure conformality. TiN thin films were deposited by Plasma-Enhanced ALD (PEALD) at 350 °C using TiCl₄ as the precursor and plasma-activated N₂/H₂ as the nitrogen source. As for the ferroelectric layer, it was deposited using thermal ALD at 280 °C, with TDMA-Hf and TDMA-Zr as the precursors and O₃ as the oxidant. As shown in Fig. 2(b) and (c), the bottom electrode (BE) and top electrode (TE) were patterned and etched separately after their deposition, whose overlapping region contains multiple parallel-connected 3D capacitor cells. To open the bottom electrodes, an additional dry etching process was induced. At this stage, all the devices would be available for electrical characterization, although they are not showing any ferroelectric behavior due to the non-ferroelectric phase of the as-deposited HZO layer. At last, all samples underwent a 500 °C rapid thermal annealing (RTA) for 60 seconds in the N₂ atmosphere, to activate the ferroelectricity by inducing a phase transition. The TEM images confirm the good coverage of the MFM layer stack on the trench sidewall. Additionally, planar capacitors were also fabricated simultaneously on the same wafer as a reference. Overall, 6 different types of devices were realized, as illustrated in Fig. 2(c), including two types of planar capacitors, one formed on top of the substrate and the other at the bottom of the etched trench, and four types of 3D capacitors with different hole diameters, corresponding to splits D1 to D4.

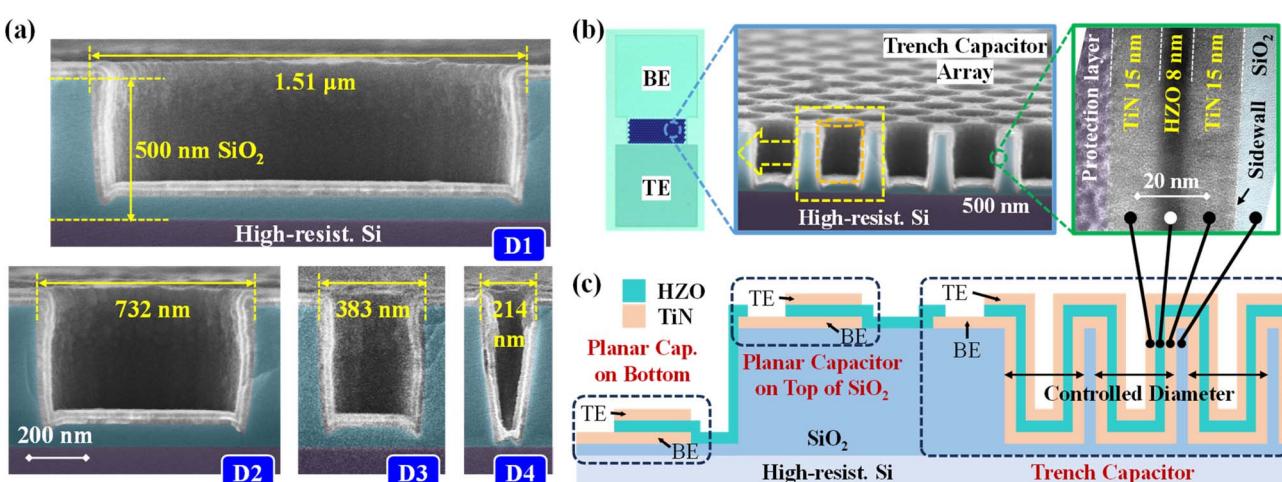


Fig. 2 (a) Cross-sectional SEM images of the holes within splits D1 to D4. (b) Top-view image of the fabricated device with a zoomed-in SEM image of the trench array and its cross-section from a tilted angle. The layer thicknesses are further confirmed by TEM. (c) Schematic diagram of the devices fabricated simultaneously, including two types of planar capacitors and four types of trench capacitors.

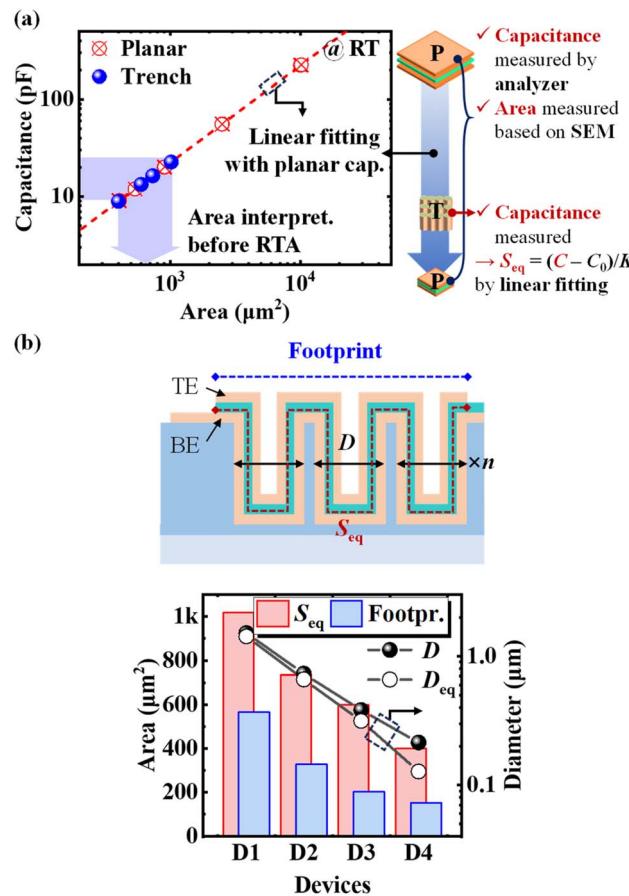


Fig. 3 (a) Measured C of planar devices before RTA in relation to their physical areas. S_{eq} of each trench capacitor split can thus be accurately obtained from the linear fitting with their C measured simultaneously. (b) S_{eq} , footprints, and hole diameters of each split.

Device characterization

Interpretation of effective areas

Accurately interpreting the equivalent area (S_{eq}) is one of the critical prerequisites for trench Fe capacitor characterization. Due to the topological complexity, direct measurement or mathematical calculation could be difficult to implement with high accuracy. In this study, an indirect method based on the measured device capacitance (C) was applied to normalize the polarization for a fair comparison. Specifically, leveraging the reference planar devices with determined physical areas (S), the relation between C and S should be obtained first with a linear fitting. Here, the C of all devices was measured with a Keithley 4200A-SCS parameter analyzer, and the S of planar devices was measured based on top-view SEM. Furthermore, S_{eq} of each trench capacitor can be extrapolated according to the measured C , as shown in Fig. 3(a). Note that all the C were obtained before RTA, where ferroelectricity of HZO was not present, to decouple the Fe effects from the S_{eq} interpretation. The bar charts in Fig. 3(b) depict the S_{eq} and footprints of each split. The difference between the red and blue bars can represent the area induced by the sidewall region, which occupies a considerable

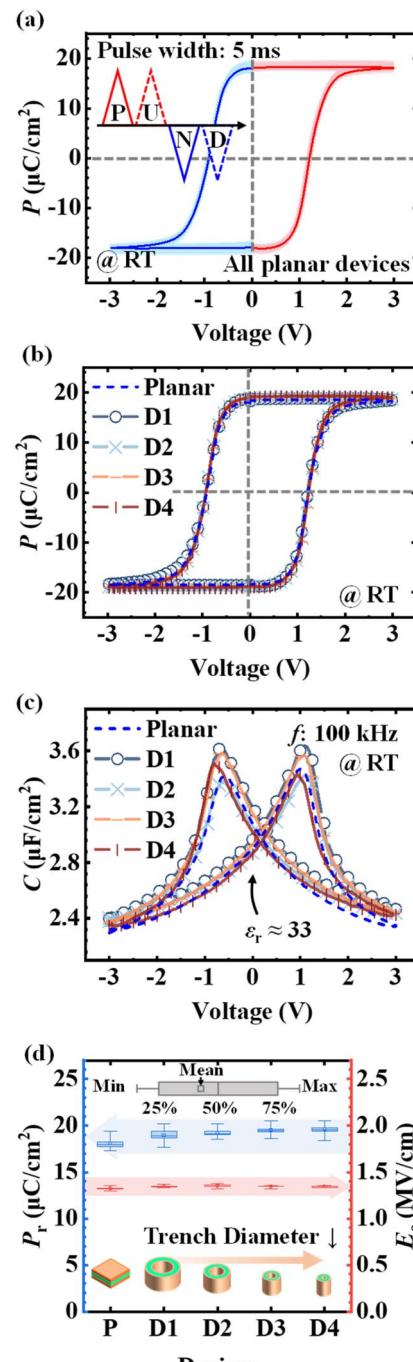


Fig. 4 (a) The P - V (after extracting the non-Fe switching response) curves obtained with the PUND measurement on planar capacitors. (b) The P - V curves of planar and trench capacitors, showing a negligible difference. (c) The C - V curves of the same devices, indicating that ϵ_r of the thin film also varies insignificantly. (d) Box chart summarizing the P_r and E_c extracted from multiple devices.

proportion in every split. In the figure, the D values are also plotted and compared with the equivalent hole diameters (D_{eq}), which are calculated using eqn (1):

$$D_{\text{eq}} = \frac{S_{\text{eq}} - \text{footpr.}}{\pi n H} \quad (1)$$

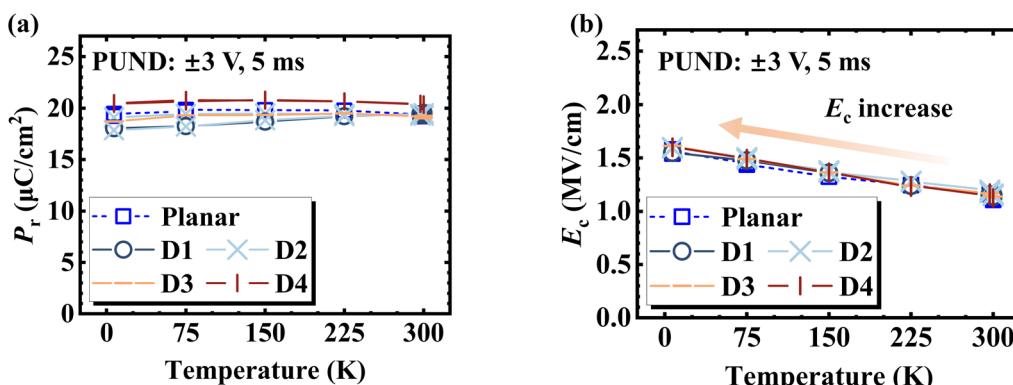


Fig. 5 Temperature dependence of (a) P_r and (b) E_c from PUND measurement of the Fe capacitors with different structures. No evident deviation among the splits is observed across a wide operating temperature range from 7 K to RT.

where n is the number of parallel-connected trench capacitors; H is the depth of the trench. D_{eq} is slightly smaller than D (the outer diameter) as expected.

Electrical characteristics

Polarization–voltage (P – V) measurements of the fabricated Fe capacitors were conducted with the PUND method, involving triangular waveforms with a pulse width of 5 ms, aimed at subtracting the paraelectric counterparts.⁸ Prior to measurement, all devices underwent a wakeup process with 10^3 pre-cycling (100 kHz, ± 3 V). Fig. 4(a) showcases P – V curves of planar devices with different areas, where both two types of devices aforementioned are included. The curves for each device are plotted in light colors, while the prominent red and blue curves represent their averages. The results indicate good uniformity of the devices. Meanwhile, the characteristics of the planar devices on the etched SiO_2 surface show no difference from the others.

Fig. 4(b) further provides the P – V curves of trench capacitors with different hole diameters, where the P of each split is normalized according to the extracted S_{eq} . The curves overlap with each other, indicating an insignificant change in the device ferroelectricity across 2D to 3D structures with different hole

diameters. In addition, we examined the devices' C – V relations after RTA, which are also close to each other after normalization using S_{eq} , as depicted in Fig. 4(c).

Fig. 4(d) summarizes the P_r and E_c from multiple devices. First, planar capacitors and 3D ones with different hole diameters all exhibit highly consistent E_c . On the other hand, from planar to 3D capacitors with gradually shrinking hole diameters, their P_r show a slightly increasing trend. Thus, we conclude that the Fe properties of TiN/HZO/TiN capacitors can be maintained in the trench structures with diameters down to ~ 200 nm, as presented in this work. Compared with PZT-based devices, such homogeneity across planar to highly curved structures stands for a significant advantage, which allows high-density memory applications with promising 3D structures. The slight increase in the ferroelectricity can be attributed to the increased radical stress in the small trench structures, which facilitates the ferroelectric orthorhombic phase and improves the polarization orientation.²²

Temperature dependence and reliability

The difference in the curvature of the cylindrical surfaces controlled by hole diameters not only affects the strain during the device fabrication (e.g., during cooling of the RTA process)¹⁹

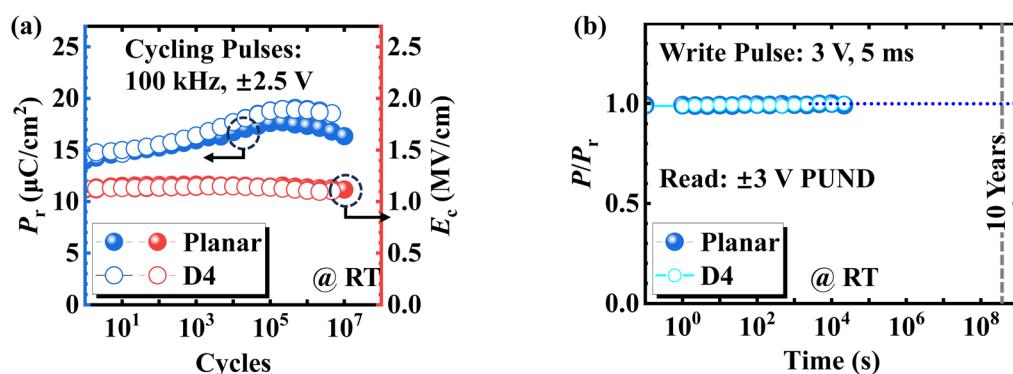


Fig. 6 (a) Endurance of the devices with 100 kHz, ± 2.5 V cycling pulses, showing a wake-up of P_r followed by fatigue. (b) Retention of the Fe capacitors, where the extrapolated retention time of more than 10 years can be obtained. All the devices are validated to ensure similar reliability.

but also may induce extra strain when the operation temperature changes. Therefore, we further conducted the measurements at varying temperatures to investigate the potential effects brought by the device structure. Fig. 5 depicts the device P_r and E_c in relation to the operating temperature ranging from 7 K to room temperature (RT). The results indicate that the differences between the devices of each split are still not evident from the strain effects induced by varying operation temperatures. The observed decrease in E_c with increasing temperature can be explained by thermally assisted domain nucleation and wall motion, which reduce the effective switching barrier, consistent with previous reports.^{23,24}

At last, we compare the device reliability with both 2D and 3D structures. It can be clearly observed that there are intrinsic wake-up and fatigue procedures before hard breakdown, as we apply 2.5 V 100 kHz cycling voltage pulses, as presented in Fig. 6(a). Considering the device variation, the slight difference in the results does not clearly demonstrate the effect of trench structure on the endurance characteristics, suggesting that the potential effects may be insignificant. On the other hand, both devices exhibit excellent retention without P_r degradation as well, and the extrapolated retention time is more than 10 years, as depicted in Fig. 6(b).

Conclusions

In conclusion, our study examines the behavior of HfO_2 -based Fe capacitors across diverse 2D and 3D trench structures. Through systematic characterization of fabricated devices, we confirm the insignificant change in ferroelectric properties of trench capacitors with varying hole diameters. The results indicate that the strain introduced by the large curvature of the trench sidewall does not observably affect the performance of HZO films. By comprehensive comparison of the Fe capacitor behavior with different structures, the study further proves the suitability of HfO_2 -based ferroelectric materials for 3D structures and their potential for high-density memory applications.

Conflicts of interest

There are no conflicts to declare.

Data availability

The data supporting this article have all been presented in the manuscript.

Acknowledgements

This work was supported by the Singapore Ministry of Education (Tier 2) under the grant MOE-T2EP50221-0008 and in part by the Singapore Ministry of Education (Tier 1) under grants A-8002150-00-00 and A-8001168-00-00.

References

- 1 X. Yin, et al., Ferroelectric compute-in-memory annealer for combinatorial optimization problems, *Nat. Commun.*, 2024, **15**(1), 2419, DOI: [10.1038/s41467-024-46640-x](https://doi.org/10.1038/s41467-024-46640-x).
- 2 W. Wan, et al., A compute-in-memory chip based on resistive random-access memory, *Nature*, 2022, **608**(7923), 504–512, DOI: [10.1038/s41586-022-04992-8](https://doi.org/10.1038/s41586-022-04992-8).
- 3 L. Jiao et al., First BEOL-compatible IGZO ferroelectric-modulated diode with drastically enhanced memory window: Experiment, modeling, and deep understanding, in *2023 Int. Electron Devices Meeting (IEDM)*, 2023, pp. 1–4, DOI: [10.1109/IEDM45741.2023.10413793](https://doi.org/10.1109/IEDM45741.2023.10413793).
- 4 Z. Zheng, et al., BEOL-compatible MFMIS ferroelectric/anti-ferroelectric FETs—Part I: Experimental results with boosted memory window, *IEEE Trans. Electron Devices*, 2024, **71**(3), 1827–1833, DOI: [10.1109/TED.2023.3326116](https://doi.org/10.1109/TED.2023.3326116).
- 5 Z. Zhou, et al., Inversion-type ferroelectric capacitive memory and its 1-Kbit crossbar array, *IEEE Trans. Electron Devices*, 2023, **70**(4), 1641–1647, DOI: [10.1109/TED.2023.3243556](https://doi.org/10.1109/TED.2023.3243556).
- 6 J. Okuno et al., SoC compatible 1T1C FeRAM memory array based on ferroelectric $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$, in *2020 Symp. VLSI Technol.*, 2020, pp. 1–2, DOI: [10.1109/VLSITechnology18217.2020.9265063](https://doi.org/10.1109/VLSITechnology18217.2020.9265063).
- 7 U. Schroeder, et al., The fundamentals and applications of ferroelectric HfO_2 , *Nat. Rev. Mater.*, 2022, **7**(8), 653–669, DOI: [10.1038/s41578-022-00431-2](https://doi.org/10.1038/s41578-022-00431-2).
- 8 J. Zhou, et al., Temperature dependence of ferroelectricity in Al-doped HfO_2 featuring a high P_r of $23.7 \mu\text{C}/\text{cm}^2$, *IEEE Trans. Electron Devices*, 2020, **67**(12), 5633–5638, DOI: [10.1109/TED.2020.3032350](https://doi.org/10.1109/TED.2020.3032350).
- 9 N. Haratipour, et al., Hafnia-based FeRAM: A path toward ultra-high density for next-generation high-speed embedded memory, in *2022 Int. Electron Devices Meeting (IEDM)*, 2022, pp. 6.7.1–6.7.4, DOI: [10.1109/IEDM45625.2022.10019560](https://doi.org/10.1109/IEDM45625.2022.10019560).
- 10 S.-C. Chang, et al., FeRAM using anti-ferroelectric capacitors for high-speed and high-density embedded memory, in *2021 Int. Electron Devices Meeting (IEDM)*, 2021, pp. 33.2.1–33.2.4, DOI: [10.1109/IEDM19574.2021.9720510](https://doi.org/10.1109/IEDM19574.2021.9720510).
- 11 X. Li, et al., Re-annealing-induced recovery in 7 nm $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ ferroelectric film: phase transition and non-switchable region repair, *IEEE Electron Device Lett.*, 2023, **44**(8), 1288–1291, DOI: [10.1109/LED.2023.3287874](https://doi.org/10.1109/LED.2023.3287874).
- 12 J. Zhou, et al., Al-doped and deposition temperature-engineered HfO_2 near morphotropic phase boundary with record dielectric permittivity (~ 68), in *2021 Int. Electron Devices Meeting (IEDM)*, 2021, pp. 13.4.1–13.4.4, DOI: [10.1109/IEDM19574.2021.9720632](https://doi.org/10.1109/IEDM19574.2021.9720632).
- 13 Z. Fu, et al., Novel asymmetric operation scheme for HfO_2 -based FeRAM based on reconstruction of ferroelectric dynamics impacts, *IEEE Electron Device Lett.*, 2024, **45**(1), 20–23, DOI: [10.1109/LED.2023.3330994](https://doi.org/10.1109/LED.2023.3330994).



14 M. H. Park, et al., Ferroelectricity and antiferroelectricity of doped thin HfO_2 -based films, *Adv. Mater.*, 2015, **27**(11), 1811–1831, DOI: [10.1002/adma.201404531](https://doi.org/10.1002/adma.201404531).

15 A. M. Walke, et al., La-doped HZO-based 3D-trench metal-ferroelectric-metal capacitors with high-endurance ($>10^{12}$) for FeRAM applications, *IEEE Electron Device Lett.*, 2024, **45**(4), 578–581, DOI: [10.1109/LED.2024.3368225](https://doi.org/10.1109/LED.2024.3368225).

16 P. Polakowski et al., Ferroelectric deep trench capacitors based on Al: HfO_2 for 3D nonvolatile memory applications, in *2014 Int. Mem. Workshop (IMW)*, 2014, pp. 1–4, DOI: [10.1109/IMW.2014.6849367](https://doi.org/10.1109/IMW.2014.6849367).

17 N. Ramaswamy et al., NVDRAM: A 32Gb dual layer 3D stacked non-volatile ferroelectric memory with near-DRAM performance for demanding AI workloads, in *2023 Int. Electron Devices Meeting (IEDM)*, 2023, pp. 1–4, DOI: [10.1109/IEDM45741.2023.10413848](https://doi.org/10.1109/IEDM45741.2023.10413848).

18 H. Kim, et al., A new approach to achieving strong ferroelectric properties in $\text{TiN}/\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2/\text{TiN}$ devices, *Nanotechnology*, 2020, **32**(5), 055703, DOI: [10.1088/1361-6528/abc115](https://doi.org/10.1088/1361-6528/abc115).

19 R. Cao, et al., Effects of capping electrode on ferroelectric properties of $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$ thin films, *IEEE Electron Device Lett.*, 2018, **39**(8), 1207–1210, DOI: [10.1109/LED.2018.2846570](https://doi.org/10.1109/LED.2018.2846570).

20 R. Han, et al., The effect of stress on HfO_2 -based ferroelectric thin films: A review of recent advances, *J. Appl. Phys.*, 2023, **133**(24), 240702, DOI: [10.1063/5.0146998](https://doi.org/10.1063/5.0146998).

21 J.-M. Koo et al., Fabrication of 3D trench PZT capacitors for 256Mbit FRAM device application, in *2005 Int. Electron Devices Meeting*, 2005, pp. 4–343, DOI: [10.1109/IEDM.2005.1609345](https://doi.org/10.1109/IEDM.2005.1609345).

22 W. Li, et al., Stress modulation of hafnium-based ferroelectric material orientation in 3D cylindrical capacitor, *AIP Adv.*, 2025, **15**(2), 025109, DOI: [10.1063/5.0230610](https://doi.org/10.1063/5.0230610).

23 D. Zhou, et al., Electric field and temperature scaling of polarization reversal in silicon-doped hafnium oxide ferroelectric thin films, *Acta Mater.*, 2015, **99**, 240–246, DOI: [10.1016/j.actamat.2015.07.035](https://doi.org/10.1016/j.actamat.2015.07.035).

24 C. Sun, et al., Temperature-dependent operation of InGaZnO ferroelectric thin-film transistors with a metal-ferroelectric-metal-insulator-semiconductor structure, *IEEE Electron Device Lett.*, 2021, **42**(12), 1786–1789, DOI: [10.1109/LED.2021.3121677](https://doi.org/10.1109/LED.2021.3121677).

