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Performance enhancement of InSnZnO thin-film transistors by modifying the dielectric–semiconductor interface with colloidal quantum dots†

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Thin film transistors (TFTs) with InSnZnO (ITZO) and Al_2O_3 as the semiconductor and dielectric layers, respectively, were investigated, aiming to elevate the device performance. Chemically synthesized $CuInS_2$/ZnS core/shell colloidal quantum dots (QDs) were used to passivate the semiconductor/dielectric interface. Compared with the pristine device, the device with the integrated QDs demonstrates remarkably improved electrical performance, including a higher electron mobility and a lower leakage current. Moreover, the integration of QDs largely mitigates hysteresis in the bidirectional transfer characteristics of the device. Improved negative bias stress stability is also observed in the device with QDs. The performance enhancement is ascribed to the reduction of the trap states induced by the defects in Al_2O_3, and the screening of electrical dipoles at the Al_2O_3/ITZO interface. This work proposes a new strategy to passivate the semiconductor/dielectric interface, which not only improves TFT performance, but also holds potential for optoelectronic applications.

Introduction

Thin film transistors (TFTs) are fundamental components in a wide array of electronic applications, including display technologies, sensors, and flexible electronics. The continuous advancement of TFT technology necessitates the exploration of novel materials and structures to enhance device performance and reliability. Indium tin zinc oxide (ITZO) offers several advantages that make it a compelling choice of semiconductor for TFTs. Firstly, ITZO TFTs exhibit high carrier mobility, facilitated by the direct spatial overlap between the 5s orbitals of Sn and In, which enhances the movement of electron carriers and improves device performance.[1] Secondly, ITZO possesses a wide bandgap, enabling high transparency within the visible light range, which makes it suitable as a transparent semiconductor layer in displays and other optoelectronic devices.[2–4] Furthermore, ITZO TFTs can be seamlessly integrated into the commercially successful IGZO TFT production lines without incurring additional costs, thus facilitating commercialization.[2] However, achieving low-voltage operation in portable and wearable electronic devices, which is crucial due to limited battery capacity, remains a challenge for oxide semiconductor TFTs. The key strategy for maintaining good device performance, such as high field-effect mobility and stability, while reducing operating voltage, is the incorporation of high-*k* gate dielectrics.[5–7] High-*k* dielectric materials, including Al_2O_3,[8,9] Ta_2O_5,[10] HfO_2,[11] and ZrO_2,[12] and their stacking[13] provide high capacitance, allowing TFTs to operate at lower voltages and thereby reducing power consumption in logic circuits.[14,15] Moreover, high-*k* dielectrics offer a larger physical thickness at the same effective oxide thickness (EOT) compared to traditional SiO_2, effectively suppressing tunnelling effects and reducing leakage current.[16,17] The high-*k* dielectrics are normally grown at relative low temperatures, inducing defects and doping.[18] For example, an Al_2O_3 dielectric layer grown by low temperature atomic layer deposition (ALD) usually has oxygen vacancies (V_O) and high levels of impurities, such as H, C and OH^- residues.[19–22]

The overall performance and lifespan of TFTs are also influenced by their stability and reliability. Factors such as device structure, dielectric materials, and manufacturing processes play critical roles in the electrical performance and stability of oxide semiconductor TFTs. Reliability tests for evaluating TFTs include threshold voltage shifts caused by hysteresis effects, observed in both organic thin film transistors (OTFTs) and metal oxide semiconductor field effect transistors (MOSFETs). Maintaining good bias stability under positive bias stress (PBS) and negative bias stress (NBS) is essential for oxide

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semiconductor TFTs. Bias instability and hysteresis effects are generally attributed to charge trapping at the semiconductor/dielectric interface or the generation of defects/traps in the semiconductor layer.[23,24] Oxygen-related defects, such as oxygen vacancies and weakly bonded oxygen, are closely linked to these instabilities.[24,25] Additionally, water and oxygen molecules absorbed from the air can create traps in the channel layer.[26] Methods such as thermal annealing,[2] doping,[27,28] and dual channel layers[29–31] are commonly used to reduce defects and improve stability issues.

To address stability issues caused by interface defects, we propose using quantum dots to passivate the interface. Here, we report ITZO TFTs based on an Al_2O_3 dielectric layer with a $CuInS_2/ZnS$ core/shell quantum dots (CIS/ZnS QDs) passivation layer. The low-cost spin-coating method was used to prepare quantum dot films in a top-gate configuration TFT. The results show that compared to pure ITZO TFTs, those passivated with quantum dots exhibit higher mobility, less electrical hysteresis, and improved bias stability. These performance enhancements reveal that the colloidal QDs can effectively improve the interface between ITZO and Al_2O_3. In light of the diverse range of QD types, this approach holds significant potential for advancing low-power, high-performance portable and wearable electronic and optoelectronic devices.

Experimental

CIS/ZnS QD synthesis and characterization

The CIS/ZnS QDs used in the study were prepared by topotactic Cu^+ to In^{3+} cation exchange in template $Cu_{2−x}S$ nanocrystals followed by heteroepitaxial overgrowth of a ZnS shell according to the previously reported procedures.[32] The detailed synthesis process is described in the ESI.† As can be seen in Fig. 1a, the product QDs are rather monodisperse and display a pyramidal shape with an average size of ∼11.1 nm. High-resolution transmission electron microscopy (TEM) images show that the QDs exhibit clear lattice fringes. The corresponding fast Fourier transform analysis of a single nanocrystal confirms that the particle has a hexagonal wurtzite crystal structure, which is highly consistent with the results of the selected area electron diffraction patterns shown in Fig. 1c and d. The diffraction pattern slightly shifts to higher angles which is likely due to a strong lattice stress caused by an ultra-thick ZnS shell (∼ten monolayers of ZnS).

Device fabrication and characterization

The ITZO TFTs studied here have a top-gate–bottom contact structure, as shown in Fig. 2a. Specifically, on a clean glass substrate, gold source and drain electrodes were deposited by thermal evaporation through a shadow mask, defining a source–drain channel with a width/length ratio of 2/0.4 mm. Then a 12 nm-thick ITZO thin film was deposited *via* radiofrequency (RF) magnetron sputtering (RF power = 60 W, pressure = 0.4 Pa, and $O_2 : Ar = 5 : 12$) using ceramic targets ($In_2O_3 : SnO_2 : ZnO = 1 : 2 : 1$ at%). Next, the ITZO film was annealed at 350 °C for 2 min using a rapid thermal process (RTP) oven. After
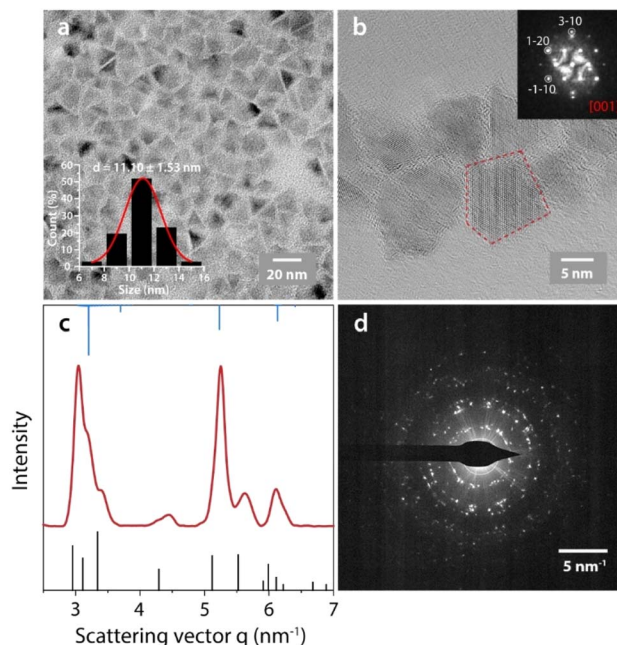

Fig. 1 Structure characterization of the product CIS/ZnS core/shell nanocrystals. (a) Conventional TEM image of CIS/ZnS quantum dots. (b) High-resolution TEM image and the corresponding Fourier transform pattern of CIS/ZnS QDs. The Fourier transform pattern is indexed to the [001] projection of hexagonal wurtzite $CuInS_2$. (c) One dimensional electron diffraction pattern obtained by the azimuthal integration of the two-dimensional electron diffraction pattern shown on the right side. The black line represents the diffraction peak of hexagonal wurtzite CIS (PDF No. 97-016-3489) and the blue line represents the diffraction peak of hexagonal wurtzite ZnS (PDF No. 97-004-2819). (d) Selected area electron diffraction pattern of the product CIS/ZnS nanocrystals.

that, the colloidal QD solution was spin-coated atop at a spinning speed of 3000 rpm for 30 seconds, forming a QD film with a thickness of about 12 nm. Then a 22 nm-thick Al_2O_3 film was grown at 150 °C by the atomic layer deposition (ALD) method,

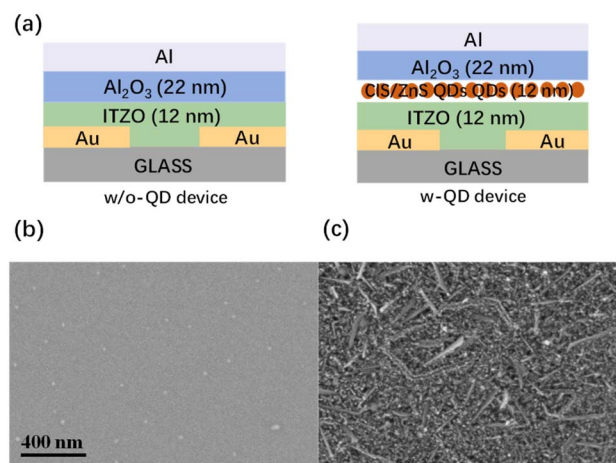**Fig. 2** (a) Schematic of the device structures. SEM images of Al_2O_3 (b) and QDs films (c).

using trimethylaluminum (TMA) and H_2O as precursors. Finally, an Al film was thermally evaporated on the Al_2O_3 film as the gate electrode. For comparison, a device without the QDs was also fabricated using the same process but with the QD film deposition step omitted. Hereafter, the ITZO TFT with QDs is referred to as the w-QD device, and the one without QDs is referred to as the w/o-QD device. The SEM images of the Al_2O_3 film and the QD film surfaces were characterized and are shown in Fig. 2b and c, respectively. The Al_2O_3 film demonstrates a flat, smooth and uniform surface. In contrast, the surface of the QD film is very rough. There are stripe-like structures in the QD film, with lengths of hundreds of nanometers and widths of tens of nanometers, which are attributed to the aggregation of quantum dots. They exhibit the different dielectric/semiconductor interfaces of the w-QD and w/o-QD devices.

The electrical characterization of the devices was performed using a combination of a probe station and a Keysight B2902B instrument in an inert gas glove box (nitrogen purity >99.99%). The capacitance measurement was conducted using a Keysight E4990A impedance analyzer.

Results and discussion

Electrical characterization was first conducted to investigate the effect of QDs on the device performance. Fig. 3a shows the representative transfer characteristics of the two types of devices under linear ($V_{DS} = 0.5$ V) and saturation ($V_{DS} = 5$ V) conditions. The ITZO TFTs exhibit a typical n-channel conduction behaviour. The w-QD device demonstrates a higher current than the w/o-QD device. Fig. 3b shows the leakage current (I_{GS}) of the two different devices. With the integration of the QDs, the leakage current gets apparently suppressed. Fig. 3c shows the output characteristics of the two devices. They verify the good ohmic contact between the electrode and ITZO, as well as the improvement of the channel current with the integration of the QDs, which is consistent with

the transfer characteristics. Eight w-QD devices and six w/o-QD devices were fabricated and characterized. The results corroborate the overall improvement in the device with the integration of the QDs. Two capacitors with different structures, $Al/Al_2O_3/Al$ and Al/Al_2O_3-QDs/Al, were fabricated. Their capacitance–voltage characteristics were measured, and their dielectric constants were calculated, as shown in Fig. S1.† The dielectric constant of the Al_2O_3 and Al_2O_3-QDs hybrid films were ascertained to be 5.59 and 7.37, respectively. On this basis, the electron mobilities of these devices are extracted and shown in Fig. 3d. It can be seen that compared to the w/o-QD device, the w-QD device exhibits higher linear and saturation mobilities. Please note that the mobilities observed in our devices are lower than those reported for some ITZO TFTs,[2,18,27,31,33–37] which may be due to the suboptimal quality of the ITZO films. However, given that all devices were fabricated using the same procedure, the comparison between the devices with and without QD passivation remains valid and meaningful.

To realize a reliable logic function, a TFT is supposed to work stably under different bias conditions including sweep direction and duration. To investigate the influence of QDs on the stability of ITZO TFTs, we conducted two tests. First, we performed repeated tests on both devices across different gate voltage ranges. The gate-source voltage (V_{GS}) was set to undergo bidirectional sweeps from negative to positive and back to negative. The sweep ranges included ten sets of tests, spanning from −1 V to 1 V, −2 V to 2 V, −3 V to 3 V, and so on, up to −10 V to 10 V. For the linear state, the V_{DS} was set to 0.5 V, and for the saturation state, V_{DS} was set to 10 V. The resulting transfer characteristic curves of the w/o-QD and w-QD devices are shown
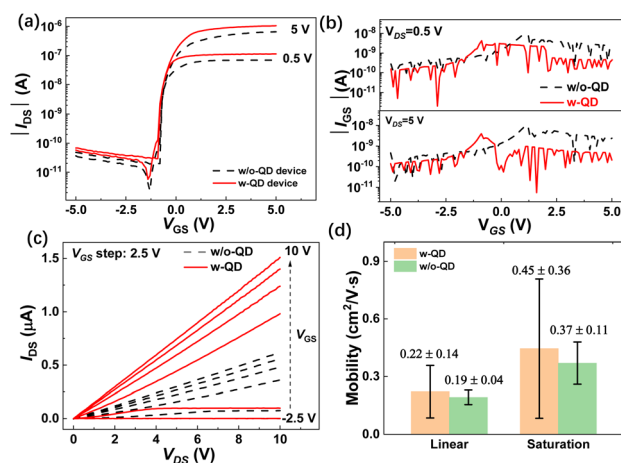
Fig. 3 Comparisons of the electrical characteristics of the w-QD and w/o-QD devices. (a) transfer characteristics; (b) leakage currents; (c) output characteristics; (d) electron mobilities. The statistical mobility data are obtained from eight w-QD and six w/o-QD devices.
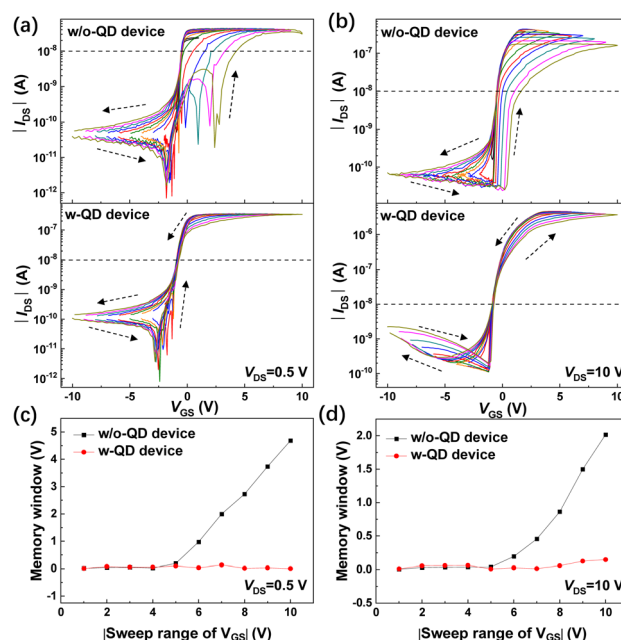
Fig. 4 Linear (a) and saturation (b) transfer characteristics of the w/o-QD and w-QD devices. The dashed lines indicate the level of I_{DS} at which the memory window value is extracted; memory windows extracted from the linear (c) and saturation (d) transfer curves.

in Fig. 4a and b. Regarding threshold voltage stability, the w/o-QD device in the saturation state exhibits a gradual rightward shift in the threshold voltage as the V_{GS} sweep range increases. In contrast, the w-QD device maintains a stable threshold voltage, indicating that QD passivation can effectively enhance threshold voltage stability. The memory window, an important indicator of the hysteresis effect, was quantitatively evaluated by selecting the difference between the two V_{GS} values corresponding to $I_{DS} = 1.0 \times 10^{-8}$ A. The memory windows obtained are plotted along with the sweeping range in Fig. 4c and d. The results indicate that for the w/o-QD device, regardless of whether it is in the linear or saturation state, when the V_{GS} sweep range exceeds −5 V to 5 V, the memory window increases linearly, reaching 4.7 V (linear) and 2.0 V (saturation) at the maximum V_{GS} sweep range (−10 V to 10 V). Conversely, for the w-QD device, under all test conditions, the maximum memory window is only about 0.1 V.

The counterclockwise hysteresis window observed suggests the presence of deep traps resembling receptors near the Al_2O_3/ITZO interface. As the scanning process starts, trapped electrons accumulate at the Al_2O_3/ITZO interface and screen the external electric field, causing a positive shift in the threshold voltage. As the scanning process reversed, the accumulated electrons started to release, inducing a negative shift in the threshold voltage.[38,39] Together, they generate a counterclockwise hysteresis. Further studies indicate that electrical dipoles in the channel/dielectric layer also contribute to the hysteresis observed in TFTs.[40] Thus, it is inferred that the Al_2O_3/QDs/ITZO interface can reduce trap density, likely due to a reduction in carbon-related impurities.[2,41] Meanwhile, the existence of the QD layer can screen the electrical dipoles at the Al_2O_3/ITZO interface, significantly mitigating the hysteresis effect during bidirectional scanning.

Secondly, negative bias stress (NBS) and positive bias stress (PBS) tests were performed on both w/o-QD and w-QD devices. During these tests, the transfer characteristics of the devices were measured after applying a gate bias stress of −10 V for NBS and 10 V for PBS, each applied for varying durations. Fig. 5a and

b display the resulting transfer characteristics of the w/o-QD (top) and w-QD (bottom) devices following NBS and PBS operations, respectively. Despite the current reduction phenomenon, both PBS tests of the w/o-QD device and w-QD device demonstrate good electrical performance, which can be ascribed to that the ionic bonding properties of Al_2O_3 that lead to the reduction of electronic traps.[42] Nevertheless, under NBS stability testing, it can be clearly observed that the current of the w/o-QD device gradually decreases with the accumulation of bias time. While the w-QD device can resist the negative bias effect after introducing QDs, maintaining the stability of the I_{DS} current, which proves that the introduction of QDs can significantly improve the stability of the device. It has been shown that NBS elevates the Fermi level in ITZO, leading to a leftward shift of the threshold voltage in the transfer characteristics.[2] However, our devices exhibit a different response. As shown in Fig. 5a, the NBS induces an increase in the subthreshold slope, rather than a shift in the threshold voltage. Since the subthreshold slope is positively related to the density of trapped charge carriers at the dielectric/semiconductor interface,[43,44] we speculate that a large number of traps are present at the Al_2O_3/ITZO interface, rather than in the ITZO bulk. The introduction of quantum dots at this interface helps to mitigate the effect of these interface traps. This conclusion is further supported by the elimination of hysteresis in the transfer curves of the QD-passivated devices (Fig. 4) and is likely responsible for the improvement in mobility observed in Fig. 3.

Conclusions

In this study, two types of TFTs using ITZO as the semiconductor and Al_2O_3 as the dielectric layer are fabricated and systemically investigated: one with $CuInS_2$/ZnS core/shell QDs integrated into the Al_2O_3/ITZO interface and one without. Through testing, it was found that the QD integration can significantly increase the on-current, decrease the leakage current, and finally improve electron mobility. Furthermore, compared with the counterpart, TFTs with QDs show transfer characteristics with less hysteresis and improved NBS stability. The overall performance enhancement can be ascribed to the passivation effect of the QDs at the Al_2O_3/ITZO interface, which can eliminate the trap states in the Al_2O_3 and screen the electric dipoles.

Data availability

The datasets used and/or analysed during the current study are available from the corresponding author on reasonable request.

Author contributions

Sijie Chen: investigation, methodology, data curation, writing – original draft. Haoran Chen: investigation, methodology, data curation. Chenghui Xia: conceptualization, methodology, supervision, funding acquisition, writing – review and editing. Zhenhua Sun: conceptualization, data curation, methodology, supervision, funding acquisition, writing – review and editing.
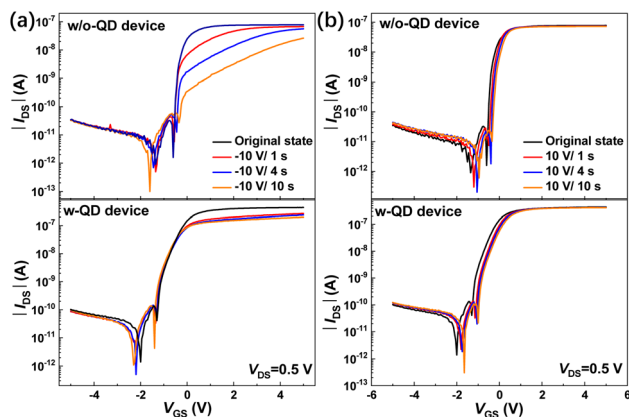

Fig. 5 Transfer characteristics of TFTs after NBS (a) and PBS (b). The transfer curves were recorded after applying gate bias stresses denoted in the figures.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

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