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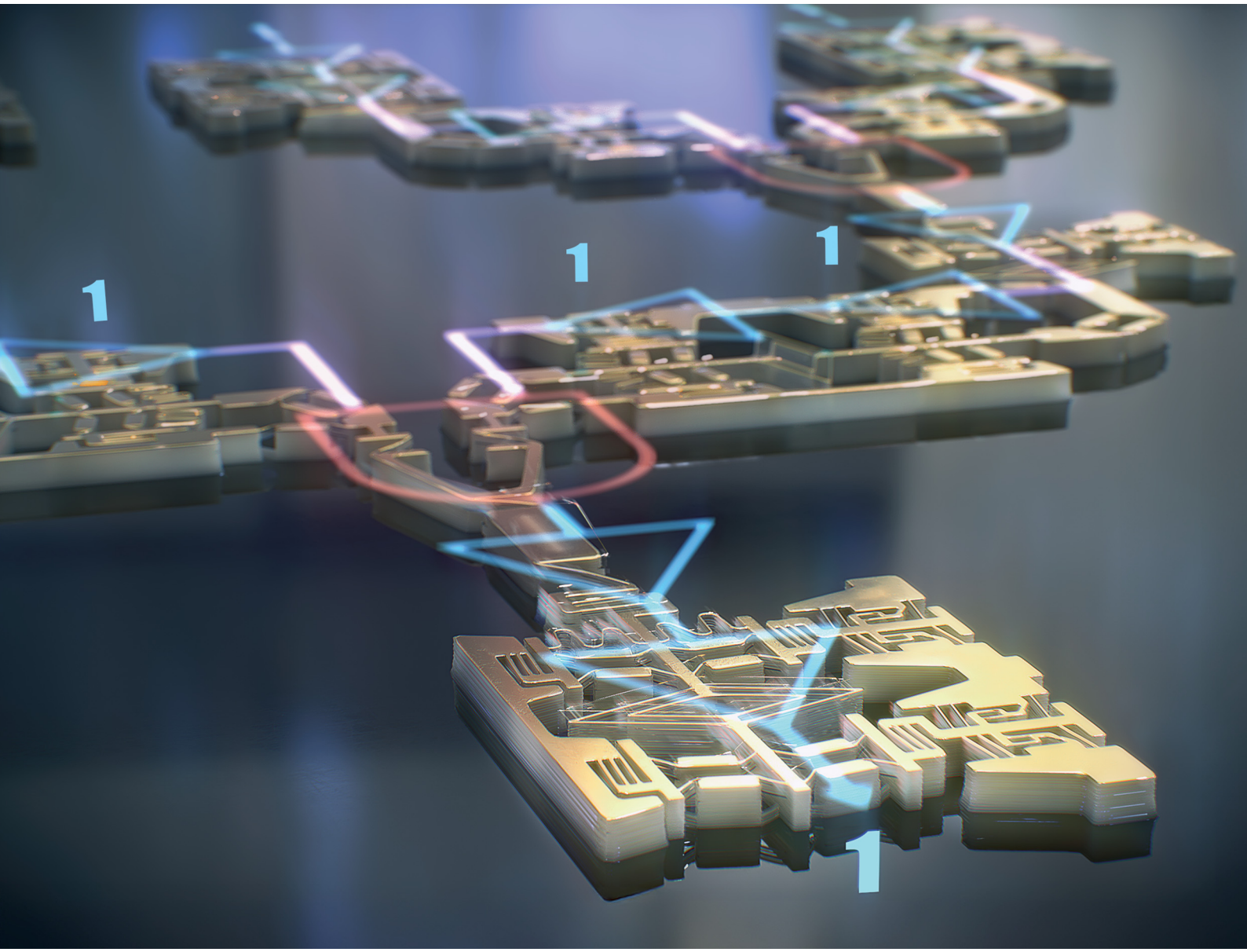

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Signal propagation in reversible digital mechanics

Hilary A. Johnson, †*[a] Robert M. Panas,†[a] Amin Farzaneh,[b] Frederick Sun,[a] Logan Bekker,[a] John Cortes,[a] Melika Ahmadi,[b] Julie Mancini,[a] Andrew J. Pascall[a] and Jonathan B. Hopkins[b]

Digital mechanics explores information processing through binary, mechanical circuits. This work demonstrates a flexural, mechanical integrated circuit (m-IC) that achieves reversible, non-reciprocal signal propagation through integrated AND logic and memory. Our approach exploits sequential bistable transitions with symmetric energy wells, tunable stiffness, impedance matching, and AND gate non-linearity, to enable signal propagation, repeatability, and reversibility. We present a generalized model of logic kinematics and energetics, validated experimentally, to study energy flows, quantify energetic limits, and identify operating regimes for reversible logic. Macro-scale experiments confirm propagation dynamics, and new fabrication methods extend the architecture to micro-scale devices. By achieving controlled, reversible signal transmission across interconnected logic and memory, this work establishes a scalable platform for robust mechanical computing and adaptive sensing.

New concepts

This work introduces flexural mechanical logic architectures that achieve reversible, energy-preserving signal propagation in networked circuits. Distinct from soliton-based approaches, which rely on elastic instabilities and nonlinear wave dynamics, our method exploits sequential bistable transitions with symmetric energy landscapes and tunable stiffness in both memory and AND operators, ensuring logic repeatability and reversibility. Prior studies separately demonstrate non-reciprocal soliton propagation, bistable reversibility, logical operations, and mechanical memory. Building on these foundations, we present the first integration of reversible, non-reciprocal signal transmission with branching mechanical circuits. By embedding energetically symmetric units into networked architectures, controlling the mechanical impedance matching between operators, and creating an energy-decrement along the signal path we achieve deterministic, non-reciprocal digital computation driven solely by input changes.The experimentally validated dynamics model quantifies kinematic displacements, stiffnesses, and energy flow, offering a generalizable framework for scalable, reversible mechanical computing for a range of materials and architectures. The novelty of this approach goes beyond bistability to achieving controlled, reversible propagation through interconnected mechanical circuits – a long-standing challenge in mechanical computing. These results establish a foundation for increasingly complex mechanical information processing and adaptive sensing systems that extend mechanical computing toward functional applications.

Introduction

Digital mechanics, an emerging field,[1–4] studies mechanical circuits that process and control information using digital signals. Diverse architectures[5–9] have demonstrated signal propagation,[8,10–13] logical operations,[14–23] and memory storage.[24–28] Mechanical integrated circuits (m-ICs) combine logic gates, inputs, outputs and memory into a physical intelligence[29] architecture, enabling promising applications such as embedded, powerless sensors and robotic actuators.

Different designs prioritize functional requirements such as: reversibility, non-reciprocity,[30] re-programmability,[31–33] and material elasticity. We categorize mechanical logic in four architectures: origami/kirigami,[16,34,35] buckled beams,[8,10,13,36] linkages,[27] and compliant flexures.[15] Each architecture leverages nonlinear instabilities (folding, beam buckling, structural buckling) to encode binary states in bistable energy wells, mapped to '1' and '0', where the energy landscape, force balance, and kinematic configuration are deterministic. Architecture and material choice further tune stiffnesses to access propagation regimes.

Important prior research explores sub-sets of digital mechanics such as non-reciprocal soliton propagation,[8,10,13,37–39] transition waves,[19,31] bistable reversibility,[30] logical operators,[14–18,21,22] and mechanical memory.[25–28,31] Building on this work, we introduce a compliant, flexural architecture that enables reversible, mechanical signal propagation through branching circuits combining logic and bistable memory (Fig. 1 and Video S1). We present a generalized dynamics model of the logic kinematics and energetics. Using the model, we studied energy flows and identified non-dimensional operating regimes in which signals propagate, and reversible logic

[a] *Lawrence Livermore National Laboratory, 7000 E Ave, Livermore, CA, USA. E-mail: johnson491@llnl.gov*
[b] *Department of Mechanical and Aerospace Engineering, University of California Los Angeles, Los Angeles, CA, USA*
† Co-first authors.

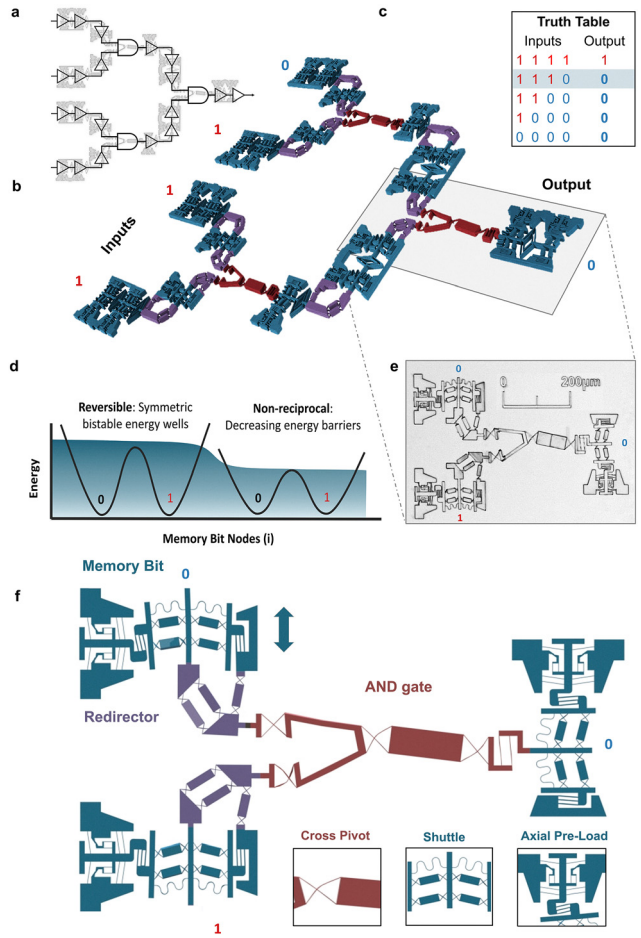

Fig. 1 Integrated mechanical logic mIC architecture. (a)–(c) 2-Layer, 4 input AND gate and memory bit circuit showing the logic schematic, design, and truth table. (d) Energy profiles with memory bit symmetry for reversibility and energy barrier decrement for non-reciprocity. (e) Micro-fabricated m-IC. (f) A pre-loaded AND gate.

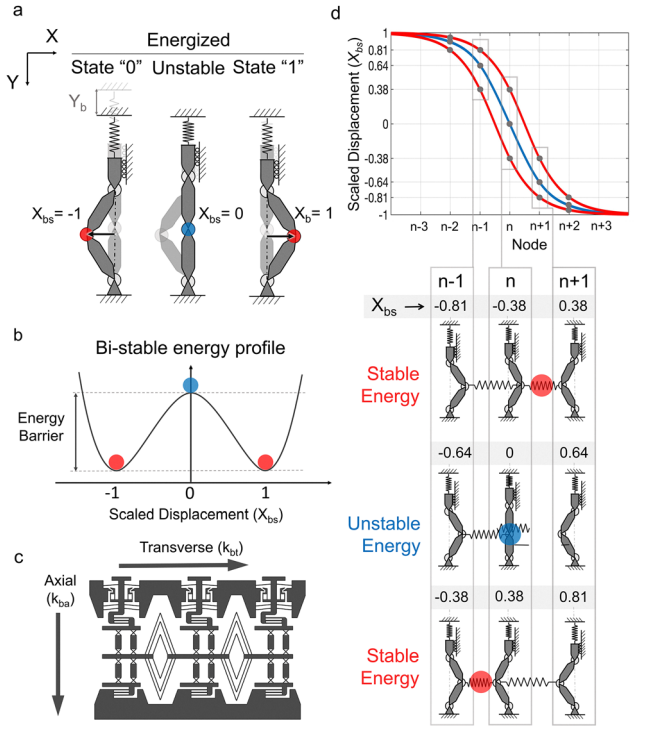

Fig. 2 Bistable element pulse propagation design region and limits. (a) Pseudo-rigid body diagram of bistable gates in the unstable and stable configurations, showing the center node displacement and preload Y_b. Gray shows previous states. (b) Equal energy wells enable reversibility. The energy barrier is the difference between the stable and unstable equilibrium. (c) Actualized gate designs of the un-preloaded memory bits with diamond inter-element springs. (d) Defining the stable and unstable equilibrium states in a chain of repeated nodes.

is possible. Experimentally, we used high-speed motion tracking to measure signal propagation and corroborate modelling results.

The parametric, cross-pivot architecture enables use of numerous materials (polymers, metals, and ceramics) at length scales from meter to micron (Fig. 1e). Combined, our work provides the foundation for the next generation of reversible mechanical computing that is robust and scalable across architectures and sizes.

Results and discussion

We investigated digital mechanics designs, behaviors, and propagation operating regimes through simulations and experiments. First, we present an overview of the dynamics simulation framework (details in SI) and validate it using the diode chain of memory bits, comparing results to prior research. Next, we explore the functionally unique AND gate, tuning inter- and intra- node compliances for signal propagation. Finally, we integrate the AND gate with input and output memory bits to form the mechanical circuit (Fig. 1f) and quantify its energetic limits and propagation dynamics.

Eulerian dynamics model

The simulation models a generalized system of logic and memory by analyzing forces, displacements, and energies across a network of nodes in both space and time. It employs force analysis, displacement fields, stiffness matrices, and energy-based methods to capture system dynamics, implemented in a MATLAB™ script. The model is initialized with parametric inputs, including the geometry, stiffness, mass, and energy dissipation behavior of the memory bits and AND gates, as well as a matrix defining the circuit connections. Starting from an initial estimate of the system's state, the simulation calculates forces and iteratively determines the resulting displacements and energies for each node. Details and equations are provided in the SI.

Bistable memory bit design and characterization

A single memory bit stores '1' and '0' states as displacements (X_{bs}) of the center node, which can displace left or right in the architecture agnostic pseudo-rigid body diagram (Fig. 2a). Energetically symmetric gates (Fig. 1d and 2b) enable reversibility, the ability to transition repeatably between '1' and '0' states in

response to push or pull inputs (Fig. 1d). In contrast, non-reversible systems with un-equal energy wells require an energy input to reset. A unidirectional gradient of the energy barrier enables stable non-reciprocal signals and inhibits backpropagation. This builds on prior research with bistable beams which showed that reversibility and nonreciprocity can be independently programmed by designing energetically symmetric units arranged in an asymmetric array.[30] The energy barrier for signal transmission is the difference between the stable (red) and unstable (blue) equilibria. Details on the kinematic and energetic models, preload trade-offs and cross-pivot rolling radii are provided in the SI (Fig. S1 and S3).

The actualized memory bit design (Fig. 1f and 2c) guides a central shuttle linearly using eight cross-pivot flexures in series and parallel. The memory bit acts as a force-transmitting element, an energy storage mechanism, and a kinematic guide. The bistable node is preloaded using parallel flexures and a latch (Fig. 1f). The assembly layers include kinematics, energetics, preload, and coupling linkages detailed in the SI 'Memory Bit', Fig. S1). We chose a compliant architecture with cross-pivot flexures,[40] which relies on beam bending, not buckling, to achieve equal energy bistability necessary for reversibility. The conservative, elastic spring force from bending stores potential energy, converting it into kinetic transitions. When several memory bits are connected in series, with an energy decrement, transition waves can propagate along the chain as each memory bit cycles through stable and unstable states. (Video S2). Fig. 2d shows the sequential node displacements at their equilibrium states at a fixed time.

Dynamic simulations reveal that pulse propagation occurs in a limited design region within the full parameter space (Fig. S5). The pulse energy map (Fig. S6) indicates a critical energy threshold to ensure propagation, emphasizing the importance of tuning both the intra- and inter- element stiffnesses. The inter-element coupling stiffness determines a node's influence on its neighbours, while the intra-element stiffness determines a node's resistance to that influence.

The intra-element transverse (k_{bt}) and axial (k_{ba}) stiffnesses modulate the bistable energy well depth (Fig. 2b, c and Fig. S7), with transverse stiffness particularly sensitive to flexural moment of inertia. The inter-element coupling stiffness (k_{bc}) controls the pulse width and propagation dynamics. In one physical design, Fig. 2c, diamond connectors represent the coupling stiffness, and the parallel and cross-pivot flexures influence the transverse and axial stiffnesses. We define a pulse stiffness ratio ($r_{kpulse} = k_{bc}/k_{bFmax}$) representing the ratio of the inter- and intra-element stiffnesses. A weak pulse stiffness ratio generates short pulse widths with only a few nodes (Fig. S5a). As the ratio increases, stronger coupling between nodes extends the pulse length towards infinity. Fig. S6a shows a pulse stiffness design region between 0.5 to 3.5.

As a pulse propagates along a chain of bistable elements, its potential energy oscillates between the unstable (UE) and stable (SE) equilibrium states (Fig. 2d). Non-reciprocal pulse propagation requires an energy decrement (E_{step}) for successive, downstream gates. This tunable energy gradient ensures that the soliton kinetic energy reaches the next SE state.

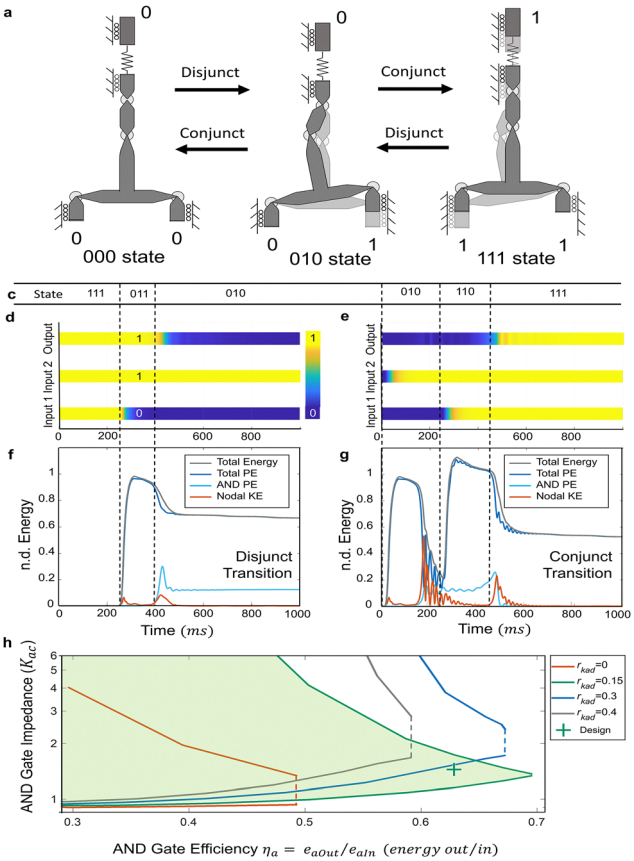

Fig. 3 AND gate design, kinematics and energy map. (a) AND gate pseudo-rigid body diagrams showing the kinematics of the disjunct and conjunct transitions. (b) An AND gate design using cross pivots joints. (c) States for (d)–(g). Time values are material and scale specific, defined in the SI. (d) The disjunct energy map starts at 111, a falling input 1 pulls it to state 011, from yellow to blue, the output logically also transitions, ending at the 010 state. (e) The conjunct energy map starts at 000, a rising input 2 pulse drives it to state 010, then a rising input 1 pulse drives it to 111. (f) The disjunct pulse increases the total energy and the AND gate PE. The nodal KE rises during the dynamic transition. (g) The conjunct transitions increase the total and potential energy during the dynamic transition and then rest at the lower stable equilibrium. Non-dimensionalized with the unstable pulse energy, details in SI 'AND gate kinematic design'. (h) The energy flow map shows AND gate operating regions achievable through impedance tuning. Details in SI 'AND gate efficiency'.

With each nodal advance, potential converts to kinetic energy, with some dissipated through non-conservative losses (Fig. S7). Application-specific requirements guide tuning the inter- and intra- stiffnesses and E_{step}. The key trade-off is small pulse energy, short travel and compact width with low pulse stiffness r_{kpulse} *versus* high pulse energy, long travel and wide pulse widths for higher pulse stiffness (Fig. S5).

AND gate design and characterization

The AND gate combines two input nodes and one output node, each in a binary 1 or 0 state (Fig. 3a). While some architectures[8] and conventional electronics combine base units, like transistors, to create higher order logic elements, we designed a functionally unique AND gate (Fig. 3a, b and Fig. S8) using

cross-pivot flexures. The AND gate functions independent of the memory bits, however they can be integrated to store the input and output states.

The AND gate exhibits two distinct kinematic and energetic transitions: the disjunct and conjunct. Fig. 3c–g illustrate the pulse structure and energy profiles of these transitions. The disjunct transition is a change from equal to opposite input states, when one input displaces to a different state than the other (*e.g.* 000 to 100 or 010; 111 to 010 or 100). The state is denoted (input 1, input 2, output) such that 111 indicates all

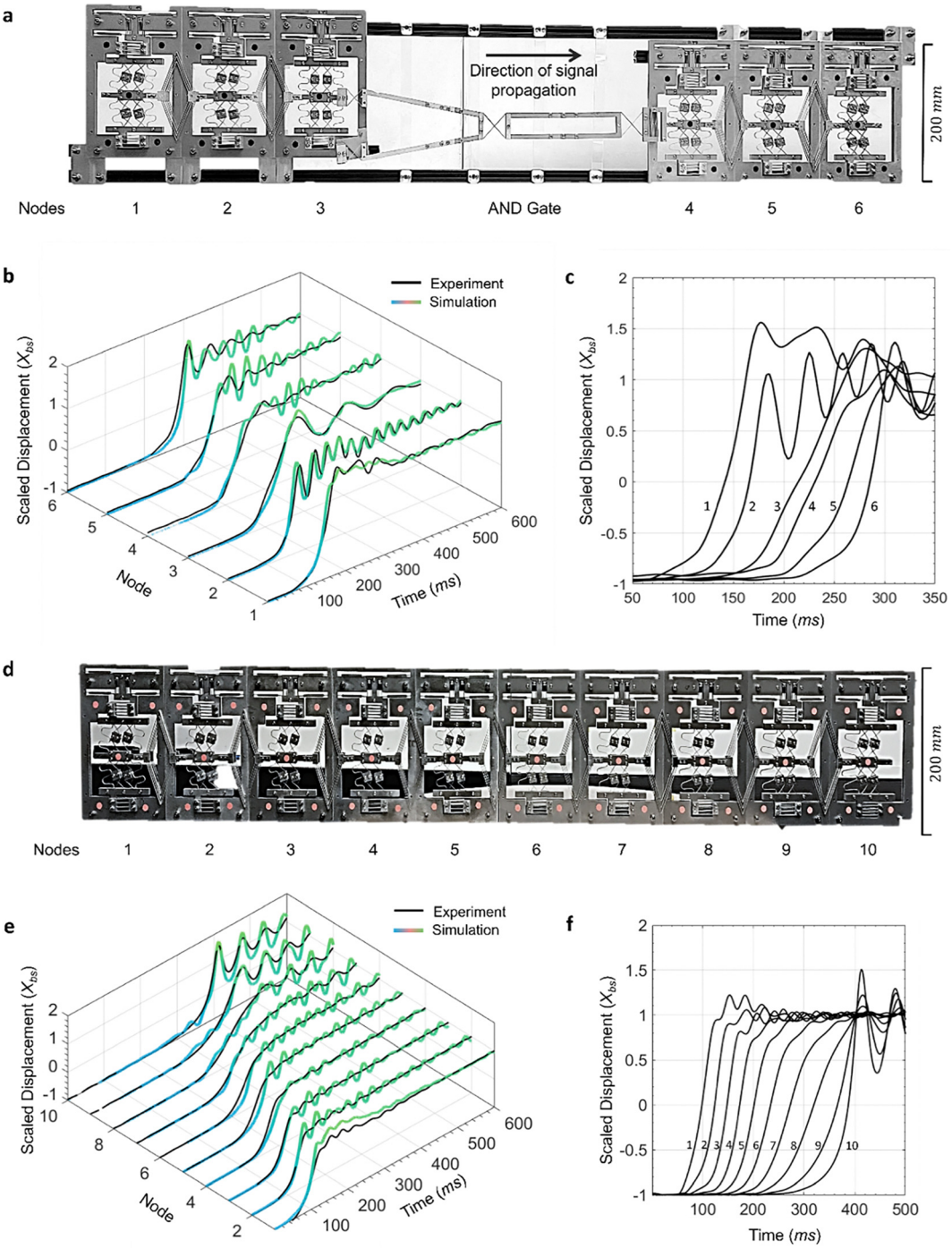

Fig. 4 Comparing experimental and simulation propagation results. (a) Macro logic chain integrating AND gate with 3 input memory bits and 3 output memory bits. (b) Time variant, nodal displacements for the macro AND gate through simulation and experiments. (c) Simulation results showing the propagation of a 0 to 1 signal through the nodes and AND gate. With parameters m_b = 0.247 kg, $k_a = 32\,789\frac{N}{m}$, k_t = 0.065, k_c = 0.06, ζ = 0.034. (d) Macro diode of 10 bistable memory bits. (e) Time variant, nodal displacements for the memory bit diode. (f) Simulation results showing the propagation of a 0 to 1 signal through the diode, with parameters m_b = 0.1775 kg, $k_a = 37\,643\frac{N}{m}$, k_t = 0.065, k_c = 0.06, ζ = 0.034 with further information in the SI 'Circuit synthesis'.

inputs and output are in the 1 state. The conjunct transition is a transition from opposite to equal states, when one input displaces to the same state as the other (*e.g.* 010 → 111). During the disjunct transition, the AND gate output is suppressed by the AND gate rotation, the critical non-linearity arising from cosine length attenuation. This is the AND gate logical operation, suppressing the output until both inputs are true. Conjunct inputs directly displace the output, enabling continued signal propagation through the AND gate.

Each AND gate transition relates to an energy storage mechanism. Differential motion of the inputs generates rotation in the two cross pivot flexural hinges. During disjunct transitions, this differential motion acts as an energetic sink, increasing potential energy and limiting the AND gate efficiency (Fig. 3f). In contrast, during conjunct transitions matching between the inputs is an energetic source and stored potential energy is converted into kinetic energy (Fig. 3g – at 200 ms). A compression spring (k_{ac}) attached to the AND gate output allows impedance matching between the compressive stiffness and the output coupling linkage stiffness. This assumes that the lumped mass-spring-damper system is stiffness dominated at the low frequency pulse signal and designed to not transmit higher frequency inertial noise. The compressive spring enables the pulse to propagate out of the AND gate. (Details in SI 'AND gate design').

Signal propagation through the AND gate is non-trivial, requiring tuning parameters to the design region. The impedance plot (Fig. 3h) identifies these design regions, bounded by an upper conjunct curve and a lower disjunct curve and defines the compressive stiffness limits as a function of gate efficiency (output to input pulse energy ratio). The horn-shaped region shows higher gate efficiencies result in smaller energy margins to compensate for imperfect transmission mechanics. As efficiency increases, the operational space narrows toward an impedance match with the output coupling stiffness (k_{acp3}). Varying the differential stiffness ratio (r_{kad}) shifts the conjunct and disjunct bounds and the maximum achievable efficiency. While $r_{kad} = 0.15$ yields the highest efficiency ($\eta_a = 63\%$), experimental designs used lower efficiency parameters to ensure wider tolerances, accommodating variations in manufactured flexure thickness. Thus, the impedance plot highlights competing dynamics between the compressive stiffness (k_{ac}) and stiffness of downstream nodes (k_{acp3}) and shows how downstream nodes backpropagate restrictions on the AND gate elastomechanics (SI 'AND Gate'). Signal propagation in mechanical integrated circuits.

Combining AND gate logic with memory bits, we demonstrate reversible signal propagation through mechanical integrated circuits (Videos S1–S5). We fabricated and built macro and micro demonstrators of both memory bit diodes and integrated AND gates. First, we set the energy and length scale for each design, then determined the topology and flexure parameters. Next, we tuned the memory bit characteristic stiffness to activate bistable behavior and tuned the coupling stiffnesses and step energy to ensure cascading propagation. Finally, we selected the AND gate coupling stiffness based on the selected differential stiffness ratio.

At the macro scale we extracted nodal displacements from high-speed video using tracking markers (Fig. 4a and d) (Videos S2, S3, and S5). For the macro AND gate, input 1, not connected to a memory bit, is pre-actuated, then conjunct displacement of input 2 completes the AND gate, triggering the output bistable node cascade (Fig. 4a and Video S5). We used these data to compare to modeled parameters to tune and corroborate model kinematics and dynamics. Fig. 4b and e demonstrate agreement between the experimental and simulated time variant, nodal displacements, capturing both the primary binary signal, as well as secondary resonances. We tuned each nodal resonance in the model and fabricated system by modulating mass,

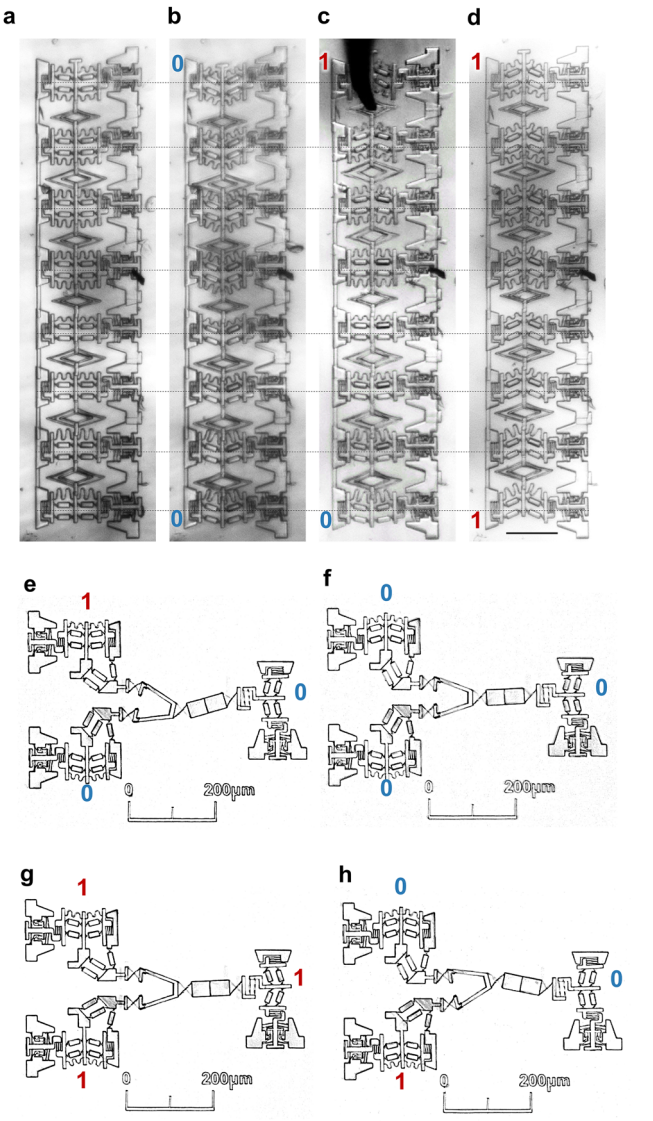

Fig. 5 Micro AND gates and memory bits. (a) Memory bit diodes microfabricated with two photon stereolithography showing no preload (b) preload in the 0 state, (c) the beginning of the signal propagating from top to bottom, (d) full propagation to the 1 state. (e)–(h) Micro-fabricated AND gates actuated into logic configurations show memory bits at each input connected to 90-degree redirectors connected to the AND gate then connected to a memory bit output.

stiffness, and damping ratios. Note that node 3 attached to the input of the AND gate shows a lower frequency, damped by the AND gate, compared to all other nodes. Results for the macro AND gate show a time delay between nodes 2 and 3, and 4 and 5, where the AND gate is connected between 3 and 4 (Fig. 4c). Signal transmission through the AND gate slightly attenuates the signal. In the memory bit diode, propagation along the diode also slightly slows (Fig. 4f).

Micro-scale, two-photon polymerization[41] printed AND gates and memory bits qualitatively demonstrate design scalability and manufacturing capability (Fig. 5 and Videos S1, S4). The flexural design enables non-contact motion, thus eliminating frictional forces and enabling micro-scale soliton and logical operation. Both the macro and micro circuits are fabricated in the unstressed state, then energized by displacing the preload mechanism. The SI details the micro-mechanical manufacturing methods used to produce functional bistable diodes with energy decrements and actuatable m-ICs with AND gate logic.

Conclusions

In this work, we demonstrated reversible, mechanical signal propagation through integrated logic and memory using a compliant flexural architecture. By combining energetically symmetric gates, AND gate non-linearity, and a unidirectional energy gradient we showed reversible, non-reciprocal signal propagation through sequential logic. The generalized dynamics model of logic kinematics and energetics quantified energy flows, operating regimes, and design limits, providing a versatile framework applicable to diverse architectures.

Experimental validation using high-speed motion tracking confirmed the modelling approach, while macro and micro propagation showcased scalability across materials and length scales from meters to microns. Together, these results establish a robust foundation for the next generation of reversible, mechanical computing.

Looking ahead, this framework is extensible to additional logic operators (OR, NOR, NAND, XOR),[15] characterization of propagation in longer, more complex or microscale circuits and a parametric sensitivity study such as further investigating the pulse stiffness ratio. Extensions towards advanced sensing, actuation, and networked architectures will further expand functionality. By addressing the key challenge of achieving reversible signal propagation in mechanical logic, this work advances digital mechanics toward practical, scalable applications in computation, robotics, and adaptive systems.

Author contributions

R. P., A. P. and J. H. conceived the research problem. A. F., L. B., and J. M. fabricated and tested the micro and macro scale logic gates. F. S., R. P. and H. J. performed the finite-element simulations and analysed the data. H. J., A. F., M. A. and R. P. wrote the manuscript and supplementary information. J. C., A. P., J. H, R. P., and H. J., managed the research work. All authors discussed the results and commented on the manuscript.

Conflicts of interest

There are no conflicts to declare.

Data availability

The data and equations supporting the findings of this study are available within the manuscript and its supplementary information (SI). Supplementary information is available. See DOI: **https://doi.org/10.1039/d5mh00509d**.

Any additional raw data required to reproduce the findings can be made available upon reasonable request.

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