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The constant demands for the better performance of consumer electronics have led to shorter usage lifespans, resulting in a significant increase in electronic waste (e-waste). Developing electronics that can be easily broken down and recycled is a promising strategy to tackle this growing e-waste challenge. Herein, we report a biocompatible and degradable organic thin film transistor (OTFT) utilizing a biocompatible semiconductor with a biodegradable dielectric and substrate. We present the first OTFT based on bispentafluorophenoxy silicon phthalocyanine (F_{10} -SiPc) integrated with a polyvinyl alcohol (PVA) and poly(caprolactone) (PCL) bilayer as the dielectric, leading to a drop in threshold voltage (V_T) from 12.7 V to -0.97 V, *versus* using SiO_2 while maintaining similar mobility values. We demonstrate the importance of the annealing temperature on PLA substrate roughness and gate electrode surface chemistry for the fabrication of working OTFT devices. We then demonstrate that the bendable OTFTs could easily be dissolved in phosphate buffer saline (PBS) solution at room temperature in less than a month, which is a crucial aspect for ensuring eco-sustainability in electronic devices. Finally, incubation of the degradation products with fibroblastic cells did not affect cell viability, suggesting that they are non-cytotoxic. These cyocompatible disintegrable OTFTs with low operating voltages will find applications in bioresorbable electronics and constitute a step towards minimizing e-waste.

Introduction

In 2021, the United Nations released a report estimating that every person will produce roughly 7.6 kg of e-waste, leading to 57.4 million metric tonnes (MMT)¹ of e-waste. This number is

predicted to rise to 74 MMT by 2030 if left uncontrolled. The need to consider the environmental effects of essential electronic components like transistors and capacitors during production and disposal is growing due to the increasing demand for these devices worldwide. Sustainable and environmentally friendly electronics are becoming increasingly important, from reducing the risks linked to e-waste to paving the way for the generation of new wearable and implantable electronics.^{2–5} The growing number of transient electronic applications such as food package sensors or single-use biosensors is also causing concern for the e-waste problem and providing an opportunity for the development of non-toxic biodegradable electronics.^{5,7}

The use of thin, plastic substrates in the fabrication of electrical devices has the advantage of lowering the total mass of the systems and imparting flexible characteristics which can lead to new applications such as wearable electronics.^{8,9} Nevertheless, there are intrinsic disadvantages to using plastic substrates, including their disintegration into microplastics that can then find their way into our soil and groundwater, contributing to environmental contamination.¹⁰ Consequently, the use of plastic substrates in flexible electronics that are not biodegradable or recyclable is unsustainable.¹¹ One of the challenges associated with using biodegradable substrates such as poly(lactic acid) (PLA) is that the glass transition temperature (T_g) of these materials is very low, which makes it challenging to integrate them into high-temperature manufacturing processes like the manufacturing of silicon semiconductors. For organic electronics, the semiconductor is carbon-based and can be deposited at lower temperatures, enabling integration onto plastic substrates while providing low energy requirements and potential economic incentives.¹² Organic thin film transistors (OTFTs) are electrical switches and are basic components in more complex circuits finding applications in next generation biological and chemical sensors,¹³ health monitors,¹⁴ stretchable devices,¹⁵ and electronic skin.¹⁶ Research on OTFT development has focused primarily on improving device performance with little attention to assessing the biocompatibility and environmental impact of the resulting materials.^{17,18}

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Biodegradable OTFTs require biodegradable substrates, dielectrics, electrodes, semiconductors, and peripheral materials such as encapsulating materials. Biobased materials, such as PLA, polyhydroxyalkanoates (PHAs), starch blends, or cellulose-based polymers, are promising substrates if the processing temperatures can be kept $<150\text{ }^{\circ}\text{C}$.¹⁹ However, biodegradable dielectrics with the desired physical and electrical properties are rare. Poly(vinyl alcohol) (PVA) is a bioresorbable dielectric that can be easily dissolved in environmentally friendly solvents such as water and breaks down naturally when exposed to suitable microorganisms.²⁰ PVA has been previously used as a dielectric material in sensors²¹ and OTFTs, either as a homopolymer or as a blend of other materials.^{22,23} However, PVA also presents challenges; its printing is difficult often requiring careful optimization such as the addition of a viscosity enhancer²⁴ and the resulting hydrophilic film is susceptible to moisture resulting in reduced reliability and stability of fabricated devices.^{25,26} Our group recently developed PVA with an interfacial, thermally crosslinked diisocyanate-terminated polycaprolactone (TPCL) leading to high- k /low- k bilayer dielectrics. The bilayer combined the desired electrical properties and high dielectric constant of the PVA with the moisture resistance of PCL, which also provides better surface matching for the subsequent deposition of the semiconductor. To further improve the shelf life and the ease of large-scale processing we then synthesized benzodioxinone-terminated PCL layer, which can be coupled to the PVA dielectric surface *via* UV radiation.²⁷ High- k /low- k bilayer dielectrics have shown several advantages, such as reduced charge trapping, improved device stability, facilitation of orthogonal processing, and prevention of direct interaction between the hydroxyl groups of PVA and the semiconductor.^{28–30} The PCL layer acts as a protective coating for the PVA layer, creating a less polar environment at the interface between the dielectric and semiconductor.^{31,32}

Phthalocyanines (Pcs) are promising semiconductors used in OTFTs that are produced on the ton scale annually and are commonly used as blue and green pigments in a variety of applications, including textiles, plastics, automotive paints, and others.^{33–35} Silicon phthalocyanines ($\text{R}_2\text{-SiPcs}$) are a class of tetravalent Pc with axial groups that can be used as handles to impart functionalities onto the molecule such as solubility or solid state engineering amenability. Their strong near-infrared (NIR) emission has also stimulated their prospective use in both *in vitro* and *in vivo* bioimaging.^{36–40} Our group has demonstrated relatively better n-type performance of various $\text{R}_2\text{-SiPc}$ derivatives in OTFTs.^{41–45} In most cases $\text{R}_2\text{-SiPc}$ -based OTFTs suffer from high threshold voltage (V_T) making them unsuitable for use in consumer electronics ($<3\text{ V}$) or in combination with printed batteries ($<1.5\text{ V}$).^{46,47} The interface between dielectrics and semiconductors in OTFT devices plays a pivotal role in enhancing charge transport by mitigating charge traps and reducing V_T .^{48–50} Hybrid gate dielectric combinations of inorganic/organic bilayers are commonly employed to achieve high-performance organic transistors.⁵¹ However these materials are non-degradable suggesting the need for biodegradable materials with a high dielectric constant (k). Recently, our group published the first $\text{R}_2\text{-SiPc}$ paired with a polymer dielectric based on methyl methacrylate and dimethyl aminoethyl methacrylate copolymers (P(MMA-*co*-DMAEMA)), attaining near-zero V_T .⁵²

While not biodegradable, this study demonstrates the potential for using polymer dielectrics in combination with $\text{R}_2\text{-SiPc}$ semiconductors in OTFTs.

In this work, we present a disintegrable and biocompatible n-type OTFT with a low V_T , based on the $\text{R}_2\text{-SiPc}$ OTFT utilizing a biodegradable bilayer PVA/UV-PCL as a gate dielectric with a biodegradable PLA substrate. Utilizing UV-PCL increased device stability and ease of processing while maintaining its encapsulation characteristics and moisture resistance for the PVA layer. We also demonstrate the aqueous disintegration of the resulting OTFTs into non-cytotoxic degradation products. These results demonstrate the broad applicability of low-voltage n-type and bioresorbable polymer dielectrics that employ scalable, economically viable $\text{R}_2\text{-SiPc}$ semiconductors.

Results and discussion

In selecting active materials, we focused on utilizing polymers that exhibit biocompatibility, biodegradability, and adequate electrical properties, and are soluble in various solvent systems enabling solution processing into thin films. Fig. 1 shows schematically the design of biocompatible and disintegrable OTFTs fabricated with bottom-gate top-contact (BGTC) architecture based on a PLA substrate, a bilayer PVA/PCL dielectric and an $\text{R}_2\text{-SiPc}$ semiconductor. The substrate, which makes up 99.89% of the overall mass of the device,⁵³ was chosen to be made of PLA, a linear biodegradable thermoplastic polyester. The physical attributes of PLA provided constraints for further device processing as a result of (i) a low melting point (T_m) and low T_g , and (ii) low chemical resistance when exposed to organic solvents and incompatibility with orthogonal processing. These characteristics indicate the need to use mild downstream processing conditions. Here, we employ water-soluble PVA as a solution-processable dielectric. PLA, PVA, and PCL are economical, easily accessible, and have a well-established history in various biomedical devices used in clinical settings.⁵³ The development of ecologically benign semiconductor materials is another critical step to overcome when fabricating fully decomposable OTFT devices.⁵⁴ $\text{R}_2\text{-SiPcs}$ exhibit non-hazardous and biocompatible properties, making them promising candidates for degradable OTFTs. Gold electrodes are used in the OTFTs due to their remarkable conductivity and biocompatible characteristics both *in vitro* and *in vivo* and because gold has been employed in a range of medical applications.^{55–57} Gold, as an inert biomaterial, has demonstrated decreased biofouling in living organisms for various biomedical implants, such as cardiovascular⁵⁸ and biomedical microelectromechanical (BioMEMS) systems.⁵⁹

The fabrication of OTFTs was accomplished by first spin-coating PLA on a quartz-coated glass substrate to coat a uniform PLA layer. This was followed by a baking process to remove any trapped solvent, according to the literature.^{60,61} The thickness of the biodegradable PLA substrate was approximately 3–4 μm which was then coated with chromium-gold (Cr-Au) where the Cr layer was used to improve the adhesion of Au on the PLA surface. The Au surface, which was deposited to cover the entire PLA substrate surface to enable automated and



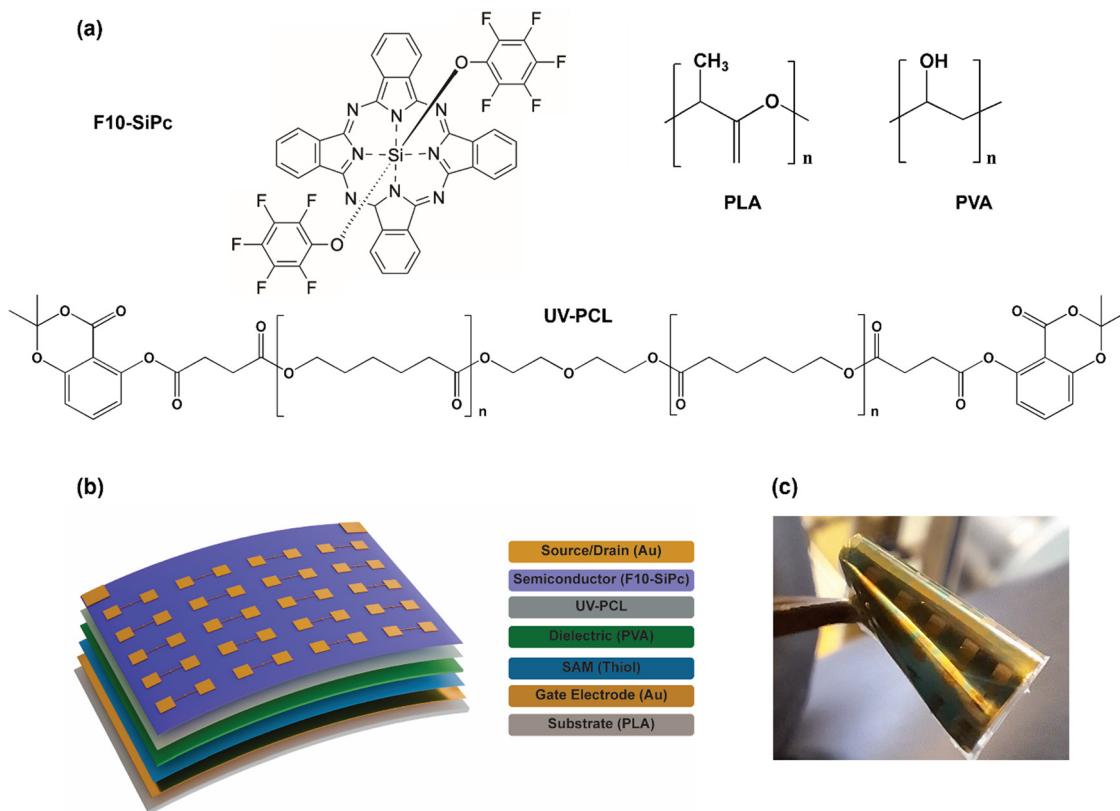


Fig. 1 (a) Chemical structures of semiconductor, substrate, and dielectric materials: F₁₀-SiPc, PLA, PVA, and benzodioxinone-terminated poly caprolactone (UV-PCL). (b) Schematic illustration of a disintegrable bottom gate top contact (BGTC) transistor device. (c) Digital photo of a PLA substrate with an array of OTFTs.

robust testing,⁶² serves as the bottom gate electrode. However, the gold surface with a water contact angle at $\sim 75^\circ$ is not sufficiently hydrophilic for the PVA solution to be coated orthogonally and form a uniform layer. To overcome this, gold was treated with a self-assembled monolayer (SAM) of hydrophilic thiol for 1 hour to improve the hydrophilicity.⁶³ Excess thiol molecules were rinsed off with pure ethanol. A decrease in the water contact angle to $\sim 40^\circ$ was observed when gold films were treated with thiol (Fig. 2a). While other methods such as plasma treatment of gold could also be used to increase hydrophilicity, thiol treatment is simple and more permanent.

The PVA dielectric was deposited by spin-coating onto a thiol-treated gold/PLA substrate followed by thermal annealing. In previous reports,^{27,49} the PVA thin film was annealed at 150 °C for 1 hour to remove the solvent. Unlike our previous studies which annealed PVA on glass substrates, in this study PVA is deposited on PLA which is temperature-sensitive. Therefore, as the substrate is exposed to high temperatures it shrinks leading to buckling and high surface roughness, which is not conducive for OTFT fabrication. An average surface roughness of less than 10 nm is typically required to avoid surface traps at the dielectric–semiconductor interface and discontinuities of the semiconductor layer.⁶⁴ Gold gate electrode-coated PLA films were vacuum annealed at different temperatures: 150 °C, 80 °C, 60 °C for 1 hour and 50 °C overnight, and the

roughness measurements were carried out utilizing a profilometer (Fig. 2b). At annealing temperatures equal to or above 60 °C, the average roughness of the gold layer was > 10 nm. We surmise that this increase in roughness is a product of different thermal expansion of the PLA substrate and gold layer leading to changes in morphology. However, when the gold-coated PLA films were annealed at 50 °C (below the T_g of PLA) overnight, the average roughness value was less than 10 nm. We also obtained microscopy images of the gold surface on a PLA substrate when annealed at different temperatures (Fig. 2c). These figures clearly show the roughness evolution upon increasing the temperature above the T_g value of PLA. Consequently, no major change in the roughness of the gate electrode surface was observed when the film was annealed at 50 °C overnight. Next, the UV-PCL solution was spin-coated onto the PVA layer, and the films were UV-cross-linked prior to rinsing the excess PCL. To confirm the crosslinking of UV-PCL, the films were rinsed with toluene, and the water contact angle was measured. As shown in Fig. 3 we report the contact angle of PVA and UV-PCL-coated PVA before and after rinsing with toluene. UV-PCL would dissolve in toluene during the rinsing process if it was not crosslinked to the PVA layer, resulting in a drop in the contact angle to match that of the bare PVA film. The UV-PCL maintained a contact angle of around 78° after two rinsing steps once crosslinking conditions were optimized (Fig. 3). The



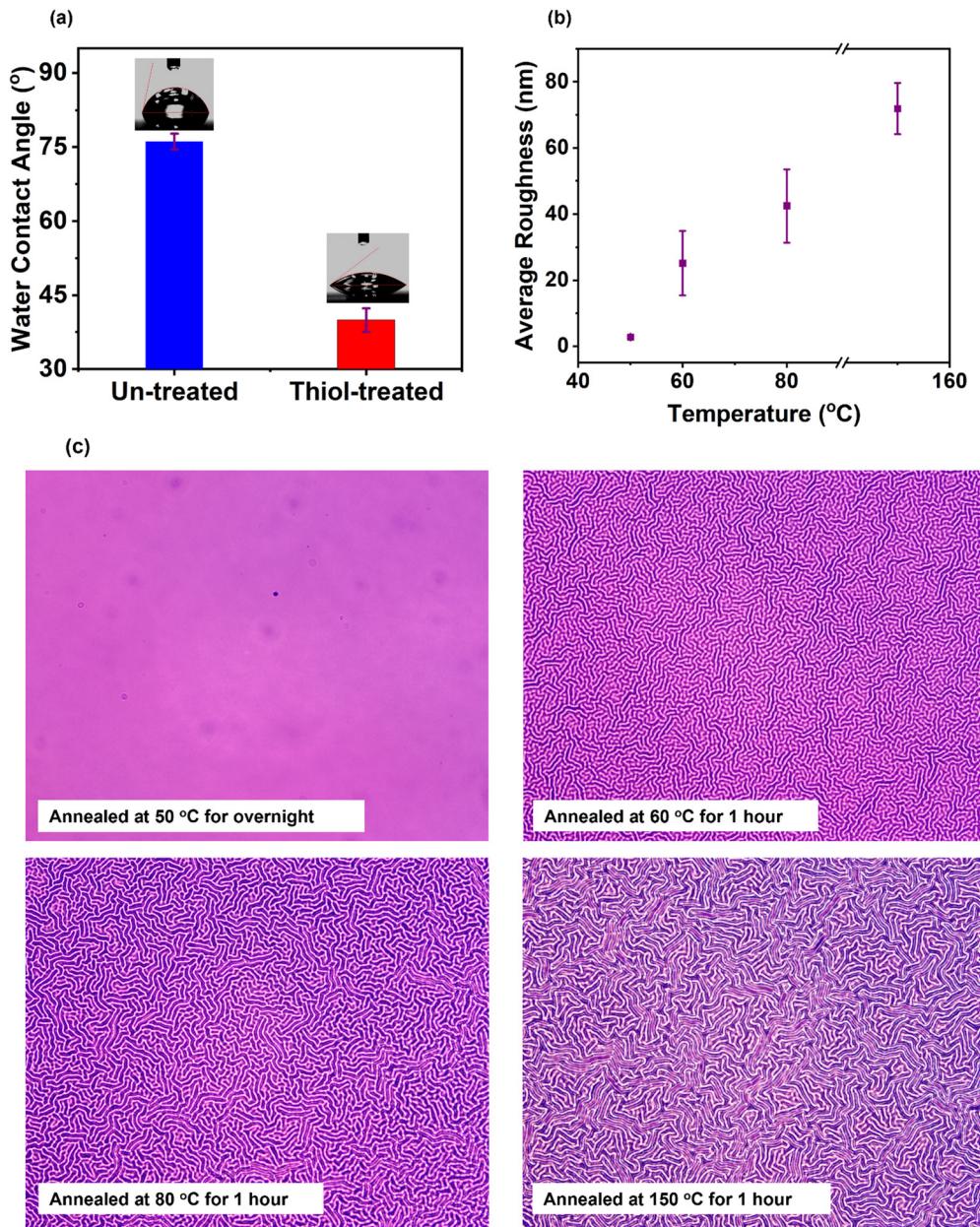


Fig. 2 (a) Water contact angle measurements of a gold film coated on a PLA substrate as a bottom gate electrode with and without thiol treatment. (b) The average surface roughness of the gate electrode surface measured with a profilometer. (c) Optical microscopy images of a gate electrode film after annealing at different temperatures.

cross-linking reaction between PCL and PVA also secures the PCL layer in position,⁶⁵ inhibiting aggregation and reducing the interfacial hydroxy groups, which can act as charge traps during OTFT operation.⁶⁶ Interfacial cross-linking also preserves a substantial amount of hydroxyl groups in the bulk of PVA, leading to a high dielectric constant (κ), while simultaneously enabling orthogonal processing.^{2,67}

The dielectric properties of the bilayer dielectric (PVA/UV-PCL) were characterized by impedance spectroscopy and are summarized in Table 1. The bilayer dielectric constant values found were well within the predicted range for PVA.^{23,30,68} It has been reported that hygroscopic polymer dielectrics when exposed

to moisture can experience an increase in the capacitance density by up to 50 times at 10 Hz.²⁷ This change is explained by the fact that moisture acts as a plasticizer, facilitating hydroxyl group alignment under an applied electric field and thereby increasing the capacitance of the PVA film.^{69,70} However, for reliable transistors in flexible circuits, the dielectric properties need to be stable. Water molecules also introduce charge traps at the dielectric–semiconductor interface, increasing the device hysteresis which is also detrimental to the transistor performance. Therefore, a monolayer ($\sim 1\text{--}2\text{ nm}$) of UV-cross-linkable PCL layer deposited on top of PVA functions as a moisture barrier, thereby reducing the impact of moisture on the dielectric properties of PVA.²⁷

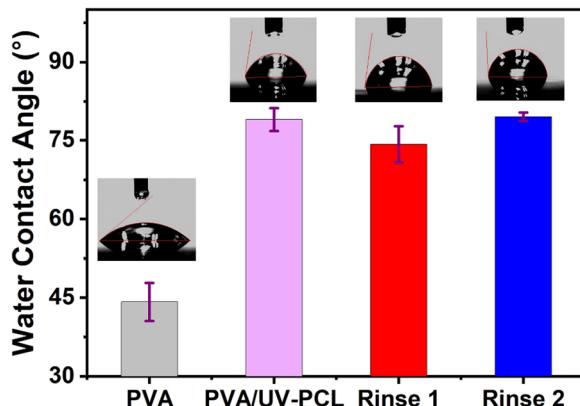


Fig. 3 Contact angle measurements for neat PVA and PVA/UV-PCL.

Table 1 Average dielectric properties of PVA/UV-PCL at 10 Hz

Dielectric	Effective dielectric constant (κ)	Capacitance density (nF cm^{-2})
PVA/UV-PCL	10.6 ± 1.6	26.70 ± 0.04

$\text{F}_{10}\text{-SiPc}$ was deposited on the UV-PCL layer. $\text{F}_{10}\text{-SiPc}$ OTFTs using OTS-treated SiO_2 as the gate dielectric were fabricated using a similar device configuration for device performance comparison.^{23,27,30,68–70} Finally Cr and then Au were deposited on the semiconductor as the source/drain electrodes using shadow masks. The Cr interlayer improves electrode durability⁷¹ and reduce contact resistance by matching the work function of the electrode with the lower unoccupied molecular orbital (LUMO) energy level of $\text{F}_{10}\text{-SiPc}$.^{72,73}

Fig. 4a-d depicts the characteristic output and transfer curves of the $\text{F}_{10}\text{-SiPc}$ OTFTs on both PVA/UV-PCL and OTS-treated SiO_2 dielectrics. The V_T , electron mobility (μ_e) and on/off current ($I_{\text{on/off}}$) were determined and are presented in Table 2. The V_T value of $\text{F}_{10}\text{-SiPc}$ OTFTs was reduced noticeably from 12.7 ± 1.7 V when using OTS-treated SiO_2 as the gate dielectric to -0.97 ± 1.4 V when using a PVA/UV-PCL bilayer as the gate dielectric. The decrease in V_T implies a reduction in polarity at the semiconductor/dielectric interface, minimizing the amount of charge trapping,^{29,74–76} which is likely due to the higher dielectric constant of PVA/UV-PCL (10.6) compared to SiO_2 (3.9), at frequencies below 1 kHz.⁷⁷ This represents a significant improvement compared to previous studies⁵³ where biocompatible and bioresorbable OTFTs were fabricated utilizing PVA as the gate dielectric with V_T values of approximately -15.4 V. A statistically similar μ_e was observed, going from $(2 \pm 0.7) \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ on the OTS/ SiO_2 gate dielectric to $(1.03 \pm 1.6) \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ when PVA/UV-PCL was used. This is consistent with previous research on bottom-gate devices that include the deposition of $\text{F}_{10}\text{-SiPc}$ on the PMMA dielectric, which provided an electron mobility of $1.1 \times 10^{-2} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, lower than that obtained with $\text{F}_{10}\text{-SiPc}$ deposited on SiO_2 .⁵² Although the $I_{\text{on/off}}$ ratios are comparatively low, this aligns with the literature reported for PVA dielectrics.⁷⁸ The high off current observed in Fig. 4d might

be due to the ambipolarity of the device as $\text{F}_{10}\text{-SiPc}$ has been demonstrated as an ambipolar semiconducting material. It is important to note that devices prepared on OTS/ SiO_2 had higher currents than devices prepared on PVA/UV-PCL which is a function of several factors including the operating conditions used to obtain the transfer and output curves, which are different in terms of V_{GS} and V_{SD} . With PVA/UV-PCL devices tested at V_{GS} and $V_{\text{SD}} = 4$ V, we obtain a current of $\approx 0.073 \mu\text{A}$, but when using OTS/ SiO_2 at the same V_{GS} and V_{SD} the device does not turn on, highlighting the low voltage requirements when using PVA/UV-PCL. A comparable current is only obtained at ~ 25 V when using OTS/ SiO_2 .

Enhanced crystallinity in MPcs deposited by physical vapour deposition (PVD) generally results in enhanced charge transport characteristics in OTFTs, leading to greater mobility and on-current values, while amorphous MPcs typically show higher numbers of defect sites, which decreases the conductivity and mobility of the semiconductor.⁷⁹ The crystallization of MPcs is impacted by substrate characteristics, molecular order of the sub-layer, surface roughness, chemistry, and deposition rate.^{80,81} Fig. 4e and f show a comparison of XRD patterns of $\text{F}_{10}\text{-SiPc}$ films deposited on OTS-treated SiO_2 and the PVA/UV-PCL dielectric. A reduction in peak intensity at $2\theta = 8.43^\circ$ for $\text{F}_{10}\text{-SiPc}$ films deposited on PVA/UV-PCL was observed compared to those on the OTS-treated SiO_2 surface which might result in a change in relative crystallinity, change in polymorph or change in crystalline domain orientation. This discrepancy can be attributed to the differing surface diffusion behaviour of $\text{F}_{10}\text{-SiPc}$ molecules on PVA/UV-PCL compared to OTS-treated SiO_2 during the nucleation of $\text{F}_{10}\text{-SiPc}$ vapours on the substrate and is consistent with the observed slight drop in device μ_e .⁵² Overall, these results demonstrate that PVA/UV-PCL is an effective green dielectric for the development of $\text{R}_2\text{-SiPc}$ -based OTFTs with a low V_T value.

Numerical simulation was carried out to investigate the device physics of the corresponding transistors.^{82–84} We determined a set of models and parameters that reproduce the major characteristics of the OTFT based on the SiO_2 /OTS dielectric including both bulk traps and fixed charge at the semiconductor/insulator interface as shown in Fig. 5a. It is worth mentioning that we will focus on the ON-state simulation data because the simulation returns purely theoretically achievable OFF currents that are typically orders-of-magnitude lower than those realistically measurable. We then took a step-by-step approach to modelling the OTFT based on the PVA/UV-PCL dielectric to identify an origin for the different behaviours of the two transistors. First, we increased the capacitance from 15 nF cm^{-2} (SiO_2 /OTS) to 27 nF cm^{-2} (PVA/UV-PCL), without changing any other material parameters (curve "1"). This simple transformation is not enough to reflect the experimental data, especially because the V_T is still too high. Next, to reduce V_T , we removed the interface charge, obtaining curve "2". Finally, we removed the trap states, obtaining curve "3", which shows an excellent agreement between experiment and simulation, in terms of both the V_T and the ON-state current levels. A detailed list of parameters used for the optimized simulation curves in Fig. 5a and b can be found in Table S1, ESI.†



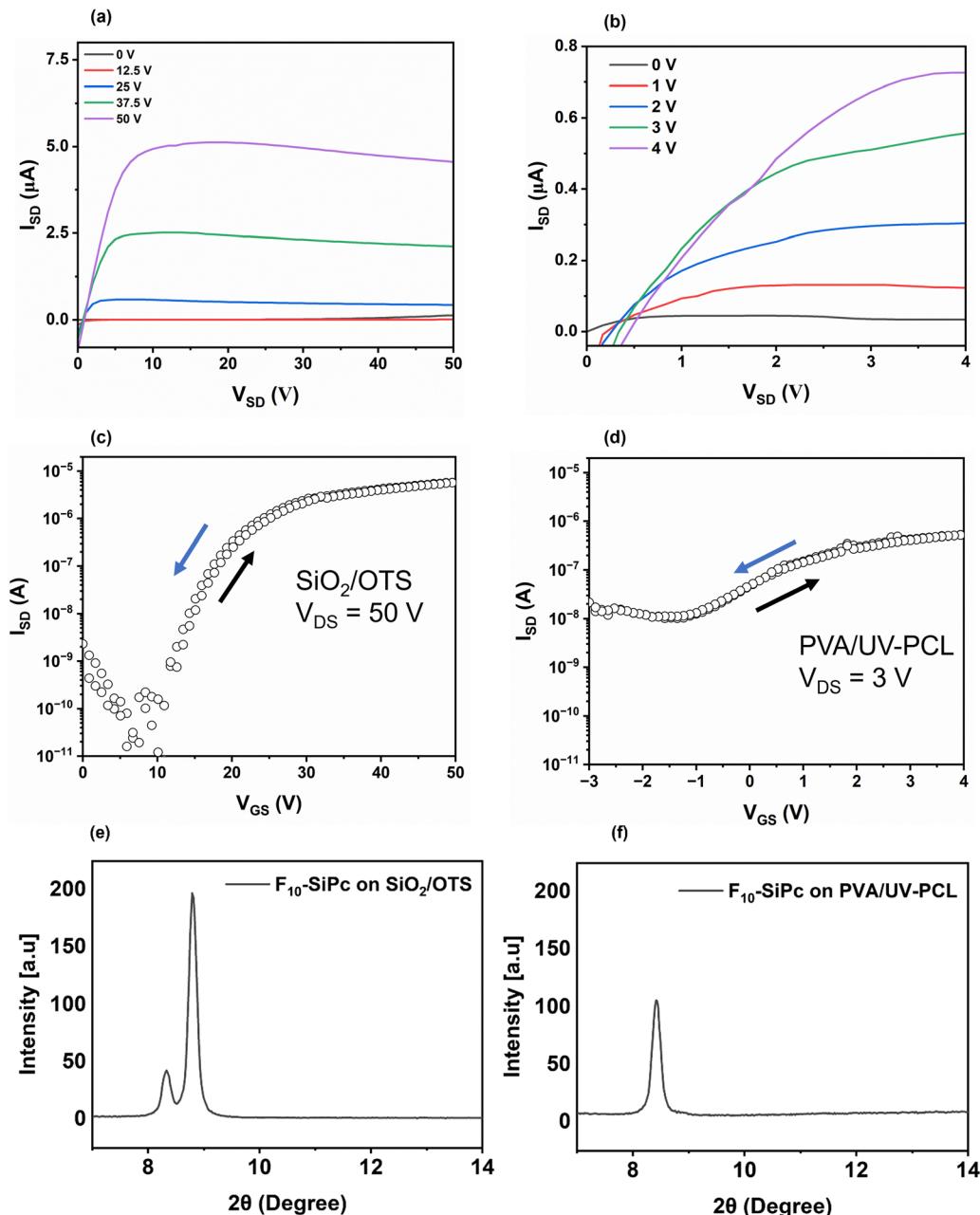


Fig. 4 Output curves of (a) SiO_2/OTS and (b) $PVA/UV-PCL$, and transfer curves of (c) OTFT on OTS treated SiO_2 and (d) on $PVA/UV-PCL$. The transfer characteristics curve versus V_{GS} were obtained for $V_{SD} = 50$ V and $V_{SD} = 3$ V, respectively. 1D XRD pattern for F_{10} -SiPc on (e) OTS treated SiO_2 and (f) on the $PVA/UV-PCL$ dielectric.

Table 2 Electrical data for OTFTs fabricated with SiO_2/OTS and biodegradable bilayer $PVA/UV-PCL$ dielectrics

Dielectric	μ_e ($cm^2 V^{-1} s^{-1}$)	V_T (V)	$I_{on/off}$
SiO_2/OTS	0.02 ± 0.007	12.7 ± 1.7	10^5 (at $V_{GS} = 50$ V)
$PVA/UV-PCL$	0.01 ± 0.016	-0.97 ± 1.4	10^1-10^2 (at $V_{GS} = 4$ V)

Our simulation reveals that $PVA/UV-PCL$ does not only offer a large capacitance but it also creates a charge-neutral and trap-minimized surface to enable low-voltage switching. Note that simple conversion of the subthreshold slope to the trap density

would lead to the values of $3.5 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ and $3.3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ for the transistors on SiO_2 and the polymer bilayer dielectric, respectively. The value for the SiO_2 based OTFT may reflect the actual trap density of states (DOS) in this device probed using numerical simulation (Table S1, ESI†). However, this method is likely to overestimate the trap density in the $PVA/UV-PCL$ based OTFT as the subthreshold slope in this sample is not only determined by trap filling but also affected by leakage currents. To further emphasize this argument, we calculated the internal distribution of electrons in the $PVA/UV-PCL$ based OTFT. Fig. 5c shows strongly depleted

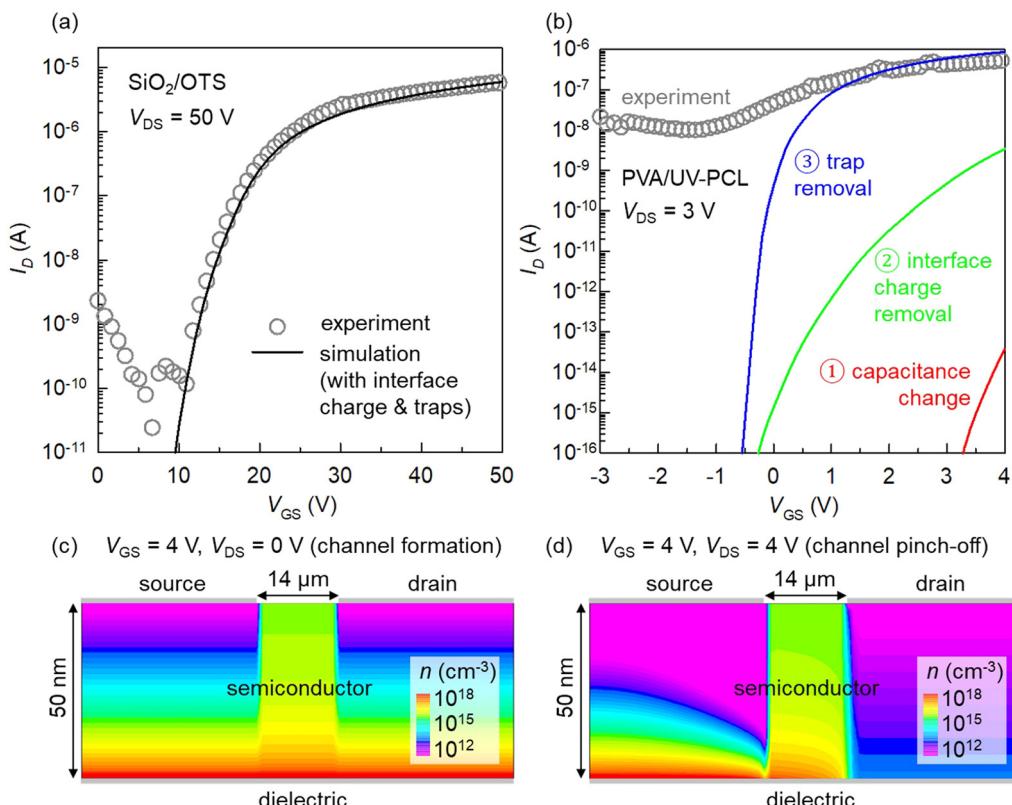


Fig. 5 Comparison between experimentally measured and numerically simulated transfer curves of the OTFT based on (a) SiO_2/OTS and (b) $\text{PVA}/\text{UV-PCL}$ dielectrics. Electron density (n) distribution on a log scale showing (c) channel formation and (d) pinch-off achieved by a low voltage in the OTFT based on the $\text{PVA}/\text{UV-PCL}$ dielectric.

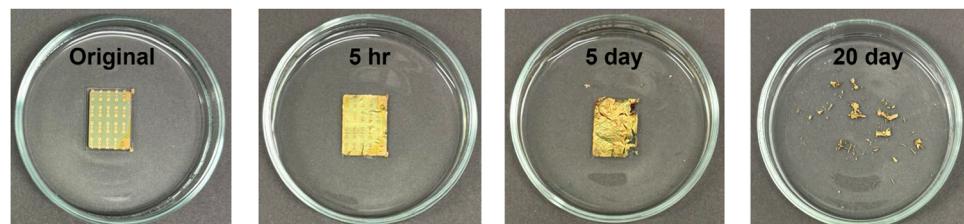


Fig. 6 Photographs of OTFTs taken at different intervals after being submerged in 1 M PBS ($\text{pH} \sim 10$) for accelerated degradation.

source/drain regions due to an injection barrier of 0.5 eV, yet the electron accumulation is clearly visible at the semiconductor/insulator interface at a V_{GS} value of only 4 V. Fig. 5d shows that by increasing the V_{SD} value from 0 to 4 V, this channel is successfully pinched-off at the drain side.

We demonstrated that these devices are capable of undergoing degradation under aqueous conditions. PLA resorption is influenced by temperature and pH, and degradation occurs slowly in phosphate buffer saline (PBS) with a pH of 7.4 at room temperature.⁸⁵ To investigate the resorption behaviour of the device, an accelerated *in vitro* degradation experiment was performed by immersing the OTFTs in a PBS solution (1 M, pH ~ 10) at room temperature. The accelerated degradation test demonstrates the complete disintegration of the device in

20 days (Fig. 6). We noticed that the PVA readily dissolved in PBS, and $\text{R}_2\text{-SiPc}$ completely disintegrated from the device within 5 hours. Afterward, a loss of structural integrity was seen, leaving PLA and gold. After 20 days, the whole device was disintegrated completely, leaving micro/nano gold particles in the PBS solution which are known to be excreted or absorbed by the human body.⁸⁶

We also investigated whether the degradation products obtained from the incubation of OTFT devices in an aqueous medium elicit cytotoxicity in mammalian cells. Degradation product extracts were prepared by incubating devices in culture medium at 37 °C for 7 days following a protocol modified from that in the study by Deng *et al.*⁸⁷ The metabolic activity of NIH 3T3 mouse fibroblast cultures following 24 hour incubation

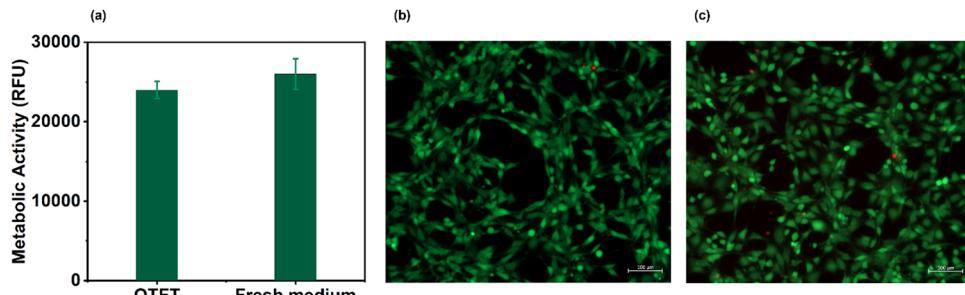


Fig. 7 (a) Metabolic activity of NIH 3T3 mouse fibroblasts following 24 hour incubation with degradation product extracts resulting from the incubation of OTFTs in culture medium for 7 days compared to incubation with fresh medium free of the degradation products, and (b) and (c) representative fluorescence images of the cells cultured with (b) and without (c) the degradation products and incubated with calcein-AM to label live cells (green fluorescence) and ethidium homodimer-1 to label dead cells (red fluorescence).

with these (OTFT) extracts was not significantly different from that of cultures incubated in fresh medium without the degradation products, whereby metabolic activity is an accepted metric for evaluating cell viability (Fig. 7a). The cells cultured in the presence and absence of degradation products were also incubated with calcein-AM to label live cells (green fluorescence) and ethidium homodimer-1 to label dead cells (red fluorescence). Fluorescence images show the presence of only a few dead cells under both culture conditions, confirming results from the metabolic activity assay (Fig. 7b and c). Overall, these preliminary cell viability studies suggest that the use of UV-PCL, F10-SiPc, Au electrodes, thiol treatment and PLA as a substrate do not cause cytotoxicity to mammalian fibroblasts following degradation of the OTFT devices in aqueous solutions.

Conclusions

Biocompatible and degradable organic transistors were presented utilizing a water-soluble polymer gate dielectric (PVA) and biodegradable substrate (PLA). The use of a PCL and PVA bilayer gate dielectric effectively lowered the V_T value of the R₂-SiPc n-type OTFT from 12.7 V to -0.97 V. Processing of the PLA device is critical for appropriate device function, including controlling the annealing conditions of the dielectric to avoid detrimental film roughening and thiol treating the gate for appropriate dielectric coating of the gate. Accelerated bio-disposability of OTFTs was shown by the successful disintegration of the developed devices in the PBS solution within 20 days. Cell viability assays were performed demonstrating negligible cell death and the absence of apparent cytotoxicity for the degradation products of OTFT devices. Owing to their non-toxic, biodegradable nature and low voltage performance, these devices show great promise for next generation environmentally friendly electronics and can minimize the effects of e-waste on the environment and ecosystem.

Experimental section

Materials

All chemicals were obtained from Sigma-Aldrich and utilized as received unless otherwise specified. Octyltrichlorosilane (OTS) (97%) was diluted with toluene (anhydrous, 99.8%) to form a

1% v/v solution in a glovebox. PCL diol ($M_w = 2000$ Da), toluene-2,4-diisocyanate (95%), PLA (230 kg mol⁻¹), PVA ($M_w = 31\,000\text{--}50\,000$ Da; 98–99% hydrolyzed) and 2-aminoethanethiol hydrochloride were procured from Sigma-Aldrich. Chromium-coated (Cr) tungsten rods and gold (Au, 99.99%) were obtained from Angstrom Engineering. Quartz-coated glass substrates measuring $15 \times 20\text{ mm}^2$ were purchased from Ossila Limited. Si wafers with a SiO₂ thickness of 230 nm and shadow masks were obtained from WaferPro and Ossila Limited, respectively. Deuterated chloroform, with a purity of 99.8%, and benzene, with a purity of 98%, were acquired from Cambridge Isotope Laboratories Inc. The synthesis of F₁₀-SiPc was carried out according to the literature.⁸⁸ 2,2-Dimethyl benzodioxinone-terminated PCL (UV-PCL) was synthesized according to the literature.²⁷

Preparation of a self-assembled monolayer solution

A solution of a self-assembled monolayer of hydrophilic thiols was prepared by dissolving 10 mM 2-aminoethanethiol hydrochloride in an ethanol solvent.

Preparation of the substrate and dielectric

PLA was selected to be used as a biodegradable substrate for the fabrication of OTFTs. A PLA solution of 80 mg ml⁻¹ was prepared by dissolving granules of PLA (230 kg mol⁻¹) in a chloroform solvent followed by filtering with 0.45-micron PTFE filters. The PVA solution was prepared by dissolving 80 mg of PVA in 1 ml of distilled water and then filtering it through a 0.45 μm cellulose filter. Next, UV-PCL was weighed and transferred into an opaque vial, where it was dissolved in toluene to obtain a concentration of 2 mg ml⁻¹. Afterwards, the vial containing UV-PCL was left on a hot plate set at 60 °C for 1 hour to guarantee full dissolution. The UV-PCL solution obtained was subsequently passed through a 0.22 μm PTFE filter into a separate opaque vial. These procedures were conducted under ambient conditions.

Fabrication of TFT

OTFTs were fabricated using a quartz-coated glass substrate ($15 \times 20\text{ mm}^2$). The quartz substrates were used as temporary substrates. The substrates were cleaned using a four-step method. The substrates were first sonicated for five minutes by sequentially immersing them in detergent mixed with



distilled water, distilled water, acetone, and methanol. Then, the substrates were rinsed with isopropanol and dried using a nitrogen stream. The PLA solution was then spin-coated at 2000 rpm for 90 seconds on glass substrates using a Laurell WS-650-23 spin coater. Subsequently, the PLA-coated glass substrates were vacuum annealed at 70 °C for 15 minutes. After baking the film of PLA, a film of ~3–4 microns was obtained. Next, using a shadow mask and the physical vapor deposition (PVD) method, a 2 nm layer of Cr (deposited at a rate of 0.5 Å s⁻¹) and a 50 nm layer of gold (deposited at a rate of 0.5 Å s⁻¹) were deposited on to the PLA substrate. Then, PLA substrates coated with gold were immersed in a hydrophilic thiol solution for one hour to form a self-assembled monolayer of thiols. The purpose of this monolayer is to enhance the hydrophilicity of the gold layer on PLA. Next, a solution of PVA (80 mg ml⁻¹) was spin-coated on gate electrode coated PLA substrate at 2000 rpm for 90 s followed by annealing at 50 °C for overnight to ensure that the PVA film was dried well. Afterwards, a 2 mg ml⁻¹ solution of UV-PCL was deposited on the PVA dielectric layer using spin coating at 2000 rpm for 90 s. The spin coated UV-PCL on the PVA dielectric film was crosslinked using an ultraviolet (UV) lamp with a wavelength of 254 nm. After that, the samples were transferred to a nitrogen glovebox connected to a thermal evaporator. The F₁₀-SiPc layer was thermally deposited by a PVD method, forming a 500 Å-thick film of F₁₀-SiPc using a square shadow mask. During the deposition procedure, the substrates were kept at room temperature, and the process was carried out at a rate of 0.2 Å s⁻¹ under a pressure of less than 2 × 10⁻⁶ torr. Then, using a shadow mask, a 2 nm layer of chromium (deposited at a rate of 0.5 Å s⁻¹) and a 50 nm layer of gold (deposited at a rate of 0.5 Å s⁻¹) were deposited to obtain source–drain electrodes with dimensions of $L = 30\text{ }\mu\text{m}$ and $W = 1000\text{ }\mu\text{m}$. A similar architecture was used for the fabrication of OTFTs with SiO₂ serving as the gate dielectric. SiO₂/Si wafers were first cleaned using the same cleaning process, and then they were treated with oxygen plasma for 15 minutes. To create a monolayer of OTS on the SiO₂ surfaces, the wafers were then immersed in a 1% v/v OTS solution in toluene for an hour at 70 °C. They were then rinsed with toluene and dried in a vacuum oven at 70 °C. Following surface treatment, the substrates were placed in a glovebox and a 50 nm layer of F₁₀-SiPc was deposited. Next, Cr–Au source–drain electrodes were deposited using similar settings to those previously mentioned.

Device characterization

The OTFT devices were tested in a N₂ glovebox utilizing a custom-built auto tester⁶² that was connected to a Keithley 2614B instrument. This configuration facilitated the control of the voltage between the source and drain (V_{SD}) and the voltage between the source and gate (V_{GS}), as well as the measurement of the current flowing between the source and drain (I_{SD}) in OTFTs. The output curves were obtained by sweeping the source–drain voltage (V_{SD}) from 0 to 4 V, while the gate–source voltage (V_{GS}) varied from -3 to 4 V. The transfer curves were obtained by setting $V_{SD} = 3\text{ V}$ for biodegradable polymer-gated OTFTs and 50 V for SiO₂-gated OTFTs. V_{GS} was then varied from

-3 to 4 V for biodegradable polymer-gated devices and from 0 to 50 V for SiO₂-gated devices. The values of electron mobility (μ_e), threshold voltage (V_T), and on/off current ratio ($I_{on/off}$) were computed by examining the transfer curves in the saturation regime which are modelled utilizing eqn (1):

$$I_{SD} = \frac{\mu_e C_i W}{2L} (V_{GS} - V_T)^2 \quad (1)$$

V_T was calculated by linearizing eqn (2) and determining the point where the line fitted to the on-state of the transfer curve intersects the x-axis. $I_{on/off}$ was determined by analysing the highest and lowest currents on the transfer curves. The capacitance (C_i) was measured using impedance spectroscopy with a Methrohm PGSTAT204 potentiostat/galvanostat workstation at a frequency of 10 Hz. The voltage was varied from 0 to 10 V. Eqn (2) was used to compute C_i , using the angular frequency (ω), real (Z''), and imaginary (Z') parts of impedance.

$$C_i = \frac{1}{\omega A} = \frac{Z''}{Z''^2 + Z'^2} \quad (2)$$

The calculation employed the total surface area (A) of each individual transistor. The mobility values were modified to compensate for variations in the channel length caused by shadowing effects that occur when depositing the source–drain electrodes.

Thin film characterization

Bruker D8 Endeavour apparatus was used to record the X-ray diffraction (XRD) patterns of 50 nm thick F₁₀-SiPc films on a SiO₂ dielectric treated with OTS, as well as a biodegradable bilayer dielectric (PVA/UV-PCL). Cu K α radiation ($\lambda = 1.5418\text{ \AA}$) was used, and the scan rate was set to 0.5° min⁻¹, covering a range of 7° < 2 θ < 14°.

Furthermore, each polymer film was subjected to a contact angle measurement (θ) with deionized (DI) water. This was obtained by dispensing 0.5 μl droplets of each reference liquid and taking an image of the drops with a VCA Optima goniometer camera (AST Products Inc.).

A Bruker Dektak XT profilometer was used to measure the dielectric layer thickness and roughness of the gate electrode surface. The thickness values were then used to correct the mobilities that were measured.

Numerical simulation

A physically based two-dimensional (2D) finite-element numerical solver was used for the simulation of OTFTs (ATLAS, Silvaco). Poisson's equation is solved on a 2D coordinate system to relate the potential variation to the space charge density,

$$\text{div}(\varepsilon_s \nabla \varphi) = -\rho \quad (3)$$

where φ is the electrostatic potential, ε_s is the semiconductor permittivity, and ρ is the space charge density. The electrical currents are modelled using a drift-diffusion mechanism,

$$\vec{J}_n = qn\mu_n \vec{E} + qD_n \nabla n, \quad (4)$$

and

$$\vec{J}_p = qp\mu_p \vec{E} - qD_p \nabla p, \quad (5)$$

where \vec{J}_n and \vec{J}_p are the electron and hole current density vectors, respectively, \vec{E} is the electric field vector, μ_n and μ_p are the electron and hole mobility, respectively, D_n and D_p are the electron and hole diffusion coefficients, respectively, q is the elementary charge, n and p are the electron and hole concentrations, respectively. The simulator self-consistently solves eqn (3)–(5) over a 2D mesh that is defined to mimic the cross-section of a fabricated device. The two major outcomes of this process are geometric solutions of the electrostatic parameters and terminal current–voltage characteristics representing the integration of current densities under different bias conditions. An exponential trap DOS at the LUMO edge and a fixed interface charge density were added for the simulation of an OTFT with SiO_2/OTS . The functional form of trap DOS is

$$\text{DOS}(E) = \frac{H_A}{k_B T_A} \exp\left(-\frac{E_c - E}{kT_A}\right) \quad (6)$$

where E is the energy, H_A is the total density of acceptor-like trap states, k_B is the Boltzmann constant, T_A is the characteristic temperature dictating the energetic width of acceptor-like traps, and E_c is the energy of the conduction band (or LUMO) edge.

Cytotoxicity evaluation

The cytotoxicity of degradation products from the incubation of OTFT devices in a culture medium was carried out according to a protocol modified from the study by Deng *et al.*⁸⁷ Briefly, devices ($15 \times 20 \text{ mm}^2$) were sterilized by incubation in 70% ethanol for 10 minutes, rinsed twice in PBS and incubated in 1 ml of high glucose Dulbecco's modified Eagle's medium (DMEM) for 7 days at 37°C . The media samples comprising degradation products were then supplemented with fetal bovine serum (FBS) to a final concentration of 10% v/v before being used for cell experiments as degradation product extracts. NIH 3T3 mouse fibroblasts were seeded in DMEM supplemented with 10% FBS at a density of 10 000 cells per well in a 48 well plate and allowed to attach for 24 hours in an incubator at 37°C in an environment characterized by 5% CO_2 and 95% relative humidity. Subsequently, the medium was replaced with the degradation product extracts or fresh medium (control) and incubated for an additional 24 hours. Select cultures were evaluated for the metabolic activity of the cells with an alamarBlue assay (Thermo Fisher Scientific), according to the manufacturer's instructions. Additional cultures were incubated with 2 μM calcein AM (Invitrogen; live cell staining; green fluorescence) and 4 μM ethidium homodimer-1 (Sigma Aldrich; dead cell staining; red fluorescence) in DMEM for 10 minutes and imaged using a Zeiss Axio Observer 7 microscope. The degradation products from 5 OTFT devices were tested for both cell viability assays.

Data availability

The data supporting this article have been included as part of the ESI.†

Conflicts of interest

There are no conflicts to declare.

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