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Ultra-simplified fabrication of all-silver memristor arrays

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Brain-inspired neuromorphic computing strives to emulate the human brain's remarkable capabilities, including parallel information processing, adaptive learning, and cognitive inference, while maintaining ultra-low power consumption characteristics. The exponential progress in cloud computing and supercomputing technologies has generated an increasing demand for highly integrated electronic storage systems with enhanced performance capabilities. To address the challenges of tedious fabrication, we innovatively offer a feasible strategy: using weaved silver electrodes combined with *in situ* formed silver oxide insulating layers to create a high-performance two-terminal memristor array configuration. This memristor possesses a high ON/OFF ratio (above 10^6) and good durability (200 cycles). Moreover, its innovative weaving-type configuration enables higher integration density while maintaining conformal attachment capability onto the skin. Our ultra-simplified fabrication strategy provides a novel alternative approach for streamlining fabrication processes, enabling the realization of advanced device integration and system miniaturization.

Introduction

Great advancements in computing neuromorphic systems based on memristors have held immense potential owing to their brain-like multilevel parallel information processing capabilities, lower energy consumption, and extended operational lifetime.[1–9] The two-terminal memristor, a fundamental component of brain-like neuromorphic computing, operates by altering its resistance value in response to signal excitation. Owing to their precise controllability, low power consumption, multi-level storage capabilities, and a large storage window, memristors hold potential for applications in optical control devices and neural computing, particularly in tasks such as facial classification,[10] vision imaging,[11] and sparse coding.[12] To overcome the limitations of conventional electronic systems, the integration of multifunctional components (*e.g.* on-chip sources, detectors, and storage devices) into a single microelectronic platform has been identified as a rational and effective strategy for advancing size scaling and intelligentization initiatives in the post-Moore era.[13–17] To advance integration and miniaturization, textile-based electronics provide an innovative platform for the development of wearable memristor-based applications, offering a versatile and compact solution for next-generation wearable computing and storage electronics.[16–18] Dong *et al.* designed a non-volatile memory array utilizing

crystalline silicon/amorphous silicon (Si/a-Si) core/shell NWs with highly controllable switching threshold voltages.[19] However, conventional two-terminal resistive switching memory devices have been limited by their intricate and labor-intensive fabrication processes.[20–30] Herein, we present an innovative and remarkably simple strategy for fabricating memristor arrays by weaving surface-oxidized metal wires with pristine metal counterparts, thereby bypassing the complex and time-consuming processes inherent to conventional fabrication approaches. Meanwhile, the miniaturization and space utilization of the device are greatly improved by a crossbar of only 0.5 mm in the silver-wire array. This work establishes a novel paradigm for streamlined fabrication and flexible integration of next-generation electronic devices.

Experimental section

Materials

Commercial Ag wires (D: 30 μm, L: 1 cm) were bought from MSC KOREA, M1536.

Fabrication method

The commercial Ag wires were directly adopted as the electrode of the memristor. Plasmon treatment (70 W, O_2 30 sccm) was utilized to oxidize the Ag electrode *in situ* into Ag_2O, serving as the insulating layer of the memristor. Subsequently, the Ag wire with an AgO-oxidized surface was woven with another Ag electrode with a vertical-horizontal cross configuration.

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Characterization

Surface morphology was observed under a scanning electron microscope (SEM) (FEI/Quanta 450 FEG). All electrical performance measurements of the memristor were performed on a Keysight B1500A Semiconductor Device Analyzer. The programming pulse voltage was recorded on the Oscilloscope DS1202Z-E.

Results and discussions

Fabrication and characterization of the textile-type memristor

Fig. 1a presents the basic structure scheme of the memristor array, with a magnified schematic diagram of a single unit in the array. A photo illustration of the array is shown in Fig. 1b. This textile-configuration memristor adopts an electrode–insulator–electrode structure, utilizing commercially available Ag wires (30 μm diameter, 1 cm length) as the electrodes. Metal–insulator–metal (MIM) configuration of two-terminal resistive non-volatile memristors is a well-known structure.[31,32] According to the conventional procedure for fabricating memristors, the separate processing of the silver oxide insulating layer[33,34] complicates the whole preparation process. Alternatively, we ingeniously oxidize the Ag electrode *in situ* to form the insulating layer of the memristor, silver oxide, achieved through a straightforward plasmon treatment process (70 W, O_2 30 sccm, 1–2 minutes). This innovative approach significantly simplifies the fabrication technology, making the process more efficient and accessible. Subsequently, the Ag wire with AgO-oxidized surface were woven with another Ag electrode in a vertical-horizontal cross configuration (Fig. 1c). Actually, metallic oxide generally serves as the insulating layer in the memristors or neuromorphic systems.[35] To verify the equivalent effect of our method to traditional atomic layer deposition (ALD) methods, scanning electron microscopy (SEM) was carried out. Fig. 1d shows SEM images of a pristine Ag electrode (left panel), a plasmon-treated Ag electrode (middle panel) and an ALD-deposited Ag_2O of Ag electrode (right panel), with the enlarged image presented at the bottom. The morphological similarity between Ag_2O formed by plasmon treatment and by ALD demonstrates the rationality of our strategy. The XPS spectra of the Ag electrodes before (pristine, black curve) and after oxidation (blue curve) are presented in Fig. S1. The prominent peak at 530 eV in the oxidized sample's spectrum corresponds to the O 1s orbital, confirming the formation of Ag_2O on the electrode surface.

Electrical performance of the single unit of the memristor

Fig. 2a presents the electrical performance of a single all-silver memristor device. An electroforming process is required to initiate the high initial OFF resistance state for high initial OFF resistance state (10^7 Ω) by applying a forming voltage of around 0.01 V to activate the bidirectional RS behaviour. Specifically, the maximum nonlinearity achieves a value of 10^6 under the relatively small voltage of 0.5 V (Fig. S2). Additionally, a steep
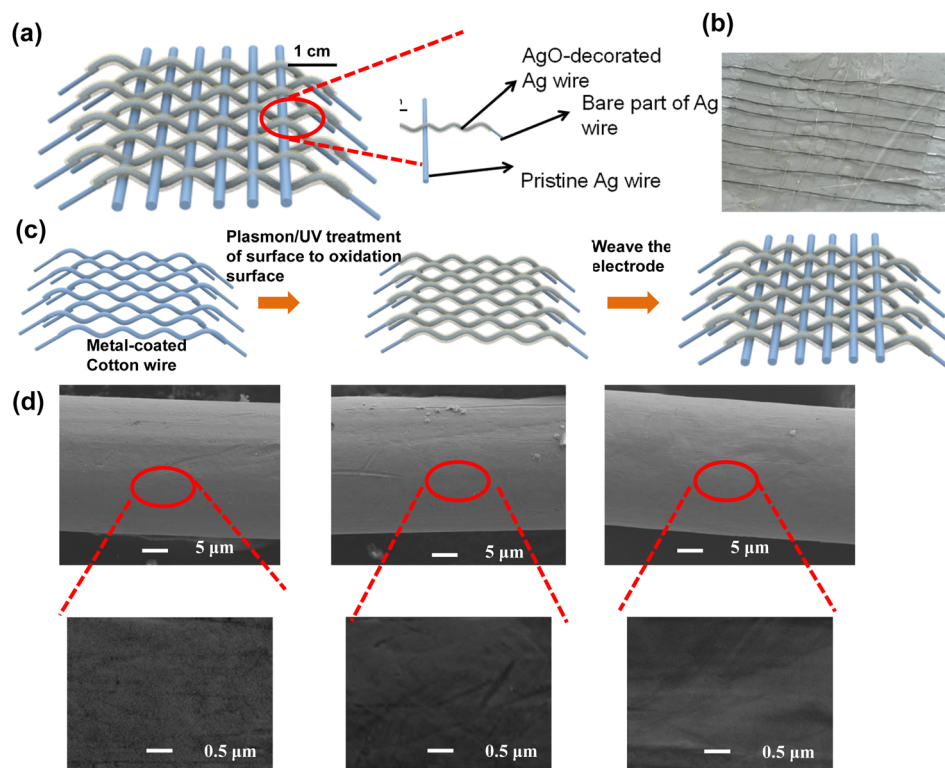

Fig. 1 (a) Schematic illustration of an integrated all-silver memristor array. (b) Photo image of a all-silver memristor array. (c) Fabrication process of the memristor array. (d) SEM images of pristine Ag electrode (left panel) and Ag electrode after plasmon treatment (middle panel) and Ag electrode decorated with AgO by ALD (right panel).
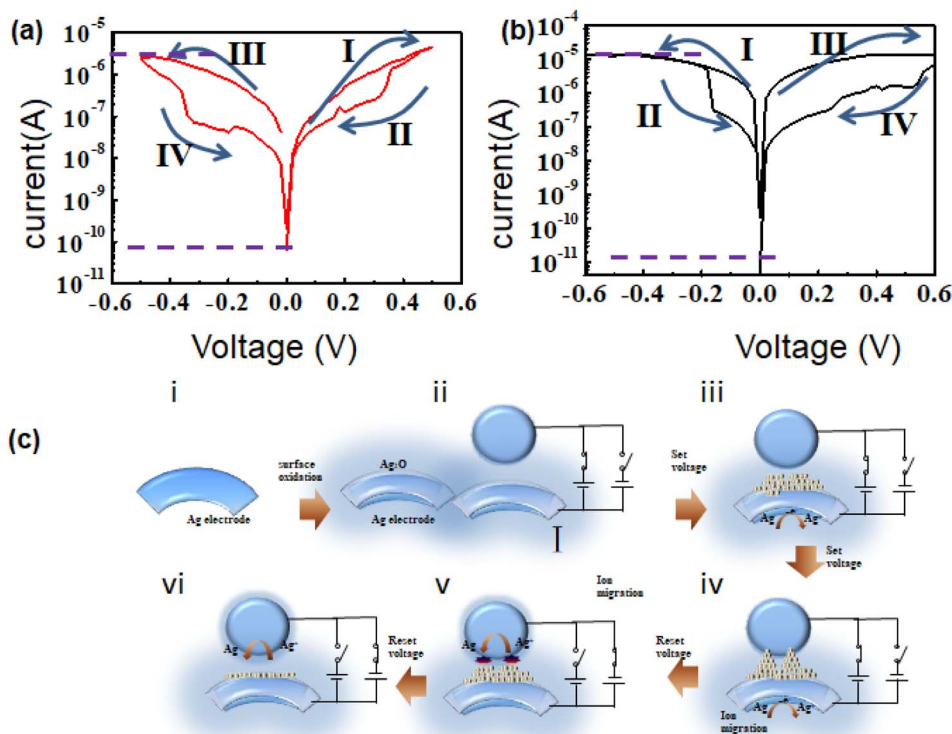
Fig. 2 Memory device characteristics. (a) The typical $I–V$ curve of device under an I_{cc} of 100 μA. (b) The typical $I–V$ curve of the device in back-forward sweep (0 V → −0.5 V → 0 V → 0.5 V → 0 V). (c) The mechanism of the textile-type memristor: (i) the pristine Ag electrode; (ii) Ag electrode undergoes *in situ* oxidization to form the insulating layer of the memristor; (iii) the application of voltage induces oxidation reaction between the vertically oriented and horizontally oriented silver electrodes, referred to as the "writing" process; (iv) continual increase in the voltage induces Ag filament growth, eventually bridging the bottom and top Ag electrodes; (v), subsequently a converse voltage (referred to as reset voltage) induces an opposite redox reaction (Ag^+ reduces to Ag), leading to the dissolution of the conductive filament and a corresponding decrease in conductivity; (vi) continuous negative bias causes complete filament collapse, resetting the device to a high-resistance state, denoted as the "erasing" process.

variation in the resistance from the initial high-resistance state to a low-resistance state occurs under a small positive voltage of about 0.01 V, corresponding to the formation of silver conductive filaments. In particular, the relatively low threshold voltage to open the device indicates low-voltage operation. It also demonstrates that the handy fabrication process does not affect the other electrical properties of the device (ON/OFF ratio, power consumption). The device shows bipolar resistive switching behaviour due to the bipolar transport characteristic of the Ag filament mechanism.[36,37] To verify the bidirectional TS character, the sweep path of 0 V → −0.5 V → 0 V → 0.5 V → 0 V was operated on the device. Fig. 2b illustrates the back sweep of the device with no pronounced variation compared to the forward sweep. This is the characteristic of the bipolar transport behavior. Furthermore, it can be observed that whether forward scan or back sweep, the window after the second return to the zero point is larger than the previous one. Due to the accumulation and variation of charges during the reverse scanning process, there is no rectification characteristic.

Fig. 2c systematically illustrates the mechanism of the textile-based memristor. As shown in Fig. 2c(i) and (ii), under the 2–3 min plasmon condition, the Ag electrode undergoes *in situ* oxidization to form the insulating layer of the memristor,

silver oxide, in the absence of an applied electrical voltage. The application of voltage induces oxidation reaction between the vertically oriented and horizontally oriented silver electrodes (Ag at the negative potential terminal oxidizes into Ag^+), along with a gradual conductivity increment, which is referred to as the "writing" process (as shown in Fig. 2c(iii), corresponding to Fig. 2a(I)). A continual increase in the voltage induces Ag filaments to grow, eventually bridging the bottom and top Ag electrodes (as shown in Fig. 2c(iv), consistent with Fig. 2a(II)). Subsequently a converse voltage (referred to as the reset voltage) induces an opposite redox reaction (Ag^+ reduces to Ag), leading to the dissolution of the conductive filament and a corresponding decrease in conductivity (as shown in Fig. 2c(v), corresponding to Fig. 2a(III)). Continuous negative bias causes complete filament collapse, resetting the device to a high-resistance state, denoted as an "erasing" process (Fig. 2c(vi) consistent with Fig. 2a(IV)).

The stability of the devices is a fundamental prerequisite for neuromorphic applications. Fig. S3 shows the nearly identical consecutive $I–V$ performance of the memory device in the initial cycle (red curve), 10 cycles (blue curve), 20 cycles (deep-red curve) and 200 cycles (purple curve). The little deviation with respect to each curve reveals the excellent cycle stability.

Furthermore, stability largely depends on relaxation behaviour, which was evaluated by pulse voltage measurements. The endurance of the low-resistance state and the high resistance state was verified by consecutive programming high-voltage pulses and low-voltage pulses, respectively. Fig. S4 illustrates that the device shows over 200 cycles under 2 V voltage pulses (red line, low-resistance state) and 0.3 V read pulses (blue line, high-resistance state) with a pulse width of 100 ms and an interval time of 1 s (1000 ms). Whether in the high-resistance state (HRS) or the low-resistance state (LRS), the retention time can last 50 ms, demonstrating good retention behaviour. Moreover, the device maintains its state over the test time range that the oscilloscope can achieve (60 seconds, 6000 milliseconds). The test provides critical evidence regarding the device's ability to maintain consistent performance, which is essential for reliable operation in neuromorphic systems. The relaxation characteristics of the flexible threshold switching show a relaxation time from 1 ms to 10 s.[38] Fig. 3a displays the typical current–voltage (I–V) curve of the device under varying compliance currents (yield current).[39] The ON/OFF ratio remains nearly consistent as the compliance current varies, although it results in a slight reduction in the resistance window. The maximum allowable compliance current for reliable device operation is approximately 10^{-3} A. This indicates that the device can maintain stable performance within this current range, which is crucial for ensuring consistent functionality. Besides current, the device also shows high tolerability to a wide voltage range. Fig. 3b presents the typical I–V curves of the device under varied sweep ranges (−1–1 V, −0.8 V–0.8 V, −0.6 V–0.6 V, −0.4 V–0.4 V), verifying that our memristor can tolerate a wide voltage range. Moreover, the comparative analysis between our work and ref. 45 indicates that the handy fabrication process does not affect the other electrical properties of the device (ON/OFF ratio, power consumption).

Fig. S6 illustrates the endurance of the device in the bending state (I–V performance of the memory device in the initial cycle,

10 cycles, 20 cycles, and 200 cycles) at a radius curvature of 38.71 cm^{-1}. The approximate curves indicate that the device exhibits rational applicability in bending and wearable scenarios. This suggests that the device can maintain its functionality and performance even when subjected to mechanical deformation. It is well-known that nonidealities have a significant impact on the training process. The nonlinearity can be defined at voltage V_{ref} as the ratio of the conductance at that voltage to the conductance at half that voltage.[40,41] The nonlinearity can be defined as follows:[42]

$$\text{Nonlinearity} = \frac{G(V_{\mathrm{ref}})}{G\left(\frac{V_{\mathrm{ref}}}{2}\right)} \qquad (1)$$

where, $G(V_{\mathrm{ref}})$ and $G(V_{\mathrm{ref}}/2)$ are the conductivities at the reference voltage and the conductivity at half the reference voltage, respectively. In this work, we also investigated the effects of I–V nonlinearity for our textile-type Ag/AgO/Ag memristor.[40] To realize a wide range of resistance states and to evaluate I–V nonlinearity, incremental positive sweeps were utilized to gradually reset the device from the low-resistance state to the high-resistance state. I–V curves of two subsets of all achieved states are shown in Fig. 3c and d. Compared with high-resistance states (in Fig. 3d), the low-resistance discrete states (in Fig. 3c) exhibit more linear behavior and exhibit minimal variability in nonlinearity. The effect of different plasmon treatment times on the properties of the devices was also studied. Fig. 3e–g present performances under different plasmon treatment conditions (1 min, 3 min and 5 min) applied on Ag. It can be observed that the device obtained by 1 min plasmon treatment turns out to have excellent properties. It can be observed that the device obtained by 1 min plasmon treatment turns out to have excellent properties, yet shows degraded properties with 3–5 min plasmon treatment. This ultra-feasibly processable all-silver memristor method can be equivalently applied to other metal electrodes for constructing a memristor.
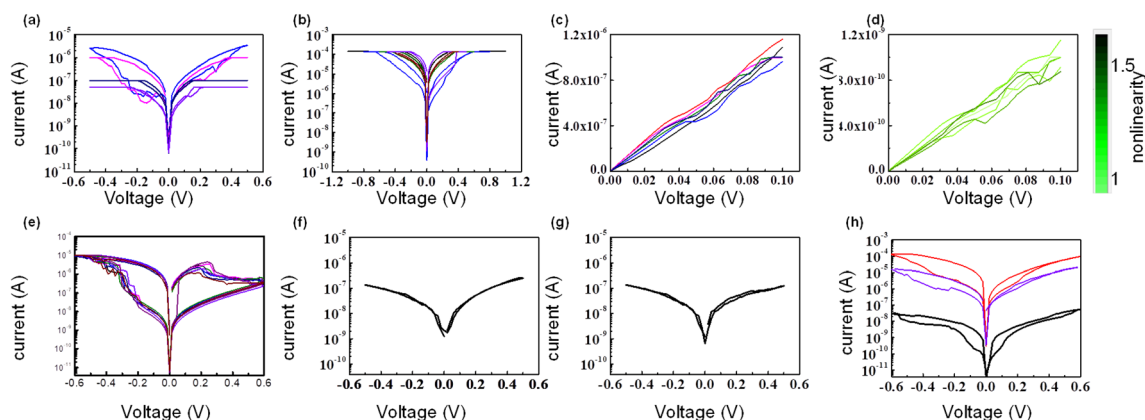

Fig. 3 (a) The typical I−V curve of device under varied compliance currents of 1 µA (blank curve), 0.05 µA (red curve), 0.01 µA (blue curve), 0.005 µA (pink curve). (b) The typical I−V curve of device under varied sweep ranges (−1–1 V, −0.8−0.8 V, −0.6−0.6 V, −0.4−0.4 V). (c and d) I−V sweeps of an Ag/Ag$_2$O/Ag device are shown for (c) a subset of the low-resistance region, and (d) a subset of the high-resistance region. For all curves, only the voltage range from 0.0 V to 0.5 V was considered. (e−g) The performance of devices under different plasmon treatment times: (e) 3 min, (f) 5 min, and (g) 10 min. (h) The performance of devices with different metals: Ag/Ag$_2$O/Pt (red curve), Ag/Ag$_2$O/Ag (violet curve), and Al/Al$_2$O$_3$/Al (blank curve).

Table 1 The comparison of the performance of different memristor materials

	R_{HRS}/R_{LRS}	Positive pulse voltage	Negative pulse voltage	Endurance [cycles]
Ag/AgO/Pt	7×10^6	0.9 V	−0.8 V	200–300
Ag/AgO/Ag	2×10^6	+6 V		200
Al/Al$_2$O$_3$/Al	10^4	1.19 V	−1.39 V	50–100
Cu/Cu$_2$O/Cu	3×10^4	0.5 V	−0.5 V	70–120

Fig. 3h presents the *I–V* characteristics of Ag/AgO/Pt (red curve), Ag/AgO/Ag (violet curve), and Al/Al$_2$O$_3$/Al (black curve). The typical resistance characteristics and high ON/OFF ratios demonstrate the versatility and effectiveness of our fabrication strategy. A majority of two-terminal non-volatile memristors with a MIM configuration share a metal filament mechanism.[43,44] Ag/Ag$_2$O/Pt (red curve) and Ag/Ag$_2$O/Ag (violet curve) adopt an Ag filament mechanism, whereas Al/Al$_2$O$_3$/Al (blank curve) utilizes an Al filament mechanism. Therefore, the performance characteristics of the devices vary significantly depending on the electrode and insulating materials. The significantly higher output current observed for Ag/Ag$_2$O/Pt (red curve), with an Ag filament mechanism, than that for Al/Al$_2$O$_3$/Al is consistent with the metal conductivity ordering. Ag is known to have higher electrical conductivity than Al.[45] To further verify the role of Ag electrodes, we also compared *I–V* characteristics of control devices with symmetric non-Ag electrodes Pt/Ag$_2$O/Pt, demonstrating its lack of resistive switching characteristics (Fig. S5). This can be attributed to the higher reduction potential of Pt electrodes which prevents the electrochemical formation of conductive filaments (compared to Ag$^+$/Ag).

Principally, the resistive switching behaviors of filamentary memristors are significantly influenced by ion migration and the growth of conductive filaments within the memristive layer. The surface of Ag wire undergoes oxidation, forming a thin layer of Ag$_2$O decorated on the Ag surface.[34,46] When an external voltage is applied, Ag undergoes oxidation, transitioning to Ag$^+$ ions, which migrate and form conductive pathways, thereby transitioning the device to a low-resistance state (LRS). Conversely, when the voltage is reversed or removed, these filaments rupture, returning the device to a HRS. The efficiency and stability of ion migration directly impact the device's switching speed, endurance, and reliability. In our previous work,[47] we utilized a transmission electron microscope (TEM) as a powerful tool to study the mechanism of memristor devices by implementing the device in a coplanar structure and using the ion beam milling technique. However, this method is restricted in the case of this device because the relatively small contact area between the orthogonal Ag electrodes is restrictive. Based on the resistance-change deviation performance of different metal electrodes in Fig. 3h, combining the inertness characteristic of silver oxide insulating layer without introducing any new mechanism in the resistance, providing the explanation that Ag filament-mechanism is the mechanism of this device.[35,48,49] The resistive-switching mechanism can be comprehensively elucidated through systematic analysis of the current–voltage (*I–V*) characteristics, particularly focusing on the high-resistance state (HRS) during each voltage sweep cycle. To gain deeper insights into the fundamental physical processes governing the resistive switching behavior, the referred equations are expressed as follows:

$$I = V^2 \exp\left(\frac{-kd}{V}\right) \quad (2)$$

$$I = AT^2 \exp\left(\frac{-q\varphi}{kT} + q\left(\frac{q^3 V}{4\pi\varepsilon}\right)^{1/2}\right) \quad (3)$$

where, A represents Richardson's constant, T denotes the absolute temperature, ε signifies the dielectric permittivity, φ corresponds to the barrier height, k stands for Boltzmann's constant, and q indicates the electronic charge. The Fowler–Nordheim (FN) tunneling process is predominantly responsible for carrier transport in the high-resistance state during the first voltage sweep. This mechanism suggests that electrons tunnel through the thin insulating barrier under the influence of a strong electric field, which is consistent with the observed behavior in the initial stages of resistive switching. As shown in Fig. S7, ln(*I*) exhibits a linear relationship with the square root of *V*, which provides strong evidence for the dominance of the thermionic emission (TE) process in carrier transport.[50,51] This is a typical Ag filament rule of reducing filament gap by barrier height reduction through an increasing number of voltage sweeps. We also compared the performance of our work with other typical bipolar memristors, which are listed in Table 1.

To further verify the reproducibility of the performance, the normal distribution diagram for sensing of 20 identical samples
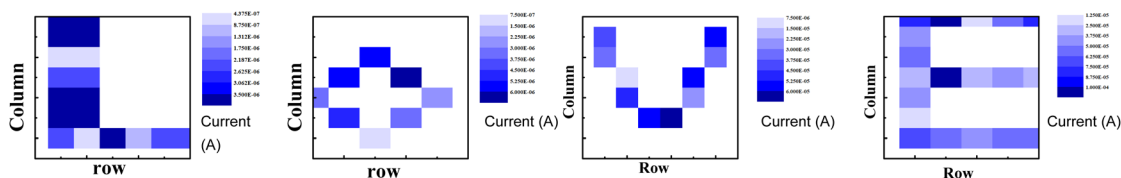

Fig. 4 The 2D mapping of the current distribution of memristor array to show an "L", "O", "V", and "E".

Table 2 The comparison of the performance of typical two-terminal memristors

	R_{HRS}/R_{LRS}	Positive pulse voltage	Negative pulse voltage	Endurance [cycles]	Ref.
Ti/Pt/BP/HfO$_2$/Cu	10^5	0.9 V	−0.8 V	1000	11
Gr/SiO$_x$/Gr	10^6	+6 V		400	20
TiN/Al/Ti/Al$_2$O$_3$/TiO$_{2−x}$/TiN/Al/Ti	10^5	1.19 V	−1.39 V	10^5	21
Al/G-O film/Al	10^8	0.5 V	−0.5 V	∼100	22
ITO/MoSe$_2$/Bi2Se$_3$/Ag	2.83×10^3	−6 V	6 V	1000	23
Au/NiSAs/N–C/ITO	10^3	+5 V	−8 V	500	24
Ti/Pt–MoS$_2$–Ti/Pt	10^2	2 V	−2 V	10^7	25
Cu/pV$_3$D$_3$/MLG/Al	10^4	−4 V	4 V	100	26
Ag/MoS$_2$/Ag	10^7	0.18 V		—	27
Gr/MoS$_{2−x}$O$_x$/Gr	10^6	+0.35 V	−0.48 V	2×10^7	28
Pt/TiO$_x$/HfO$_2$/Pt	—	1.5 V	−1.5 V	1.06×10^3	29
Ag/CVD-15-18L-hBN/Au	10^{11}	5 V/2 µs set pulses, 0.1 V/2 µs read pulses		80 000	30
Ag/Ag$_2$O/Ag	10^7	2 V pulses for LRS, 20 mV pulses for HRS		200	Our work

is presented (Fig. S8). As shown in the normal distribution diagram for sensing, the ON/OFF ratio and threshold voltage are respectively concentrated at 1.2×10^6 and 0.012, verifying good reproducibility of our device, which offers reliability for practical applications.

Weaving represents a promising approach for realizing flexible and integrated electronic systems. Yue Liu has proposed textile-type memristor arrays that are mechanically durable to withstand hundreds of bending and sliding deformations, seamlessly unified with sensing, power-supplying, and displaying textiles to form all-textile integrated electronic systems for the new generation of human–machine interactions.[52] The advantage of simplified processing, flexible integration, miniaturization and high-efficient space utilization enables the devices to be preferable for highly integrated weave-type devices. On the basis of a single memristor device, a 6 × 8 memristor array has been constructed (this 6 × 8 configuration aligns with the shapes of letters of "L", "O", "V", and "E"). Each pristine silver electrode and each silver electrode decorated with a thin silver oxide insulating layer on the surface (having experienced *in situ* oxidation treatment) were woven with a vertical-horizontal cross configuration (Ag/Ag$_2$O/Ag) to construct the memristor array. Prior to the testing on the array, a normal distribution diagram of 48 devices, with regards to current distributions across all cells, retention stability, and variation in write/read pulses, is shown in Fig. S9. The current error, write/read pulses variation, and retention time are concentrated at 5.9%, 5.2%, and 5444 ms, respectively. This memristor array, with its well-characterized and consistent performance, can be readily applied to coding applications. The array adopts a loose contact mode, where a 0.5 V voltage was applied between the longitudinal electrode and the transverse electrode. The current is almost 0 because the electrodes are not fully in contact. The longitudinal electrode and the transverse electrode are in a contact state when an external force is applied to each device. The greater the pressure, the larger the contact surface becomes, leading to a reduced resistance and an increase in current. As shown in Fig. 4, the output current distribution shows a given pattern "LOVE". Meanwhile, only the sensing pixel showed output signals according to the

approaching process, indicating no crosstalk in the array. The potential sources of error and limitations are attributed to two aspects: (1) the stability issue of constituent materials compromises device reliability and operational lifespan, and (2) limitations in theoretical modeling necessitate further refinement and optimization of these models to enhance their predictive accuracy and utility in guiding device design.[53–55] The linear and continuous conductance regulation,[56] as well as the ability to faithfully replicate multimodal perception[57] has emerged as a research hotspot (Table 2).

Conclusion

The ever-increasing development of integration and miniaturization of advanced electronic devices and systems has imposed much higher requirements for continuously deepening and exploring novel integrated electronic systems. As a summary, we ingeniously offer a considerably simple approach to construct an all-silver memristor without other reagents, featuring a fibre-style configuration to achieve high-level integration and miniaturization. Our all-silver memristor array exhibits a high ON/OFF ratio (above 10^7) and good durability (200 cycles). This straightforward preparation method significantly enhances processing efficiency while maintaining high performance and integration, holding great practical significance. Additionally, the weaving-type memory array conformally attaches to the skin, offering a novel pathway for the feasible processing and flexible integration of highly integrated and miniaturized memristors. This ultra-feasible and high-efficiency fabrication strategy provides a novel alternative approach for streamlining fabrication processes, enabling the realization of advanced device integration and system miniaturization. It opens a novel avenue for the accessibility of feasible processing and flexible integration of high-level integrated and miniaturized memristors.

Conflicts of interest

The authors declare no competing financial interest.

Data availability

All data generated or analyzed during this study are included in this published article and its SI files. The datasets generated and/or analyzed during the current study are available from the Royal Society of Chemistry publisher and are accessible *via* https://pubs.rsc.org/en/content/articlepdf/2025/NA/D5NA00611B?page=search. See DOI: https://doi.org/10.1039/d5na00611b.

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