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Infiltration issues in printed mesoporous carbon perovskite solar cells: a troubleshooting guide

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Printed mesoscopic carbon perovskite solar cells (CPSCs) represent a potential frontrunner to perovskite commercialisation due to their inherent stability and easily scaled fabrication methods. Devices consist of three screen printed mesoporous layers of TiO_2, ZrO_2 and carbon, which are subsequently infiltrated with perovskite. It is well established that complete infiltration, or filling, of the base TiO_2 layer is key to achieving peak performance and reproducibility in both lab-scale devices and modules. A thorough understanding of the factors influencing infiltration is therefore essential for both lab-scale research and scale-up. TiO_2 infiltration is easily examined by optical microscopy through the glass substrate. This work identifies common characteristic infiltration defects at multiple scales, caused by specific issues in the manufacturing process such as mesh marking, printing issues, contaminant damage and environmental fluctuations. Likely causes and potential solutions are presented for each type of defect, to produce a troubleshooting reference resource for tackling this problem at multiple scales. This should help enhance lab-scale reproducibility providing a simple method for quality control in future large-scale ventures.

Introduction

Since their advent in 2009, perovskite solar cells have quickly evolved to produce champion PCEs of 25.6%, surpassing that of many commercially available silicon modules.[1,2] Amenable to solution-based processing, perovskites therefore represent an exciting opportunity for developing low-cost thin film photovoltaics.

However, champion efficiencies are generally attained at small scale and achieved using non-scalable techniques such as spin coating.[2] Additionally, devices are prone to degradation on exposure to light, water, and oxygen.[3–5] This is particularly pertinent in the case of high-performance planar devices, which frequently rely on expensive and unstable hole transport materials such as SPIRO-OMeTAD to achieve peak performance.[6,7]

Mesoporous carbon perovskite solar cells (CPSCs) represent a more stable, scalable alternative to planar architectures. Despite historically exhibiting much lower PCEs than planar architectures, champion device performance has risen dramatically in recent years to a record of 19%.[8,9]

Devices consist of three screen printed mesoporous layers of TiO_2, ZrO_2 and carbon, which are subsequently infiltrated with perovskite precursor.[10] The lack of an expensive organic hole transport material reduces the manufacturing cost and improves stability, which is further enhanced by the thick hydrophobic

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carbon back electrode.[11,12] Incorporating 4-aminovaleric acid, which passivates surface defects and inhibits MAI loss by sitting at grain boundaries has enabled these devices to pass stringent IEC61215:2016 standards, highlighting their resilience under environmental stress.[13–15]

However, perhaps the main advantage of these cells is the ease of large-scale fabrication. Screen printing is already industrially available at multiple scales using relatively low-cost equipment.[16] As such, 220 cm^2 active area modules of over 9% PCE have already been presented in the literature.[17]

One of the key requirements for producing high-performing CPSCs is achieving complete infiltration, or filling, of the base TiO_2 layer.[18–21] Unfilled, perovskite free voids at the base of the stack represent areas of poor perovskite–electrode contact, producing low currents and limited charge extraction, as well as reducing light absorption.[18,21] Stability is also impacted, as poor stack filling has been linked with high defect density, producing increased recombination and decreased lifetime.[18–20]

Infiltration issues can present at multiple scales, from visually obvious defects to micron-scale voids. Even devices that appear uniform to the naked eye may therefore present differently once examined with a microscope. Recent work quantified the base infiltration of TiO_2 layers using optical microscopy and paired image analysis, to find that the proportion of unin-filtrated TiO_2 strongly correlated with performance.[22] This quick and non-destructive method could therefore be used for PCE prediction of devices or modules.

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Determining the root cause of poor infiltration can be extremely complex. Devices are usually fabricated in ambient conditions and infiltration is influenced by many different factors, including solvent viscosity, crystallisation time, and layer roughness.[17] As such, inter-batch variations are often blamed on the ambient nature of the fabrication process. Developing a thorough understanding of the causes and presentation of different types of infiltration defect will allow for targeted problem solving upon experiencing these issues.

This work presents common characteristic infiltration defects observed in CPSCs. The presentation and likely cause of each problem is discussed, and potential methods for remedying each issue are identified, with the aim of producing a reference resource of methods for targeting these problems in both lab-scale devices and modules. Linked with specific manufacturing issues, each defect type can be reduced or prevented by addressing problems in the fabrication process. This should help both

researchers and future scaled initiatives in achieving more reproducible infiltration and performance.

Results and discussion

This work will present several characteristic infiltration problems commonly observed in CPSCs along with their likely cause and potential solutions. It should be noted that although discussion will be mostly in the context of devices, the causes and solutions presented are equally applicable to modules.

For quick identification of problems, Fig. 1 shows a diagrammatic representation of identified common, characteristic infiltration defects observed at the micro (blue) and macro (green) scale in CPSCs, alongside checks for potential causes. Each issue will be discussed in greater detail in a following subsection, with a final section covering causes of low performance in the absence of defects.
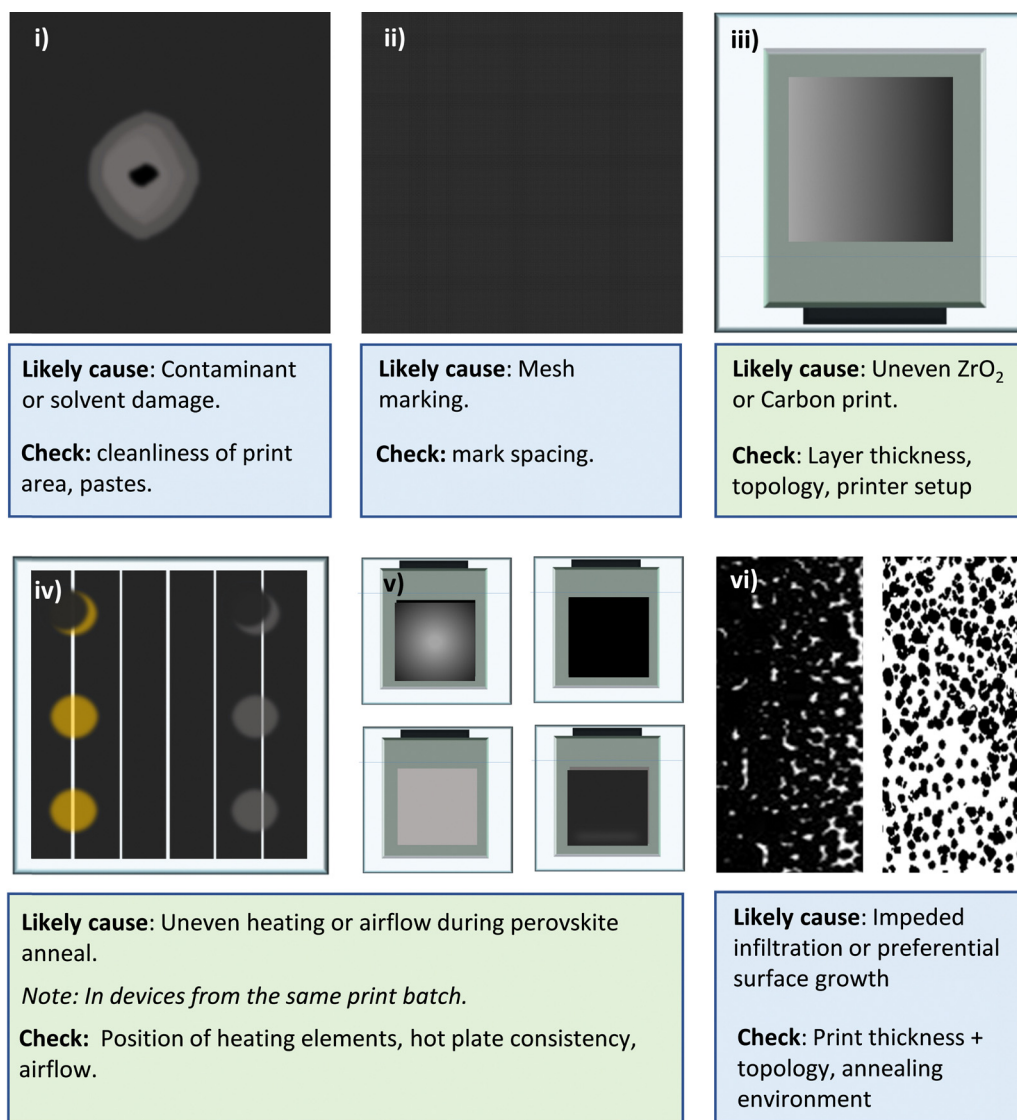

Fig. 1 Diagrams of common large (green text box, (iii)–(v)) and small-scale (blue text box, (i), (ii) and (vi)) infiltration issues in cells and modules, alongside likely causes and suggested checks. Each defect is discussed seperately in the relevant numbered section below.

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Note that each defect type can appear at a range of scales, and poorly infiltrated devices often exhibit many defects – sometimes with a combination of many types. The specific impact on device performance will therefore be highly dependent on defect size, spread, and prevalence. The effect on performance may also vary depending on perovskite formulation. Thus, it is not possible to provide a representative or accurate value for the performance increase attained by removing a given defect type, as its negative impact will be different in each cell. Specific performance data is not therefore presented in this work, instead focusing on the specific manufacturing issues that cause these characteristic defects and how to overcome them.

Recent work has found that device performance is intrinsically linked to the proportion of uninfiltrated, perovskite free TiO_2 observable through the glass substrate, where it was found that even a small increase in uninfiltrated area from 0.16% to 1.17% reduced PCE from 14.88% to 12.36%.[22] Critically, PCE losses increased more drastically as uninfiltrated area increased.

Therefore, should readers wish to predict or compare the potential detrimental impact of a given defect type in their unique device or module, optical examination of the uninfiltrated area produced by each defect type could be employed. This can be done through qualitative examination, or quantitatively using image analysis.[22] Note that the specific effect of uninfiltrated area (and thus a given defect) on performance may vary with perovskite precursor formulation, stack composition, or layer thicknesses.

Issue (i) contamination

Often (but not always) visible at the macro-scale, contaminants and solvent damage produce similar issues in completed devices, producing uneven defects of varied size, sometimes with a distinctive 'halo' or ringed surrounding pattern (Fig. 2). In the case of physical contaminants, a particle can be present at the defect centre, whereas solvent contamination issues are particle free. Particles will be visible through the glass substrate if the associated contamination is under, in, or on the TiO_2 print. Particle contamination of the ZrO_2 and carbon may also result in defects, but the given particle is unlikely to be visible through the glass substrate.

While solvent damage can be easily prevented through careful handling of liquids around printed stacks (especially when wet), physical contamination can be more persistent depending on the source. Wet and dry printed layers, screens and printing equipment should all be stored under covers to protect from dust and other airborne particulates. Placing wet films in areas of high airflow is not advised, as it can prevent film settling/slumping and increase the likelihood of particle contamination.

Upon observing these defects in cells or modules, pastes, screens, and printing equipment should be carefully inspected for particles or blockages. Blocked screens require cleaning, while contaminated pastes should be disposed of. If equipment and materials appear clean, the printing, film relaxation/slumping, annealing and storage areas should be wiped down to eliminate the source of particles, and storage procedures reviewed where necessary.
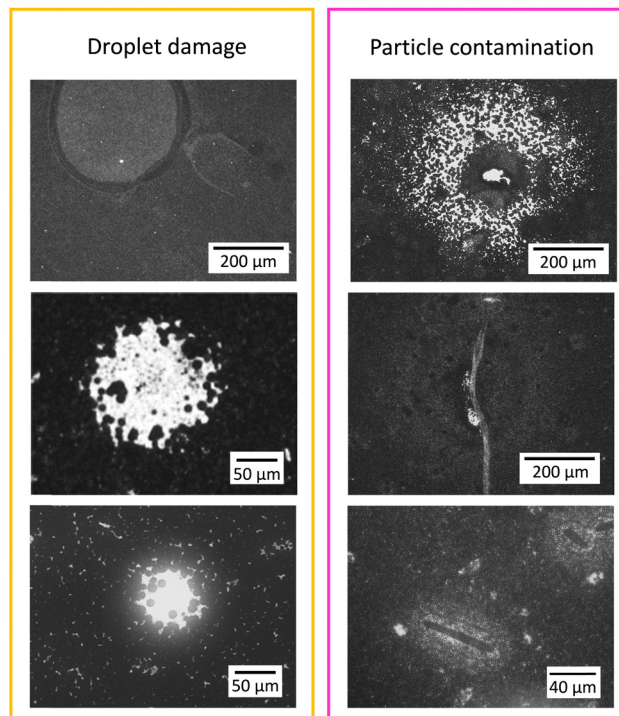

Fig. 2 Optical images of infiltration defects caused by solvent droplet damage and particle contamination.

Issue (ii) micron sized, evenly spaced defects

Perhaps the most characteristic defects are those caused by mesh marks; troughs or peaks at the surface of a screen printed layer. Mesh marks occur due to ink filaments forming at mesh crossover sections as the screen separates from the substrate during printing. This produces round, evenly spaced infiltration defects in the finished device. Usually present across a large area, these features are obvious when examining the infiltrated TiO_2 layer with an optical microscope (Fig. 3a–c). Critically, mesh marks in the ZrO_2 or carbon print can cause infiltration defects at the base of the TiO_2. (Fig. 3a–c) shows optical microcopy images of infiltrated TiO_2 layers from three devices, which respectively show evidence of TiO_2, ZrO_2 and carbon related mesh mark infiltration defects.

As presented in Fig. 3, observed infiltration defects will correspond with the mesh dimensions of the relevant screen. Therefore, if different screens have been used for TiO_2, ZrO_2 and carbon, defect spacing can be measured to conclude in which layer the problematic marks reside. For example, the small defects in Fig. 3a must correspond with those from the TiO_2 layer, as this was the only deposition where a fine mesh was used (Fig. 3c). Note that defects may only appear (or be more severe) at alternate cross sections, as is the case in Fig. 3b and c. If similar mesh screens are used for different layers, the problematic layer can be identified using WLI (white light interferometry) of any remaining uninfiltrated devices single prints (Fig. 3b).

Crucially, marks in a given layer are not necessarily due to printer setup issues in that layer. For example, it has been
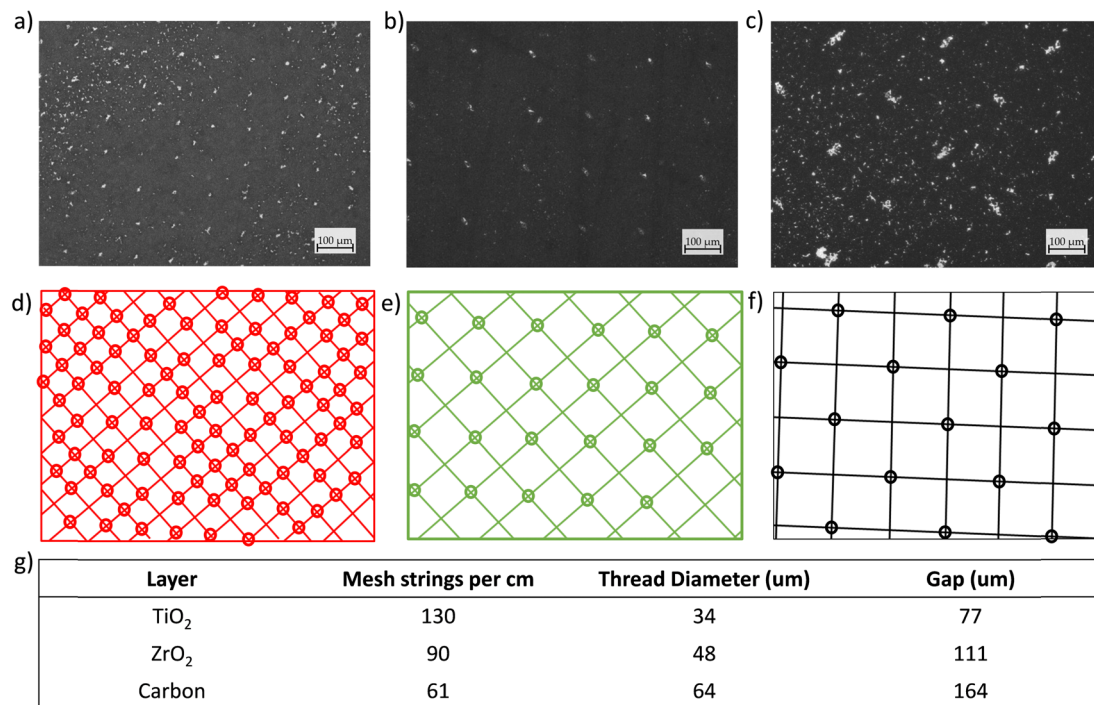
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Layer	Mesh strings per cm	Thread Diameter (um)	Gap (um)
TiO_2	130	34	77
ZrO_2	90	48	111
Carbon	61	64	164

Fig. 3 Optical images of infiltrated TiO_2 in devices showing mesh mark defects from (a) TiO_2, (b) ZrO_2, and (c) carbon screens. (d)–(f) Show diagrams of mesh dimensions of TiO_2, ZrO_2 and carbon screens respectively, with circles representing cross sections where an infiltration issue is present in the device. (g) Shows mesh types and calculated gap size for each layer.

shown that slight increases in ZrO_2 roughness can cause severe increases in marking of the subsequent carbon print.[22] Therefore, the topology of all layers (in an uninfiltrated sample) should be examined upon observing mesh marking to ascertain the root cause of the problem.

As mesh marks are caused by ink filamentation during printing, printer setup and ink formulation are critical to their prevention. Printer setup techniques to avoid mesh marking include using the minimum printable squeegee pressure or switching to a finer mesh.[22,23] It should be noted that not all pastes are suitable for fine mesh screens- for example, the large graphite flakes in carbon inks are likely to cause blockages. A flow coat print regime, where paste is spread over the screen before a single squeegee pass can also reduce marking. Unless pastes are considerably viscous, a print–print (or two squeegee passes) is not likely required and unnecessarily increases the risk of severe marking.[22,23] Alternatively, pastes can be altered to reduce filamentation by lowering viscosity and/or elasticity.[23] This can be achieved with careful dilution or by changing the amount or type of binders used.[22]

To avoid any detriment to device performance, film thickness and topography should be checked after any alteration to printer setup, regime, or ink formulation.

Issue (iii) gradient infiltration

Clear colour intensity gradients across the active area are indicative of printing inconsistencies such as uneven thickness or topology. Print variation in any layer can produce infiltration issues, although the thicker ZrO_2 and carbon are more likely to

cause problems, as precursor must travel further to penetrate these films. This can occur across the width of a single cell or module, or across several cells when printing small-scale devices. Such films then cause large performance variations within a batch of cells, or decreased power output and performance in a module.

Sub-optimal printer setup is usually the cause of these issues, although glass warping can also cause similar problems. Consequently, it may be a more prevalent issue in more manual screen-printing equipment, as advanced machines will be able to detect screen, squeegee or substrate misalignment. As shown in Fig. 4a, uneven squeegee or flow coat setup can produce thickness variation across the print. In extreme cases, one side of the print will be extremely thick (limiting infiltration), and the other thin with pronounced mesh marking (as depicted in Fig. 4a). Note that small inconsistencies in the ZrO_2 can cause large problems in the subsequent carbon print, so sub-optimal inhomogeneous carbon prints may not be a consequence of printer setup during carbon deposition.[22]

In the case of glass warping, observed infiltration gradients will align with the substrate warp, with areas further from the screen usually producing thicker prints, and areas closer to the screen producing thinner ones (sometimes accompanied by mesh marking).

It is advisable to retain an uninfiltrated device stack from each print batch, as print thicknesses or substrate warp can be then examined with profilometry, while white light interferometry provides quick topological data. Infiltrated devices are more difficult: although mesh marking problems can be
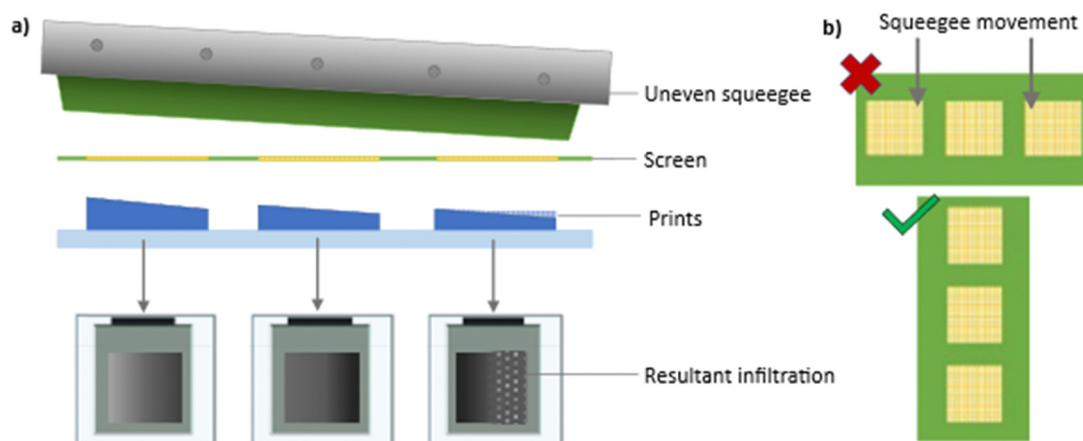
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Fig. 4 (a) Diagrammatic representation of the consequences of uneven squeegee pressure and its resultant impact on device infiltration. Note that mesh marking defects in real samples will only be visible *via* optical microscopy. (b) Screen alignment to limit horizontal print variations.

observed through the glass substrate, cross sectional analysis may be required to examine thickness across the printed layer.

Careful setup and pressure monitoring can help prevent squeegee related issues. Changing screen designs to limit the horizontal print width (depicted in Fig. 4b) can also improve uniformity and batch variation. In the case of glass warping, ramped heating and cooling steps for blocking layer spraying and each high temperature anneal can help minimise these issues.

Issue (iv) extreme infiltration variation between cells in a single print batch, not linked to position on the print bed/large grey or yellow areas in otherwise well infiltrated modules.

Crystallisation speed is well documented to impact infiltration, with longer crystallisation times having been found to improve the infiltration of perovskite precursors based on a variety of solvents. This means that inconsistencies in temperature or airflow during infiltration or annealing can produce very different infiltration depending on the position of the device on the hot plate or oven (Fig. 5a and b). This is the case even where the print quality is consistent across the batch or module. Unless care is taken to note the hot plate position of each device during annealing, the infiltration variation across a batch may appear random. It is therefore advisable to examine each device upon removal from the hot plate or oven after annealing and note the position of any which exhibit obvious infiltration issues.

This issue can occur at multiple scales and using different equipment setup. For example, Fig. 5c shows a 30×30 cm^2 module annealed on a conveyor dryer. Through the glass substrate, greyish white and yellow defects can be seen, impacting multiple cells. The grey or white perovskite free voids indicate an infiltration issue caused by fast crystallisation and high airflow, whereas the yellow areas show accelerated degradation due to uneven heating. On examination of equipment, the yellow defects corresponded with overhead heating elements in the dryer and the white and grey with areas of high airflow.

A simple partial cover was thus applied, to protect the module surface while allowing sufficient solvent removal. This completely eliminated the defects, as shown in Fig. 6.

Issues (v) and (vi) random void or crystallite spacing at micro or macro-scale

Perhaps the most difficult to diagnose is when devices present with apparently random infiltration issues spread. As shown in Fig. 7a, this can appear at multiple scales with extreme variation in the shape and distribution of observed defects.

There exist two distinct mechanisms that can cause these problems, depicted in Fig. 7b. Impeded infiltration (Fig. 7b(i)) occurs when precursor cannot effectively reach the base of the stack, while preferential surface growth (Fig. 7b(ii)) is seen when nucleation and crystal growth occurs more favourably atop or within the carbon layer, reducing crystal formation in the small pores of the TiO$_2$ electrode. Both mechanisms can also occur concurrently: *e.g.* upon applying a new precursor formulation that favours surface crystal growth to a batch of cells with thick, rough carbon prints.

Example photographs of devices with particularly severe infiltration issues caused by each mechanism are shown in Fig. 7b. It should be noted that although the devices in the example look very different, they are not characteristic of the associated infiltration issue: without further examination or specific knowledge of the given sample, is not possible to tell visually which mechanism is present.

The causative mechanism can sometimes be identified through monitoring perovskite crystallisation speed across a batch and subsequently examining infiltration. To induce different crystallisation speeds, samples can be deliberately annealed at different temperatures. In the case of impeded infiltration, the best infiltration will be attained in devices that crystallised slowly, as the precursor had more time to percolate the stack. Conversely, with preferential surface growth the best infiltration will present in rapidly crystallised devices, as the infiltrated precursor rapidly forms small grains within the TiO$_2$ pores instead of slowly growing larger grains at the carbon

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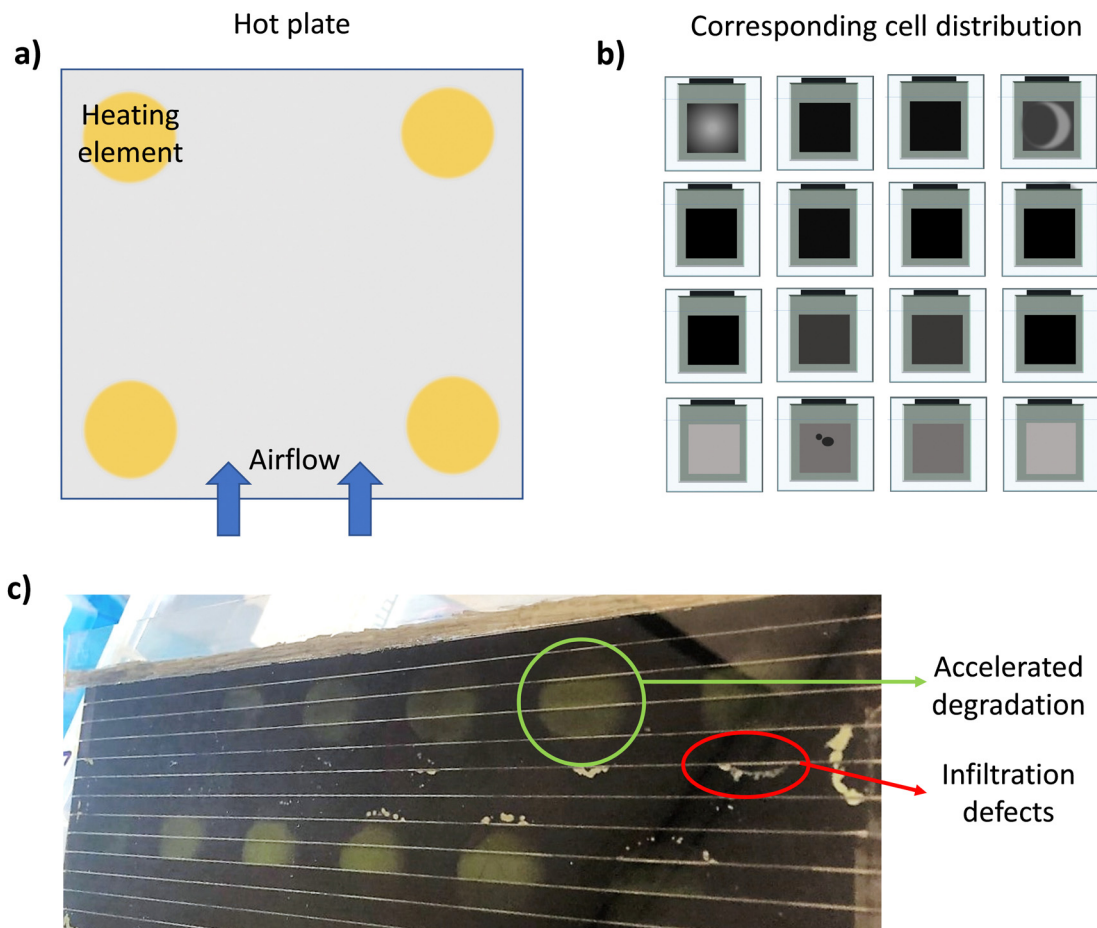*J. Mater. Chem. C*, 2024, **12**, 9401–9411 | **9405**

Fig. 5 Diagrammatic representation of (a) an unevenly heating hot plate and (b) resultant impact on device infiltration. Depicted in (c) is a photograph of damage on a 30 × 30 cm^2 module caused by heating elements and airflow during perovskite annealing.

electrode. If both issues are present, crystallisation speed will likely have little impact on infiltration.

Impeded infiltration can be caused by anything that can restrict the flow of precursor through the stack. This includes increased print roughness or thickness, horizontal graphite flake alignment, insufficient binder removal during annealing and increased precursor viscosity. The problem can then be exacerbated by suboptimal annealing conditions such as high temperatures or surface airflow.

Severe issues are usually caused by multiple concurrent problems acting in tandem. Fig. 8 shows images of TiO$_2$ infiltration from two devices from the same print batch, (a) annealed on the hot plate and (b) under a partial cover to limit surface airflow. Reducing surface airflow has produced better infiltration in sample b, revealing mesh marking defects that were not observable in the more sparsely filled sample a. Both issues (high surface airflow and mesh marking) therefore require resolving to ensure high-quality infiltration.

To help resolve severe impeded infiltration, the following steps can be taken:

• Consider depositing a larger volume of perovskite precursor to increase the overall crystallisation time.

• Examine the annealing environment for potential exposure of samples to high airflow or high temperature. Partial covers can reduce surface airflow, and lower annealing temperatures may assist infiltration. If a solvent is poorly wetting or particularly viscous, a specially designed cover may be necessary to achieve acceptable infiltration.[24]

• Examine any better infiltrated areas for evidence of problems such as mesh marking. Minor mesh marking (especially in the TiO$_2$ layer) should not cause extreme infiltration issues by itself, so evidence of this any layer is unlikely to be the sole cause.

• Check any uninfiltrated prints for defects such as increased layer roughness or extreme thickness. If no uninfiltrated stacks from the relevant printing batches remain, cross sectional imaging may provide some insight into layer thickness or roughness.

• Place carbon prints directly on the hot plate after printing and infiltrate precursor directly after annealing the carbon layer to minimize horizontal settling of graphite plates.

• Consider methods to reduce precursor viscosity or improve wetting. This could entail heating the precursor, incorporating a solvent additive, or reducing precursor concentration. Bear in mind that heating can induce precipitation in some precursors, and so is not always a suitable method.[25]

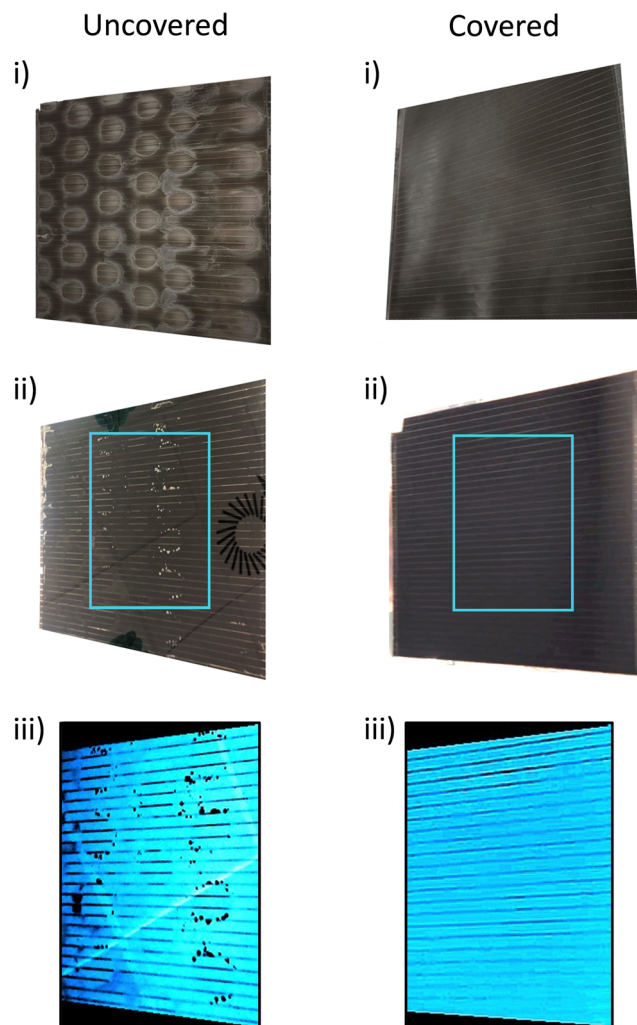Preferential surface growth is more associated with the perovskite precursor itself. Changes in formulation that limit

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Uncovered

Covered

Fig. 6 Photographs of 519 cm^2 active area modules with (RHS) and without (LHS) a cover during perovskite annealing. (i) Back electrode, (ii) through glass substrate, (iii) magnified with applied colour filter to highlight infiltration problems.

nucleation and favour large grain growth, such as introducing highly coordinating precursor solvents may therefore produce this problem. Poorly dissolved or precipitated precursors may also induce surface growth, with undissolved particulates or precipitated crystallites deposited atop the stack acting as nucleation sites.

To help resolve preferential surface growth, the following methods can be trialled:

• Consider depositing a smaller amount of precursor, to limit the amount at the device surface.

• Replace top-down drop casting with edge infiltration, depositing precursor at the ZrO$_2$ edges and allowing capillary action to drive device filling.

• Consider molecular additives that promote nucleation within the stack, such as 5-aminovaleric acid. Note that additives can slow device response times and limit grain size.[13,26,27]

• Some work has shown that applying highly optimised covers extremely close ($\sim$50 μm from the cell surface) can promote crystal growth within the stack, as the resultant high concentration of solvent vapour at the cell surface prevents surface growth. Note that

such annealing processes are extremely long ($\sim$20 hours) and can have extremely narrow processing windows.[28]

The impact of these changes will be highly dependent on the precise precursor formulation and device structure, and effectiveness may therefore be highly variable. A universal solution for preventing this infiltration issue in all CPSCs cannot therefore be presented.

Issue (vii) performance drops and hysteresis changes without infiltration problems

Upon experiencing benchmark performance drops without obvious infiltration issues, layer thickness in the relevant print batch should be examined. Sub optimally thin ZrO$_2$ layers can lower benchmark performance and dramatically increase hysteresis, although it should be noted that the optimal ZrO$_2$ thickness may vary depending on the perovskite composition.[29–31]

Carbon layers are optimally of 10–20 μm thickness.[32–34] Thin ($<$10 μm) carbon layers or blocking layers can cause overall benchmark performance losses as thinner layers are more resistive, and resultant devices suffer from poor charge extraction and increased recombination.[32–34] Optimal blocking layer thickness is approximately 30 nm.[34] Note that excessively thick ($>$75 nm) blocking layers can also cause extraction issues, with devices presenting a high shunt resistance.[34]

If any uninfiltrated samples remain, ZrO$_2$ and carbon thickness can be examined with profilometry. Ideally, uninfiltrated samples should have a dried (*i.e.* not annealed) carbon layer for any thickness measurements. This is because the carbon layer post-annealing is mechanically fragile and easily damaged by profilometry or cross-sectional sample preparation. If only infiltrated samples are available, cross-sectional SEM is required.

Summary table

To aid in fast defect identification and prevention, a summary table is provided below. Defect types, scale and causes are highlighted alongside potential checks and solutions (Table 1).

Conclusion

Complete TiO$_2$ infiltration is critical in CPSCs and modules to achieve high PCE and stability. However, as devices consist of multiple layers deposited in ambient conditions, identifying the causes of poor infiltration can be complex, challenging, and time consuming.

This work highlights a number of characteristic TiO$_2$ infiltration defects caused by specific issues in the manufacturing process such as mesh marking, printing issues, contaminant damage and environmental fluctuations. Likely contributing factors and potential solutions are presented alongside each identified issue, to produce a troubleshooting reference resource for tackling this problem in CPSCs and modules.

As defects are easily observed through the glass substrate either visually or with a microscope, the causes of poor infiltration can be quickly and non-destructively identified using low-cost equipment. This work therefore presents facile and low-
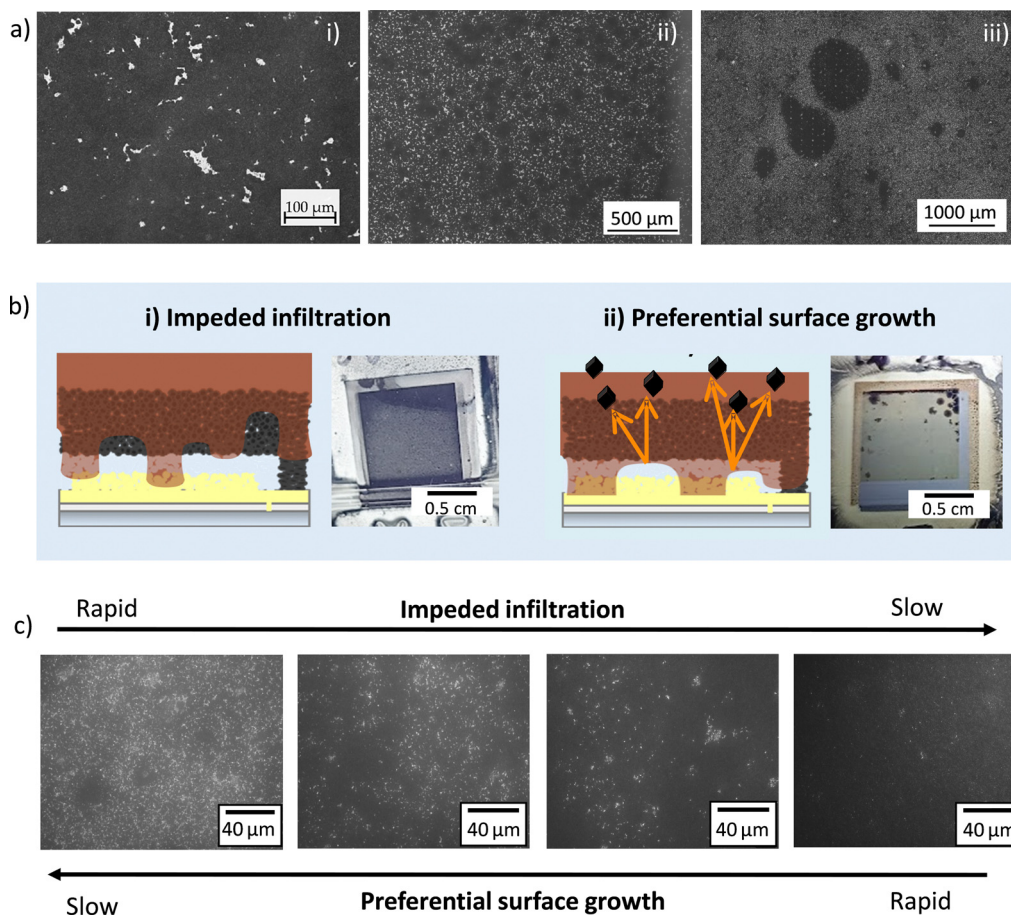
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Fig. 7 (a) Optical microscopy images of randomly distributed infiltration defects at different scales. (b) Diagrammatic representation and example photograph of (i) impeded infiltration and (ii) preferential surface growth. (c) The impact of crystallisation speed with each mechanism.
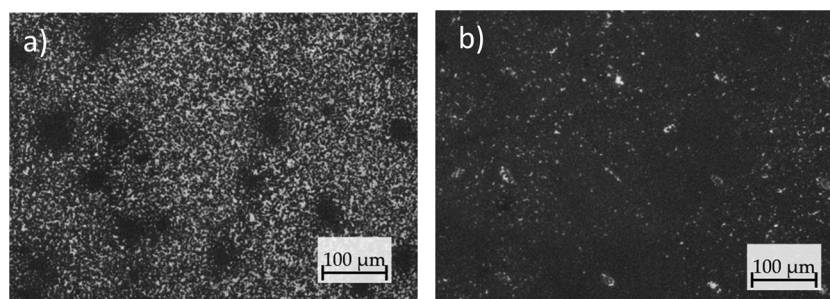

Fig. 8 Optical microscopy images of two devices with impeded infiltration, (a) annealed on an open hot plate and (b) under a partial cover. (b) Reveals mesh marks not observed.

cost solutions for monitoring and improving CPSC performance and reproducibility, ensuring quality control and preventing production bottlenecks in both research environments and future commercial ventures.

Experimental

Materials

PbI_2 (99%, Sigma-Aldrich), MAI (CH_3NH_3I, anhydrous, Dyesol), 5-ammonium valeric acid iodide (5-AVAI, Dyesol), γ-valerolactone (GVL, Sigma Aldrich) and anhydrous MeOH (Sigma Aldrich) were used as received.
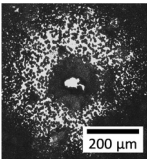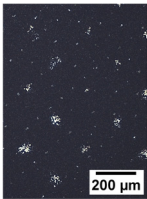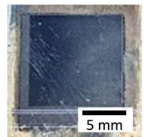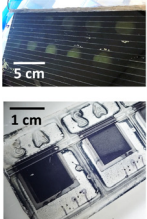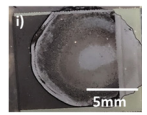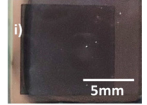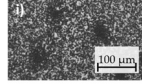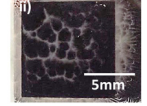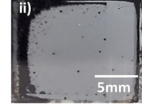
For device stacks, titanium diisopropoxide bis (acetylacetonate) (TAA, 75% in IPA, Sigma-Aldrich), anhydrous 2-propanol (IPA, 99.5%, Sigma Aldrich), TiO_2 paste (30NR-D, GreatCell Solar), ZrO_2 paste (GreatCell Solar), carbon paste (Gwent electronic materials) and terpineol (95%, Sigma-Aldrich) were used as received.

Device fabrication

Substrates were washed with Hellmanex and deionised water, rinsed with acetone and IPA, and dried with N_2. They were

Table 1 Summary of characteristic infiltration issues presented in this work alongside causes, suggested checks and potential solutions. Please refer to the relevant section of the paper for more detailed discussion on each defect

Issue	Example	Scale	Cause	What to check	Potential solutions
Particle/solvent damage.		Depends on the size of the particle/droplet.	Particle contaminant or solvent damage.	• Inspect paste, equipment, and storage areas for contamination. • Droplet damage has no central particle.	• Replace bad paste, clean equipment, printing, slumping and storage areas. • Ensure substrates are particle free before printing. • Cover prints when slumping and annealing.
Mesh marking.		Depends on screen mesh spacing and thread widths.	Filamentation during printing. Could be due to rough print in the layer below.	• Spacing corresponds with thread spacing of the relevant screen. May only appear at 2x spacing. • Marks/roughness on affected print and the one underneath (WLI recommended).	• Print using minimum effective squeegee pressure. • Trial a flow coat method. • Trial a finer mesh screen (may need multiple layers). • Slight dilution of very viscous pastes.
Gradient infiltration.		Macro-scale (mm–cm), across cell or module width/length.	Uneven printer setup or substrate warping.	• Printer setup. • Glass substrate warping (profilometry recommended).	• Careful printer setup. • Regularly change squeegees to minimise wear. • Reduce warp with slower ramps to all heating/cooling steps.
Large module patches/extreme variation within a device batch.		Scale variable, generally mm to cm.	Uneven heating or airflow during perovskite annealing/infiltration. Incomplete binder removal.	• If defects correspond to position on print bed, check printer setup. • Check that paste and perovskite annealing hot plates/ovens are consistent and accurate. • Prevent high airflow during perovskite annealing.	• Ensure full binder removal during stack anneals. If unsure on removal temperatures, perform a TGA. • Apply a partial cover during perovskite annealing (limit airflow and protect from top-down heating elements).
Random void or crystal spacing.		Very variable in scale and shape. Well infiltrated sections may reveal other issues (e.g. mesh marking).	(i) Impeded infiltration.	• Does faster perovskite crystallisation reduce infiltration? • Does precursor spread well upon deposition? (contact angle). • Does cross sectional examination reveal a large number of horizontally aligned graphite flakes?	• Reduce perovskite annealing temperature or increase infiltration volume. • Add/extend room temperature infiltration step (increase percolation time). • Reduce precursor viscosity (change solvent mix or concentration). • Limit horizontal graphite: do not slump carbon layers and infiltrate immediately once cool.
			(ii) Preferential surface crystal growth. Note: (i) and (ii) can occur concurrently.	• Does faster perovskite crystallisation increase infiltration?	• Increase perovskite annealing temperature or reduce infiltration volume. • Consider additives that impact crystallisation (e.g. AVAI). • Try a low annealing cover, as in ref. 27. • Change carbon paste formulation.

then placed in a Nano plasma system (Diener Electronics) and plasma cleaned for five minutes in an O_2 environment. The substrate was heated to 300 °C on a hot plate and a compact TiO_2 blocking layer deposited by spray pyrolysis of 0.2 M titanium di-isopropoxide-bis(acetylacetonate) in IPA.

To form the mesoporous TiO$_2$ layer, the titania paste (30NRD) was diluted 1 : 1 by weight in terpineol, screen printed and sintered at 550 °C for 30 minutes after a slow ramp. Next, ZrO$_2$ and carbon were printed and annealed at 400 °C for 30 minutes each. Layer thicknesses were 600–800 nm, $\sim$2.6 μm and $\sim$17 μm for TiO$_2$, ZrO$_2$ and carbon respectively. All layers were printed and annealed in ambient conditions.

Devices were cooled to room temperature in ambient conditions (30–50% RH, 18–21 °C), before drop casting of 20 μl room temperature precursor onto the stack. Devices were left for fifteen minutes in ambient conditions after drop casting precursor to ensure adequate infiltration, before annealing on a hot plate for 1.5 h at 45 °C.

Contacts were applied with an ultrasonic solder at 180 °C. Humidity treatments were applied for 16 hours in a humidity oven at 25 °C and 70% RH and a subsequent 4–10 hours under vacuum before storage in an airtight box in dark ambient conditions. Non-treated devices were stored in an airtight box in ambient conditions once soldered.

Module fabrication

The interconnects between the cells were patterned using the scribing method.[29] The P1 scribes in the FTO layer were created *via* a Nd:YVO4 laser. The substrates were then cleaned as per the cell fabrication method. The 30 cm × 30 cm FTO coated glass superstrate was heated to 300 °C on a hot plate and the compact TiO$_2$ blocking layer was deposited by spray pyrolysis. The mesoporous layers were deposited with an ATMA 1400 semi-automatic screen-printing press. The measured mesoporous layer thicknesses were 0.8, 2 and 10 μm for TiO$_2$, ZrO$_2$ and carbon, respectively. The P2 and P3 scribes to create the interconnects in the other layers were conducted on a Workbee CNC instrument with a steel blade under 0.54 N mm^{-1} pressure, to mechanically create the patterns. The scribe widths measured 50 μm, 600 μm and 200 μm for P1, P2 and P3, respectively, resulting in an active area of 518 cm^2 across 40 cells, with a geometric fill factor of around 80%. The length of each scribe is 272 mm, traversing the width of the relevant layer. The perovskite precursor was deposited *via* a LOCTITE 400D deposition robot at a speed of 12 m s^{-1} with a 12-gauge syringe tip at 1 bar of pressure, then cured in a Thieme conveyor dryer at 45 °C for 1.5 hours. Contacts were applied manually *via* ultrasonic soldering at 180 °C, wires were subsequently soldered to the contacts. Modules were stored in a blacked out, airtight box in ambient conditions once soldered.

Device characterisation

Devices were unencapsulated during storage and testing, and stored in ambient conditions (18–20 °C, 30–60% RH) before and after all measurements.

For IV testing the 1 cm^2 active area was masked to 0.16 cm^2 and placed under a fan for testing. A Keithley 2400 source meter and class AAA solar simulator (Newport Oriel Sol3A) at 1 sun were used, calibrated against a KG5 filtered silicon reference cell, Newport Oriel 91150-KG5. Devices were scanned at a rate of 0.126 V s^{-1} from V_{oc} to J_{sc} and *vice versa* after a light soaking period of 180 s. For stabilised current measurements, devices were held at the maximum power point (as determined by the preceding IV scan) for a period of 200 s to account for slow device response times.

XRD measurements were performed on a Bruker D8 Discover diffractometer with a Bragg–Brentano geometry source and a Cu (λ = 1.54 Å) source was used to obtain 2θ scans between 10° and 65° using a step size of 0.03°. Devices were analysed the day after fabrication (after soldering), then subjected to HT or ambient storage before re-examination (18–20 °C, 30–60% RH).

Optical microscopy for infiltration comparison

The tested area of each device was marked with permanent marker before IV testing and optical analysis, to ensure the imaged and tested area were identical. Images were taken through the glass substrate of completed devices using a Zeiss Axio Observer ZIM inverted compound microscope. To improve contrast between infiltrated and uninfiltrated areas, darkfield imaging was used. Images were stitched using Zeiss control software, which was then analysed in Zeiss ZEN Blue software.

Author contributions

Conflicts of interest

We have no conflict of interest to disclose. Data is available on request from the author.

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