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An extremely low-power-consumption reconfigurable two-dimensional tellurene artificial synapse for bio-inspired wearable edge computing†

Bolim You,‡[a] Jeechan Yoon,‡[ae] Yuna Kim,[a] Mino Yang,[b] Jina Bak,[a] Jihyang Park,[a] Un Jeong Kim,*[d] Myung Gwan Hahm*[ac] and Moonsang Lee *[a]

Neuromorphic electronics are gaining significant interest as components of next-generation computing systems. However, it is difficult to develop flexible neuromorphic electronics for implementation in various edge applications such as bio-implantable electronics and neuroprosthetics. In this study, we present a reconfigurable 2D tellurene (Te) artificial synaptic transistor on a flexible substrate for neuromorphic edge computing. Single-crystalline 2D Te flexible synaptic transistors exhibit potentiation and depression modulated by gate pulses with an extremely low power consumption of 9 fJ, 93 effective multilevel states, excellent linearity and symmetry, and an accuracy of 93% in recognizing the Modified National Institute of Standards and Technology (MNIST) patterns. Furthermore, it was observed to be a flexible synaptic transistor with outstanding gate tunability and endurance characteristics, even under a 2% curvature in both the concave and convex states. We believe a robust 2D Te flexible artificial synapse will effectively function as a building block for wearable neuromorphic edge computing applications.

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Introduction

Unstructured data such as text, video, and images are being generated exponentially owing to the rapid development of artificial intelligence (AI) and the Internet of Things (IoT). However, the existing computing architectures face a considerable challenge in performance due to the conventional von Neumann bottleneck and memory walls.[1–5] The discrete processor and memory structures of the von Neumann architecture significantly deteriorate the computing speed and energy efficiency, causing undesirable energy consumption and computational latency in the computational hardware, which includes edge devices, data centers, and cloud computing infrastructure.[6–10] A neuromorphic computing platform that mimics the biological nervous system can address these issues by integrating the memory, computation, and communication in distributed modules and performing large-scale parallel computations.[11,12] In a biological nervous system, synapses are basic links that transfer information signals between pre- and post-neurons. The biological information can be connected by releasing and accepting neurotransmitters from presynaptic neurons to postsynaptic neurons, thus enabling the learning and memory behaviors of living things with parallel processing and low energy consumption.[11,13,14] Therefore, it is essential to develop electronic devices capable of mimicking synaptic functions for implementing highly efficient neuromorphic edge computing.

Furthermore, a high demand exists for neuromorphic electronics with flexible functionality for implementation in various edge applications such as wearable,[15,16] bio-implantable,[17,18] and soft electronics,[19] interactive robotics,[20] and neuroprosthetics.[21]

[a] Department of Materials Science and Engineering, Inha University, 100 Inha-ro, Michuhol-gu, Incheon 22212, Republic of Korea. E-mail: mghahm@inha.ac.kr, mslee@inha.ac.kr
[b] Korea Basic Science Institute Seoul, 6-7, Goryeodae-ro 22-gil, Seongbuk-gu, Seoul 02841, Republic of Korea
[c] Institute for Bio-Medical and Translational Health Care, Inha University Hospital, 27 Inhang-ro, Jung-gu, Incheon 22332, Republic of Korea
[d] Department of Physics, Dongguk University, Seoul 04620, Republic of Korea. E-mail: ujjanekim@dongguk.edu
[e] WONIK IPS CO., LTD, 75, Jinwisandan-ro, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, Republic of Korea

† Electronic supplementary information (ESI) available: Schematics of solvent-assisted thinning and drop casting processes, OM and Raman mapping images of 2D Te, surface potential and work function of 2D Te on p-type Si, schematics and OM images of the fabrication method for the flexible 2D Te transistor, data of the comparison before and after O_2 plasma treatment on h-BN, schematics of the concave and convex bending models, table summarizing the gate tunability performance of the 2D Te synaptic transistor, performance comparison of previously reported 2D material-based synaptic devices, and performance summary table of convex and concave bending of a 2D tellurium flexible FET (PDF). See DOI: https://doi.org/10.1039/d4tc00530a

‡ These authors contributed equally to this paper.

Flexible electronics with neuromorphic platforms present considerable potential in connecting edge devices with cloud computing to provide intelligence and AI services in real time, leading to a hyperconnected era. Flexible electronic devices with low power consumption and high performance are crucial for realizing edge devices, and flexible synaptic electronics are suitable since they exhibit these characteristics.[22,23] Various materials such as metal oxides,[24,25] quantum dots,[9,26] organic materials,[27,28] perovskites,[29,30] nanowires,[31,32] and two-dimensional (2D) nanomaterials[33–35] have been used to satisfy these requirements. In particular, 2D nanomaterials are highly promising owing to their unique characteristics, such as excellent flexibility, thermal and mechanical stability, strong electrostatic tunability, low power consumption, monolithic integration, and high scalability.[36–39] Among them, 2D Te presents excellent mechanical flexibility, environmental stability, and optoelectronic tunability, along with high carrier mobility, which can provide a breakthrough for implementing flexible electronics for neuromorphic edge computing.[40–44] Previous studies have reported 2D Te synaptic devices with ultra-low power consumption, excellent synaptic plasticity, and environmental stability, demonstrating the potential of 2D Te for implementation in synaptic devices.[45]

In this study, we present a 2D Te flexible artificial synaptic transistor for bio-inspired wearable neuromorphic edge computing. Flexible artificial Te synapses exhibit an ultralow energy consumption of 9 fJ, 93 effective multilevel states, and excellent short- and long-term plasticity with good linearity and symmetry even under a 2% curvature in both the concave and convex shapes. The simulation of the Modified National Institute of Standards and Technology (MNIST) pattern recognition accuracy presents a high pattern recognition accuracy of 93%, demonstrating excellent biological synaptic imitation. Particularly, stable synaptic characteristics without significant degradation under compressive and tensile stress demonstrate the excellent potential of neuromorphic edge computing architectures in wearable applications. We believe that this study provides a strong foundation for a flexible, artificial synapse-based neuromorphic edge computing architecture.

Experimental

Material preparation

Ne_2TeO_3 (100 mg) and polyvinylpyrrolidone (PVP) (500 mg) were placed in 33 mL of deionized (DI) water, and a uniform mixture was formed through magnetic stirring. Ammonia solution (1.8 mL, 25%, wt/wt%) and hydrazine hydrate (3.6 mL, 80%, wt/wt%) were added to the prepared solution and placed in a Teflon-lined stainless-steel autoclave. The autoclave was then heated at 180 °C on a hot plate for 15 h. Subsequently, the autoclave was cooled to room temperature. 0.1 mL of the silver-gray solution was then mixed with 0.9 mL of DI water, and the mixture was washed three times at 1000 rpm for 5 min each using a centrifuge. After removing the DI water and leaving only the Te flakes, 0.9 mL of a thinning solution was added, which was prepared by mixing acetone, an ammonia solution, and hydrazine hydrate in a 1 : 1 : 2 ratio. After 3 days, 0.1 mL of the thinned solution and 0.9 mL of ethanol were placed in a centrifuge and spun at 1000 rpm for 5 min. Then, the ethanol was removed entirely, leaving only Te flakes, and 0.9 mL of DI water was added. Drop-casting was performed on the substrate using this solution, followed by cleaning with acetone, IPA, and DI water to obtain an extremely thin 2D Te material.

Material characterization

The atomic structures and electron diffraction patterns of the Te nanoflakes were analyzed using TEM (Titan, Thermo) equipped with a spherical aberration probe corrector (CESCOR, CEOS) and a HAADF detector. The chemical composition of the Te flakes was analyzed using XPS (K-Alpha, Thermo Scientific). The thickness of the Te nanoflakes was measured using atomic force microscopy (AFM, NanoScope MultiMode IVa, Bruker) at the Research Institute of Standards and Analysis. The OM images were obtained through optical microscopy using an OLYMPUS BX43 microscope (Tokyo, Japan). The Raman spectra of the Te nanoflakes on SiO_2/Si were acquired using a Raman spectrometer (XperRAM-S456, Nanobase) with a 532 nm laser at room temperature. KPFM was performed using an Agilent 550 SPM system.

Fabrication and electrical property characterization

Flexible Te synaptic transistors were fabricated with a top-gate structure using hexagonal boron nitride (h-BN) as the dielectric layer. The Te nanoflakes, synthesized using a hydrothermal process, were transferred onto a PET substrate by drop-casting. The source/drain (S/D) electrodes with a channel length of 5 μm were patterned using photolithography, and an Au (30 nm) metal layer was deposited using an e-beam evaporator. Mechanical exfoliation of h-BN was performed using the scotch-tape technique, which was then transferred onto a PDMS substrate, followed by O_2 plasma treatment using a reactive ion etcher. The treatment conditions were as follows: the reactive ion etcher power was 60 W; the treatment time was 5 min; the O_2 flow rate was 10 sccm; and the frequency was 50 kHz. Subsequently, the dry transfer process of h-BN was conducted using a mask aligner, ensuring h-BN was transferred to encapsulate the entire Te flake between the S/D electrodes. The h-BN and PET substrate with Te nanoflakes were loaded onto the mask holder and wafer chuck of the mask aligner, respectively, for alignment. The gate electrode was fabricated with a Ti/Pd/Au (5/55/30 nm) metal using the same method as that for the S/D electrodes. Finally, the synaptic device was placed on a hot plate for 5 min to remove the moisture. The electrical characteristics of the device were determined using a semiconductor parameter analyzer (Keithley 4200-SCS). Electrical pulse measurements were performed using a source meter (Keithley 2612 B) and a function generator (Tektronix AFG1022). All the electrical properties were measured using a vacuum probe station (MS Tech) under low-pressure conditions below 3.0 mTorr.

Pattern recognition simulation

The MNIST pattern recognition simulation was conducted using the CrossSim simulator, which was provided by Sandia National Laboratory. An ANN simulation was used to explore

the learning and recognition performance using 10 LTP/LTD cycles' data points obtained from the 2D Te synaptic transistor. A two-layer perceptron neural network was applied with 784 input neurons, 300 hidden neurons, and 10 output neurons. A total of 60 000 MNIST images with 28 × 28 pixels, comprising handwritten digits from 0 to 9, were trained using the back-propagation algorithm. Subsequently, the MNIST pattern recognition test was performed on 10 000 images.

Results and discussion

A facile hydrothermal process was conducted to synthesize the atomic-layered Te.[40] Following a solution-based thinning process, the 2D Te flakes were drop-casted onto a PET substrate (Fig. S1, ESI†). The optical microscopy image shows the atomic-layered Te flake with a length of 36 μm and a width of 4 μm (Fig. 1(a)). The selected-area electron diffraction (SAED) pattern indicates the single-crystal structure of the synthesized Te over a large area, as shown in the inset of Fig. 1(b). The pattern was recorded along the [10$\bar{1}$0] direction in the transmission electron microscopy (TEM) mode using an aperture with a radius of 30 μm. The high-angle annular dark-field (HAADF) image in Fig. 1(b), captured in the scanning transmission electron microscopy (STEM) mode, demonstrates that the synthesized Te flakes form a perfect 2D atomic structure at the atomic level. It can be observed that the atomic structure in this image is three-fold symmetric with a helical chain along ⟨0001⟩, and the interplanar distances of the (1$\bar{2}$10) and (0001) planes were ∼2 and 6 Å.[46] Raman spectroscopy was conducted to elucidate the atomic vibrational mode of the synthesized atomic-layered Te, as shown in Fig. 1(c). The Raman spectrum of the Te flakes illustrates four vibrational modes located at 91.8, 103.4, 120.3, and 139.7 cm^{-1} corresponding to the E_1-TO, E_1-LO, A_1, and E_2 peaks.[40] The Raman mapping images of the 2D Te flakes exhibit uniform Raman spectral distribution (Fig. S2, ESI†). This indicates that the 2D Te flakes present a uniform crystalline quality in all the regions. X-ray photoelectron spectroscopy (XPS) was performed to analyze the chemical composition of the Te nanoflakes as shown in Fig. 1(d). The XPS energy levels of Te $3d_{3/2}$ and $3d_{5/2}$ are located at 582.6 and 572.1 eV, which are attributed to the spin–orbit doublets of the Te–Te bond, respectively. The small peak is attributed to the Te–O bond, indicating a slight oxidation in the hydrothermal process.[47] Fig. 1(e) shows the height profile of the Te nanosheet with a thickness of 16 nm, which is obtained using atomic force microscopy (AFM). Kelvin probe force microscopy (KPFM) analysis was then performed to confirm the charge distribution on the surface of the Te nanoflake, as shown in Fig. S3 (ESI†). The difference in the surface potential distribution between Te and p-Si was estimated to be ∼0.12 V, indicating that the Te nanoflakes present a work function of ∼5.06 eV, which is consistent with the literature.[48]

The electrical characteristics of the h-BN/Te device were studied to determine its feasibility as an artificial synapse. A flexible h-BN/Te top-gate device was fabricated on a polyethylene terephthalate (PET) substrate, as shown in Fig. 2(a). Considering the variation in electrical characteristics based on the crystal orientation of 2D Te, a device channel with a length of 3 μm and a 3 μm width between the source and drain was

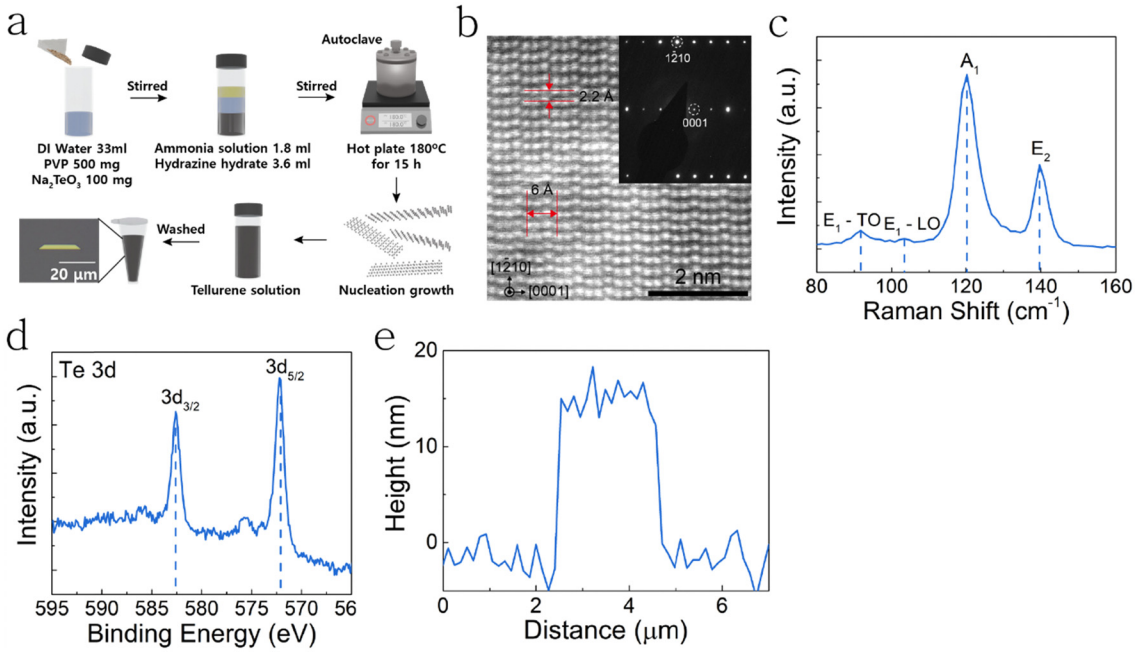

Fig. 1 Material preparation and characterization of 2D Te. (a) Schematic of the synthesis process for the 2D Te crystal; the scale bar in the optical microscopy image is 20 μm. (b) HAADF image and SAED pattern obtained with the synthesized 2D Te flake. The atomic structure exhibits three-fold symmetry with a helical chain along ⟨0001⟩. (c) Raman spectra of tellurene. The Raman intensity corresponds to the A_1, E_1, and E_2 modes. (d) XPS spectra of the Te 3d region. (e) Height profile of a 16 nm-thick 2D tellurene flake.

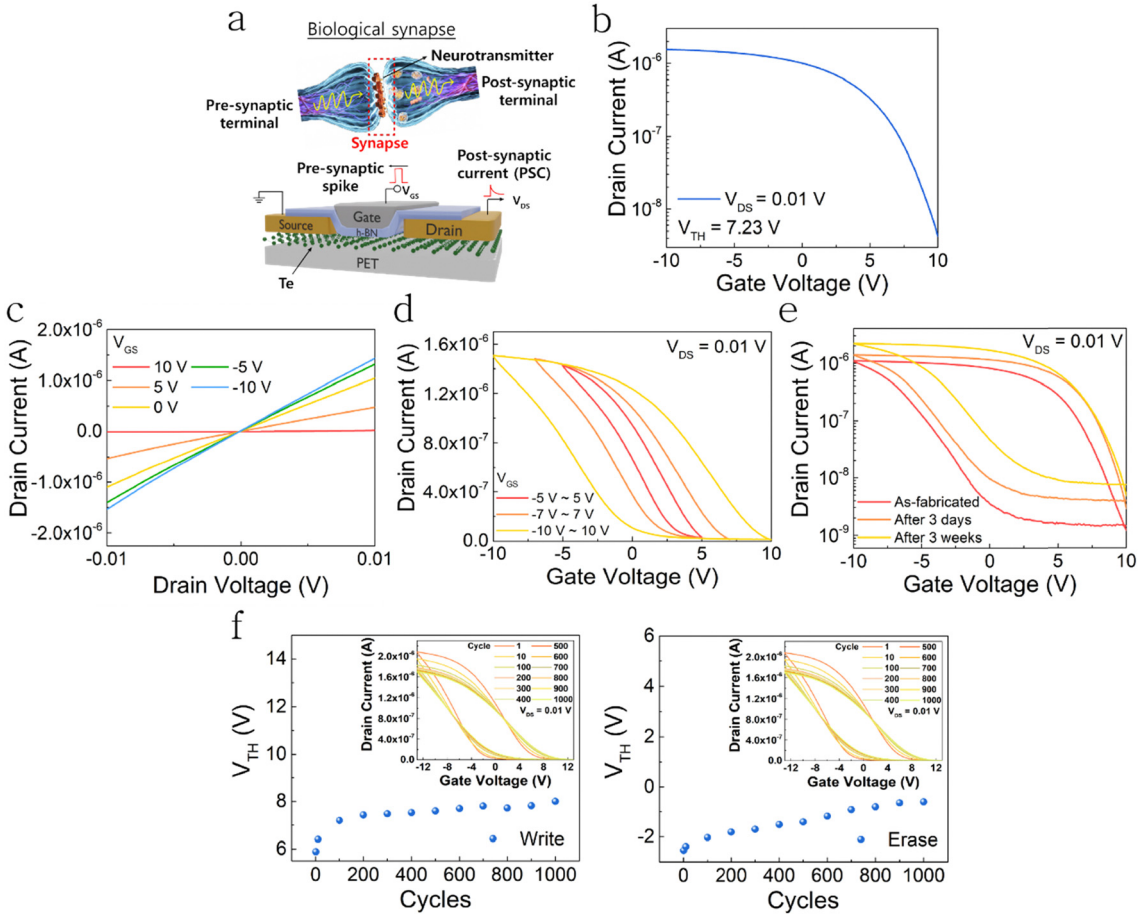

Fig. 2 Electrical characteristics of a flexible h-BN/Te top-gate transistor. (a) Schematic of the h-BN/Te synaptic device. (b) Transfer curves and (c) output curves of the h-BN/Te FET. (d) Hysteresis curves in transfer characteristics under V_{DS} = 0.01 V. (e) Hysteresis curves of the h-BN/Te device over time after fabrication. (f) Endurance characteristics of the h-BN/Te transistor.

constructed along the [0001] direction through the conventional photolithography technique (Fig. S4, ESI†).[40] A charge-trapping layer must be formed to facilitate charge-trapping or de-trapping.[49] We made the channel conductivity adjustable by applying O_2 plasma treatment to h-BN (Fig. S5, ESI†). The Raman spectra and Raman mapping images of the h-BN transferred onto Te demonstrate that h-BN uniformly encapsulated the entire Te nanoflake, indicating the formation of a charge-trapping layer in all regions of the 2D Te flake (Fig. S6, ESI†). Fig. 2(b) illustrates the electronic transfer characteristics of the h-BN/Te device at V_{DS} = 0.01 V. The transfer curve exhibits a threshold voltage (V_{TH}) of 7.23 V with p-type conductivity. Furthermore, the h-BN/Te field-effect transistor (FET) showed a field-effect mobility of 56.2 $cm^2\ V^{-1}\ s^{-1}$, along with a subthreshold swing of 2.06 V per decade. The current on/off ratio within a 20 V bias is 3.6 × 10^2. These results demonstrate that the h-BN/Te top-gate device was effectively fabricated. The output characteristics of the FET exhibit distinct symmetric and linear behaviors. This indicates the successful formation of Ohmic contacts within the source and drain electrodes, as shown in Fig. 2(c). Notably, anticlockwise hysteresis characteristics were observed in Fig. 2(d), indicating that the operating mechanism is charge-trapping or de-trapping.[50] The hysteresis window was broadened with the increase in ΔV_{GS}. These gate-controlled electronic transfer characteristics verify the existence of programmable multilevel conductance states in the h-BN/Te FET. We exposed the h-BN/Te device to ambient conditions for 3 weeks to demonstrate its environmental stability. The transfer characteristics of the h-BN/Te device exhibited negligible hysteresis and current level changes for 3 weeks under ambient conditions, as shown in Fig. 2(e). In addition, a slight variation in V_{TH} was observed in the write and erase operation modes over 1000 cycles, indicating excellent reliability (Fig. 2(f)). These results demonstrate that the h-BN/Te top-gate transistor is suitable for wearable synaptic devices.

Biological synapses are microscopic gaps between the pre- and postsynaptic terminals.[51,52] A presynaptic neuron generates an action potential when an input spike exceeding the threshold is applied. Subsequently, neurotransmitters are released from the presynaptic terminals and engage with receptors on the dendrites of the postsynaptic terminals. Owing to this interaction, the synapses shape the biological memory and behaviors of human beings.[53] We reconfigured the gate and drain electrodes of the 2D Te FET as the presynaptic and postsynaptic neurons, respectively, to replicate these interactions. To confirm the short-term synaptic plasticity of the

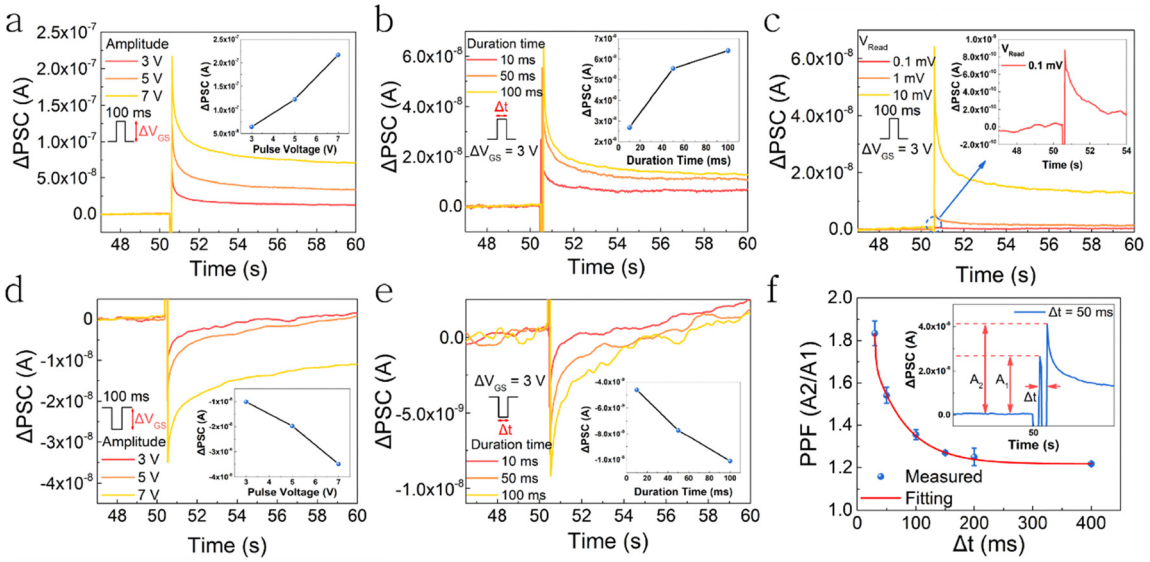

Fig. 3 The gate terminal, which is a presynaptic terminal, was modified to mimic biological synaptic behavior. EPSC characteristics under (a) different amplitudes of 3, 5, and 7 V (read voltage: 0.01 V, time duration: 100 ms) and (b) different time durations of 10, 50, and 100 ms (read voltage: 0.01 V, amplitude: 3 V); inset: EPSC change curves under different pulses. (c) EPSC curve under different read voltages of 0.1, 1, and 10 mV (amplitude: 3 V, time duration: 100 ms); inset: enlarged EPSC curve with a read voltage of 0.1 mV. IPSC characteristics under (d) different amplitudes of 3, 5, and 7 V (read voltage: 0.01 V, time duration: 100 ms) and (e) different time durations of 10, 50, and 100 ms (read voltage: 0.01 V, amplitude: 3 V); inset: IPSC change curves under different pulses. (f) PPF index with different time intervals with a V_{GS} of 2 V for 50 ms (read voltage: 0.01 V); inset: EPSC curve triggered by a pair of presynaptic spikes with an interval.

wearable artificial synaptic transistors, we explored their excitatory and inhibitory postsynaptic current (EPSC and IPSC) characteristics, as shown in Fig. 3(a)–(f) where different pulse amplitudes and time durations were applied to the gate-generated PSCs in the artificial synapses.

Fig. 3(a) illustrates the EPSC characteristics of the flexible 2D Te artificial synaptic transistors as a function of different gate voltages (V_{GS}) under a constant drain read voltage of 0.01 V and pulse width of 100 ms. The increase in the gate voltage amplitudes from 3 to 7 V increased the ΔPSC from 65 to 217 nA. Furthermore, the increase in the spiking pulse width increased the EPSCs at a fixed pulse magnitude of 3 V and read voltage of 0.01 V, as shown in Fig. 3(b). Additionally, an increased V_{DS} resulted in enhanced EPSCs, as shown in Fig. 3(c). Fig. 3(d) and (e) show the IPSC contours for an identical platform. They exhibited a trend similar to that of the EPSC characteristics, except for the opposite negative pulse polarity. These results demonstrate that the electrical modulations of the pre- and postsynaptic terminals regulate the short-term synaptic plasticity of the flexible 2D Te artificial synaptic transistors, indicating excellent replication of biological networks. We analyzed the paired-pulse facilitation (PPF) of the flexible 2D Te artificial templates to obtain a deeper insight into their short-term synaptic plasticity characteristics, as shown in Fig. 3(f). PPF is a form of short-term synaptic plasticity triggered by presynaptic spikes with pulse interval times (Δt) and defined by A_2 over A_1.[54,55] Here, A_1 and A_2 represent the peaks of the first and second PSC spikes, respectively, as shown in the inset of Fig. 3(f). The strength of PPF in the artificial platform steadily weakened with the increase in Δt. The short-term plasticity strength of the flexible 2D Te artificial synaptic transistors clearly belongs to the following double exponential decay equation:[56]

$$\mathrm{PPF} = C_1 \cdot \left(-\frac{\Delta t}{\tau_1}\right) + C_2 \cdot \left(-\frac{\Delta t}{\tau_2}\right), \quad (1)$$

where Δt represents the time interval between A_1 and A_2. C_1 and C_2 represent the initial facilitation magnitudes of the fast and slow phases, respectively. τ_1 and τ_2 represent the relaxation times of the rapid and slow phases, respectively, which were estimated to be 1.83 and 55.5 ms, respectively. These values concur well with the spiking activity dimension of the typical biological nerve network. All the results effectively demonstrate that the flexible artificial 2D Te transistor exhibits the short-term plasticity (STP) characteristics of a biological synaptic system. Additionally, this demonstrates that the artificial 2D Te synaptic architectures show excellent neuromorphic computational capabilities. Furthermore, to assess its potential as an artificial synaptic device with edge-computing capabilities, we calculated the power consumption using the following equation:[57]

$$E_{\mathrm{consumption}} = V_{\mathrm{read}} \times I_{\mathrm{peak}} \times t_{\mathrm{pulse}}, \quad (2)$$

where V_{read}, I_{peak}, and t_{pulse} represent the drain voltage, EPSC peak current, and pulse width, respectively. We obtained an extremely low power consumption of 9 fJ in a flexible 2D Te artificial synaptic transistor under a single pulse with a V_{DS} of 0.1 mV, an amplitude of 3 V, and a duration of 100 ms. We attribute the remarkable energy efficiency, achieved without the need for intricate fabrication processes, to the physical characteristics of 2D Te with a narrow band gap and high carrier density. This demonstrates that the power consumption characteristics of the flexible 2D Te artificial devices were comparable

or superior to those of other 2D synaptic transistors reported in previous studies, presenting an energy-efficient wearable neuromorphic edge architecture.[34,58–61] Furthermore, it is proved that the flexible 2D Te synaptic transistor can properly emulate artificial synaptic systems considering synapses in the human brain consume approximately 10 fJ per pulse.[19]

We analyzed the long-term potentiation (LTP) and depression (LTD) characteristics of flexible 2D Te artificial synaptic transistors under various electrical presynaptic triggers to elucidate their long-term synaptic plasticity and reconfigurable capacity. Fig. 4 depicts five different LTP/LTD patterns of the artificial synaptic transistor under 100 consecutive electrical potentiation and depression-spiking modulations. One hundred constant single pulses with an amplitude of 4 V, a pulse width of 50 ms, and an impulse interval time of 70 ms were applied for both potentiation and depression, as shown in Fig. 4(a). They demonstrate robust write and erase operations for learning and memory behaviors in the flexible artificial synapses. This presented an abrupt increase in the conductance for both the LTP and LTD. The corresponding potentiation impulse and decreased gate spiking magnitude from −4 to −1 V in the depression array resulted in a moderately decreased slope in the LTD, as shown in Fig. 4(b). Fig. 4(c) illustrates the ascending stepwise gate impulse magnitude arrangement from 1 to 4 V for the potentiation and the depression at a fixed negative spiking progression of −1 V. A more moderate increment in conductance in the LTP sequence was observed when compared to that in Fig. 4(b). A stepwise presynaptic electrical spiking array from 1 to 4 V in both the potentiation and depression arrangements improved the symmetry of the LTP/LTD curve, as shown in Fig. 4(d). A reduced gate spiking magnitude of −0.1 V with a spiking step of 40 mV at the starting point of the depression arrangement and the corresponding potentiation bias from Fig. 4(e) shaped a more balanced erasing feature in the depression stage. The gate tunability of the learning feature governs the figure-of-merit of the artificial synaptic devices, such as multilevel states, the dynamic range, symmetry, and linearity.[62] The high multilevel states improve the training capability and robustness of the device. The dynamic range, which is the ratio between the maximum conductance (G_{max}) and minimum conductance (G_{min}), is crucial in terms of the power consumption and mapping capability.[63] The symmetry and linearity of the LTP/LTD curve can improve the recognition accuracy of the artificial neural network system. The linearity and symmetry of the LTD/LTD for the flexible 2D Te artificial synaptic transistor were estimated as follows:[64]

$$G_p = B(1 - e^{-P/A_p}) + G_{min}, \quad (3)$$

$$G_d = -B(1 - e^{(P-P_{max})/A_d}) + G_{min}, \quad (4)$$

$$B = \frac{(G_{max} - G_{min})}{\left(1 - e^{-P_{max}/A_{p,d}}\right)}, \quad (5)$$

$$AR = \frac{\max\left|G_p(n) - G_d(n)\right|}{G_p(n_{max}) - G_d(n_{max})} \text{ for } n = 1 \text{ to } 100, \quad (6)$$

where G_P and G_D represent the conductances of long-term potentiation and depression, respectively; P and P_{max} represent the number of pulses and maximum number of pulses, respectively; A_p and A_d represent the non-linearities (NL) for potentiation and depression, respectively; and B denotes a fitting constant. The wearable 2D Te synaptic transistor exhibited good linearity, and the dynamic ranges (G_{max}/G_{min}) were evaluated as 1.08, 1.06, 1.05, 1.06, and 1.05 for Fig. 4(a)–(e). The asymmetry ratio (AR) values were calculated as 0.65, 0.59, 0.27, 0.2, and 0.2, respectively. The values of effective conductance state, which is the entire conductance difference ($\Delta G = G_{max} - G_{min}$) above a threshold of 0.5%, were estimated to be 42, 40, 85, 93, and 93, respectively (Table S1, ESI†). The variations of the LTP/LTD curve through gate tunability demonstrated that the wearable 2D Te synaptic transistor exhibited outstanding long-term plasticity and reconfigurability for the learning behaviors of the neuromorphic-edge-computing platform. Additionally, it is remarkable that the synaptic performance of the 2D Te flexible synaptic device is comparable or superior to others reported previously (Table S2, ESI†).

Electrical stability under mechanical modulation is highly promising for flexible electronics such as wearable edge computing, soft robotics, and neuroprosthetics. To elucidate the mechanical stability and flexibility of the flexible 2D Te artificial template, we analyzed the LTP and LTD stabilities of the 2D Te artificial synaptic transistors under different bending strains, as shown in Fig. 5. Fig. 5(a) shows a photograph of a flexible 2D Te FET mounted on a PET substrate with a bending force. Fig. 5(b) shows the endurance characteristics in the flat, convex, and concave bending states. The bending strain was calculated as $\varepsilon = t/\rho$, where t denotes the thickness of the substrate and ρ denotes the bending radius (Fig. S7, ESI†).[65] The trajectory of the LTP/LTD sequence was achieved by applying 2000 sequential electrical pulses for V_{GS}, from 1 to 4 V (with a ΔV of 30 mV) for potentiation and from 0.1 to 4.1 V (with a ΔV of 40 mV) for depression, along with a V_{DS} of 0.01 V. It can be observed that the flexible 2D Te artificial synaptic transistors exhibit excellent mechanical stability and reconfigurability *via* gate tunability, regardless of the bending status on the devices, demonstrating their potential for future applications (Table S3, ESI†). Notably, artificial synapses with convex and concave bending exhibited 100 and 79 effective states, respectively. The effective state in the flat state was 93. Furthermore, the flexible artificial synaptic transistor with concave bending exhibited a much lower conductance level over the entire measurement range when compared to other synaptic devices. These characteristics are attributed to the generation of the piezoelectric field and variation in the surface contact area of O_2 or H_2O molecules. The piezoelectric effect occurs when strain is applied to the lattice of Te, which has a trigonal crystal lattice structure. This strain causes a deformation that eliminates the inversion symmetry of the Te crystal lattice, leading to the emergence of ion charge polarization.[66] In this case, according to the convenience of piezoelectric theory, the piezoelectric polarization charges are regarded as surface charges on the bulk piezoelectric material.[67] When a negative piezoelectric polarization charge is induced in a p-FET, it causes the majority carriers, which are holes, to accumulate at the interface,

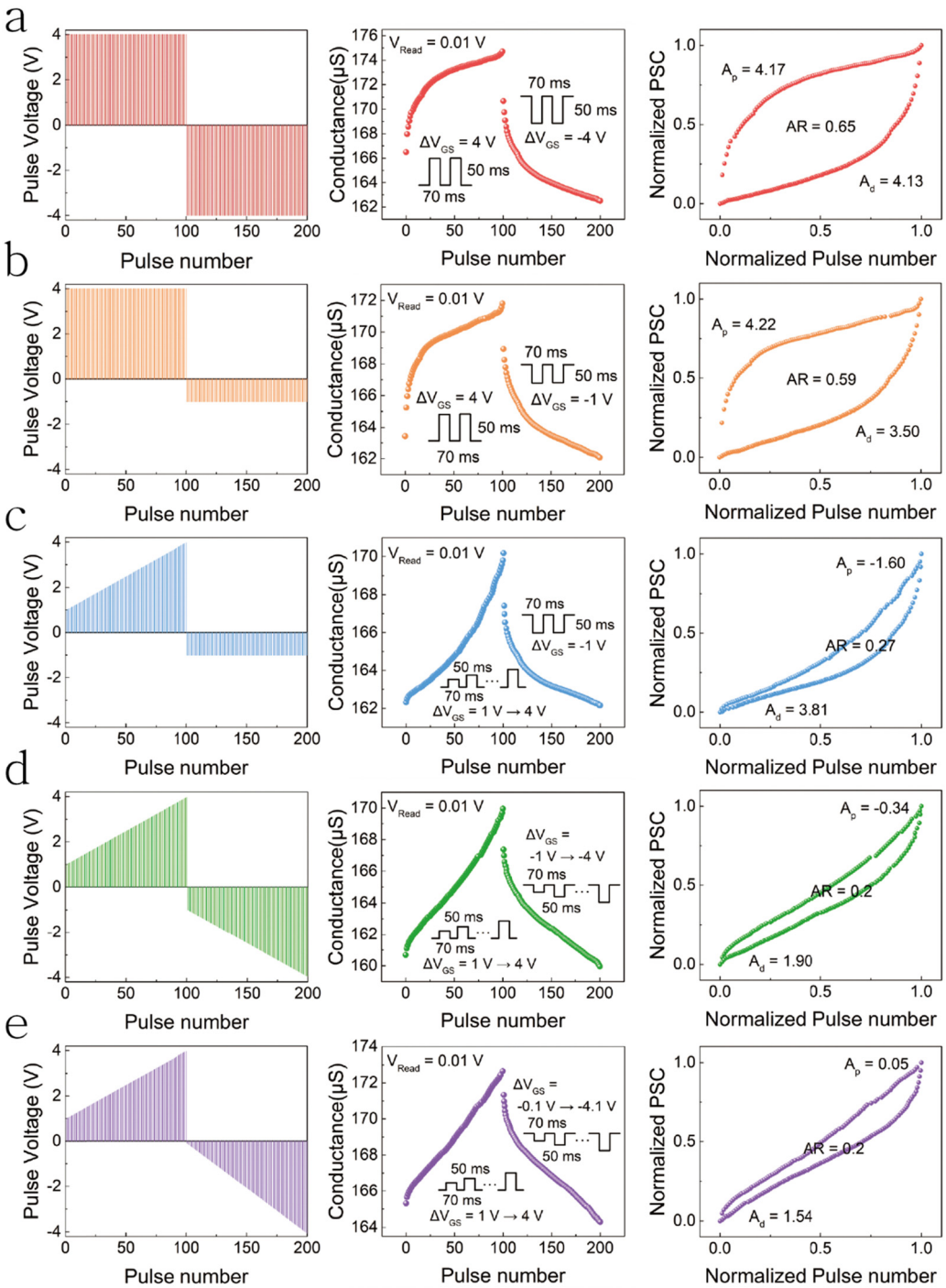

Fig. 4 Controllability of LTP/LTD characteristics for different pulse patterns under a read voltage of 0.01 V (base: 3 V). (a) LTP/LTD characteristic curves under potentiation pulses with a V_{GS} of 4 V and depression pulses with a V_{GS} of −4 V. (b) LTP/LTD characteristic curves under potentiation pulses with a V_{GS} of 4 V and depression pulses with a V_{GS} of −1 V. (c) LTP/LTD characteristic curves under potentiation pulses with a gradual increase in V_{GS} from 1 to 4 V (in steps of 30 mV) and depression pulses with a V_{GS} of −1 V. (d) LTP/LTD characteristic curves under potentiation pulses with a gradual increase in V_{GS} from 1 to 4 V (30 mV step) and depression pulses with a gradual decrease in V_{GS} from −1 to −4 V (30 mV step). (e) LTP/LTD characteristic curves under potentiation pulses with a gradual increase in V_{GS} from 1 to 4 V (30 mV step) and depression pulses with a gradual decrease in V_{GS} from −0.1 to −4 V (40 mV step).

resulting in a reduction of the Schottky barrier height (SBH). Conversely, the induction of a positive piezoelectric polarization charge repels holes from the interface, leading to an increase in the SBH.[68] In convex bending, a negative piezoelectric polarization charge is induced on the source–Te interface and a positive charge on the drain–Te interface. This leads to a decrease in the SBH at the source side and an increase at the drain side, facilitating the flow of more holes

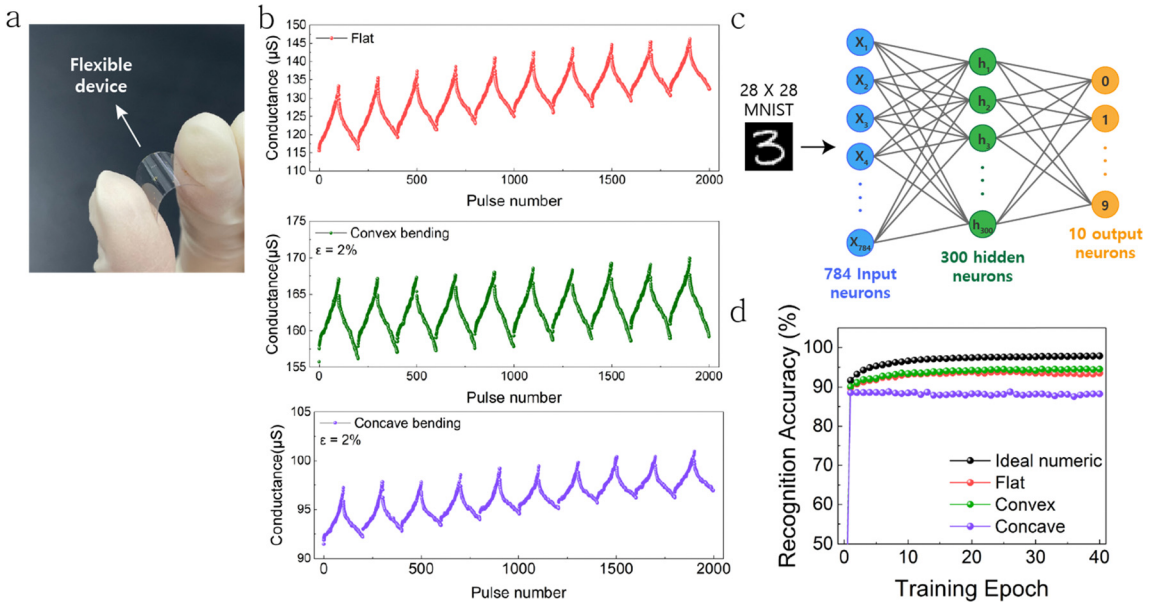

Fig. 5 (a) Photograph of the 2D Te synaptic transistor on a PET substrate. (b) Endurance characteristics of wearable devices for 10 cycles operating under flat, convex, and concave bending strain. (c) Schematic of a two-layer perceptron neural network on the MNIST 28 × 28 pixel handwritten digit data set. (d) Simulated recognition accuracy based on MNIST dataset comparison for flat, convex bending, and concave bending conditions.

and improving FET conductance. Conversely, in concave bending, a positive piezoelectric polarization charge is induced on the source–Te interface and a negative charge on the drain–Te interface. This results in an increased SBH at the source side and a decreased SBH at the drain side interface, causing a reduction in hole flow compared to the flat state and resulting in reduced performance. Furthermore, the crystallographic orientation of the Te lattice can govern the direction of the piezoelectric polarization charge.[69,70] This nature is currently under study. Another reason for conductance changes due to bending is changes in the surface contact area of O_2 or H_2O molecules, which can change the amount of charge carrier trapping/detrapping, leading to changes in conductance values.[71,72] Based on the results of the 10 cycles LTP/LTD curve, we implemented a backpropagation algorithm to confirm the learning and recognition characteristics of artificial neural network (ANN) simulation. The network structure is a simple model, as shown in Fig. 5(c). It is a two-layer perceptron neural network with 784 input neurons, with 300 neurons in the hidden layers and 10 neurons in the output layers. We used handwritten digits of 28 × 28 pixels based on the MNIST dataset. The pattern recognition accuracy was indicated by 40 training epochs, and Fig. 5(d) shows the simulation results of the flexible 2D Te synaptic transistor with different strains. In the case of convex bending, the artificial 2D Te synaptic transistor immediately achieved an accuracy of 90% in the first training epoch and subsequently achieved a high recognition rate of 94%. The flexible 2D Te artificial platform with concave bending exhibited an accuracy of approximately 88%, which is slightly lower than the accuracy of 93% in the flat state but still considered a comparable or superior level compared to those of previous studies.[45,73] In conclusion, the flexible 2D Te artificial synaptic transistor presents considerable potential in wearable neuromorphic edge computing devices requiring outstanding mechanical stability.

Conclusions

In this study, we fabricated flexible artificial synaptic transistors using 2D Te on a flexible substrate for bio-inspired wearable neuromorphic edge computing. The dielectric layer, h-BN, underwent O_2 plasma treatment, forming a charge-trapping/de-trapping layer, which enabled the adjustment of the channel conductivity. The 2D Te synaptic transistor demonstrated an extremely low power consumption of 9 fJ and exhibited excellent synaptic plasticity under various pulse conditions. Furthermore, it exhibited high linearity and symmetry in the LTP/LTD characteristics, resulting in an impressive accuracy of 93% in recognizing MNIST patterns. Additionally, it was observed to be a flexible synaptic transistor with outstanding gate tunability and endurance characteristics, even under a 2% curvature in both the concave and convex states. This study presents a promising platform for flexible synaptic transistors by employing robust 2D Te and contributes significantly to the realization of future wearable neuromorphic edge computing applications.

Author contributions

B. You and J. Yoon designed the experiments, analyzed the data, performed the experiments, interpreted the results, and wrote the manuscript. Y. Kim performed all the experiments. M. Yang analyzed the data. J. Bak and J. Park conducted the experiments. U. Kim supervised the research. M. G. Hahm supervised the

study. M. Lee designed the experiments, wrote the manuscript, and supervised the project.

Conflicts of interest

The authors declare no competing financial interests.

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