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Low voltage-driven, high-performance TiO_2 thin film transistors with MHz switching speed†

Xiaoping Chen,[abc] Jiancong Ni,[abc] Weiqiang Yang,[abc] Shaoying Ke*[d] and Maosheng Zhang *[abc]

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High-speed circuits based on thin film transistors (TFTs) show promising potential applications in biomedical imaging and human–machine interactions. One of the critical requirements for high-speed electronic devices lies in high-frequency switching or amplification at low voltages, typically driven by batteries (~3.0 V). To date, however, most electrical performances of metal oxide TFTs are measured under direct current (DC) conditions, and their dynamic switching behaviour is scarcely explored and studied systematically. Here in this work, we present low voltage-driven, high-performance TiO_2 thin film transistors, which can be operated at a switching speed of MHz. Our proposed TiO_2 TFTs demonstrated a high on–off ratio of 10^7, together with a subthreshold swing (SS) of ~150 mV Dec^{-1} averaged over four orders of magnitude, which can be further reduced below 100 mV Dec^{-1} when the temperature cools to 77 K. Additionally, the TiO_2 TFTs exhibit excellent gate-pulse switching at various frequencies ranging from 1.0 Hz to 1.0 MHz. We also explored the potential application of the TiO_2 TFTs as logic gates by constructing a resistive-loaded inverter, which shows stable operation at 10 kHz frequency and various temperatures. Thus, our results show the great potential of TiO_2 TFTs as a new platform for high-speed electronic applications.

1. Introduction

Thin film transistors (TFTs) have attracted much interest due to their ever-growing application in liquid-crystal matrix displays and radio frequency identification tags.[1–3] Typically, polycrystalline and amorphous silicon thin films have been used as the semiconducting layer thanks to their material abundance in nature and mature fabrication process. However, the low electron mobility and non-transparency in the visible range of (polycrystalline and amorphous) silicon thin films hinder further development, for instance, as portable electronics driven by battery-supplied voltages.[4–6] Thus, metal-oxide semiconductors, such as TiO_2, ZnO, InGaZnO, and InZnO, have emerged as promising alternatives with their outstanding properties including larger energy bandgap, higher electron mobility, optical transparency, and better film uniformity.[7–11] In particular, titanium oxide (TiO_2) has shown great potential as an active channel material in n-type TFTs owning to its superior advantages such as low cost, material abundance, non-toxicity, and mechanical stability. Although tremendous efforts have been devoted to improving the electrical performance of TiO_2 TFTs operated at battery-supply voltages, most electrical performances of TiO_2 TFTs have been focused on DC operation, and the corresponding dynamic switching behaviour is typically ignored and not reported as a figure of merit.[12–14] In recent years, high-speed circuits based on thin film transistors have shown promising potential applications in biomedical imaging and human–machine interactions.[15–17] In this regard, it is crucial to implement reliable, stable, and high-speed switching thin film transistors with a sufficiently high on/off ratio, an acceptable carrier mobility, and a low-driven voltage.

In this paper, we fully investigate the static DC performance and dynamic switching behaviour of the proposed TiO_2 thin film transistors including on–off ratios as high as 10^7, subthreshold swings of averaged 150 mV Dec^{-1} (four orders of magnitude), a contact resistance of 0.13 Ω cm^2, an effective mobility of 3.87 cm^2 V^{-1} s^{-1}, and a gate-pulse switching frequency beyond 1.0 MHz. Furthermore, the potential application of the TiO_2 TFTs as logic gates is explored *via* the construction of a resistive-loaded inverter, which can operate at 10 kHz frequency with a gain of 4.8 V V^{-1}. Our work shows a tremendous potential of TiO_2 TFTs as fast-switching speed matrix displays and high-speed logic operations.

[a]*Department of Chemistry, School of Chemistry and Chemical Engineering and Environment, Minnan Normal University, Zhangzhou 36300, China. E-mail: zms0557@mnnu.edu.cn*

[b]*Fujian Provincial Key Laboratory of Modern Analytical Science and Separation Technology, Minnan Normal University, Zhangzhou, 363000, China*

[c]*Fujian Provincial University Key Laboratory of Pollution Monitoring and Control, Minnan Normal University, Zhangzhou 36300, China*

[d]*College of Physics and Information Engineering, Minnan Normal University, Zhangzhou 363000, China. E-mail: syke@mnnu.edu.cn*

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2. Experimental

2.1 Device fabrication

Fig. S1† illustrates the stepwise fabrication process flow and the corresponding cross-section schematic for TiO_2 thin film transistors. The TiO_2 thin film transistors were fabricated using Si–SiO_2 substrates and the thickness of SiO_2 dielectric is 285 nm. Thermally activated atomic layer deposition (ALD) was then utilized to deposit TiO_2 as channel materials, which was then annealed at 500 °C for 30 min in an oxygen atmosphere for better thin film quality. The TiO_2 layer was deposited at a relatively low temperature (~250 °C) and its thickness was controlled by the cycling loops (0.12 nm for each cycle). TiO_2 strips were then etched using the ICP dry etching system and CF_4/Ar mixture was used as the etching gas. The etched region was defined by a standard photo-lithography procedure using a direct laser writer. AZ1500 photoresist was spin-coated and the baking temperature was 100 °C for 1 min. Another photo-lithography step was repeated to define the source and drain areas, and double layers of metal Al/Pt (50/30 nm) were then sputtered onto the substrate. Al was selected as the contact metal since a good ohmic contact can be formed between Al and TiO_2 annealed at 450 °C for 5 min, while Pt is used as a capping layer to prevent the Al layer from oxidization.[18] A layer of Al_2O_3 dielectric with a thickness of 8 nm was chosen as the insulating gate oxide, which was deposited by plasma-enhanced ALD technique at a low temperature of 350 °C. Finally, the top gate region was defined by another photo-lithography step and double layers of Ti/Pt (10/50 nm) were then deposited as contact metals. To improve the quality of the TiO_2/Al_2O_3 interface, the fabricated devices are annealed at 400 °C for 30 min (Ar/H_2). The thickness of each layer is labeled accordingly in the corresponding cross-section illustrations.

2.2 Material characterization

To investigate the TiO_2 film quality as the channel material, the X-ray diffraction technique, and the optical ellipsometry measurement were utilized to characterize the crystalline phase, film thickness, and uniformity. X-ray diffraction (XRD) was performed *via* Empyrean equipment, and the 2 theta linearity over the whole range is equal to or better than ±0.1°. The optical ellipsometry measurement was conducted by an imaging Ellipsometer Nanofilm-ep4 (spectral range: 250–1700 nm). The highest lateral resolution of Nanofilm-ep4 is around 300 nm, which can be used to measure the thickness and the optical index over the smallest area of 1 μm^2. Raman spectra were collected *via* LabRAM HR Evolution Confocal Raman Microscope. The wavelength of the scanning laser is located at 325 nm, and the Raman shift ranges from 100 cm^{-1} to 800 cm^{-1}. X-ray photoelectron spectroscopy (XPS) measurement of TiO_2 thin film before and after O_2 annealing was conducted using Thermo Fisher ESCALAB XI+ and the incident energy of X-ray (Al Kα) is set to be 1486.6 eV, which allows high-resolution surface element analysis. The surface roughness of TiO_2 thin film was visualized using atomic force microscopy (AFM, Cypher S/Oxford Instruments Asylum Research) and the corresponding profile images were collected at an area of 1 × 1 μm^2 under fast scan mode. All the material characterization was conducted at room temperature and atmosphere.

2.3 Electrical measurement setup

The electrical measurement was performed within a six-arm low-temperature Lakeshore vacuumed probe station, which consists of four DC probes and two high-frequency tips. The available temperature range starts from 77 K to 350 K. The temperature-dependent electrical data was collected when the chamber heated up for higher temperature accuracy. DC probes were directly approached to metallic pads and the silicon substrate was connected to the stage using conductive tapes. The electrical signals were applied and visualized *via* an Agilent B1500A semiconductor device analyzer, which allows various modes of sweeping I(V), fast I(V) scan, and C(V) measurement. The applied maximum voltage can be up to 200 V with a maximum current of 1 A. The current resolution at room temperature is at the order of a few fA if grounded appropriately. In terms of the fast I(V) scan mode, a waveform-generating module was utilized to apply arbitrary and programmable electrical signals at a pulse width of 10 ns. Meanwhile, the minimum collection speed is limited to 10 ns and it should be noted that the signal noise increases significantly as the collection time shortens. In terms of the dynamic response of resistive-loaded inverters, the input signals were generated *via* a function generator (Keysight 33500B true form generator), which offers a maximum frequency (~100 MHz) of square waveforms. At the same time, the fast-switching electrical signals were collected and visualized by a digital bench oscilloscope (Tektronix TBS2074B series). To prevent the electrical propagation loss and crosstalk of high-speed signals, all the electrical connections were connected *via* broad-bandwidth SMU cables.

3. Results and discussion

3.1 Device schematics and transistor performance at T = 300 K

Fig. 1a shows the schematic illustration of TiO_2 thin film transistors fabricated on top of SiO_2/Si substrates. Thermally activated atomic layer deposition (ALD) was utilized to deposit ~15 nm TiO_2 as channel materials followed by annealing at 500 °C for 30 min in an oxygen atmosphere to improve the crystalline and mobility. Another layer of Al_2O_3 (~8 nm) was chosen as the insulating oxide due to its excellent film quality and large bandgap.[18–20] Fig. 1b illustrates the corresponding cross-section view, where Al was selected as the contact metal since a good ohmic contact can be formed between Al and TiO_2 without annealing, while Pt is used as a capping layer to prevent the Al layer from oxidization. In addition, double layers of Ti/Pt (10/50 nm) function as top gate contacts. An overview of device fabrication is well-elaborated in Fig. S1.† The active device area of TiO_2 TFTs is 18 (length) × 10 (width) mm^2, while the contact pads are designed as 100 × 100 mm^2 for probe electrical measurement (Fig. S2†). The film quality and thickness of the

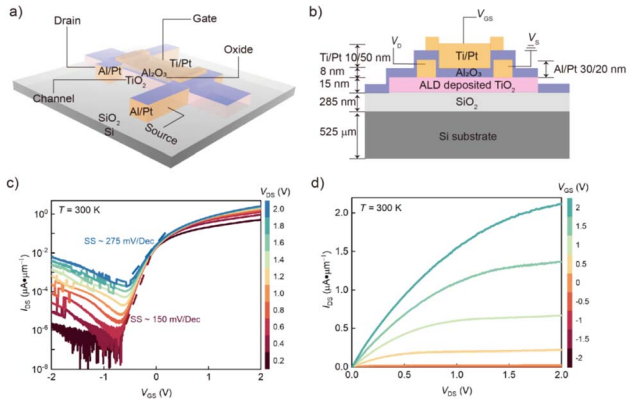

Fig. 1 Device schematics and transistor performance. (a) Schematic illustration of TiO_2 thin film transistors and the electrical connection. (b) Cross-section structure diagram with labeled thickness for each layer. (c) Room temperature transfer curves (I_{DS}–V_{GS}) of TiO_2 TFTs collected at constant V_{DS} ranging from 0.2 V to 2.0 V at an interval of 0.2 V. (d) Output characteristics (I_{DS}–V_{DS}) as a function of V_{GS} ranging from −2.0 V to +2.0 V in 0.5 V step.

annealed TiO_2 thin film as channel material were investigated *via* XRD, Raman, XPS, AFM, and optical ellipsometry techniques, respectively. Our result suggests that the as-deposited TiO_2 thin films show an amorphous phase and the formation of anatase polycrystalline phase after O_2 annealing was confirmed based on XRD and Raman spectra (Fig. S3†).[21,22] Typically, the electron mobility of crystallized TiO_2 thin film is much better than the counterpart of amorphous phase due to less traps and lattice scattering.[23–25] Meanwhile, the XPS result suggests that the annealing process may remove the defects of non-totally oxidized Ti, therefore improving the crystalline lattice and electron mobility (Fig. S4†).[26,27] Furthermore, the thickness and surface uniformity were characterized by optical ellipsometry and AFM technique, where the averaged thickness is 15.8 ± 0.4 nm (Fig. S5†) and surface roughness is around 0.3 nm (Fig. S6†).

Fig. 1c presents the subthreshold characteristics of TiO_2 TFTs at various drain-to-source voltages (V_{DS}), where negligible hysteresis window was observed. Our proposed TiO_2 TFTs demonstrated a negative turn-on voltage, a significant on–off ratio of 10^7, and a subthreshold swing (SS) of ~150 mV Dec^{-1} averaged over four orders of magnitude at V_{DS} = 0.2 V. The ohmic contact behaviour was confirmed *via* the transfer length method as shown in Fig. S7† and the specific contact resistivity (ρ_C) is extracted to be around 0.13 Ω cm^2. It is the high contact resistivity that contributes to the low source-to-drain current (I_{DS}) ~210 nA at V_{DS} = 1.0 V when no gate bias was applied. The gate leakage current density is determined to be lower than 10^{-6} A cm^{-2} and the corresponding breakdown voltage is around 4.8 V, suggesting the deposited Al_2O_3 layer is of good insulating quality over the gate-to-source voltage (V_{GS}) measurement range (Fig. S8b†). Fig. 1d illustrates the collected output (I_{DS}–V_{DS}) curves as a function of V_{GS}, where current saturation and pinch-off are visualized. We noticed that the spacing of output (I_{DS}–V_{DS}) curves measured at V_{GS} = +2.0 V is sub-linear, indicating the possible effect of self-heating. To extract the effective mobility of TiO_2 thin film, we have also presented the transfer curve at V_{DS} = 100 mV in Fig. S8d† and the estimated electron mobility is 3.87 cm^2 V^{-1} s^{-1}, comparable to the as-far best-reported value (~10.7 cm^2 V^{-1} s^{-1}).[25]

3.2 Temperature-dependent electrical characterization

To further elucidate the charge transport process of TiO_2 TFTs, we have performed the transfer characteristics at different temperatures ranging from 300 K to 77 K at an interval of 30 K. Fig. 2a and b demonstrate the temperature-dependent subthreshold behaviour measured at V_{DS} = 0.2 V and 2.0 V, respectively. As can be seen, the collected transfer curves become steeper and the corresponding turn-on voltages shift to more positive values when the temperature cools down. In addition, the on–off ratio shows insensitive temperature dependence, which suggests that our proposed TiO_2 TFTs can operate at quite broad temperature ranges. Fig. 2c presents the extracted temperature-dependent SS plotted against I_{DS}. The averaged SS extracted over four orders of magnitude decreases from 150 mV Dec^{-1} at T = 300 K to 100 mV Dec^{-1} when the temperature cools to 77 K (V_{DS} = 0.2 V). The charge transport mechanism for our TiO_2 TFTs is dominated by thermionic emission, therefore, the extracted SS should be linear as a function of temperature.[28,29] Fig. 2d illustrates the extracted minimum SS plotted against temperature, where the experimentally measured SS scales linearly as a function of temperature as expected and shares a similar slope to the theoretical values following the Boltzmann limitation. Detailed temperature-dependent SS analysis is discussed in ESI Section 9.†

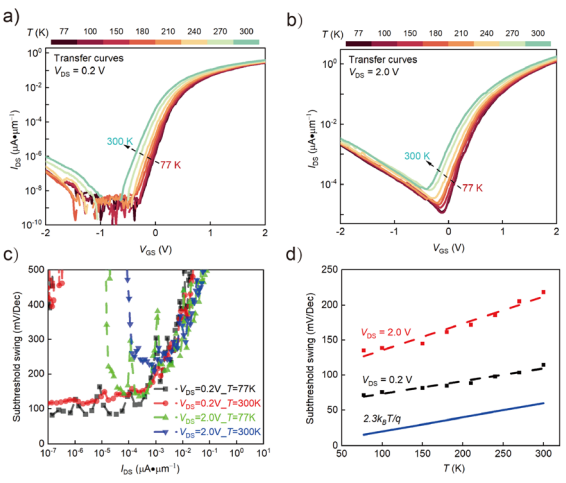

Fig. 2 Temperature-dependent transistor performance. (a and b) Subthreshold behaviour measured at various temperatures ranging from 77 K to 300 K while the V_{DS} remains constant at 0.2 V and 2.0 V, respectively. (c) SS plotted against I_{DS} at the lowest and highest temperatures (V_{DS} = 0.2 V and 2.0 V). (d) Extracted minimum SS as a function of temperature. The red and black dotted curves represent the experimentally measured values, while the blue line refers to the theoretical value following the Boltzmann limitation (2.3 k_BT/q).

3.3 Dynamic switching response and transient performance

To explore the time-resolved dynamic switching characteristics of TiO_2 TFTs, transient time traces of source to drain current (I_{DS}) were analyzed by applying pulsed gate voltages (V_{GS} from −1.0 V to +2.0 V) at constant V_{DS} = +2.0 V. Fig. 3a–f displays different dynamic responses of TiO_2 TFTs collected at frequencies ranging from 100 Hz to 10 MHz at a step of one order. To begin with, we observed noise-free and stable currents (I_{DS}) being switched on and off at frequencies below 1.0 MHz. The on and off states of I_{DS} agree well with the previous DC result. Subsequently, Fig. 3e shows that I_{DS} can still be switched on and off, but the noise level of I_{DS} becomes significant at a frequency of 1.0 MHz. The reason may be due to the shorter collection time of each cycle at higher frequencies (the noise level increases significantly when the collection averaging time decreases, especially when the averaging time is shorter than 1 μs). Furthermore, the switching rise time and fall time can be defined as the time elapse when the switched-on current decays from 90% to 10% and *vice versa* in the transient time trace.[30,31] Since the rise time and fall time are both around 100 ns, the maximum switching speed is calculated to be around 5.0 MHz *via* the following equation

$$f_{max} = 1/(\tau_{Rise} + \tau_{Fall})$$

Finally, the device cannot be switched on and off consistently when the applied frequency exceeds 10 MHz (Fig. 3f) probably due to the response time of the device itself or the limitation of our electrical setup (the collection time should be longer than 10 ns and the noise level becomes significant when the frequency is above 10 MHz). Thus, it requires more effort and higher-speed measurement equipment to estimate the accurate response time in our future work. Notably, our proposed TiO_2 TFTs can be switched on and off even at a temperature as low as 77 K (Fig. S10†). The dynamic switching response and transient performance of TiO_2 TFTs switch on more opportunities for high-speed electronic devices based on metal oxide TFTs.

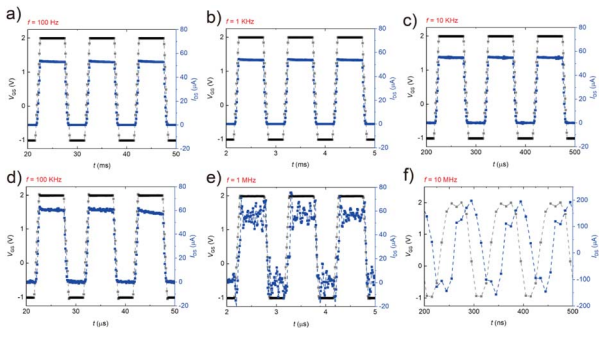

Fig. 3 Dynamic switching behaviour of TiO_2 TFTs. Transient time traces collected at various frequencies by applying pulsed gate voltages (V_{GS} from −1.0 V to +2.0 V) at constant V_{DS} = +2.0 V. (a–f) represent the corresponding time traces collected at different frequencies from 100 Hz to 10 MHz at an interval of one order of magnitude.

3.4 Static and dynamic resistive-loaded inverter characteristics

To further explore the potential application of TiO_2 TFTs on high-speed circuits, we have constructed a resistive-loaded inverter and studied the static and dynamic transient behaviour. Fig. 4a shows clear voltage transfer curves collected at various resistive loads ranging from 100 kΩ to 1.0 MΩ. The inset illustrates the circuit design with a fixed supply voltage (V_{DD} = 2.0 V). We observed that the output voltages (V_{out}) can be "pulled down" to near 0 V as the load resistor increases to 1.0 MΩ. Fig. 4b displays the voltage transfer characteristics as a function V_{DD}, where stable and consistent inverting behaviour can be observed at different supply voltages ranging from 0.2 V to 3.0 V. Fig. 4c illustrates the corresponding gain curves, which exhibit a maximum voltage gain of ~4.8 at V_{DD} = 3.0 V. Notably, the maximum voltage gain shows an insensitive dependence on temperature ranging from 77 K to 300 K, which suggests that the resistive-loaded inverter can operate at a quite broad regime (Fig. 4d). Our proposed TiO_2 TFTs may find potential applications as quantum computing components and active backplane matrix operated at cryogenic temperatures. The last section is the dynamic performance of the resistive-loaded inverter, which

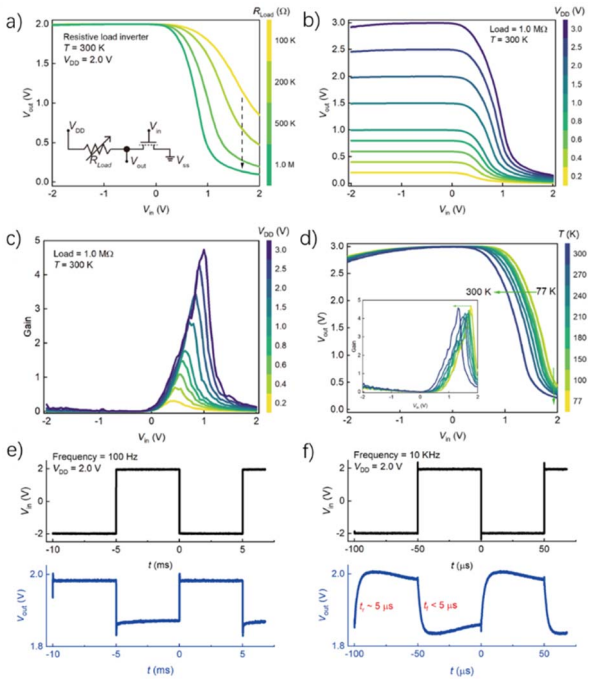

Fig. 4 Static and dynamic resistive-loaded inverter characteristics. (a) Voltage transfer curves are collected at different resistive loads while the supply voltage remains constant (V_{DD} = 2.0 V). The inset presents the circuit design and electrical connection. (b) Voltage transfer curves as a function of V_{DD} and the resistive load is 1.0 MΩ. (c) Calculated gain curves at different V_{DD} levels ranging from 0.2 V to 3.0 V. (d) Temperature-dependent voltage transfer curves and related gain curves at V_{DD} = 3.0 V and load = 1.0 MΩ. Dynamic behaviour of resistive-loaded inverter in response to square-waveform input signals with a frequency of 100 Hz (e) and 10 kHz (f). The amplitude of input signals is 4.0 V with a 50% duty cycle and the supply voltage is constant at 2.0 V while the resistive load is 1.0 MΩ.

was evaluated by applying square-waveform input signals with an amplitude of 4.0 V, a 50% duty cycle, no offset voltage, and various frequencies. To visualize the transient behavior, the external resistive load was fixed at 1.0 MΩ. Meanwhile, the fast-switching time traces of output electrical signals were collected and visualized by a digital bench oscilloscope. Fig. 4e and f demonstrate the transient behaviour in response to square-waveform input signals with a frequency of 100 Hz and 10 kHz, respectively. A stable and consistent inverting performance can be observed at different frequencies. In addition, the rise (t_r) and fall time (t_f) of switching events in Fig. 4f can be fitted by simple exponential functions to estimate the inverter response time.[17,32] Both the rise and fall time are calculated to be around 5 ms, thus, the maximum speed of the resistive-loaded inverter is no more than 100 kHz. However, it is noteworthy that this maximum speed is not limited by the device itself but by the resistive-capacitive time constant (RC delay) of the constructed circuit. Table S1† benchmarks the electrical performances and highlights the differences between our proposed TiO_2 TFTs and other types of devices. Our work studies systematically the static DC performance, dynamic switching behaviour, and logic gates of resistive-loaded inverters, which paves the way towards forthcoming high-speed and low voltage-driven electronic components based on metal semiconductors.

4. Conclusions

In summary, we have presented low voltage-driven, high-performance TiO_2 thin film transistors, which can be operated at a switching speed of MHz. The static DC performance and dynamic switching behaviour of the proposed TiO_2 TFTs are studied systematically. The film quality and thickness of the prepared TiO_2 thin film were investigated *via* XRD, Raman, XPS, AFM, and ellipsometry techniques. Our work shows that there is still plenty of room to explore and improve the switching frequencies of metal oxide thin film transistors, which may find their future application in the next generation of display backplanes and high-speed electronic circuits.

Author contributions

Xiaoping Chen: conceptualization, investigation, formal analysis, methodology, visualization, writing – original draft, writing – review & editing. Jiancong Ni: resources, formal analysis. Weiqiang Yang: investigation, formal analysis. Shaoying Ke: supervision, resources, formal analysis, writing – review & editing. Maosheng Zhang: supervision, resources, conceptualization, formal analysis, writing – review & editing.

Conflicts of interest

There are no conflicts to declare.

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