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Democratizing digital microfluidics by a cloud-based design and manufacturing platform

Qining Leo Wang, [a] Eric Hyunsung Cho,[a] Jia Li, †[a] Hsin-Chuan Huang,‡[b] Sarath Kin, [c] Yuhao Piao, §[a] Lin Xu,¶[a] Kenneth Tang, [d] Shounak Kuiry, [d] Zifan He,[d] Danning Yu,||[d] Brian Cheng, **[e] Chang-Chi Wu,[b] Connor Choi, [d] Kwanwoo Shin, [c] Tsung-Yi Ho [f] and Chang-Jin "CJ" Kim *[aeg]

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Akin to the impact that digital microelectronics had on electronic devices for information technology, digital microfluidics (DMF) was anticipated to transform fluidic devices for lab-on-a-chip (LoC) applications. However, despite a wealth of research and publications, electrowetting-on-dielectric (EWOD) DMF has not achieved the anticipated wide adoption, and commercialization has been painfully slow. By identifying the technological and resource hurdles in developing DMF chip and control systems as the culprit, we envision democratizing DMF by building a standardized design and manufacturing platform. To achieve this vision, we introduce a proof-of-concept cloud platform that empowers any user to design, obtain, and operate DMF chips (**https://edroplets.org**). For chip design, we establish a web-based EWOD chip design platform with layout rules and automated wire routing. For chip manufacturing, we build a web-based EWOD chip manufacturing platform and fabricate four types of EWOD chips (*i.e.*, glass, paper, PCB, and TFT) to demonstrate the foundry service workflow. For chip control, we introduce a compact EWOD control system along with web-based operating software. Although industrial fabrication services are beyond the scope of this work, we hope this perspective will inspire academic and commercial stakeholders to join the initiative toward a DMF ecosystem for the masses.

[a] *Mechanical and Aerospace Engineering Department, University of California, Los Angeles (UCLA), Los Angeles, California 90095, USA. E-mail: cjkim@ucla.edu*
[b] *Department of Computer Science, National Tsing Hua University, Hsinchu, Taiwan*
[c] *Department of Chemistry, and Institute of Biological Interfaces, Sogang University, Seoul 04107, Korea*
[d] *Computer Science Department, University of California, Los Angeles (UCLA), Los Angeles, California 90095, USA*
[e] *Department of Bioengineering, University of California, Los Angeles (UCLA), Los Angeles, California 90095, USA*
[f] *Department of Computer Science and Engineering, The Chinese University of Hong Kong, Hong Kong, China*
[g] *California NanoSystems Institute, University of California, Los Angeles (UCLA), Los Angeles, California 90095, USA*
† Current address: Omnitron Sensors Inc., 1100 Glendon Avenue, Los Angeles, California 90024, USA.
‡ Current address: BioPro Scientific Co., Ltd., Center of Innovative Incubator, Hsinchu City 30013, Taiwan.
§ Current address: Key Laboratory of Metabolic Engineering and Biosynthesis Technology of Ministry of Industry and Information Technology, School of Environmental and Biological Engineering, Nanjing University of Science and Technology, Nanjing 210094, China.
¶ Current address: College of Artificial Intelligence, Nankai university, 38 Tongyan Road, Haihe Education Park, Tianjin 300350, China.
|| Current address: Stripe, Inc., 354 Oyster Point Blvd, South San Francisco, California 94080, USA.
** Current address: Department of Biological Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA.

1. Introduction

Digital microfluidics (DMF)[1–3] have emerged as a revolutionary advancement in microfluidics, enabling independent control over individual droplets using electric signals alone.[3–5] Distinct from continuous flow (*i.e.*, analog) microfluidics[6–8] and flow-carried droplet microfluidics,[9–11] DMF manipulates discrete droplets with an array of planar electrodes, where four basic droplet operations (*i.e.*, creating, transporting, merging, and cutting) can be performed.[12] Resembling a digital integrated circuit (IC) chip with numerous transistors processing digits for logic functions, a DMF chip with numerous electrodes can manipulate droplets for fluidic functions. In the same way that processing electric signals in bits made digital microelectronics compact and highly reconfigurable, handling liquids in droplets makes DMF systems uniquely simple and reconfigurable, with no hardwired fluid pathways. This distinctive feature positions DMF as a platform technology capable of programming complex fluidic protocols on a given chip,[13–16] paving the way for standardized design and manufacturing of lab-on-a-chip (LoC) devices and systems. Despite the name, which originated from IC chips, most microfluidics chips are the size of a small plate (*i.e.*, in centimeters) rather than a chip (*i.e.*, in millimeters).

Enabling electric control over various types of liquid on a hydrophobic surface, electrowetting-on-dielectric (EWOD)[17–20] started the concept of DMF and has become the most popular driving mechanism for DMF.[5,21–23] Like digital IC, which revolutionized electronics and ushered in the era of information technology (IT), DMF holds the potential to transform fluidics (*i.e.*, liquid handling) and empower LoC. However, despite a wealth of research and publications on EWOD DMF, its commercialization has been painfully slow.[24] A few companies started exploring library preparation for DNA sequencing—a typical DMF application today—in the mid-2000s. For example, NuGEN Technologies (acquired by Tecan) worked with Advanced Liquid Logic (acquired by Illumina) to develop a DMF system called Mondrian SP Workstation,[25] which was on the market only briefly around 2010. Next, Illumina launched NeoPrep in 2015 but also discontinued it soon for undisclosed reasons.[26] In 2016, Miroculus (acquired by Integra) started developing a DMF-based system called Miro Canvas for library preparation after acquiring Kapplex[27] and launched their product in 2022.[28] In 2018, Volta Lab was formed to utilize DMF with an open-configuration for sequencing library preparation, and they released their product in 2024.[29] Additionally, MGI (a subsidiary of BGI) launched their library preparation product (DNBeLab Series D) in China in 2022.[30] Typically, it has taken over five years for a company to develop an EWOD-based DMF product.

Difficulties in optimizing a variety of chip parameters and overcoming reliability issues of EWOD DMF chips are generally considered to be the main bottleneck that slows product

Qining Leo Wang

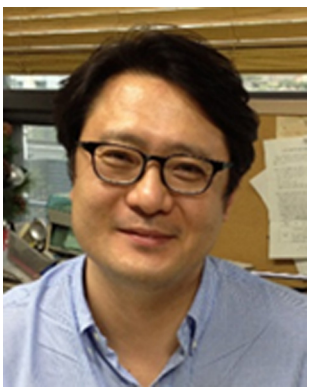
Qining Leo Wang is a doctoral student in Mechanical Engineering at the University of California, Los Angeles (UCLA). As an engineer, researcher, and entrepreneur, he is dedicated to democratizing digital microfluidics (DMF) to transform wet labs for molecular and cell biology. Leading a team of graduate and undergraduate students with a multidisciplinary background, he developed a proof-of-concept DMF chip design and manufacturing platform as well as a DMF control system, which are used by 60+ users in 4 countries. As a doctoral student, he received the UCLA University Fellowship, UCLA Dissertation Year Award, and SLAS Tony B. Travel Award.

Eric Hyunsung Cho

Hyun-Sung "Eric" Cho is a Mechanical Engineering Ph.D. candidate at the University of California, Los Angeles (UCLA). He performs research in MEMS with a focus on electrowetting-on-dielectric (EWOD) and digital microfluidics (DMF) in Micro and Nano Manufacturing Lab led by Professor CJ Kim. He received a B.S. from the Mechanical and Aerospace Engineering Department of Seoul National University. He interned in Soft Robotics & Bionics Lab at Seoul National University, led by Professor Yong-Lae Park. He also interned at the University of Michigan under Professor Katsuo Kurabayashi.

Jia Li

Jia Li is a senior MEMS engineer at Omnitron Sensors, Inc. He earned a Bachelor's Degree in Electronics Engineering from the University of Electronic Science and Technology of China (UESTC) and a Ph.D. in Mechanical Engineering from the University of California, Los Angeles (UCLA). His research focuses on the design and commercialization of electrostatic MEMS devices.



Kwanwoo Shin

Kwanwoo Shin is a Chemistry Professor at Sogang University, Korea. He holds a B.S. from Sogang University, an M.S. from KAIST, and a Ph.D. in Materials Science and Engineering from Stony Brook University. He serves as President of the Research Foundation at Sogang University and Scientists and Engineers Without Borders. He has received the National Medal of Merit and the Month of Scientist Awards from the Korean government. He was a visiting professor at Harvard University in 2012 and 2020. His research focuses on biological interfacial phenomena, with goals including artificial cells, hierarchical tissues, and paper-based biosensors

development. Without standardized chip fabrication processes, each company or research lab has to reinvent the wheel by developing its own fabrication processes and operation techniques. Furthermore, adoption of EWOD DMF remains limited to few applications. For example, despite the versatility for numerous molecular diagnostic applications, currently only three products are on the market: ePlex by GenMark[31] for respiratory pathogen detection, and SEEKER and FINDER by Baebies[32] for lysosomal storage disorders (LSD) detection and glucose-6-phosphate dehydrogenase (G6PD) deficiency, respectively. The limited applications of EWOD DMF, despite its inherent versatility, are also associated with the technical and cost barriers of chip fabrication. Additionally, the design of chips and the development of control systems pose a practical challenge, discouraging students, resource-limited research labs, and startups from exploring EWOD DMF for their own ideas or applications when quick proof-of-concept verifications are highly desired.

Drawing a comparison to digital ICs, Fig. 1 illustrates the obstacles encountered by EWOD DMF today. The remarkable success of the IC industry can be attributed to the standardized infrastructure that makes chip design and manufacturing accessible for a vast user base, as shown in Fig. 1(a). This standardization enables high-volume production, which in turn lowers technological hurdles and reduces manufacturing cost, creating a positive feedback loop that fosters industry growth. In contrast, without standardized infrastructure for EWOD DMF, users have to build everything themselves—from design and fabrication of the DMF chip to the development of the DMF control system—before they can test their ideas and applications, as shown in Fig. 1(b). Two decades of anecdotal experiences and numerous observations have led us to identify that the lack of standardized design and manufacturing is the main obstacle hindering the wide adoption and commercialization of EWOD DMF. These challenges are categorized and discussed below:

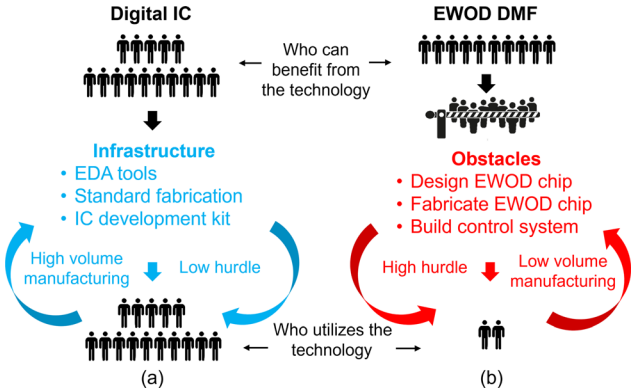


Fig. 1 The current ecosystems of (a) digital IC *vs.* (b) EWOD DMF.

Chip design

Designing a manufacturable EWOD chip requires following the foundry's design rules akin to the design rules of IC. However, most potential users of EWOD DMF, who often have backgrounds in molecular biology and chemistry, are not familiar with the photolithographic fabrication of IC or micro electromechanical systems (MEMS). Consequently, it takes a long time for them to acquire the fabrication knowledge and understand the design rules. Furthermore, the lack of specialized electronic design automation (EDA) tools for EWOD DMF forces designers to create chip layouts with conventional software and manually perform wire routing. This practice is time-consuming and error-prone, necessitating multiple rounds of costly fabrication and testing.

Chip fabrication

The fabrication of functional and reliable EWOD chips presents a significant challenge. Various parameters, including those

Tsung-Yi Ho

Tsung-Yi Ho is a Professor in the Department of Computer Science and Engineering, the Chinese University of Hong Kong (CUHK). He received his Ph.D. in Electrical Engineering from the National Taiwan University in 2005. His research interests include several areas of computing and emerging technologies, especially in design automation and the testing of microfluidic biochips. He was a recipient of the Best Paper Award at the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems in 2015. Currently, he serves as the VP Conferences of IEEE CEDA. He is a distinguished member of ACM and a fellow of IEEE.

Chang-Jin "CJ" Kim

Chang-Jin "CJ" Kim is a Distinguished Professor and the Volgenau Endowed Chair in Engineering at the University of California, Los Angeles (UCLA). He received his B.S. from Seoul National University, M.S. from Iowa State University, and Ph.D. from the University of California, Berkeley. Directing Micro and Nano Manufacturing Lab at UCLA, he performs research in MEMS with a focus on utilizing surface tension. The recipient of the NSF CAREER Award, Ho-Am Prize in Engineering, and IEEE Bosch MEMS Award, and fellow of ASME, IEEE, and AIMBE, Professor Kim serves on the editorial board of several journals and as co-Editor-in-Chief of Droplet.

atypical for IC fabrication (*e.g.*, material, thickness, deposition conditions, hydrophobic layer) must be properly selected, depending on many factors such as the sample liquid properties, operation conditions (*e.g.*, temperature), chip configuration (*i.e.*, parallel plates or coplanar configuration), and actuation parameters (*e.g.*, voltage, frequency). For prototyping, if an academic lab or startup opts to develop its own fabrication process, it typically takes several months for a student or technician to obtain basic training and longer to fabricate simple EWOD chips. For commercialization, where reliability is crucial, even after successful prototyping, three well-known EWOD chip failure mechanisms may undermine its reliability: current leakage (a short-term failure),[33–35] electric charging (a long-term degradation),[36,37] and biofouling.[38,39] While these fundamental problems have not been fully resolved, certain techniques can help alleviate the problems to achieve an acceptable product life cycle.[38–41] However, learning and applying these techniques further complicate the development of EWOD DMF, resulting in slow commercialization and limited applications.

Chip control

Operating an EWOD chip requires a relatively high voltage (*i.e.*, rarely below 40 V and commonly over 100 V) to independently power many electrodes, often involving multiple electronic instruments including a high-voltage source. The absence of a user-friendly control system is frequently a practical deterrence, especially for biology and chemistry researchers without an engineering background. While open-source hardware such as OpenDrop[42] and Dropbot[43] exist, they have a limited number of independent control channels (*e.g.*, less than 128). Moreover, in practice, these devices only work with their own EWOD chips, lacking the versatility to serve a diverse user base with widely different needs.

Consequently, the lack of standardized design, convenient manufacturing processes, and versatile control systems renders EWOD DMF inaccessible to a wide range of users. At the same time, the technological hurdles in chip manufacturing prevent readily available fabrication services, leading to high chip costs. This, in turn, discourages potential foundries and other entities from investing in manufacturing infrastructure, creating a chicken-and-egg dilemma that prevents industry growth and hinders the full potential of DMF from being reached, as summarized in Fig. 1(b).

2. Framework and workflow of the platform

To overcome the above obstacles and democratize DMF, a cloud-based cybermanufacturing ecosystem for EWOD DMF has been envisioned.[44,45] Here, we report the first proof-of-concept design and manufacturing platform for EWOD DMF, laying the groundwork for the envisioned DMF ecosystem. The platform consists of four main components: (i) an EWOD chip design platform, (ii) an EWOD chip manufacturing platform, (iii) a marketplace for EWOD control systems and ancillary modules, and (iv) an online DMF community. The workflow of the platform is schematically described in Fig. 2. To design an EWOD chip, a user can visit the design platform and create a layout file by drawing desired patterns of EWOD electrodes on a virtual canvas and allowing the embedded software to generate the wire routing, thereby completing a design file. To have EWOD chips fabricated, a user can upload the design file to the manufacturing platform and select the desired specifications (*e.g.*, chip type and quantity), based on which the platform will suggest chip foundries. Once the user selects a foundry and places an order, the foundry manufactures, packages, and ships the chips to the user. To utilize EWOD chips, a user can order an electronic control system and ancillary modules (*e.g.*, an overhead camera, temperature controller, and magnetic actuator) through the online marketplace. To perform their own experiments on the EWOD chip, a user can program the desired droplet operation protocols using a web-based graphic user interface (GUI) available on the platform and execute these protocols on the chip *via* the control system. Through an online community, users are encouraged to share their chip designs, droplet protocols, and experiences with fellow users and providers.

The ultimate vision of this initiative is to establish a publicly accessible platform that allows anyone to utilize EWOD DMF at an affordable cost, without the need to develop any infrastructure themselves. The platform would support design and manufacturing for common types of EWOD chips, whose fast growth to a large volume is likely to attract commercial foundries. It would also provide a platform for users to obtain control systems, software, and ancillary modules for different experiment protocols offered by various hardware and software developers. As achieving

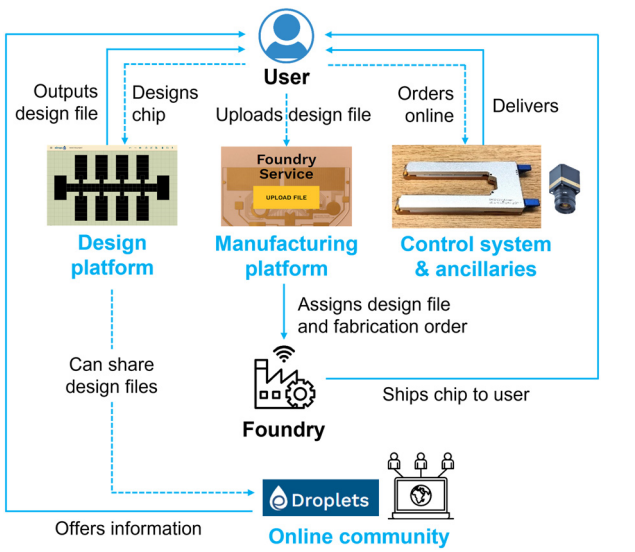


Fig. 2 Workflow of the cloud-based design and manufacturing platform for EWOD DMF. Broken lines and arrows indicate user operations, while solid lines indicate platform operations.

the full vision is beyond the scope of this paper, we will instead demonstrate a proof-of-concept platform with a basic workflow and outline the current development status of the platform in the following sections. The goal is to inspire and attract both academic and commercial entities to participate in the development of the cloud platform and overcome the technological obstacles of EWOD DMF in a collective and synergistic manner.

3. EWOD chip design platform

Since its layout essentially comprises a large number of similar electrodes, EWOD DMF presents a unique opportunity to build on standard unit cells predefined to meet the design rules for manufacturing, lowering the barrier of EWOD chip design and ensuring manufacturability. Inspired by EDA tools for IC, which incorporate IC design rules, we have developed an EWOD chip design platform (**https://cad.edroplets.org/**) that incorporates EWOD design rules. Currently, the design platform offers two exemplary chip types fabricated in two labs acting as foundries for this report: single-layer glass-based chips by Nanolab at UCLA and single-layer paper-based chips by Biological Interface Lab at Sogang University. Here, single layer means that all EWOD electrodes are fabricated on one conductive layer.

For EWOD DMF, a unit cell (referred to as the "unit electrode" hereinafter) can be defined by the (i) electrode pitch (*i.e.*, size + gap), (ii) shape (*e.g.*, square, hexagon), and (iii) gap between adjacent electrodes. As illustrated in Fig. 3, the design workflow allows users to draw desired layouts of unit electrodes on a canvas using a "painting pen" function. We selected the common square shape with a few different pitches (*i.e.*, 500 μm, 1000 μm, 1500 μm, 2000 μm, and 3000 μm) as a set of unit electrodes. Based on the fabrication capabilities of the two acting foundries, 5 μm and 30 μm were selected as electrode gaps for the glass-based and paper-based EWOD chips, respectively. These conservative design rules would ensure that any allowed design will lead to a working chip, despite the uncertainties in current fabrication and assembly, which will improve over time. A virtual canvas with variable grid size was implemented in the design platform to define the available sizes and positions of unit electrodes. By arranging and merging multiple unit electrodes on the canvas, one can create electrodes with various shapes and sizes for complex layouts while following the design rules. As an example of a standardization that dramatically simplifies the overall experience of users, we assume all the EWDO chips will have contact pads that match the pogo pins in the electronic control system detailed in section 6.

For a single-layer EWOD chip, drawing routing wires to connect many EWOD electrodes with as many contact pads can be time-consuming and error-prone, and is especially challenging if the number of electrodes exceed 100. To address this issue, an automated wire routing algorithm has been developed,[46,47] implemented in the design platform, and utilized here for glass-based and paper-based chips with various electrode sizes and shapes. The wire routing algorithm consists of three primary steps: (1) routing graph generation, which creates a graph with meshes to define the available wire paths between the EWOD electrodes and contact pads based on design rules; (2) path selection and routing, which determine the optimal wire connection point and the shortest wire path for each electrode, thereby generating wires to connect electrodes with contact pads; and (3) chip design file generation, which produces a .dxf file that foundries can use for chip fabrication. The user may ask the software to either create all the 256 contact pads to match the 256 pogo pins of the electronic control system described in section 6 or create only those wired to EWOD electrodes among the 256 contact pads. The former is useful for glass chips with a transparent indium tin oxide (ITO) layer, for which the full array of 256 contact pads helps the user align the chip to the control system (detailed in section 6), while

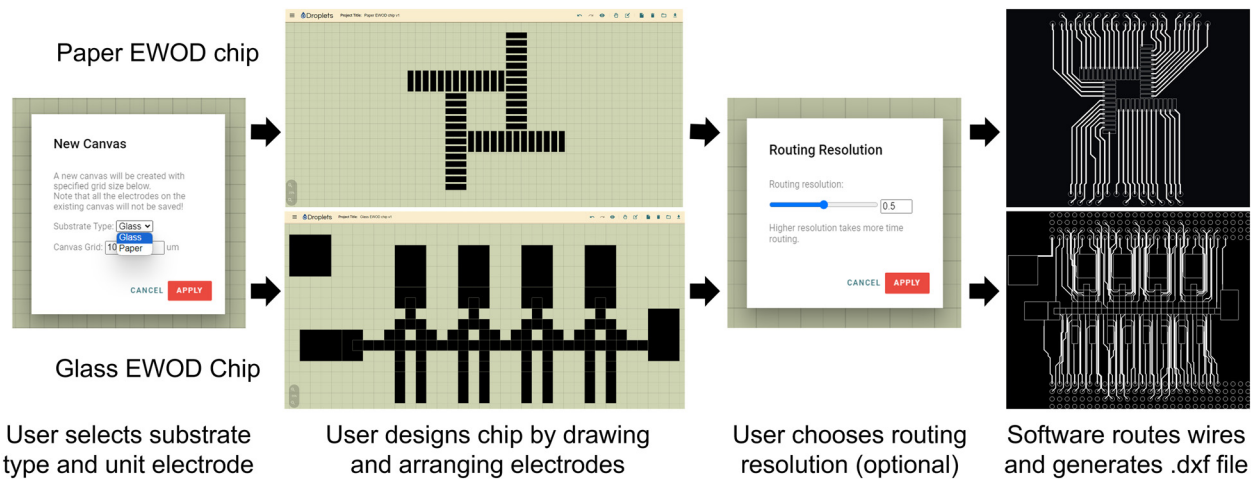


Fig. 3 Workflow of the EWOD DMF design platform for a single-layer EWOD chip (**https://cad.edroplets.org**).

the latter is useful for paper chips with a printed conductive layer, where a small number of silver contact pads helps reduce ink consumption.

Equipped with a drawing canvas, which features embedded design rules and automatic wire routing as well as a user-friendly workflow, the platform offers an accessible design tool that helps lower technological barriers and expedite the EWOD chip design process. Importantly, the design algorithm includes design rules as variable parameters, which can be easily modified to satisfy different design rules from different foundries. Currently, the platform supports the design of single-layer EWOD chips and has demonstrated its utility *via* glass-based and paper-based chips. Single-layer EWOD chips are suitable for relatively simple on-chip protocols as they can accommodate only a limited number of electrodes due to wire-routing constraints.[48] For applications requiring a dense array of electrodes, multi-layer (*e.g.*, PCB) or active matrix (*e.g.*, TFT) EWOD chips provide more practical solutions. To design multi-layer and active matrix EWOD chips, which the design platform is expected to serve in the future, open-source (*e.g.*, KiCAD) or commercial software (*e.g.*, Altium Designer and Cadence Virtuoso) can be used.

4. EWOD chip fabrication

Learning from the IC industry, which significantly benefited from standardization and modularity, we advocate to establish standardized fabrication processes for EWOD chips; this will free users from the need to develop their own fabrication processes and learn the intricacies of addressing reliability issues. To start, Table 1 categorises the currently prevalent types of EWOD chips and compares their key characteristics, such as common number and size of the electrodes, surface roughness, fabrication cost, and unique features.

Glass-based single-layer EWOD chips are a popular choice for academic research[1,18,22,49] due to several advantages. Glass is available as a circular wafer and is compatible with IC clean room processes like silicon, allowing small EWOD electrodes with a small gap between them. It is also transparent and smooth, offering additional freedom for sample observation and lowering the required voltage for droplet manipulation (*e.g.*, below 100 V),[50] respectively. Paper-based single-layer EWOD chips can be fabricated using an inkjet printer without requiring a photomask or clean room facilities. Featuring fast, simple, and low-cost manufacturing, paper-based EWOD chips are particularly suitable for rapid prototyping and are even considered favorable for environmental sustainability.[51] However, paper-based EWOD chips are limited by surface roughness and low printing resolution, which necessitates higher voltages and larger electrode sizes for droplet actuation.[52,53] Practically all single-layer EWOD chips share the inherent drawback of a limited number of electrodes due to wire-routing constraints.[48] Developed to overcome the routing issue on a single-metal-layer substrate, PCB-based EWOD chips allow a large number of electrodes on a given substrate.[54–58] They have become the choice for most commercial EWOD products today, in part benefiting from the large price drop in the PCB industry in the 2000s. However, PCB EWOD chips are restricted by their high surface roughness and pattern steps, which require a filler fluid or higher voltage (*e.g.*, more than 120 V) for droplet manipulation unless the PCB surface is polished.[54,55] More recently, thin-film-transistor (TFT)-based active matrix (AM) EWOD chips have emerged as a promising technology for DMF.[59–62] Leveraging the infrastructure of the display industry, tens of thousands of electrodes of ~100 μm size and each powered by a set of transistors can be fabricated on a glass substrate, opening the door to high-throughput, high-resolution applications (*e.g.*, single-cell based assay).[63–65] Although the TFT-based EWOD chip was considered to be prohibitively expensive, some companies in the display industry have begun to explore AM EWOD, utilizing their existing TFT manufacturing facilities[66,67] and leading to more affordable fabrication.

To accommodate various application requirements (*e.g.*, number of electrodes, cost, and driving voltage), we propose establishing standard fabrication processes for four types of EWOD chips: (i) glass-based single-layer EWOD chip, (ii) paper-based single-layer EWOD chip, (iii) PCB-based multi-layer EWOD chip, and (iv) TFT-based AM EWOD chips. If the fabrication processes are standardized, users can focus on their applications without the burden of developing their own fabrication processes, thereby accelerating technology adoption. Although single-layer glass EWOD chips have been the most popular choice in the past two decades, especially for academic research, we anticipate some of them will be replaced by TFT-based EWOD chips in the coming years, particularly for commercial applications.

Establishing standard fabrication processes for all the above EWOD chip types will require extensive process development and involve commercial foundries, which is beyond the scope of this paper. To get started, in this study we utilized commonly used fabrication processes to fabricate

Table 1 Comparison of the four main substrate types for EWOD chips

Chip Type	Glass	Paper	PCB	TFT
# of electrodes	~100	~50	~500	>10 000
Electrode size	~1 mm	~3 mm	~2 mm	0.1–1 mm
Surface roughness	Low	High	High	Low
Cost	High	Low	Medium	High
Key feature	Transparent	Fast process	Multi-layer	Active matrix

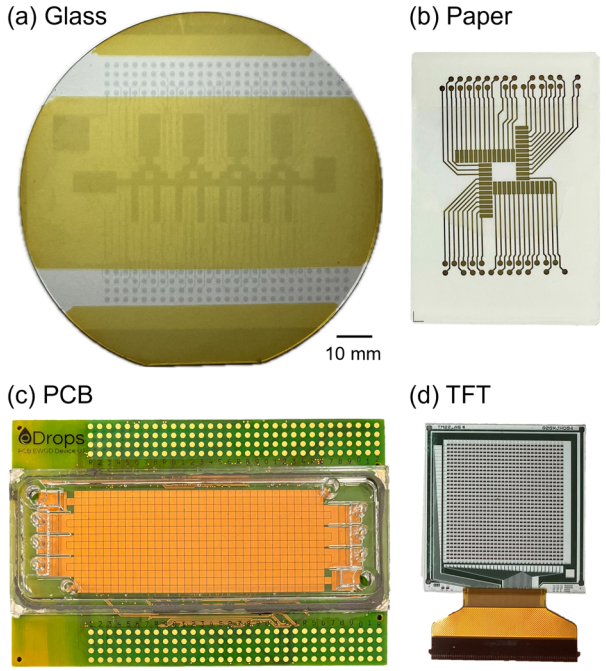


Fig. 4 Pictures of four types of EWOD DMF chips fabricated to support the platform. (a) A glass-based chip, (b) paper-based chip, (c) PCB-based chip, and (d) TFT-based chip. The scale bar applies to all pictures.

the aforementioned four types of EWOD chips with distinct configurations, as summarized in Fig. 4. As shown in Fig. 4(a), a single-layer glass-based EWOD chip was designed using the EWOD design platform described in section 3. The chip was designed with a parallel-plate configuration (*i.e.*, closed device with top and bottom plates) to enable droplet creation. The substrate (*i.e.*, bottom plate) of the chip was fabricated on a 4 inch glass wafer covered with a 180 nm-thick ITO layer. ITO was patterned using photolithography and wet etching to form the EWOD electrodes. A 2 μm-thick silicon nitride layer was deposited using plasma-enhanced vapor deposition (PECVD). The hydrophobic topcoat was made by spin-coating 70 nm Cytop. The contact pads were protected by a Kapton tape as a shadow mask while the dielectric and hydrophobic layers are coated and subsequently exposed for electrical connection. To make the cover (*i.e.*, top) plate, ITO glass was purchased (University Wafer) and coated with Cytop. Two layers of copper tape were used to create a 200 μm gap between the top and bottom plate and electrically connect them.

As shown in Fig. 4(b), a single-layer paper-based EWOD chip was designed using the EWOD design platform described in section 3. The chip had a one-plate configuration (*i.e.*, open device with no top plate) to enhance the featured simplicity, low cost, and fast turn-around. The electrode patterns were printed using a Fujifilm Dimatix printer equipped with silver nanoparticle (AgNP) conductive ink. The printed conductive ink electrode was sintered at 170 °C for 15 minutes, resulting in low resistance. Subsequently, a dielectric layer of polysulfone and a hydrophobic layer of Teflon were deposited by spin coating. The spin-coated films were annealed at 100 °C for 15 min after each coating process to relieve internal stresses. Finally, the chip was immersed in silicone oil (5 cSt) for 12 h, resulting in an oil-impregnating surface that facilitates liquid movement.

As shown in Fig. 4(c), the multi-layer PCB-based EWOD chip was designed using an open-source software, *i.e.*, KiCAD. The chip had a parallel plate configuration (*i.e.*, closed device with top and bottom plates) with filler oil to facilitate droplet operations. More than 500 electrodes were implemented on a single chip to accommodate various complex protocols. The bottom plate including a dielectric layer was fabricated by a PCB manufacturer and covered with a hydrophobic layer by spin-coating Cytop at UCLA. The top plate was ordered from a plastic injection molding company and coated with a conductive polymer and a hydrophobic layer at UCLA. Developed as the first standard EWOD chip for the proposed platform, the PCB-based EWOD chip will be reported in detail as a separate publication.

As shown in Fig. 4(d), a TFT-based EWOD chip with a square array of 32 × 32 electrodes each 1 mm in size was ordered from TIANMA Microelectronics Corp. The chip was completed at UCLA to have a parallel-plate configuration with an air environment (*i.e.*, no filler oil used), to showcase the advantage of its smooth surface and low topography. The bottom plate was hydrophobized by spin-coating Cytop, and the top plate was fabricated and assembled with the bottom plate using the process described for the glass-based EWOD chip above.

We have verified the four types of EWOD DMF chips for basic droplet operations and got some of them tested by a small number of collaborating labs (see Acknowledgements). Most of the fabrication services will be open in the near future for select groups of users to further improve and validate the fabrication processes. After a few additional phases of progress for quality control, we aim to open the fabrication platform to the public, thereby enabling broader participation from academic labs, startups, and foundries.

5. EWOD chip manufacturing platform

Once fabrication processes are standardized and foundry processes ready for service in the future, we envision a fully functional manufacturing platform. When matured, the platform will allow users to access fabrication capabilities and pricing information from various foundries so that users can select a suitable foundry for their applications. The standardized fabrication processes will define critical fabrication parameters, such as (i) type and size of chip, (ii) thickness and deposition method of dielectric and hydrophobic layers, and (iii) gap between top and bottom plates for parallel-plate devices. Consequently, foundries would only require two pieces of information from the user: a chip design file made on the design platform and the

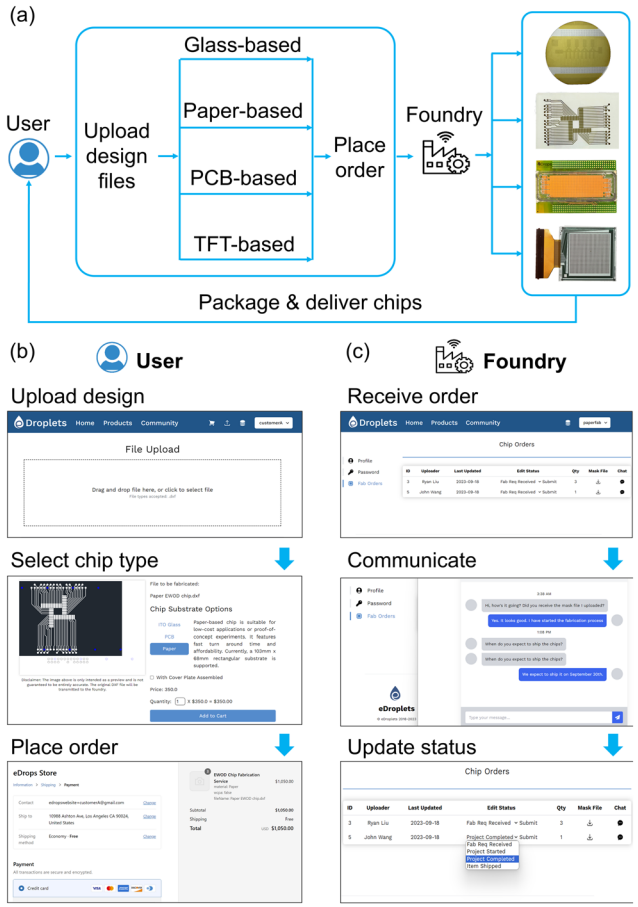


Fig. 5 Workflow of the EWOD DMF manufacturing platform. (a) Overview of the foundry service workflow. (b) Web interfaces of the platform for users, and (c) web interfaces of the platform for foundries.

quantity of chips being ordered. This streamlined approach will simplify the foundry service workflow, making the chip ordering easy, even to users with little background in EWOD technology.

Currently, we have prototyped a manufacturing platform that demonstrates a foundry service workflow, as schematically illustrated in Fig. 5(a). As shown in Fig. 5(b), users can upload chip design files, select chip types and quantities, and place an order. Upon confirmation and payment, the platform assigns the order to a designated foundry for manufacturing. As shown in Fig. 5(c), foundries can log into the platform with their own accounts and accept the assigned order, update the project status, and ship the fabricated chips to users. Until commercial foundries are established, which will take some time, Biological Interface Lab at Sogang University and Micro and Nano Manufacturing Lab at UCLA may act as provisional foundries to fabricate the paper-based and glass- or PCB-based EWOD chips, respectively. For TFT-based EWOD chips, TIANMA Microelectronic Corp. has been currently identified as a potential foundry. Although not all the fabrication services outlined here will be available to the public soon, most of them will be open for a limited number of requesting users while improving the utility and reliability of the cloud-based manufacturing platform. As the standardization matures and user base grows, we anticipate that commercial foundries will join the platform to provide industrial fabrication services, helping the platform grow toward a self-sustaining ecosystem for DMF.

6. Marketplace for EWOD control systems and ancillary modules

Once EWOD chips are received from a foundry, a user will need an electronic control system and perhaps ancillary modules (*e.g.*, overhead camera, temperature control module, magnetic actuator) as well to operate the chip for their experiments. We envision an online marketplace for users to order various open-source or commercial control systems as well as ancillary modules provided by hardware developers and companies. The format of the chip–system interface (*e.g.*, a contact pad array with fixed pitch for passive EWOD chips; a flexible printed circuit (FPC) with fixed number of pins for AM EWOD chips) will be standardized and released to hardware developers and other users *via* the platform. The standardized format of the chip–system interface is also implemented in the chip design platform so that all the chips designed and fabricated through the platform can be operated by any control system and ancillary as far as they follow the standard.

In the present study, to completely demonstrate the workflow from chip design and fabrication to chip control, we developed a compact electronic control system compatible with all passive EWOD chip types (*e.g.*, glass, PCB, silicon, and paper) of diverse shapes, sizes, and thicknesses,[68] as shown in Fig. 6(a). As shown in Fig. 6(b) the control system is powered and operated by a computer through a USB cable. A web-based GUI (**https://gui.edroplets.org/**) was developed for the operation and is accessible on the platform. As shown in Fig. 6(c), a user can create the virtual electrode layout on the GUI canvas after simply converting the design file to an operation file (named .ewds for EWOD sequence) on the platform. By assigning actuation parameters (*i.e.*, voltage and frequency) and selecting virtual electrodes for on or off, a user creates one actuation step (referred to as "frame" in the GUI). Multiple frames define an actuation sequence, and a user can run the sequence on the computer, which transfers electric signals to the control system *via* USB. Actuation sequence files can be saved in a standardized format named as .ewds, facilitating the sharing of experiment protocols.

As shown in Fig. 6(a) and (b), the EWOD control system includes four main components: (1) system hardware (chassis), (2) electronic circuits, (3) chip–system interface, and (4) web-based GUI. The system hardware, which consists of two aluminium chassis (plates), arrays of pogo pins, and an alignment stencil, ensures quick and easy loading and unloading of the EWOD chip. Housed in the aluminum chassis, the control circuits utilized HV3418, a serial-to-parallel high-voltage converter, to provide voltages in the range of 40–180 V DC or 80–360 V_{pp} AC at a frequency of up

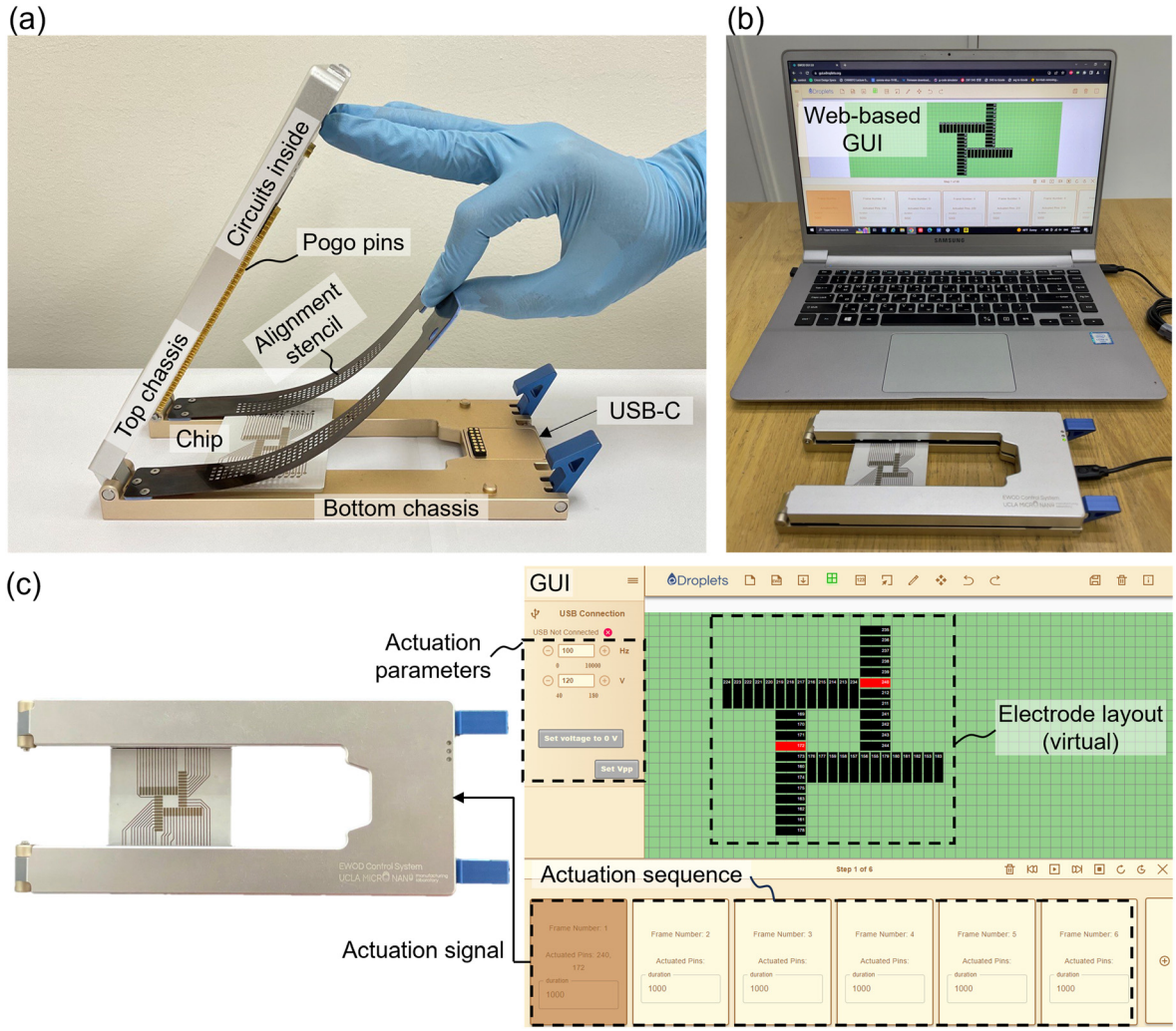


Fig. 6 An electronic control system developed for passive EWOD chips (shown with a paper-based chip). (a) A picture of the system when opened, (b) a picture of the system connected *via* USB to a computer, which provides power and software, and (c) the web-based GUI in the actuation sequence programming mode using the electrode layout imported from the design file.

to 10 kHz through 256 output channels. The chip–system interface utilizes a 256 spring-loaded pogo-pin array that aligns with and presses on the 256 contact pads on an EWOD chip to provide electric signals. A unique chip–system alignment mechanism was designed by using a polyimide stencil with 256 through-holes. After placing an EWOD chip on the bottom stage (chassis) and letting the stencil rest on the chip, the user can nudge the chip until all the contact pads on the chip are clearly seen through the holes, which indicates successful alignment. Then, the system can be swung closed until the latches lock and secure the chip. With all the pogo pins passing through the holes and landing on the contact pads, electric connection between the system and the chip is established and ready for operation. The U-shape chassis design accommodates integration of ancillary modules, such as heaters or sensors, by leaving sufficient space below the installed chip.

For most simple biological and chemical protocols, 256 independent control channels should be sufficient to control passive EWOD chips for on-chip experiments. However, more complex protocols or highly multiplexed assays may require an AM EWOD chip to independently control a large number of electrodes. In this study, for testing, we used a prototype electronic control system for the AM EWOD chip provided by TIANMA Microelectronics. Companies such as ACXEL have also developed AM EWOD control systems for various applications. Developing a universal AM EWOD control system will require more complicated driving circuits and control algorithms to manage a large number of electrodes (*i.e.*, more than 100 000). Developers and companies with expertise in display module design may develop a universal AM EWOD control system and make it available *via* the marketplace platform in the future.

7. DMF online community

We have developed an online community, which currently includes a project gallery and a user forum. Drawing inspiration

Fig. 7 EWOD DMF online community (**https://community.edroplets.org**). (a) Home page of the project gallery, (b) web page of a shared project, and (c) web page of questions on the user forum.

from open-source project repositories in the software industry (*e.g.*, GitHub), a DMF project gallery allows users to share their chip designs and experiment protocols in a standardized format, as shown in Fig. 7(a). This enables other users to download, modify, and create derivative designs and protocols. Currently, the project gallery allows users to share their EWOD chip designs by uploading files in a .dxf format and write a description of the key features of their chips. It also allows other community users to comment on the project for questions and discussions. Fig. 7(b) shows the web page of an example project. Additionally, an online forum offers a place where users can ask questions, provide answers, share practical experiences, and offer feedback on tools and services. Fig. 7(c) shows a list of example questions on the user forum web page. By fostering sharing, the online community will help create additional knowledge, generate new data, and expand the user pool to facilitate synergistic growth of the DMF ecosystem.

8. Conclusion and Outlook

Identifying technological and resource hurdles as the main culprit for the slower-than-expected adoption of EWOD DMF, we have proposed a standardized design and manufacturing platform for EWOD DMF to catalyse an easy and widespread adoption of the technology for education, research, and commercialization. In line with this vision and to kickstart EWOD DMF adoption, we have developed a proof-of-concept cloud-based design and manufacturing platform for EWOD DMF chips composed of four components: (i) a chip design platform with automatic wire routing; (ii) a chip manufacturing platform with the foundry service workflow; (iii) a marketplace for control systems and ancillary modules; and (iv) a community to share information. Four EWOD chip substrate types (*i.e.*, glass, paper, PCB, and TFT) have been fabricated and tested for common droplet operations, setting the direction toward a fully functional platform with a set of standardised fabrication processes for various applications in the future. By demonstrating that the workflow of the platform lowers engineering and cost burdens for prospective users, we anticipate growing acceptance of EWOD DMF. As the technology becomes more accessible, we envision that the user base will reach a critical mass so that an increased production volume lowers the manufacturing cost, which would further expand the user base. This resulting positive feedback loop, akin to the IC industry, would allow EWOD DMF to achieve the much-anticipated revolution for LoC applications.

Data availability

No new experimental data were generated or analyzed as part of this article.

The code for the EWOD DMF design platform can be found at: **https://github.com/tommy44458/eDroplets-CAD**. The version of the code employed for this study is in the Master branch.

The code for the EWOD DMF manufacturing platform and GUI is currently deposited in a private GitHub repository, which will be made available to the public when the platform matures with improved cybersecurity features.

Author contributions

Conceptualization: C.-J. K., J. L., and Q. L. W. Investigation: Q. L. W., E. H. C., J. L., H.-C. H., S. K., Y. P., and L. X. Methodology: Q. L. W., E. H. C., J. L., H.-C. H., S. K., L. X., K. S., T.-Y. H., and C.-J. K. Project administration: C.-J. K. and Q. L. W. Resources: C.-J. K., T.-Y. H., and K. S. Funding acquisition: C.-J. K., T.-Y. H., K. S. Software: Q. L. W., H.-C. H., K. T., S. K., Z. H., B. C., D. Y., C.-C. W, and C. C. Supervision: C.-J. K., T.-Y. H., and K. S. Writing – original draft: Q. L. W. and C.-J. K. Writing – review & editing: Q. L. W., H.-C. H., S. K., K. S., T.-Y. H., and C.-J. K.

Conflicts of interest

There are no conflicts to declare.

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