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Thermally tunable anti-ambipolar heterojunction devices†

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Two-dimensional materials and their van der Waals heterostructures have emerged as a research focal point for constructing various innovative electronic devices due to their distinct photonic and electronic properties. Among them, anti-ambipolar devices, characterized by their unique nonlinear electrical behavior, have garnered attention as novel multifunctional components, positioning them as potential contenders for building multi-state logic devices. Utilizing the properties of few-layer $As_{0.4}P_{0.6}$ and $PdSe_2$, we have constructed an anti-ambipolar heterojunction device. At 300 K, the device exhibits a peak voltage (V_{peak}) of −3 V and a peak-to-valley ratio (PVR) close to 8×10^3, and the PVR can be modulated by bias voltage. Furthermore, by characterizing the anti-ambipolar attributes at different temperatures ranging from 80 K to 330 K, we have elucidated the thermally tunable feature of the device. At 330 K, a certain PVR ($\sim 10^3$) and a large V_{peak} (~ -16 V) are obtained, while a PVR exceeding 10^8 has been achieved at 80 K. This temperature-related sensitivity empowers the device with significant potential and thermal tunability in various applications.

1. Introduction

In recent years, two-dimensional (2D) materials and their van der Waals heterojunctions (vdWHs) have shown great potential to gradually replace conventional semiconductors as building blocks for multifunctional devices due to their unique optical, electronic, and magnetic properties, and their dangling bond-free surface.[1–8] Various device types based on heterojunctions have been demonstrated, such as tunneling field-effect transistors,[5,9,10] memory devices,[11,12] photodetectors,[13,14] p–n junction diodes,[15,16] rectification devices,[17–19] *etc.* Among them, the anti-ambipolar property device, which was initially realized by a gate-tunable carbon-nanotube/monolayer-layer MoS_2 p–n heterojunction,[20] has attracted a great deal of attention. The anti-ambipolar property exhibits a nonlinear feature, which results in a significant decrease in electrical current with an increase in the gate voltage.[21,22] Recently, this property has also been observed in numerous vdW p–n heterojunctions, such as p-WSe_2/n-SnS_2,[23] p-WSe_2/n-WS_2,[24] p-WSe_2/n-MoS_2,[25] *etc.* Considering that the anti-ambipolar property behaves similarly to a negative differential resistance (NDR), it also shows promise for applications in logic circuit design.[26] Even more exciting, in these anti-ambipolar devices, the peak-to-valley ratio (PVR), serving as a crucial parameter for evaluating device performance, can reach as high as 10^3–10^5 at room temperature,[23] significantly surpassing existing NDR devices.[27,28] These advantages make anti-ambipolar devices potential candidates for constructing three-channel devices for signal processing and information storage, and make them more promising for practical applications in multi-valued logic circuits compared to NDR devices.[25,29,30]

However, to date, the comprehension of the mechanism behind anti-ambipolar behaviors remains the main requirement for in-depth and extended investigation,[21] and although recent studies have begun to explore the temperature-dependent anti-ambipolar characteristics,[31,32] there remains a lack of comprehensive research on ambipolar behavior across a wide temperature range. Specifically, the influence of temperature on the PVR from 77 K to 330 K has not been thoroughly investigated. Additionally, the design and fabrication of appropriate anti-ambipolar field-effect transistor (FET) devices using vdWHs pose a huge challenge, thereby impeding the advancement of logic

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devices founded on this distinctive characteristic.[21,33–35] Recently, arsenic phosphorus ($As_{0.4}P_{0.6}$), a material synthesized from ultrapure gray arsenic and red phosphorus,[36–38] has attracted more attention. $As_{0.4}P_{0.6}$ with high carrier mobility and a narrow bandgap of about 0.36 eV typically exhibits p-type behavior. This is a suitable material for building devices, inspired by black phosphorus (BP)-based FETs.[39,40] Also, palladium diselenide ($PdSe_2$) is an emerging air-stable n-type dominant 2D material, with high room temperature mobility and a widely tunable bandgap (0.03–1.3 eV).[41–43] Considering band alignment and material properties, $As_{0.4}P_{0.6}$ and $PdSe_2$ are suitable materials for constructing p–n heterojunctions and probable anti-ambipolar devices.

In this study, we have presented an anti-ambipolar device built upon the vdWH composed of $As_{0.4}P_{0.6}$ and $PdSe_2$. Our research demonstrates the realization of high-performance thermally tunable anti-ambipolar devices, where the drain is implemented using $As_{0.4}P_{0.6}$, the source employs $PdSe_2$, and the heterojunction area serves as the channel. At room temperature, a PVR of $\sim 8 \times 10^3$ and a peak voltage (V_{peak}) of -3 V can be attained. In particular, we uncover the thermally tunable sensitivity of the anti-ambipolar device, which can be used to finely tune the PVR and V_{peak} of the device *via* the temperature. At low temperature, we achieved a PVR exceeding 10^8. Furthermore, as the temperature reached 330 K, the anti-ambipolar characteristics were suppressed to a certain degree. Our work presents a heterojunction device fabricated using the previously unreported combination of $As_{0.4}P_{0.6}$ and $PdSe_2$, aiming to contribute to the field of anti-ambipolar devices. We believe that the distinctive behavior observed in the $PdSe_2/As_{0.4}P_{0.6}$ heterojunction, particularly its thermally tunable anti-ambipolar characteristics, offers valuable insights and potential applications in multifunctional device design.

2. Experimental

2.1. Fabrication and characterization of the anti-ambipolar heterojunction device

The few-layer $PdSe_2$ and $As_{0.4}P_{0.6}$ were achieved by mechanical exfoliation from their bulk counterpart using tap (NITTO 224S) and clean polydimethylsiloxane (PDMS). A Si substrate covered by a SiO_2 layer (285 nm) was cleaned in turn with acetone, isopropanol, and deionized water for 10 min. The few-layer $As_{0.4}P_{0.6}$ and $PdSe_2$ were transferred onto the PDMS and then onto the SiO_2/Si substrate in turn. After that, the SiO_2–Si substrate with $As_{0.4}P_{0.6}$ and $PdSe_2$ was spin-coated with PMMA 950K (3000 rpm, 60 s) and placed on a hot plate at 180 °C for 2 min. The electrode pattern was defined using standard electron beam lithography (Vistec EBPG 5000plus ES), and Cr (5 nm)–Au (60 nm) electrodes were deposited using electron beam evaporation (BOC-500).

2.2. Characterization analyses

An optical microscopic image of the device was obtained using an optical microscope (Olympus, LEXT-OLS4000), the electron microscopic image of the device was characterized using a transmission electron microscope (TEM, Tecnai G2 F20 U-TWIN), and the thickness of the sample was characterized using an atom force microscope (AFM, Bruker Multimode 8HR). The material quality was characterized using a Raman spectroscope (Renishaw InVia plus, 514 nm excitation laser). All the electrical measurements were conducted on a manual probe station (Lakeshore, TTP4) equipped with a vacuum pump, a temperature control system, and a semiconductor characterization system (Keithley 4200A-SCS).

3. Results and discussion

A schematic of the three-dimensional view of the $PdSe_2/As_{0.4}P_{0.6}$ vdWH device is shown in Fig. 1a. The few layers of $PdSe_2$ and $As_{0.4}P_{0.6}$ were acquired by mechanical exfoliation from bulk materials, and then stacked through an all dry transfer method (details are given in the Experimental section and Fig. S1, ESI†). As shown in the blue dashed frame in Fig. 1, crystalline $PdSe_2$ has a pentagonal structure, and $As_{0.4}P_{0.6}$ belongs to the typical orthogonal crystal phase. To further confirm their lattice structure, the exfoliated $PdSe_2$ and $As_{0.4}P_{0.6}$ flakes were transferred onto Cu grids for TEM measurements, respectively. $As_{0.4}P_{0.6}$ on a Cu grid is shown in Fig. S2a (ESI†), and the high-resolution TEM image of $As_{0.4}P_{0.6}$ (Fig. S2b, ESI†) clearly shows the pentagonal structure of the $As_{0.4}P_{0.6}$ with the (001) planes (lattice constant of 4.4 Å) and (100) planes (lattice constant of 3.5 Å). The high-quality single-crystal nature of $As_{0.4}P_{0.6}$ is further confirmed by the corresponding selected area electron diffraction (Fig. S2c, ESI†). The low-magnification TEM image of the $PdSe_2$ is presented in Fig. S1d (ESI†), and the high-resolution TEM and SAED images (Fig. S2e and f, ESI†) show that the lattice spacings are 2.92 Å and 2.82 Å, which are attributed to the (020) and (200) planes of the $PdSe_2$, indicating that the $PdSe_2$ is a single crystal with an orthogonal crystal structure.

An optical microscope (OM) image of the fabricated device is shown in Fig. 1b; the white dashed frame outlines the $PdSe_2$ and the red dashed frame outlines the $As_{0.4}P_{0.6}$. Raman characterizations of $PdSe_2$, $As_{0.4}P_{0.6}$, and the heterojunction area ($PdSe_2$ as the top layer) are shown in Fig. 1c. The A_g^1–B_{1g}^1, A_g^2, B_{1g}^2, and A_g^3 modes of the $PdSe_2$ are positioned at 143, 206, 222, and 256 cm^{-1}, respectively. Furthermore, the three peaks of $As_{0.6}P_{0.4}$ at 253, 349, and 430 cm^{-1} correspond to the A_g^1, B_{2g}, and A_g^2 modes, respectively. The characteristic peaks of both $PdSe_2$ and $As_{0.4}P_{0.6}$ can be seen in the Raman spectra of the heterojunction, indicating that $As_{0.4}P_{0.6}$ and $PdSe_2$ remain unchanged after the formation of the heterojunction. Fig. 1d shows an AFM image of the heterojunction, measured along the white dashed lines in Fig. 1d, respectively. Thicknesses of 8.38 nm and 4.03 nm were obtained for the few-layers of $As_{0.4}P_{0.6}$ and $PdSe_2$, respectively, as shown in Fig. 1e and f.

Utilizing heavily doped silicon as the back gate, individual characterization of the transfer curves for $PdSe_2$ and $As_{0.4}P_{0.6}$ was conducted, as depicted distinctly in Fig. 2a, prior to

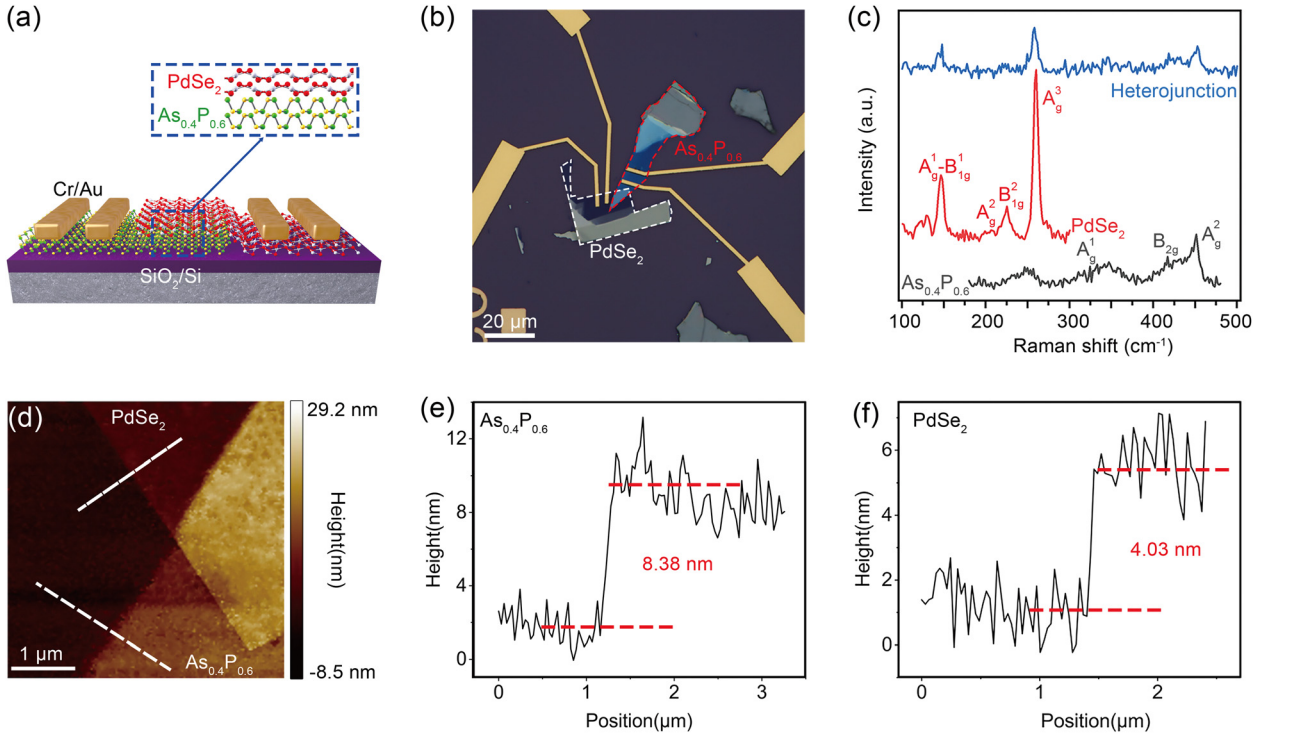

Fig. 1 Characterizations of the heterojunction device. (a) Three-dimensional schematic representation of the device, where the enlarged region within the blue dashed box highlights the heterojunction area. The lower layer is $As_{0.4}P_{0.6}$, while the upper layer is $PdSe_2$. (b) The OM image of the device, the white dashed box represents the presence of $PdSe_2$, while the red dashed box highlights $As_{0.4}P_{0.6}$, scale bar: 20 μm. (c) The Raman spectra of $As_{0.4}P_{0.6}$, $PdSe_2$, and the heterojunction, respectively. The Raman peaks within the heterojunction exhibit characteristic peak positions including both materials. (d) Localized AFM images of the heterojunction. (e) The thickness of $As_{0.4}P_{0.6}$ with the measurement curve taken along the white dashed line on $As_{0.4}P_{0.6}$ in (d). (f) The thickness of $PdSe_2$ with the measurement curve along the white dashed line on $PdSe_2$ in (d).

measuring the electrical properties of the heterojunction. The transfer characteristics obtained reveal that the current through $As_{0.4}P_{0.6}$ augments concomitantly with increasing negative gate voltages, indicative of its p-type behavior. On the other hand, the current of $PdSe_2$ exhibits an inclination to increase in response to both positive and negative gate voltages, with a minimum current manifesting at a gate voltage of −30 V, which corresponds to the OFF state and unequivocally signifies a preponderance of n-type dominant ambipolar behavior. The output characteristics of $PdSe_2$ and $As_{0.4}P_{0.6}$ under diverse bias voltages are respectively illustrated in Fig. S3 and S4 (ESI†), evincing an absence of pronounced rectification. This suggests that the contact potential barrier between the electrode and the material is minimal, ensuring that the electrical tests can accurately reflect the intrinsic properties of the materials. Based on the p–n behavior exhibited by the two materials, the $As_{0.4}P_{0.6}$ side is designated as the drain electrode, while the $PdSe_2$ side serves as the source electrode.

Fig. 2b shows the transfer characteristics of the device under several forward biases, manifesting pronounced anti-ambipolar properties. When the gate voltage is below −30 V, the device is primarily in the OFF state. With increasing gate voltage, the current gradually increases under a constant bias. When the gate voltage is over the V_{peak} (∼−3 V), the current exhibits a decreasing trend that is similar to negative differential conductance. It is observed that as the bias voltage increases from 0.2 V to 2 V, the magnitude of the current decline also increases, showing increasingly prominent anti-ambipolar properties. The mapping plot of this phenomenon is clearly illustrated in Fig. 2c. To further investigate the current variation within the gate voltage range of −30 to 20 V, the PVR is calculated by taking the ratio of the maximum and minimum currents. The resulting PVR curve demonstrates a monotonically increasing trend, and the PVR can reach a maximum of approximately 8×10^3 at a bias voltage of 1.8 V, showing the high performance of the anti-ambipolar characteristic at room temperature.

The transfer curve, demonstrating an analogous negative differential transconductance phenomenon, has engendered our focal interest. Fig. 3a illustrates the transfer curve at V_{ds} = 0.5 V. The transfer curve can be divided into four regions. In region I, the back gate voltage is less than −40 V, and the $PdSe_2$ channel is depleted, which results in the minimum drain current and indicates that the device is fully turned off. In region II, the back gate voltage is about −40 to −10 V, the bias current starts to be dominated by the $PdSe_2$ channel, and the holes in $As_{0.4}P_{0.6}$ and the electrons in $PdSe_2$ are gradually accumulated and participate in the current transport, leading to the ON-state in the entire p–n junction. In region III, the back gate voltage is about −10 to 15 V, and it is partially pinched off due to the depletion of electron carriers in the $As_{0.4}P_{0.6}$ channel being much faster than the increase in the

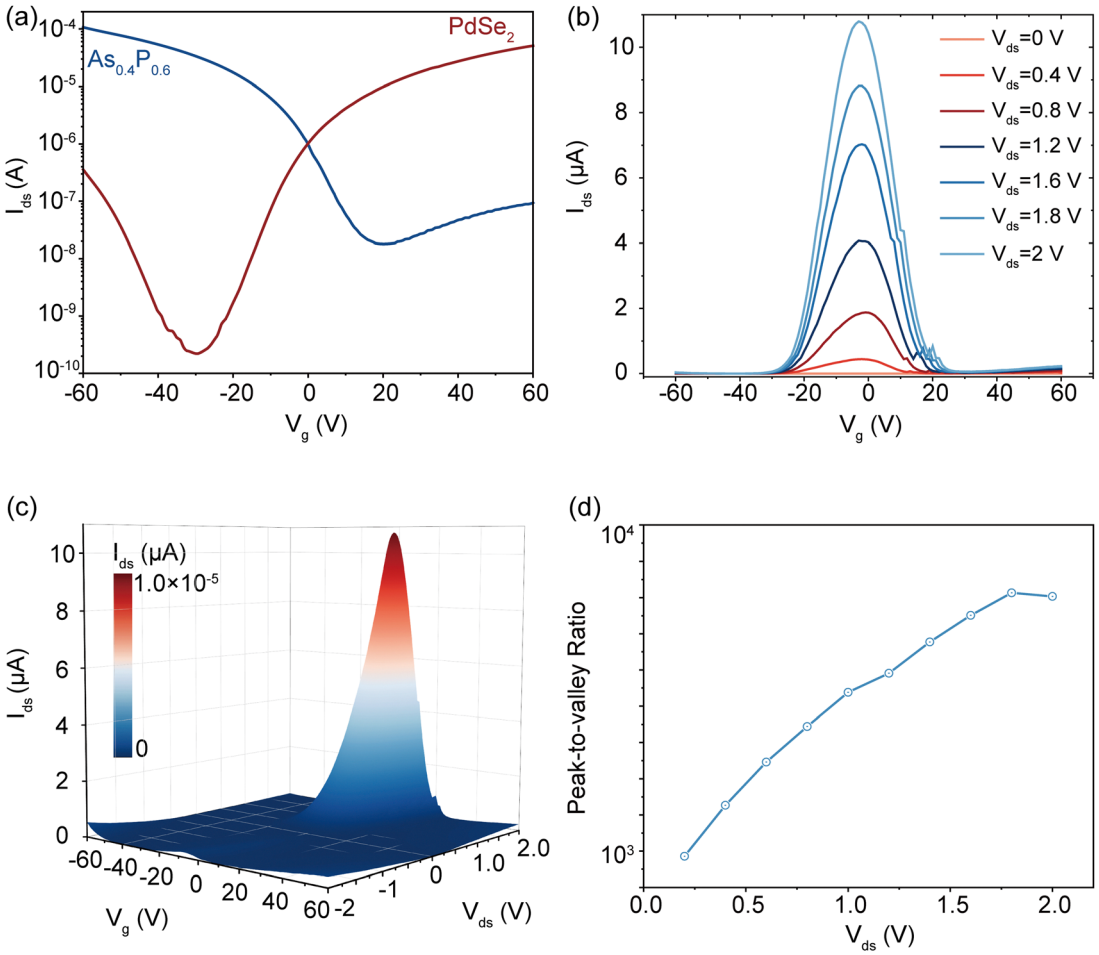

Fig. 2 Characterization of the transfer properties of the heterojunction device. (a) The transfer characteristics curves of $As_{0.4}P_{0.6}$ (in blue) and $PdSe_2$ (in red) under a forward bias voltage of 1 V. (b) The transfer characteristics curves of the heterojunction under various forward biases (from 0.2 V to 2 V, step 0.2 V). (c) The three-dimensional transfer characteristics curves of the heterojunction under various forward biases. (d) The dependence of PVR on forward biases.

$PdSe_2$ channel, causing the decrease in overall channel current. On the other hand, the whole device cannot be completely turned off because of the small band gap (0.326 eV) of $As_{0.4}P_{0.6}$ and the strong capacitance screening effect, which is similar to that in BP.[44] This phenomenon leads to the device having two OFF-states, and the ON/OFF ratios are about 10^4 and 10^2, respectively. In region IV, the back gate voltage is over 15 V, the $PdSe_2$ channel regains dominance and the current in both channels starts to increase. In conclusion, the transfer curve can be modulated by the gate voltage.

The energy band diagrams of this heterojunction under gate voltage are shown in Fig. 3b. The band diagram of $PdSe_2$/$As_{0.4}P_{0.6}$/SiO_2/Si before contact is shown in Fig. S5 (ESI†), showing a type-II band alignment between $As_{0.4}P_{0.6}$ and $PdSe_2$. The energy positions of the valence and conduction band are referred from previous reports.[36,45,46] The gate voltage can provide the unique behavior by controlling the bending of the energy band in the channel region. When the forward gate voltage is less than −40 V and the bias is forward, both $As_{0.4}P_{0.6}$ and $PdSe_2$ are p-type, with their Fermi levels close to the valence band, the barrier formed at the interface between $As_{0.4}P_{0.6}$ and $PdSe_2$ hinders the hole transport, resulting in the device being in an almost completely OFF state. As the gate voltage is increased, $PdSe_2$ transitions to n-type, and the Fermi levels are close to the conduction band. The energy band of $PdSe_2$ bends upwards and the energy band of $As_{0.4}P_{0.6}$ is pulled downwards, reducing the barrier between the two materials. Under forward bias, electrons transfer from $PdSe_2$ to $As_{0.4}P_{0.6}$, while holes transfer from $As_{0.4}P_{0.6}$ to $PdSe_2$, resulting in an increase in current. However, when the gate voltage exceeds −10 V, although the energy bands of $As_{0.4}P_{0.6}$ continue to pull downwards, further reducing the barrier and allowing electrons to transfer from $PdSe_2$ to $As_{0.4}P_{0.6}$, the holes in $As_{0.4}P_{0.6}$ are rapidly depleted as the gate voltage increases. This significant reduction in hole transfer from $As_{0.4}P_{0.6}$ to $PdSe_2$ results in a decrease in current. When the gate voltage increases to exceed 15 V, as the energy bands of $As_{0.4}P_{0.6}$ continue to be pulled downwards, a type-I heterojunction is formed, allowing a substantial number of electrons to transfer from $PdSe_2$ to $As_{0.4}P_{0.6}$, leading to an increase in current. With increasing gate voltage, the current of the device initially increases and reaches a peak at V_g = −10 V and then decreases, demonstrating obvious

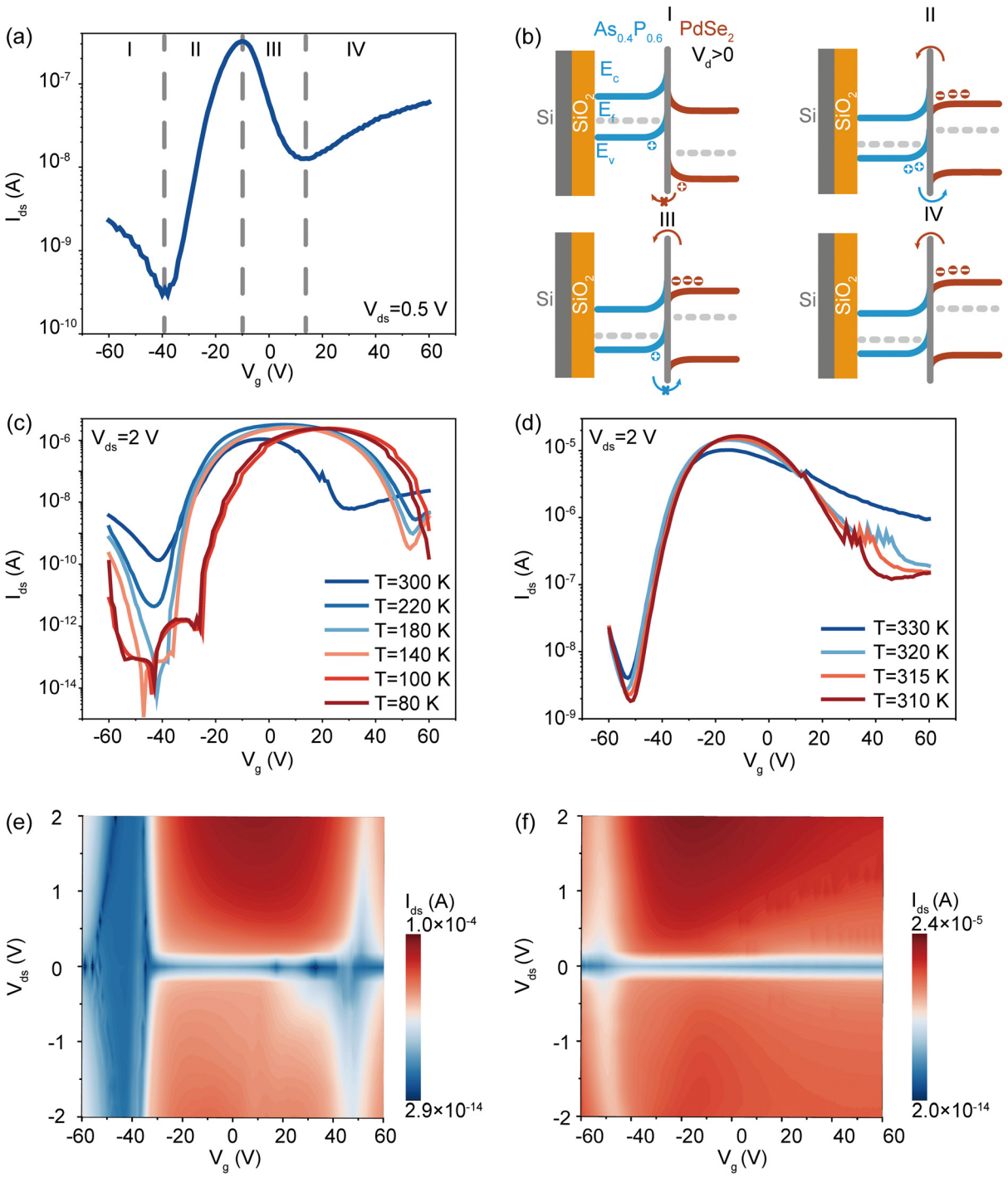

Fig. 3 Energy band and thermally tunable transfer properties of the heterojunction device. (a) The transfer characteristic curve at a forward bias voltage of 0.5 V, which can be divided into four regions. (b) The corresponding energy band bending of the four regions in the transfer characteristic curve in (a). (c) The transfer characteristic curve of the heterojunction under a forward bias voltage of 2 V for temperatures ranging from 80 K to 300 K. (d) The transfer characteristic curve of the heterojunction under a forward bias voltage of 2 V for temperatures ranging from 310 K to 330 K. (e) At a temperature of 140 K, the bias current mapping plot of the heterojunction is presented on a semi-logarithmic scale as a function of bias voltage and gate voltage. (f) At a temperature of 330 K, the bias current mapping plot of the heterojunction is presented on a semi-logarithmic scale as a function of bias voltage and gate voltage.

anti-ambipolar behavior. Here the band alignment between $As_{0.4}P_{0.6}$ and $PdSe_2$ has a shift with a change in gate voltage and thereby regulates the transport of electrons and holes within the heterojunction, which is crucial to the anti-ambipolar behavior.

To further understand the transport of the $PdSe_2/As_{0.4}P_{0.6}$ heterojunction device, the electrical transport was also investigated at different temperatures and different directional drain biases. Fig. 3c shows the I_{ds}–V_{ds} curves on a semilog coordinate

at low temperatures when a 2 V forward bias is applied. It can be noted from the curves that the gate voltage control of the band bending is still present at low temperatures and that the gate voltage of the device in the OFF state increases as the temperature decreases. The two OFF-state voltages of the anti-ambipolar increase from −40 V and 20 V at 300 K to −35 V and 45 V at 140 K, respectively. At temperatures below 100 K, there will be no $PdSe_2$ channel-dominated electron transport, and the current will not increase again after the gate voltage has increased to the threshold, as the thermionic emission is completely suppressed. Considering the different electrical transport behavior after complete suppression of thermionic emission,[47] the devices were warmed up to further investigate the effect of thermionic emission on the devices. As shown in Fig. 3d, when the temperature of the device rises to 330 K, it is obvious that the current change resulting from the gate voltage modulation of the band bending disappears. It is thought that as the gate voltage pulls the valence band of the $As_{0.4}P_{0.6}$ near the $PdSe_2$ conduction band, the drain current is maintained rather than falling rapidly due to the strong hot electron emission, which suppresses the ambipolar characteristics.

Fig. 3e shows mapping of the I_{ds} at 140 K for the device as functions of V_g and V_{ds}. This mapping diagram clearly illustrates that the band bending can be regulated by gate voltage at 140 K to produce two OFF-states at $V_g < -40$ V and 40 V $< V_g <$ 60 V, and can return to an open state again at higher gate voltages, making this anti-ambipolar characteristic well-suited for the fabrication of logic devices such as inverters. In Fig. 3f, I_{ds} mapping at 330 K, shows the disappearance of the second OFF-state and the reduction in the range of the first OFF-state as the device warms up, indicating that at 330 K the device is only in the OFF-state when the gate voltage is about 40 V, demonstrating flexibility in the construction of multifunctional devices.

To gain a more profound comprehension of the anti-ambipolar characteristics of the device, the study of the device at different temperatures is further investigated, as shown in Fig. 4a. At V_g = 2 V, the anti-ambipolar properties exhibit pronounced temperature dependence, notably manifested in the discernible shift of V_{peak}. At 300 K, the V_{peak} stands at −3 V. As temperature decreases, the V_{peak} experiences a slight augmentation, reaching 20 V at 80 K. Conversely, with rising temperature, the V_{peak} undergoes a declining trend, eventually

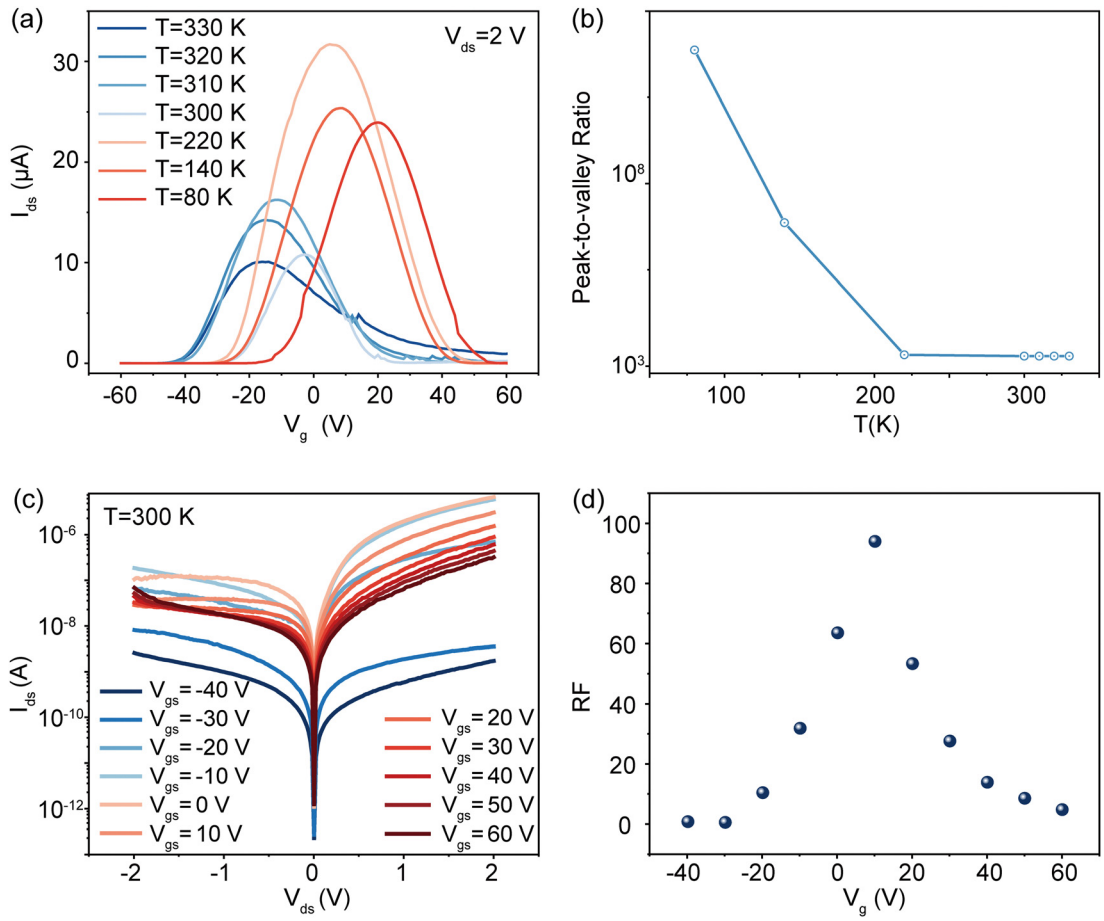

Fig. 4 Thermally tunable anti-ambipolar and gate-dependent output properties of the heterojunction device. (a) The transfer characteristic curve under a forward bias of 2 V at different temperatures (from 80 K–330 K). (b) The relationship curve between multiple forward biases and their corresponding PVR. (c) The output characteristic curve at room temperature under different gate voltage (from −40 to 60 V). (d) The corresponding rectification ratios (RF ratio = I_{2V}/I_{-2V}) under different gate voltages (from −40 to 60 V).

reaching −16 V at 330 K. This phenomenon shows potential for the construction of multifunctional logic devices. However, at temperatures exceeding 300 K, the peak current (I_{peak}) depicted in the transfer curve registers a decrease compared to the low-temperature regime. Considering the varying OFF-state currents at different temperatures, further characterization of the PVR across different temperature conditions is presented in Fig. 4b. Notably, as the temperature descends to 80 K, an exceptionally high PVR surpassing 10^8 is attained. This signifies an unprecedentedly high PVR value, emphasizing the outstanding performance of the device. Even at temperatures around 330 K, the PVR remains consistently above 10^3, reflecting the ability of the anti-ambipolar device to maintain excellent performance at higher temperatures.[21] At low temperatures, thermally excited carriers are suppressed, resulting in an extremely high PVR. As the temperature increases, thermal excitation leads to more carriers being excited from the valence band to the conduction band, increasing the carrier concentration. Consequently, more electrons and holes participate in conduction, which may increase the device's current. Additionally, the carrier mobility increases with rising temperature, further enhancing the device's conductivity. These factors may contribute to a reduction in PVR. As for V_{peak}, the increased carrier concentration and mobility at higher temperatures reduce the voltage required to reach the peak value. V_{peak} and PVR, as two critical parameters for evaluating anti-ambipolar devices, exhibit robust performance across a wide temperature range. Notably, the changes in V_{peak} and PVR with temperature are inversely related, enabling precise control of the device's V_{peak} and PVR by adjusting the temperature. This allows for flexible modulation of the anti-ambipolar behavior. These characteristics indicate that it is possible to modulate the PVR and V_{peak} *via* temperature adjustments, and thus achieve a degree of thermal tunability of the anti-ambipolar behavior, which offers new avenues for the design of multifunctional logic circuits.

When the gate voltage is −40 V, the device is in the OFF state and exhibits reverse rectification. As the gate voltage increases, the reverse rectification effect gradually decreases, as shown in Fig. 4c. At a gate voltage of −20 V, the device changes from reverse to forward rectification. When the gate voltage is at 10–20 V, gate voltage regulation of the band bending reduces the forward bias current from 10^{-6} A to 10^{-7} A. With a further increase in gate voltage, the reverse current gradually increases due to the dominance of the current generated by hot electron emission, and the device again shows a tendency toward reverse rectification. Fig. 4c shows the relationship between the corresponding rectification ratios and the gate voltage, which implements the conversion between reverse and forward rectifications.

4. Conclusions

We have successfully constructed a high-performance thermally tunable anti-ambipolar device by using an $As_{0.4}P_{0.6}/PdSe_2$ heterojunction. At room temperature, the device exhibits an anti-ambipolar characteristic with a PVR of around 8×10^3 and a V_{peak} of −3 V, exhibiting outstanding anti-ambipolar properties. Furthermore, our anti-ambipolar heterojunction device demonstrates temperature-dependent behavior, maintaining a high PVR while achieving a low V_{peak} of −20 V at high temperature. At lower temperature, an exceptionally high PVR of 10^8 is achieved, demonstrating exceptional performance. These findings underscore the outstanding performance of our device, with immense potential in applications for constructing multifunctional circuits like multi-valued logic circuits and analog circuitry.

Author contributions

Qian Liu, Xinzheng Zhang, and Cong Wang conceived and directed the study. Shengyao Chen, Jiyou Jin, and Wenxiang Wang carried out the investigations. Shengyao Chen, Jiyou Jin, Shu Wang, Xiaoshan Du, Feng Wang, Lijun Ma, and Junqi Wang discussed and optimized the parameters of the devices. Shengyao Chen, Jiyou Jin, Wenxiang Wang, Qian Liu, Xinzheng Zhang, and Cong Wang wrote the manuscript. All authors discussed the results, commented on the paper, and approved the final manuscript.

Data availability

The authors confirm that the data supporting the findings of this study are available within the article and its ESI.† Further data and information can be obtained from the corresponding authors.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

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