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Surface modifications by wet oxidation method removing getter layer in crystalline silicon cells

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Reducing the impurity atom content in crystalline silicon (c-Si) can effectively reduce the recombination current density (J_0) and improve the photoelectric conversion efficiency (PCE) of solar cells. Phosphorus diffusion gettering (PDG) has been proven to be an effective method to remove impurity atoms from c-Si. However, the research studies show that the traditional tube thermal diffusion method will cause a large number of dislocations on the silicon surface during the oxidation process, reducing the effectiveness of gettering. In this paper, the wet oxidation method is systematically used to remove phosphorus-rich layers (PRL) and modify the surface. The gettering effectiveness is measured by the minority carrier *lifetime* (τ_{eff}) and bulk carrier *lifetime* (τ_{bulk}) of silicon wafers. The results show that wet oxidation can reduce J_0 by 27.0% and increase τ_{eff} by 26.3%. For the bulk region, the average τ_{bulk} can be increased by more than 6–14%. In addition, with the final PCE comparison, the efficiency of the wet oxidation cell will be improved by 0.12%. These works indicate that the wet oxidation method can significantly improve the gettering effectiveness and the PCE of c-Si solar cell fabrication.

1. Introduction

In the context of the global energy shortage, solar energy as a renewable energy source has achieved rapid development in recent years. The International Technology Roadmap for Photovoltaics (ITRPV) predicts that the global annual market and shipments will exceed 1000 GWp in 2035 and close to 4000 GWp in 2050.[1] Such high productions correspond to the quality of silicon wafer concerns. Compared with micro-electronic silicon, the content of impurities in the bulk region of solar-grade silicon is much higher than that of the former because of the manufacturing cost. Moreover, with the use of a passivation contact structure in high-efficiency solar cells, surface recombination is low enough. However, the loss caused by the relative bulk region recombination is increasingly prominent.[2] Getter is an effective way to improve the performance of silicon wafers.[2–4] It is of great significance to reduce bulk region recombination with a gettering process. But metal impurities introduce additional recombination centers within the material band gap. With the increase of the recombination centers, the recombination current density (J_0) also increases and the lifetime of minority carriers decreases. Therefore, it is important to reduce the content of metal impurities in the silicon wafer.[5] Getter makes use of the different solid solubility of the impurities in materials,[6] to reduce the impurities and improve the performance of the silicon wafer.

The gettering process of crystalline silicon (c-Si) solar cells is generally carried out in the process of preparing the emitter. The most commonly applied getter source are phosphorus (P), boron (B) or aluminum (Al).[5–8] Compared to P and Al gettering, boron diffusion gettering (BDG) is very sensitive to the process parameters, and the former does not absent boron–oxygen defects.[8] At present, Al is rarely used as the emitter of the solar cell, the metallization process of Al as a metal electrode to form the Al–Si alloy only takes a few seconds the time is so short that the gettering effect is limited. Therefore, phosphorus diffusion gettering (PDG) is used extensively.[8–10]

PDG consists of three steps: impurities are released at high temperatures, diffused to the getter region, and captured in the getter layer. Generally, the layer of phosphorus-rich layer (PRL) is deposited on the surface of silicon as the impurity getter region.[3,11] The PRL as a getter layer is difficult to remove and is insoluble in neither water nor KOH and HF, is and called a dead layer.[12] Therefore, at the end of the PDG process, excess O_2 is used to oxidize PRL to phosphorus silicate glass (PSG). The PSG and impurities "captured" in it can be removed with the HF solution. However, the test results by K. Adamczyk *et al.* showed that the recombination activities of grain boundaries increase during PDG.[13] This is caused by the accumulation of a large number of dislocations on the surface which are caused by lattice mismatch during the oxidation of PRL to PSG.[3,14] On the one hand, the increase of dislocation recombination leads to a decrease in minority carrier lifetime.[15] On the other hand, the captured impurities are returned to the surface of the silicon wafer due to dislocation generation. We show the whole process of PDG in Fig. 1.

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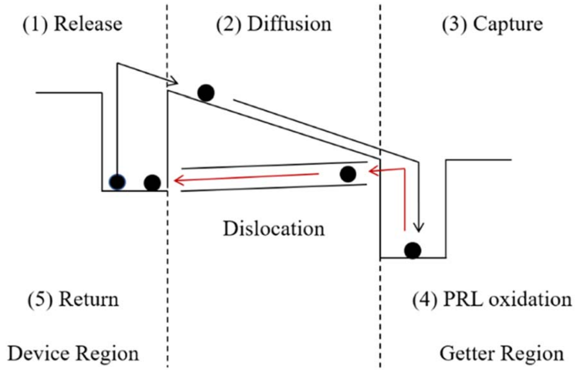


Fig. 1 Concept of the PDG process involving release, diffusion, capture, PRL oxidation, and impurities return.

Due to the difference between the thermal expansion coefficient and lattice constant, a large number of dislocations were generated on the surface during the conversion of PRL to PSG, which resulted in the PDG effect being completely negated. In this paper, we added only a small amount of O_2 at the end of the PDG process to retain a part of the PRL. In order to remove the PRL, we use a mixture solution of H_2O_2 and HF. We judge whether PRL and PSG are removed completely by the hydrophobicity of the surface,[16] and change the concentration of H_2O_2 to select the best solution ratio. The wet chemical method using the solution is a "gentle" method of removal. Lattice mismatches are released before they accumulate into dislocations.

2. Experiments and methods

Even though the most efficient silicon solar cells are N-type, the current PV market is still overwhelmingly P-type.[1] The samples used in all experiments are untreated P-type c-Si with a sheet resistance of 0.75 Ω sq^{-1}, the thickness of 170 μm, and the size of M10 (182 mm × 182 mm) from Longi Green Energy Technology Co., Ltd., Xi'an, Shanxi, China.

2.1. Thermal oxidation

Before the wet oxidation experiment, we designed the traditional thermal oxidation PDG experiment I. Experiment I is designed with the different gettering processes and a control group. We use B and P as the source of the getter.[5–8] The process in this work is outlined in Fig. 2, the first group (S1) only performs PDG, the second group (S2) with BDG and PDG, the third group (S3) only performs BDG, and the fourth group as the control group (S4) does not perform the process of gettering. In the experiment, each group has 30 pieces.

As for PDG, samples are diffused at 800 °C, and driven-in at 870 °C using the $POCl_3$ source. As for BDG, the samples are diffused at 850 °C, and driven-in at 1000 °C using the BBr_3 source. At first, treated with texturing to make the surface better in contact with the getter source. After the first gettering process, HF was used to clean the surface oxide. Then a second texturing begins. This is to remove the impurities trapped by the surface getter layer and erase the influence of the previous getter source during the second gettering process. The second texturing also be performed for S4, the thickness of all samples is consistent. The passivation structure was prepared after gettering treatment. Atomic layer deposition (ALD) and plasma-enhanced chemical vapor deposition (PECVD) were used to grow the layers of 10 nm Al_2O_3 and 80 nm SiN_x on double sides of the sample, respectively.

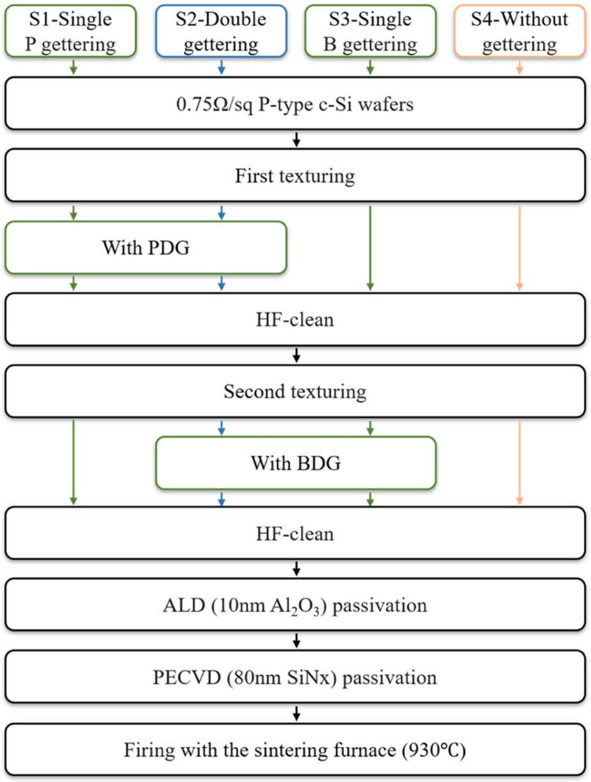


Fig. 2 The specific process of experiment I.

After firing with the sintering furnace, we measuring the performance of total samples by quasi steady-state photoconductance (QSSPC, Sinton WCT-120).[17] A sensor (a coil built into the instrument stage) is placed near the sample and sends electromagnetic waves into the silicon light (1 sun) is then pulsed onto the sample to create the excess carriers, and the coil circuit senses the increase in conductance of the sample due to the carriers. We test four corners and the central position of each piece, and the average value obtained from the test is regarded as the test result. *Lifetime*, J_0, implied open-circuit voltage (i-V_{OC}) and implied fill factor (i-FF) are listed in Table 1 of experiment I.

Table 1 Sinton test results of experiment I

	Lifetime (μs)	J_0 (fA cm^{-2})	i-V_{OC} (mV)	i-FF (%)
S1	524.0	6.4	707	83.39
S2	654.6	16.7	708	83.79
S3	464.5	15.3	704	83.21
S4	324.1	4.8	706	82.14

According to the results in Table 1, S2 with PDG and BDG is good at *lifetime*, i-V_{OC}, and i-FF and it is easy to explain that the gettering process improves the performance of the samples. But there is a difference with the result of J_0. We interpret the result as follows. According to references,[18,19] minority carrier *lifetime* of the device (τ_{eff}) depends on bulk (τ_{bulk}) and surface (τ_{surf}) recombination:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surf}}. \tag{1}$$

Combining with the data and summary results in Table 1, it is not difficult to see that getter can effectively improve the τ_{eff} and τ_{bulk} of the device, but also lead to the deterioration of surface performance. In Fig. 1, this process is shown in the gettering process the impurities in the bulk region are "enriched" to the surface. When the getter layer is removed, the impurities are not completely removed, which deteriorates the surface region. Due to the dislocation mentioned above and the impurities return, the impurities on the surface are more concentrated than before gettering. But for the whole sample, the impurities concentration is reduced. As a result, τ_{bulk} is greatly increased, in contrast, τ_{surf} is slightly reduced. According to (1), the result of τ_{eff} is still increased, which is consistent with the result of Table 1. In each gettering, the *lifetime* increase, but J_0 decrease.

As follows, the τ_{bulk} or τ_{surf}, depends on the Shockley–Read–Hall recombination (τ_{SRH}), band-to-band radiative recombination (τ_{rad}) and Auger recombination (τ_{Auger}),[19,20]

$$\frac{1}{\tau_{bulk}\ \text{or}\ \tau_{surf}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{Auger}}. \tag{2}$$

Among (2), τ_{SRH} is closely related to the content of impurities. The less the content of impurities, the smaller the SRH recombination.

2.2. Wet oxidation

In order to improve the gettering effect as much as possible, it is necessary to design a new method so that the impurities will not be returned to the wafer after being "captured". The return of impurities mainly occurs in the process of PRL oxidation to PSG. Therefore, we designed experiment II to retain a part of PRL in the PDG and use wet oxidation to "gently" remove PRL. The process of experiment II flow is outlined in Fig. 3(a). Experiment II consisted of the control group SP1 without PDG, the conventional thermal oxidation group SP2, and the wet oxidation series SP3. Because SP2 and SP3 are used different PDG recipes, to avoid the influence of doping on τ_{bulk} calculation, the sheet resistance is kept at 55–60 Ω sq^{-1}.[21,22] Each group is also set with 30 pieces.

The getter source used in experiment II is also $POCl_3$, which is decomposed into PCl_5 and P_2O_5 at a high temperature great than 600 °C. The reaction equation is:[23]

$$5POCl_3 \xrightarrow{>600^\circ C} 3PCl_5 + P_2O_5. \tag{3}$$

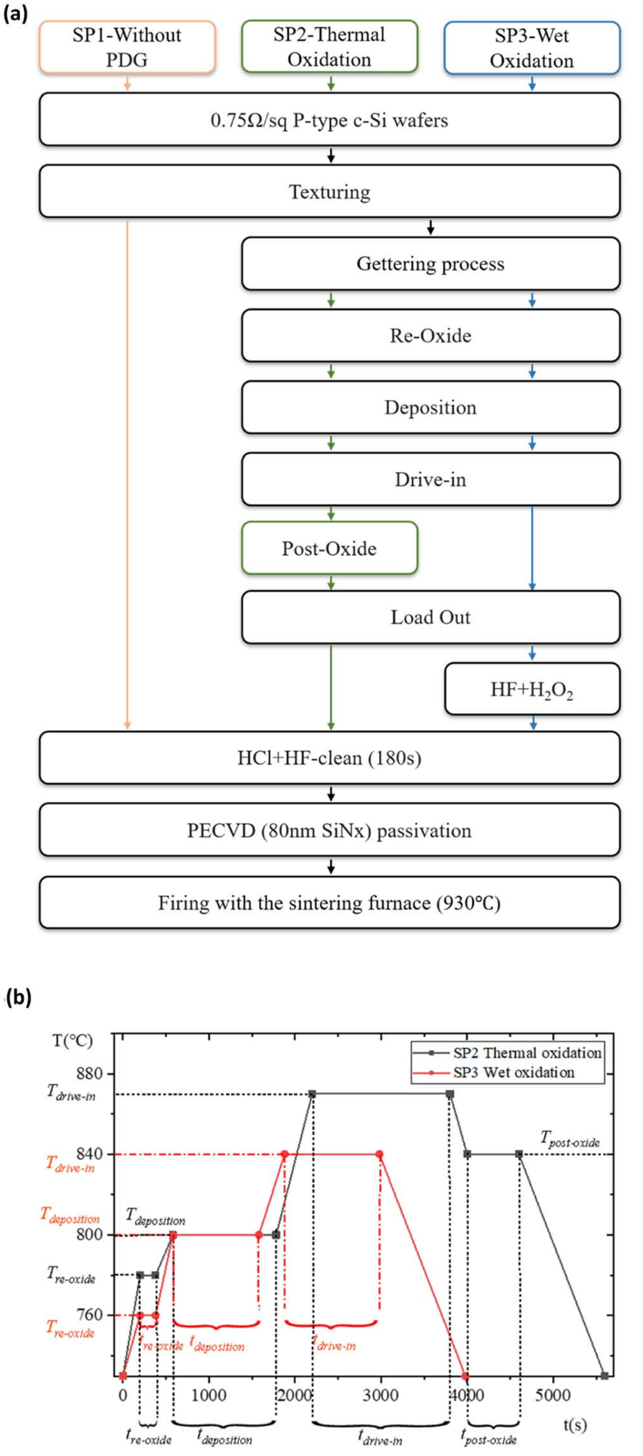

(a)
SP1-Without PDG
SP2-Thermal Oxidation
SP3-Wet Oxidation
0.75Ω/sq P-type c-Si wafers
Texturing
Gettering process
Re-Oxide
Deposition
Drive-in
Post-Oxide
Load Out
HF+H2O2
HCl+HF-clean (180s)
PECVD (80nm SiNx) passivation
Firing with the sintering furnace (930°C)
(b)
T(°C)
880
840
800
760
T drive-in
T drive-in
T deposition
T deposition
T re-oxide
T re-oxide
T post-oxide
SP2 Thermal oxidation
SP3 Wet oxidation
t re-oxide
t deposition
t drive-in
t re-oxide
t deposition
t drive-in
t post-oxide
0
1000
2000
3000
4000
5000
t(s)

Fig. 3 (a) The specific process of experiment II. (b) The doping recipes of SP2 and SP3.

Then, P_2O_5 reacts with the silicon atoms on the surface of the wafer at the diffusion temperature to form SiO_2 and P atoms:

$$2P_2O_5 + 5Si = 5SiO_2 + 4P\downarrow. \tag{4}$$

It can be seen from (3) that the $POCl_3$ is insufficient when it is thermally decomposed, resulting in the formation of PCl_5

which is not easily decomposed. Therefore, in the process of deposition, a certain amount of O_2 is generally required to promote the further decomposition of PCl_5 into P_2O_5 and the release of Cl_2. The reaction equation is:[23,24]

$$4PCl_5 + 5O_2 \xrightarrow{\text{mass } O_2} 2P_2O_5 + 10Cl_2\uparrow. \qquad (5)$$

According to (4), the generated P_2O_5 further interacts with silicon atoms and finally forms PRL. Therefore, total PRL cannot be retained. Compared with SP2, SP3 omit the post-oxide process, but certain O_2 must be fed into the deposition process to promote the complete decomposition of $POCl_3$. (4) and (5) must occur at high temperatures. Under this condition, O_2 dissociates into a single atom since the radius of the O(Si) is smaller than that of the Cl(P), the former will be more oxidizing Cl^- can be oxidized to Cl. The situation in (4) is similar. The doping recipes of SP2 and SP3 are shown in Fig. 3(b), where T and t stand for degree centigrade (°C), and second (s).

SP3 removes PRL and PSG by wet oxidation with a mixture solution of H_2O_2 and HF after the end of the diffusion process. SP3 is further divided into five different groups SP3-1, 2, 3, 4, and 5 according to the different concentrations of H_2O_2 oxidant used.[25,26] In total groups, the proportion of HF remained unchanged, accounting for 10%. The proportion of H_2O_2 in SP3-1 is 20% and increases by 5% in each group until the content of H_2O_2 in SP3-5 reaches 40%. The rest of the solution is DI water (Deionized water). Total groups were equipped with the monitor that used alkali (KOH) polishing as the source of surface characterization information. To facilitate the 3D optical microscope measure the surface morphology information. The concentration of chemical reagents HF, HCl, and KOH are all 45 wt%, H_2O_2 is 30 wt% the purity is chemical pure (CP) from Kunshan Fuller Chemical Co., Ltd., Soochow, Jiangsu, China. The proportions in this paper are all volume ratios (%).

After oxidation, total samples (including the SP1 and SP2) are cleaned for 180 s with the solution of 10% HCl and 25% HF. Cl^- can combine with metal ions to form the complex, thereby metal impurities from the wafer surface are thorough.[27–29] We test the sample by electrochemical capacitance–voltage (ECV) profiling. And test the monitor with a 3D optical microscope. PECVD is used to grow the layer of 80 nm SiN_x on double sides of the total samples as the passivation layer. After firing with the sintering furnace we measuring the performance of total samples by Sinton WCT-120 and photoluminescence (PL). The PL test should be carried out first, and other tests should be carried out to avoid the influence of sample scratches on the PL test results. PL uses a light source with the wavelength of 918 nm and a working light intensity of 1 sun in this paper.

Moreover, wet oxidation at room temperature is undoubtedly more economical than thermal oxidation at high temperature. To verify whether the wet oxidation process can be easily introduced into the production line, and improve the efficiency of wet oxidation, at the end of experiment II, we selected the group with the best performance in the SP3, and compare the PCE.

3. Results and discussion

3.1. Thermal oxidation

Lifetime (τ_{eff}), J_0, i-V_{OC}, and i-FF are shown in Fig. 4 of experiment II.

It can be seen that the surface of c-Si solar cells can be effectively modified by the method of wet oxidation. In Fig. 4(b), it can be found that, although the surface of SP2 and SP3 is still worse than that of the SP1 group without a getter, which we have explained before, parameter J_0 in 1, 2, and 3 of SP3 are smaller than SP2. Due to the surface modification by wet oxidation, the gettering effect is further improved. It shows that the *lifetime* of SP3-2 is 26.3% higher than that of SP2, about 132 μs.[19,20]

3.2. Surface region

The sample has also been subjected to the PL to test the quality of the overall region of the device. Representative PL images of each group are selected and shown in Fig. 5.

The PL images further prove that wet oxidation can significantly improve the gettering effect, but with the increase of H_2O_2 concentration, the brightness of images becomes more and more uneven it is because that wafer is etched and the reaction products are H_2O, dissolved Si (H_2SiF_6), and possibly O_2 from the decomposition of H_2O_2 (6):

$$Si + H_2O_2 + HF \rightarrow H_2SiF_6 + H_2O. \qquad (6\text{-}1)$$

$$2H_2O_2 \rightarrow 2H_2O + O_2. \qquad (6\text{-}2)$$

H_2O_2 as an unstable oxidant is very easy to decompose in the chemical reaction and will produce a large number of bubbles.[30,31] This is why we see obvious "waves" on images in groups with a high concentration of H_2O_2.

In experiment II, each group is set with the monitor. We observe the surface structure of each group with the 3D optical microscope as shown in Fig. 6.

The results show that H_2O_2 with high concentration, causes some corrosion on the wafer surface, and it is no longer smooth. In the group SP3, a certain amount of etch pits is observed. The higher the concentration of H_2O_2, the greater the density of etch pit. This is also the reason for the deterioration of the properties of the high concentration group in SP3. In Fig. 4(a) and (b), with the increase of concentration H_2O, at first, the recombination region becomes larger, next the J_0 increases, and at last, the gettering effect is canceled. This result makes the lifetime of wet oxidation worse than that of the thermal oxidation group,[32] lifetime of SP3-5 is 14.3% lower than that of SP2, about 72 μs.

3.3. Bulk region

The significance of the wet oxidation method is that it can improve the removal of impurities in the gettering process and the quality of silicon wafers. Therefore, we compare the performance of the bulk region of two getter methods by calculation. We take the minority carrier lifetime in the bulk region (τ_{bulk}) as the standard. We show the calculation method of τ_{bulk} in[33]

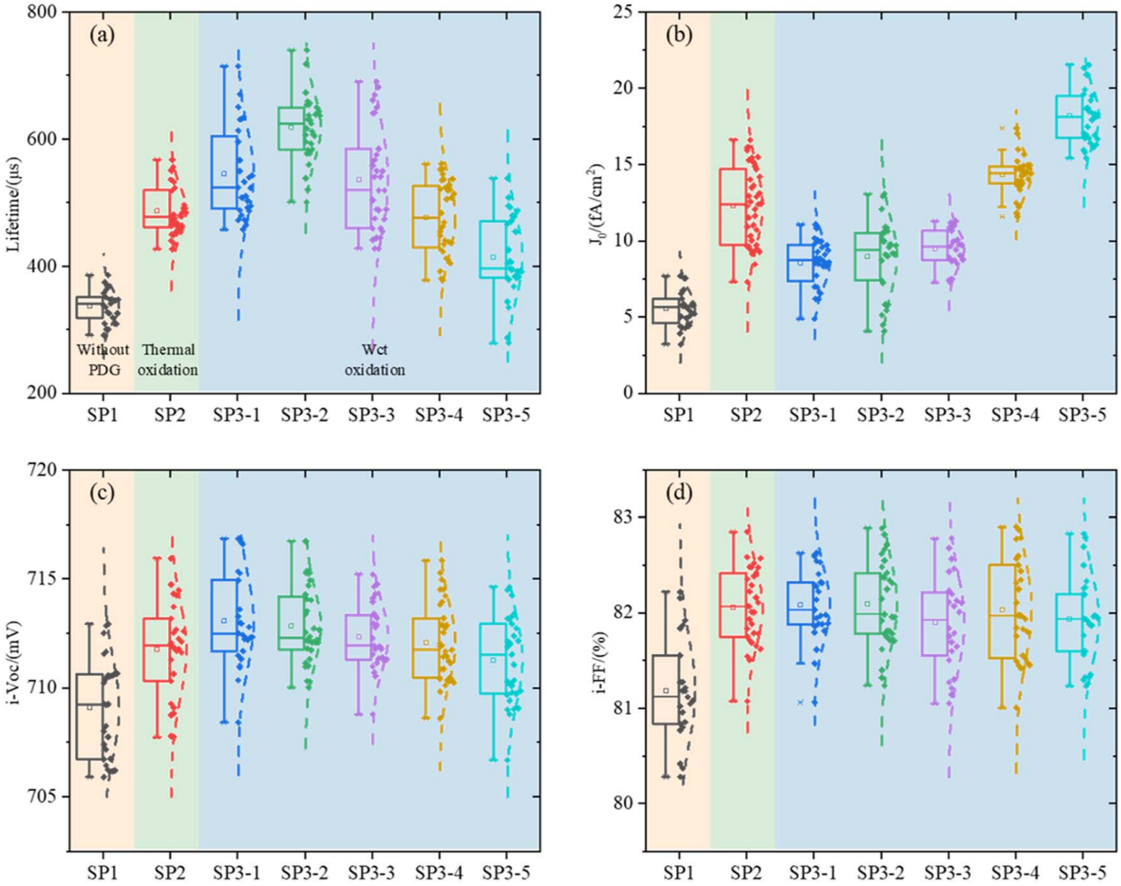


Fig. 4 Sinton test results of the experiment II, (a) lifetime (τ_{eff}), (b) J_0, (c) i-V_{OC}, (d) i-FF.

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{bulk}}} + \frac{J\left(N_{\text{dop}} + \Delta n\right)}{q{n_{\text{i}}}^2 W}. \tag{7}$$

Among (7), N_{dop} is intrinsic doping concentration, and the value is 5E15 cm^{-3}. Δn is excess carrier concentration, and the value is 1E15 cm^{-3}. q is the amount of electron charge, and the value is 1.6×10^{-19} C. n_{i} is the intrinsic carrier concentration of silicon, and the value is 8.6×10^{9} cm^{-3}. W is the thickness of the wafer, and the value is 170 μm. Here J refers to the sum of $J_{0,\text{front}}$, and $J_{0,\text{rear}}$, the sample has a symmetric structure, and the data of J_0 in Fig. 4(b) can be directly used.

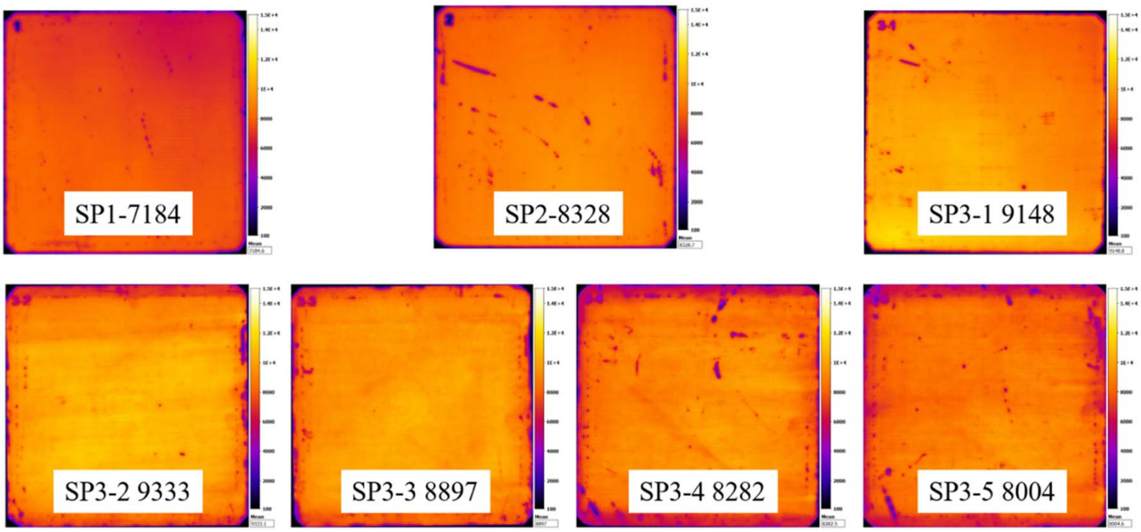


Fig. 5 PL images of each group (exposure time is 0.3 s).

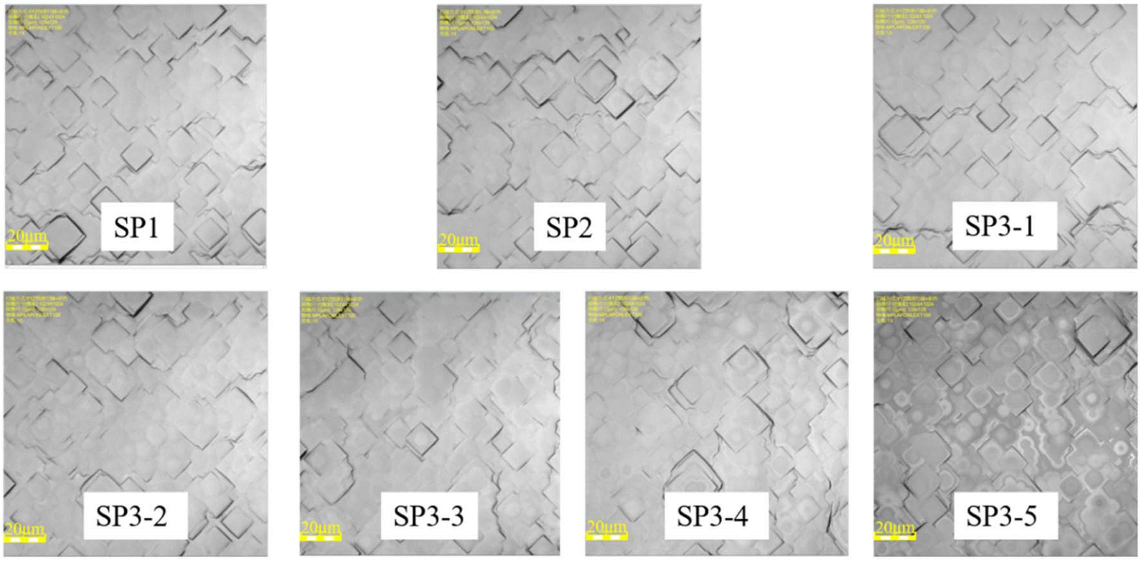


Fig. 6 Results of 3D optical microscope observation.

The dopant diffusion profiles of each group sample are by using ECV to calculate the τ_{bulk}.

In Fig. 7, there is almost no difference in the dopant diffusion profiles of each group which indicate that the influence of doping concentration can be negligible on τ_{bulk}. In Fig. 7(b), we can see that the ECV test results of total SP3 samples processed in the same tube are significantly different in the 0–10 nm. This further validates Sinton's results in Fig. 4. With the appropriate of doping concentration, i-V_{OC} increases.[34] However, H_2O_2 with high concentration etches the surface thickness 0–10 nm, and the i-V_{OC} of each group of SP3 in Fig. 4(c) show a changing trend of first increasing and then decreasing.

After that, we calculate τ_{bulk} according to (7). The data in Fig. 8 further indicates that the τ_{bulk} of SP3-4 in the wet oxidation group is 14% higher than that of SP2, about 81 μs. Combining the information in Fig. 4–8, although thermal oxidation can improve the values of τ_{eff}, the gettering effect is negated by the deterioration of the surface. Therefore, there should be a compromise between surface and bulk, and the compromise is wet oxidation. Although the surface will eventually be damaged due to the factors of principle wet oxidation with appropriate solution concentration can improve the

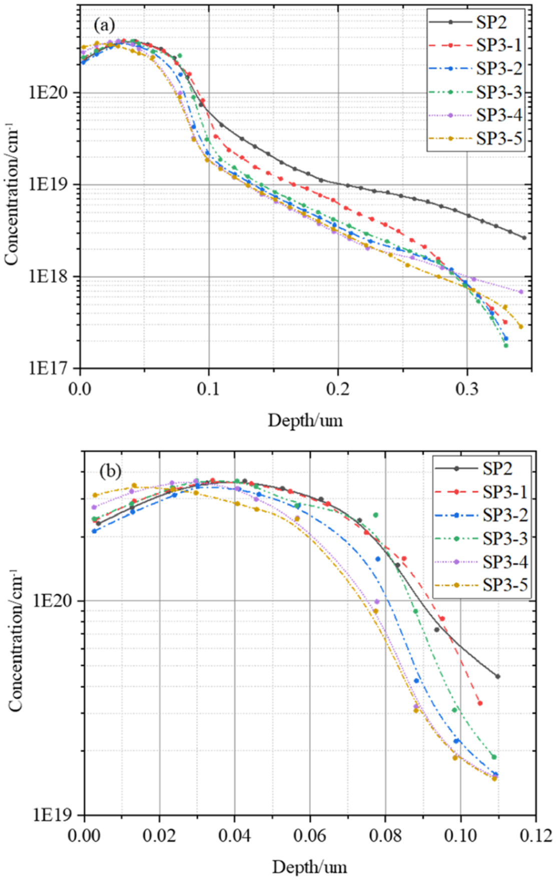


Fig. 7 The dopant diffusion profiles of each group samples, (a) 0–0.35 μm, (b) 0–100 nm.

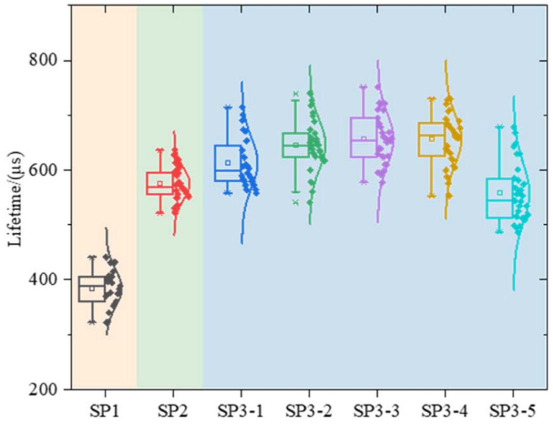


Fig. 8 The calculated result of τ_{bulk}.

performances of the bulk region thus the performances of the whole device are improved.

3.4. Cell manufacturing

In experiment II, we believe that the group SP3-2 is the champion considering the surface and bulk region. The SP3-2 recipe is introduced into the existing production line equipment then we compare the PCE for traditional oxidation.

In silicon solar cell manufacturing, the emitter is prepared by diffusion process.[17] Nevertheless, the diffusion process will cause of wrap-around, which would cause a short circuit in the final solar cell. Therefore, at the end of the diffusion process, the single sided etching process is implemented to remove the diffused rear side region. In the solar cell, it's so-called "edge isolation".

The RENA InOxSide machine and classic acidic with a mixture of HF/HNO_3 are used for the thermal oxidation group to edge isolation. The rear side is treated the same way for the wet oxidation group. Wafer only needs to go through the etch bath. And the water wheel automatically turns the equipment into the "wet oxidation bath". In the wet oxidation bath, PRL and PSG are removed, and the process is about 170 s. Then carry out HF/HCl rinse bath, and the remaining oxide is removed from the surface. The results show that compared with the traditional "thermal oxidation and etching", the wet oxidation process is introduced into the existing production line only by adding automatic turning equipment, and H_2O_2 consumption needs 86 L/10 000 pieces. However, it can be seen from Fig. 3(b) that wet oxidation can reduce 1100 s of the recipe time. At thermal oxidation, the heating power is generally 60–80 kW, and the constant temperature power is 25–30 kW for the furnace tube in industrial production. Its production capacity is generally 1000–1500 pieces per tube. In contrast, the transmission power of the inline machine in wet oxidation is only 1.5–2.5 kW, the speed is 3–4 m min^{-1}, and it usually has five tracks at least. For the processing of 10 000 M10 silicon wafers as a comparison. Thermal oxidation will consume about 65 kW h more electric energy. Moreover, the price of CP H_2O_2 used in industrial production of wet oxidation is very low, it is only about US$ 0.09 per L. Taking into account the additional use of gases such as O_2 in thermal oxidation, wet oxidation becomes more advantageous.

After the passivation layer, we screen-print the Al finger grid on the rear side as the metal electrode. The silver (Ag) finger grid is printed on the front side of an electrode. All samples are manufactured into P-PERC cells (P-type Passivated Emitter and Rear Cell). We compared the PCE of the two methods. The results are shown in Fig. 9. The test results indicate that in small batch manufacturing, the PCE of wet oxidation will increase by about 0.12%. This is further evidence that the wet oxidation method proposed enhances the gettering effect and removed more metal impurities. In the subsequent wet oxidation process, the weak oxidizing H_2O_2/HF mixture is used to oxidize and remove PRL and PSG, preserving the front side pyramid structure as much as possible.

Although wet oxidation will cause some damage to the surface. But it can be seen from the results in Fig. 6 and 7 that the damage is minimal. We test by the EL (electroluminescence, EL uses direct current, voltage is 16 V, current is 6 A), it is found damage on the edge of some samples (Fig. 10). This may be due to the failure of the water film protection. And the bubbles are caused by H_2O_2 decomposition, a part of the solution is splashed to the edge of the wafer. Because wet oxidation is applied to the front surface, the rear surface was hydrophobic. Cause the edge of the wafer is etched for H_2O_2. But, H_2O_2 oxidation is weak, even in the case that the water film cannot fully protect, it will only affect the edge region. From the results of PCE, the gain is greater than the damage. Even though wet oxidation will bring additional damage to edge etch compared to thermal oxidation with mature technology, the final result can still improve the PCE.

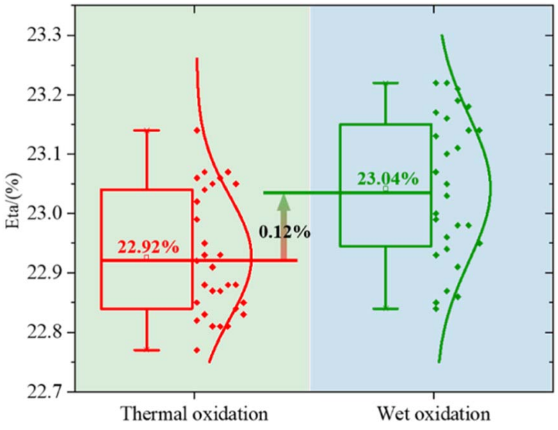
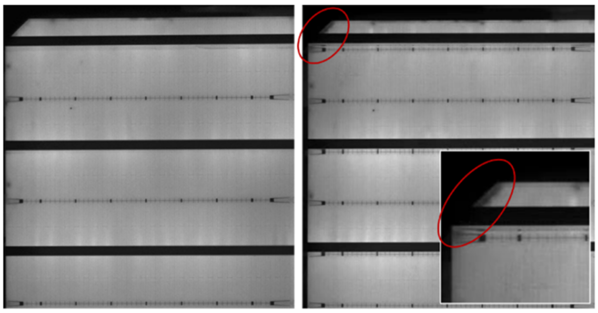


Fig. 9 The PCE results of thermal/wet oxidation.



Thermal oxidation Wet oxidation

Fig. 10 EL images of thermal/wet oxidation.

4. Conclusions

Combined the discussion in this paper, shows that the getter is very effective at removing impurities. However, oxidizing the PRL to PSG thermally will release the captured impurities back into the wafer. Hence the gettering effect is negating. We propose a new method, surface modifications by wet oxidation method removing getter layer. In the process of PRL removal by oxidation, a little of Si will always be etched, causing some damage to the surface, but provided the appropriate ratio of solution concentration is selected, more impurities can be removed and gettering effect can be improved on the premise of reducing the surface damage as much as possible. Wet oxidation of the PDG method, not only can be used as a getter means to improve the performances of wafers, through the ECV results, but it can also be integrated into the cell manufacturing process, as an n^+ emitter preparation method. Comparing the PCE of the two kinds of cells, it was found that the efficiency of the wet oxidation cell was significantly improved. These results are useful in developing suitable high-efficiency c-Si solar cells.

Conflicts of interest

There are no conflicts to declare.

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