MATERIALS CHEMISTRY
FRONTIERS

REVIEW

View Article Online
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Cite this: *Mater. Chem. Front.*, 2023, 7, 5215

Organic–inorganic hybrid perovskite materials and their application in transistors

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Received 22nd June 2023,
Accepted 19th July 2023

DOI: 10.1039/d3qm00697b

rsc.li/frontiers-materials

The emerging hybrid organic–inorganic perovskites (HOIPs) have attracted significant attention owing to their versatile and tunable structures and properties. Employing organic cations, HOIPs can integrate the advantages of both organic and inorganic components. To date, HOIPs have been widely investigated in various fields, including photovoltaics, light-emitting devices, and field-effect transistor (FETs). HOIPs possess characteristics similar to conventional inorganic semiconductors, such as high charge carrier mobility and long diffusion length. Moreover, the capacity of solution processing ensures the facile fabrication of devices. Those advantages make HOIP materials a promising candidate for semiconductors in FETs. The first HOIP-based FET was reported in 1999, which was ten years earlier than the first HOIP-based solar cell. However, currently, reports on perovskite FETs are relatively rare, possibly due to the environment-dependent apparent mobilities, instability, and hysteresis caused by the intrinsic properties of perovskites. In this review, we aim to summarize the strategies developed by the pioneering works to improve the performances of HOIP-based FETs. We begin by providing a brief introduction to structure, properties, and versatile fabrication methods. Afterward, reports on HOIP-based FETs are reviewed. FETs were divided into ambipolar, p-type, n-type, and functional portions, and the potential applications of HOIPs in FETs are highlighted, which aim at being instructive for future investigations.

1. Introduction

Perovskites describe any crystal sharing the analogous structure of the mineral $CaTiO_3$. The name "perovskite" is derived from the name of Russian mineralogist Count Lev Alekseyevich von Perovski. Natural perovskites discovered in the early years adopt the formula ABO_3 in which divalent and tetravalent cations occupy the A and B sites, respectively. Subsequently, people synthesized halide perovskites employing monovalent halide anions (X^-) to replace O^{2-}. Consequently, the valence numbers of A and B cations should be halved to satisfy the charge balance. In the crystal structures of perovskites, the B-site cation and adjacent anions form BO_6 (or BX_6) octahedra. The corner-sharing octahedra form the backbone of the perovskite, while A-site cations occupy the 12-fold coordination


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vacancy between the octahedra. The ideal perovskites adopt a cubic phase in which all the B–O–B (or B–X–B) angles are strict 180°. However, octahedra usually distort, leading to the low-symmetry tetragonal and orthorhombic phases.

In conventional inorganic oxide or halide perovskites, A, B, and X are all inorganic ions. In 1978, Weber first synthesized hybrid organic–inorganic perovskites (HOIPs) by introducing organic cations into halide perovskites.[1] Nowadays, not only A-site cations but also X-site anions can be replaced by organic components. Hybrid metal halide, formate, azide, cyanide, dicyanometallate, and borohydride perovskites can be obtained by employing different types of organic ions.[2]

HOIPs successfully integrate the excellent optoelectrical properties of the inorganic component and solution-processability of the organic component. They exhibit outstanding optical and electrical properties, including high and wide light absorption intensity and band, suitable bandgap, and high as well as balanced hole and electron diffusion lengths and mobilities.[3,4] Moreover, the facile fabrication process is superior to conventional materials. Notably, various substrates can be used to deposit perovskite films, which provide a versatile platform for their application. For instance, by fabricating HOIPs onto flexible substrates, flexible electronics have been successfully demonstrated.[5,6] Due to the above-mentioned abundant merits, the emerging HOIPs have received increasing attention as promising candidates for multiple devices, such as solar cells,[7–9] photodetectors,[10,11] light-emitting diodes,[12] semiconductor lasers,[13] memory devices,[14–16] thermoelectrics,[17] and field-effect transistors.[18]

Among them, photovoltaics is undoubtedly the most intensively investigated field. Solar cells employing halide perovskites as light-absorbing materials have attracted significant attention since Kojima *et al.* reported the first hybrid perovskite solar cell in 2009.[7] To date, the power conversion efficiency has been elevated significantly by the initial 3.8% in 2009 to 25.8% (certified 25.5%) in 2021.[7,19]

Beyond solar cells, the field-effect transistor (FET) is a three-terminal electronic used to modulate the current by an applied electric field. A typical FET generally contains a gate electrode, gate dielectric layer, semiconducting channel layer, and source/drain electrodes. Traditional inorganic semiconductors such as metal oxide, organic semiconductors such as pentacene and poly(3-hexylthiophene-2,5-diyl) (P3HT), and all-inorganic perovskites-based FETs have been abundantly investigated.[20,21] Hybrid organic–inorganic perovskites are also promising candidates for semiconductors in FETs due to their high mobility, facile fabrication process, tunable properties, and other unique advances.[18,22]

This review mainly focuses on HOIPs applied in various FETs. The structures, properties, and fabrication methods of HOIPs are summarized, and previous reports focusing on HOIPs-based field-effect transistors are reviewed. We divided perovskite-based FETs into ambipolar, p-type, n-type, and functional transistors. Finally, the prospects of future development are reviewed.

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2. Structure and properties of hybrid organic–inorganic hybrid perovskites (HOIPs)

Conventional perovskites refer to any structure adopting a structural framework similar to $CaTiO_3$. The structure is also called "3D perovskites" because of their isotropic in three dimensions. Interestingly, the 3D structure can transform into low-dimensional counterparts by adding bulk cations. The structures and properties of 3D and low-dimensional HOIPs are discussed in this section.

2.1. 3D HOIPs

Typically, halide perovskites adopt the ABX_3 formula, in which A represents the monovalent cation for inorganic perovskites and the organic cation for hybrid perovskites. For hybrid perovskites, A-site cations are always organic ammonium ions, *i.e.*, RNH_3^+. The A-site cation occupies an interval between the corner-sharing BX_6 octahedra in the perovskite crystal structure. Fig. 1a exhibits a typical perovskite structure, in which yellow, blue, and red spheres represent A-site, B-site, and X-site ions, respectively.

To form the framework of 3D perovskite, the essential geometric constraints should be satisfied. The Goldschmidt tolerance factor t and octahedral factor μ were inferred by treating all ions as rigid spheres. The two fundamental parameters can be determined by eqn (1) and (2).

$$t = \frac{R_A + R_X}{\sqrt{2}(R_B + R_X)} \tag{1}$$

$$\mu = \frac{R_B}{R_X} \tag{2}$$

here, R_A, R_B, and R_X are the effective radii of A, B, and X ions, respectively.[26] Normally, $0.80 \leq t \leq 1.0$ and $0.44 \leq \mu \leq 0.90$ should be satisfied in most perovskites. This is called the "phase stability".[27] Specifically, when t is between 0.90 and 1.0, the ideal cubic phase (α-phase) structure can be obtained.[23] If the ionic radius R_A is too large (*e.g.*, $CH_3CH_2NH_3PbI_3$, $t = 1.03$, calculated by effective radii reported in ref. 23) or too small (*e.g.*, NH_4PbI_3, $t = 0.763$), the crystal structure would distort, and geometrically stable perovskite structure cannot form.[28]

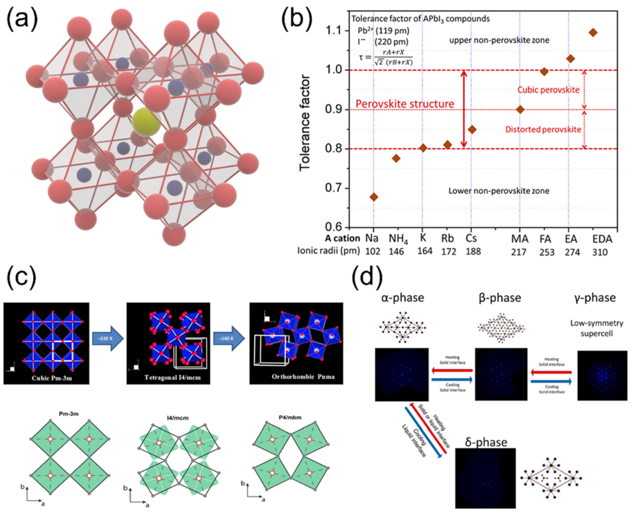

Fig. 1 (a) Crystal structure of perovskites. Yellow, blue, and red spheres represent A-site, B-site, and X-site ions, respectively. (b) Calculated tolerance factors for different cations in the lead iodide perovskite system. Reproduced with permission.[23] Copyright © 2019, American Chemical Society. (c) The relative rotations of neighboring layers of octahedra along the *c*-axis. A-site cations are not shown. Reproduced with permission.[24] Copyright © 2016, P. S. Whitfield *et al.* (d) Schematic illustrations of phase transitions in hybrid perovskites. Reproduced with permission.[25] Copyright © 2013, American Chemical Society.

Instead, nonperovskite structures (in which the octahedra are not corner-sharing), such as post-perovskites, are obtained.[29] Nevertheless, in some systems, no stable perovskite structures can form even though t meets the requirements, indicating that other requirements should be satisfied simultaneously. The octahedral factor μ is also a vital parameter. If μ is less than 0.44, the BX_6 octahedron unit could not be stable. Therefore, the perovskite structure was not realizable.[30] In 2019, Bartel *et al.* presented a now tolerance factor, τ. This modified tolerance factor exhibited an overall prediction accuracy of 92% for more than 1000 kinds of perovskites, including various double perovskites ($A_2BB'X_6$).[31] For 3D metal halide perovskites, the group XIV Sn and Pb are the most likely B-site metal since no transition metal is expected to adopt the metal halide perovskite structure due to the large radii of halides.[32] The rare pair of B-site metal and X-site halogen ions strictly restricts the selection of A-site organic cations. Generally, only MA^+ (methylammonium, $CH_3NH_3^+$, t = 0.912 for $MAPbI_3$) and FA^+ (formamidinium, $CH(NH_2)_2^+$, t = 0.987 for $FAPbI_3$) can satisfy the tolerance factors. The tolerance factors of different cations in lead iodide perovskite are summarized and plotted in Fig. 1b.

Phase (transition). Perovskites can adopt different phases, including cubic phase (α-phase, $Pm\bar{3}m$ space group), tetragonal phase (β-phase, $I4/mcm$ space group), and orthorhombic phase (γ-phase, $Pnma$ space group). Phase transition phenomenon is the nature of perovskite materials (Fig. 1c and d).[24,25] As the temperature rises, the perovskite can undergo 2 phase transition processes to elevate the symmetry from the initial γ-phase to β-phase and finally reach α-phase. For HOIPs, these two processes occur at 160 K and 330 K, respectively.[33] The structural phase transition can significantly alter the perovskites' electronic and optical properties.[34]

Different types of HOIPs have versatile properties, including semiconductivity, light-emitting properties, dielectricity, ferroelectricity, and mechanical properties due to their structural diversity. Moreover, these properties can be fine-tuned by changing the organic and inorganic components in the perovskite structure. For metal halide perovskite semiconductors, which are principally discussed in this review, the tunable band gaps, long charge carrier lifetime, and high light-absorption efficiency are the critical advantages of FETs.

Although 3D HOIPs exhibit versatile advances, they also have their disadvantages. The instability of the material is one of the biggest issues hindering their application. Unfortunately, HOIPs are sensitive to moisture, oxygen, light, and heat, respectively. For Pb-containing 3D HOIPs, lead can leak out of perovskites, especially in the presence of water, which threatens water quality and human health.[35,36] For instance, $MAPbI_3$ can degrade into MAI and PbI_2 under moisture. Notably, the preparation of the perovskite utilizes another direction of this reversible reaction. Limiting lead leakage mainly in solar cells has been an emerging topic these past years. Strategies containing encapsulating solar cells and absorbing or recycling Pb^{2+} have been investigated to deal with the tough issue.[37] Encapsulating the device is the most direct approach to limiting lead leakage. Although the encapsulation of solar cells has been widely investigated, it still requires progress to meet the practical demands. For instance, to address the issue of possible damages in outside environments, Jiang *et al.* employed epoxy resin-based polymers as the encapsulation material, which could heal while heating.[38] By adding Pb^{2+} adsorbents into the device structure, the released toxic ions out of the cell can be effectively reduced. Adsorbents such as polymers, small organic molecules, and metal–organic frameworks can be placed either at both sides of the cell or around the cell since Pb^{2+} can leak out in every direction.[39,40] Adsorbents could also be used to encapsulate the cells and was able to capture 99.9% of leaked Pb^{2+} without harming the performance.[41] To minimize the disposal of the toxic heavy metal as well as reduce the overall cost, solar cells at their end of life are worth-recycling. Versatile approaches have been developed to recycle the device components (mainly PbI_2) or make the device easier to recycle, *e.g.*, polar solvent extraction, employing additives, and solvent engineering.[42–44] These strategies are promising to overcome the critical toxic metal leakage barrier and can be useful guidelines for HOIPs-based FETs. There is another solution to radically overcome this issue, which is applying lead-free HOIPs. These perovskites can adopt low-dimensional structure, such as $(PEA)_2SnI_4$.

2.2. Low-dimensional HOIPs

When the size of the A-site cation is too large for the space between the BX_6 octahedra, the octahedra network will be destructed; thus, nonperovskite structures such as low-dimensional layered perovskite will form instead.[45,46]

Low-dimensional HOIPs can be hypothesized as the product of the intercalation of organic layers or the cutting from the bulky ABX_3 "parent".[47] Based on the different "cutting" orientations, low-dimensional HOIPs can have different directions such as ⟨100⟩, ⟨110⟩, and ⟨111⟩. In this review, all the mentioned 2D HOIPs belong to the ⟨100⟩ orientation. Low-dimensional HOIPs can be divided into 2D and quasi-2D segments based on the layer thickness. A 2D perovskite only contains a single octahedra layer, while the quasi-2D counterpart comprises more than one layer of octahedra. Two main phases describing low-dimensional perovskites are the Ruddlesden–Popper (RP) and Dion–Jacobson (DJ) phases, which have the chemical formula $L_2A_{n-1}B_nX_{3n+1}$ and $L'A_{n-1}B_nX_{3n+1}$, respectively. For RP phase perovskites, L represents the bulky monovalent RNH_3^+ cation, *e.g.*, the aliphatic butylammonium ($C_4H_9NH_3^+$, BA) or Phenethylammonium ($C_6H_5CH_2CH_2NH_3^+$, PEA). A, B, and X represent small monovalent cations, divalent metal cations, and halide anions, respectively, analogous with conventional 3D HOIPs. However, the DJ phase employs divalent bulky cations instead, mainly $[NH_3\text{-R-}NH_3]^{2+}$, in which R can also be aliphatic or aromatic. Both the RP phase and DJ phase adopt a sandwich-like geometry as the inorganic component is clamped by adjacent organic layers constituted by L ligands. The integer n represents the number of metal-halide octahedron layers between the bulky L layers. When $n = \infty$, the 3D ABX_3 structure is formed; when $n = 1$, the L_2BX_4 monolayer structure is considered to be two-dimensional; when $1 < n < \infty$, the "transition phase" quasi-2D structures are obtained. The structures of low-dimensional perovskites are schematically illustrated in Fig. 2a and b.[48]

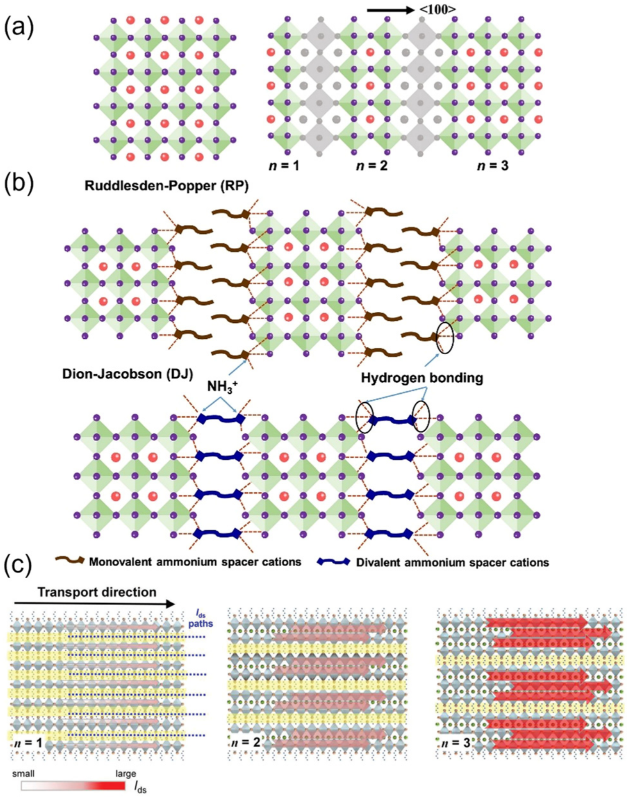

Fig. 2 (a) Crystal structure of a 3D perovskite and schematic of cutting the 3D perovskite from the ⟨100⟩ plane to form the layered perovskites. (b) Crystal structures of RP and DJ phase low-dimensional perovskites ($n = 3$). Reproduced with permission.[48] Copyright © 2022, American Chemical Society. (c) Schematic illustration of the transport behavior of the $BA_2MA_{n-1}Pb_nI_{3n+1}$ perovskite crystal for $n = 1$ to $n = 3$. Red arrows and their corresponding shading indicate the direction of current flow and intensity in the conduction channel, respectively. Reproduced with permission.[49] Copyright © 2018, John Wiley & Sons.

Generally, in low-dimensional HOIPs, bulky organic cations are spacers between metal halide octahedra layers. By varying n, the thickness of the inorganic sheet can be modified. Thus, their optical and electronic properties can be fine-tuned. Typically, the bandgap and exciton binding energy are reduced when n increases.[50]

The alternative organic and inorganic layers form the quantum well (QW) structure, where inorganic and organic layers act as wells and barriers, respectively; thus, unique properties can exhibit.[51] For instance, photoluminescence can be enhanced by the suppression of forbidden electronic transition due to their decreased structural symmetry, which makes them suitable for application in light-emission devices.[52,53] The significant difference in the dielectric constants (κ) of adjacent organic and inorganic layers brings relatively high exciton binding energies (up to hundreds of meV, while only 45 meV for $MAPbI_3$). This phenomenon is named the dielectric confinement effect in low dimensional systems and was demonstrated to have a critical influence on exciton binding energies.[54,55]

However, the instability of 3D hybrid perovskites under moisture, oxygen, electron fields, or light illumination has been a challenging issue that researchers must face to commercialize products containing 3D HOIPs.[56] Fortunately, the chemical stability of low-dimensional HOIPs is found to be superior to their 3D counterparts. Some researchers suggest that the unstable organic cations lead to the instability of hybrid perovskites. However, for low-dimensional HOIPs, the organic A-site cations are well-protected by highly hydrophobic layers constituted by L.[57] Nevertheless, other than the mainly Pb-based 3D HOIPs, most low-dimensional perovskites are Sn-based, and the easy oxidation from Sn^{2+} to Sn^{4+} leads to additional air instability to perovskites.

2.2.1. 2D HOIPs.

2D HOIPs adopt ultrathin perovskites containing BX_6 octahedra monolayer between bulky organic ligand layers. The interlayer forces between adjacent organic layers (mainly the van der Waals interaction) are much weaker than forces of bonds between organic ligands and inorganic BX_6 octahedra counterparts (ionic and hydrogen bonding), which makes it likely to separate and form homogeneous and smooth surfaces.[58]

2D HOIPs have individual electron, optical, magnetic, and mechanical properties because of their low dimensional nature.[59] For instance, the dielectric confinement, optical nonlinearity, and anisotropic charge transport can be observed from functional 2D HOIPs.[60] Excitons in 2D HOIPs are considered as ideal 2D confinement, which has strong confinement in one dimension and free carrier transport in the other two dimensions.[60] However, the relatively low mobility and large bandgap are the disadvantages of pure 2D HOIPs compared to 3D, which hinder their applications in electronics. Applying quasi-2D HOIPs may be a promising strategy to overcome the bottleneck.

2.2.2. Quasi-2D HOIPs. Quasi-2D HOIPs adopt the structure within the two extremes of 2D and 3D. In quasi-2D HOIPs, the large and small organic ligands (act as spacers and "perovskitizers", respectively) simultaneously exist.[61]

Quasi-2D HOIPs combine the high optical and electrical properties of 3D perovskites and the improved stability of 2D counterparts. The carrier mobility of quasi-2D HOIPs is superior to 2D counterparts because of the higher ratio of the inorganic backbone (Fig. 2c).[49] At the same time, the presence of a hydrophobic organic spacer can prevent the inner parts from harmful moisture, which significantly inhibits spontaneous perovskite degradation.

Although quasi-2D HOIPs provide extra tunability between mobility and stability, the enhanced complexity inevitably increases the difficulty of their preparation, purification, and modification. Specifically, it is not easy to obtain quasi-2D HOIPs pure crystals when n is higher than 5.

2.3. Carrier transport in HOIPs

It has been proved that the organolead trihalide perovskites ($APbI_3$, A represents organic monovalent cations) are direct bandgap semiconductors.[62] Theoretical investigations revealed that the cubic phase $MAPbI_3$ has a bandgap of $\sim$1.7 eV, which consists of its experimental optical bandgap ($\sim$1.6 eV).[63] Their outstanding semiconductivity is fundamental for applications in both field-effect transistors and solar cells.

We can understand the charge carrier mobility of HOIPs by the Drude model. In Drude's picture, mobility is found to be

$$\mu = \frac{e\tau}{m^*} \tag{3}$$

where m^* is the carrier effective mass and τ is the temperature-dependent scattering lifetime. Taking $MAPbI_3$ for instance, the effective masses of electrons and holes are both between 0.1 and $0.15m_0$ (m_0 is the free electron mass) and are approximate to those for the inorganic high-performance semiconductor such as GaAs, indicating excellent carrier transport abilities for both electrons and holes in HOIPs, *i.e.*, the balanced ambipolar transport characteristic.[2,64] Moreover, *ab initio* calculations demonstrated that not only small effective masses but also weak electron–phonon and hole–phonon couplings in 3D HOIPs benefit from their high mobilities.[65] In general, it can be concluded that HOIPs' behavior is more like the traditional inorganic semiconductor due to their inorganic ion-dominated band structure.[66] In this case, the intrinsic mobility of HOIPs should be comparable to their inorganic counterparts ($>10^3$ cm^2 V^{-1} s^{-1}).

We can also understand charge transport in HOIPs according to their structures. In organic–inorganic hybrid perovskites, the inorganic component forms a strict network through covalent and ionic interactions.[18] Charge carriers flow mainly *via* the inorganic backbone, which agrees with the above conclusion. In this model, organic cations hardly participate in the charge transport process. However, the function of organic cations in HOIPs is still under debate. Many researchers believe that the organic component only has a structural space-filling effect and does not significantly contribute to electronic structure near the Fermi level because of the weak contributions of orbitals of atoms in organic cations. Nevertheless, some investigations in the past few years suggested that the orientation of the organic cation may deform the perovskite structure and thus have the potential for changing the band structure.[67,68]

Hysteresis. The hysteresis phenomenon can be observed in various HOIPs-based electronics, including solar cells as well as FETs.[69,70] Specifically, in the *J–V* curves of solar cells, the forward and reverse curves always cannot match. For FETs, the transfer curves of the two scanning directions sometimes differ from each other, as shown in Fig. 3a and b. Thus, the hysteresis phenomenon should be attributed to some intrinsic properties of perovskites. Three mechanisms were proposed to explain the hysteresis, which were the polarization effect, charge-trapping effect, and ion migration.[69]

Ferroelectric behavior was found in some HOIPs. Under bias, hybrid perovskites are found to be slowly polarized, which can alter their electrical behavior (Fig. 3c and d).[72] There are high concentrations of defects in perovskites, such as ion vacancies and intervals. The defects on interfaces can act as carrier traps. Good contact between electrodes and perovskites can be achieved once the traps are filled to observe superior device performances. The slow filling and emptying of traps caused the hysteresis. The ion migration describes ion drift under bias, and this process is associated with defects (Fig. 3e and f). For instance, an iodide anion can transfer to an iodide vacancy and remain in another iodide vacancy at its initial location. The activation energies of migration of I^-, MA^+, and Pb^{2+} in $MAPbI_3$ were calculated to be 0.58, 0.84, and 2.31 eV, respectively, indicating that iodide anions are the dominating species migrating in $MAPbI_3$.[73] Consequently, iodide vacancies (V_I) should be mainly focused to inhibit ion migration in $MAPbI_3$. Ion migration was thought to be the dominant factor of hysteresis.[73] For FETs, the ionic transport also causes the screening effect. The serious screening effect can result in the inhibition of the actual gate voltage applied on the semiconductor, which significantly reduces the measured mobility. Consequently, mobilities far lower than the theoretical value or even no mobility can be observed in HOIPs-based FETs.[70] Moreover, the ion migration can also cause gate pulse-dependent mobility. In the previous work carried out by Docampo...

As mentioned above, ion migration is the main barrier to obtaining high-performance perovskite transistors. Moreover, the accumulation of defects that remain by ion migration can also lead to perovskite degradation. To reduce the influence of the ion migration phenomenon, some researchers tested the device properties at low temperatures (approximately 77 K). Labram *et al.* investigated the temperature-independent electrical characteristics of $MAPbI_3$ thin film FETs. The device showed no field-effect feature at room temperature, but once the temperature decreased below 220 K, the gate voltage-modulated drain current was observed. In addition, higher mobility was achieved at lower temperatures. The temperature-independent phenomena resulted from the drifting ionic species and polarization under

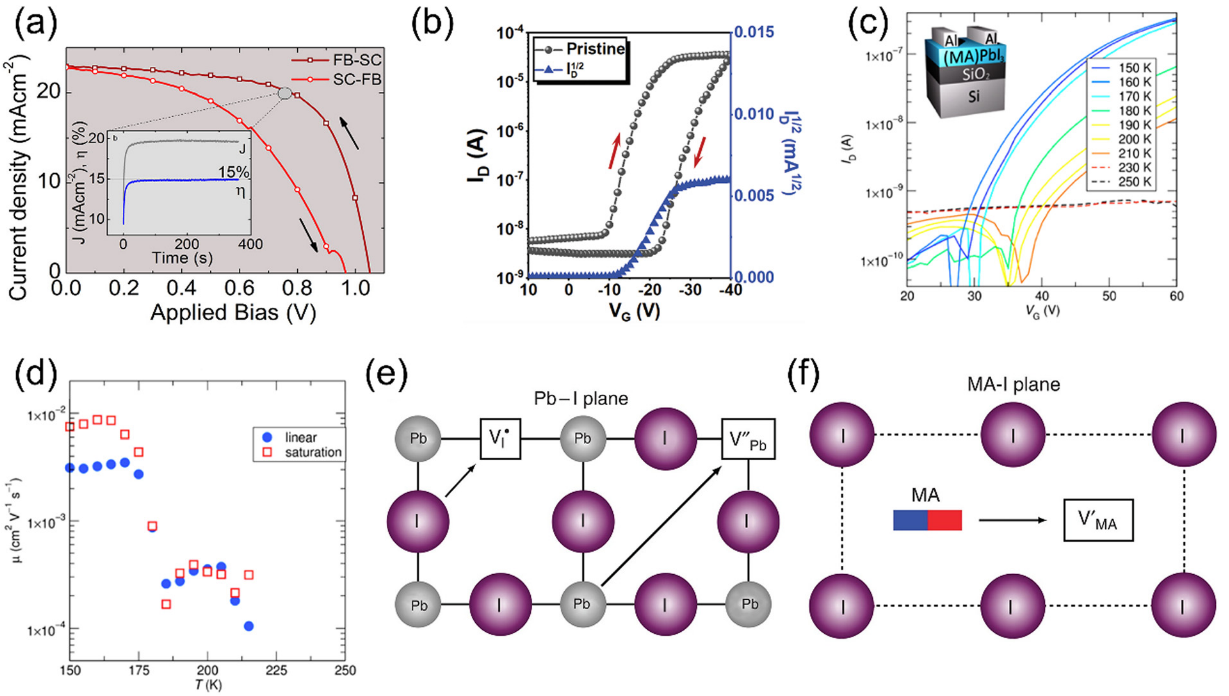

Fig. 3 (a) and (b) Hysteresis phenomenon in different perovskite-based electronics. (a) *J–V* curves of a solar cell. Reproduced with permission.[69] Copyright © 2014, American Chemical Society. (b) Transfer curves of a field-effect transistor. Reproduced with permission. Copyright © 2023, Wiley-VCH.[71] (c) and (d) Polarization-induced hysteresis in field-effect transistors. (c) Transfer curves of $MAPbI_3$ FET measured at various temperatures between 150 and 250 K. (d) Field-effect mobility as a function of the temperature. Reproduced with permission.[72] Copyright © 2015, American Chemical Society. (e) and (f) Schematic illustrations of ionic transport mechanisms in the $MAPbI_3$ perovskite, including (e) the transport of I^- and Pb^{2+} and (f) transport of MA^+. Reproduced with permission.[73] Copyright © 2015, American Chemical Society.

gate bias. Also, both of them could be activated by high temperatures.[72] Moreover, the carrier diffusion length in the $MAPbI_3$ single crystal was proved to be larger under low temperatures, partly because of the reduced optical phonon scattering.[75] Another strategy against ion migration and polarization is applying low-dimensional perovskites due to their quantum and dielectric confinement effects and the less mobile nature of the contained species.[72,76,77] For instance, Sn-based 2D or quasi-2D perovskites are promising for low hysteresis devices because of the high activation energy of the dominating Sn^{2+} vacancies.[78] Other parameters, such as the ratio of precursors, have already been demonstrated to inhibit ion migration.[79] However, finding a universal strategy to overcome this issue is still challenging.

3. Fabrication methods of HOIPs

This section summarizes versatile fabrication methods for fabricating HOIP films. Facile solution-process ability is one of the advantages of perovskites, whereas most of the published works used this fabrication strategy. However, vapor deposition and other new-type methods have also been applied to obtain high-quality or functional perovskite films. Notably, not all methods mentioned in this section are used to fabricate HOIPs-based FETs. Some strategies developed to process other types of electronics, such as solar cells, are also illustrated because of similar acquirements to obtain high-performance devices, such as the large grain size and smooth surface.

3.1. Preparation of polycrystalline perovskite films

The self-organization ability of organic–inorganic perovskites gives the capacity of the facile solution fabrication process of preparing polycrystalline films. To date, most of the reported HOIPs-based electronics have utilized solution-fabricated films.

Spin-coating. Among all methods, one-step spin-coating (also called spun-coating) is the simplest and most widely used way to prepare the hybrid perovskite film.[80] Literally, most of the reported works adopted spin-coated perovskite films, including the first HOIP-based field-effect transistor and solar cell.[7,18] In the spin-coating process, precursors (*e.g.*, MAI and PbI_2 for $MAPbI_3$) are dissolved in a polar solvent (DMF, DMSO, *etc.*). The solution is subsequently dropped on a fast-spinning plate. Due to the centrifugal force, the solution tends to move outward of the plate and finally overspreads the plate. Self-organization and crystallization occur during the volatilization of the solvent. Moreover, the thickness of the as-fabricated films can be controlled by varying the rotation speed. Typically, polycrystalline perovskite films with relatively small grain sizes are formed through this process. However, spin-coating is a wasteful method because most of the precursor solution is inevitably spread out of the plate during the process.

Vapor-assisted solution process. A vapor-assisted solution process was a type of *in situ* synthesis of perovskite films. Generally, polycrystalline perovskite films are formed while solution-deposited inorganic films (*e.g.*, PbI_2) contact with the organic vapor (*e.g.*, MAI). This method was first demonstrated by Yang's group to fabricate perovskite films with controllable film quality in solar cells.[81] Wu *et al.* applied this approach to fabricate field-effect transistors. The as-fabricated $MAPbI_3$ film showed full surface coverage, uniform grain structure with large grain size, and excellent field-effect performance.[82] A high hole mobility of 21.41 $cm^2\ V^{-1}\ s^{-1}$ was then achieved by Li *et al.* using this method.[83]

Chemical vapor deposition. Vapor deposition, including chemical vapor deposition (CVD) and physical vapor deposition (PVD), is a technique of depositing the vaporized source material onto a substrate in a high vacuum tube. Highly oriented products can be formed under appropriate deposition conditions such as substrate, temperature, and vapor flow speed. The advantages of the one-step fabrication of highly orientated films and nontoxicity make solvent vapor deposition a powerful method for preparing high-quality perovskite films.

Chemical reactions occur during the CVD process to form perovskites. Due to the controlled growing process of perovskites, the single crystalline film can be observed using CVD. Wang *et al.* prepared an ultrathin $MAPbCl_3$ single crystal with 10 nm thickness and centimeter size *via* CVD, where MACl and $PbCl_2$ sources were in the tube simultaneously, as shown in Fig. 4a.[84]

Dual-source vapor deposition is an emerging progress of CVD. In dual-source vapor deposition, two kinds of precursors are evaporated, respectively. By the control of sensors, vapor could meet and form the perovskite on the substrate (Fig. 4b). It is obvious that films prepared by dual-source vapor deposition exhibited a much more uniform morphology than the solution-processed films, as shown in Fig. 4c and d. This method is found to be very appropriate for fabricating multilayer structures.[85] For instance, Matsushima *et al.* applied PEAI and SnI_2 as organic and inorganic sources, respectively, and a 31-nm-thick $(PEA)_2SnI_4$ film was obtained to fabricate a field-effect transistor. Also, they demonstrated that substrate heating while depositing is significant for film quality.[86]

Niu *et al.* fabricated near-two-dimensional perovskite solids on different substrates by applying a two-step method. Firstly, the highly crystalline PbI_2 nanoplatelets were obtained using physical vapor deposition. The PbI_2 nanoplatelets could further convert to perovskites using a CVD system where MAI was applied as the source.[87] In conclusion, the (dual source) vapor deposition is a promising method to process uniform perovskite thin films, but the crystallization mechanism is still under debate.[80]

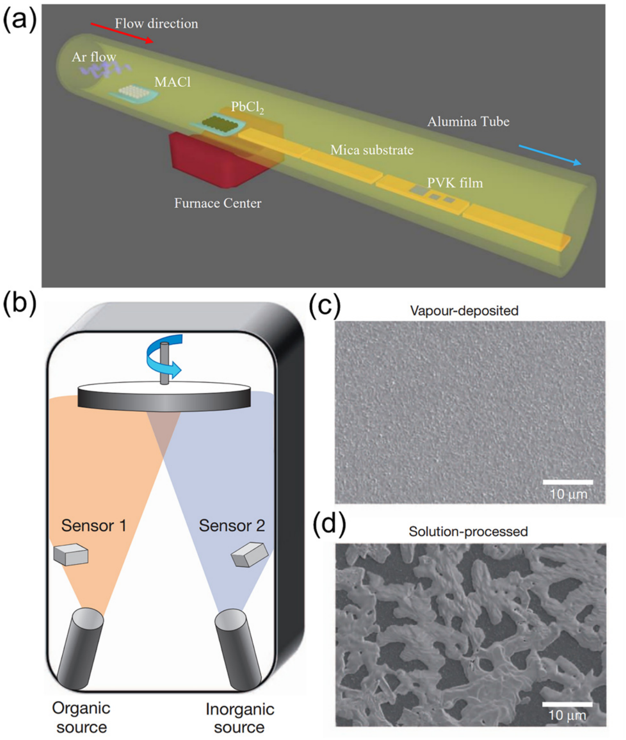

Fig. 4 (a) Synthesis of $MAPbCl_3$ by the CVD method. MACl and $PbCl_2$ sources were placed in different places in a single CVD tube. Reproduced with permission.[84] Copyright © 2015, American Chemical Society. (b) Schematic illustration of the dual-source thermal evaporation system. (c) and (d) SEM top views of a vapor-deposited perovskite film (c) and a solution-processed perovskite film (d). Reproduced with permission.[85] Copyright © 2013, Springer Nature.

3.2. Preparation of perovskite crystals

Applying single crystals is advantageous for obtaining improved performance, including higher mobility, uniformity, and enhanced stability due to the reduced structural and ionic defects and free of grain boundaries.[88] However, the rigorous conditions to obtain single crystals increased the difficulty of studying them. To the best of our knowledge, most of the perovskite single crystals are prepared *via* solution processing.

Solvent evaporation. Raghavan *et al.* developed a novel slow evaporation at constant-temperature (SECT) method to prepare low-dimensional perovskite single crystals. The conventional solvent cooling method may not be compatible with the more complicated 2D and quasi-2D perovskites due to the existence of bulky organic moieties. The SECT method could control the crystal growth more effectively and reduce the polycrystalline stacking, which benefited the formation of high-quality single crystals.[89] Single-crystal flakes can be further exfoliated from the as-grown bulk crystal to fabricate single crystal perovskite transistors.[49]

Nonsolvent/antisolvent strategy. The antisolvent approach is a promising method to fabricate perovskite nanoplatelets/nanocrystals. While hybrid perovskites and the precursors are soluble in DMF, the addition of a nonsolvent (*e.g.*, toluene) can cause the deposition of perovskites. This method has been successfully used to fabricate quasi-2D,[15,90,91] 2D,[92] and 3D perovskite nanocrystals.[93] Tian *et al.* demonstrated antisolvent-assisted single crystal growth. By the diffusion of antisolvent vapor in a confined container, the 2D perovskite $(PEA)_2SnI_4$ single crystals were induced to grow in the precursor solvent (Fig. 5a and b).[94]

Wang *et al.* presented a novel method to obtain a perovskite crystal array. Firstly, the PbI_2 solution was dropped on a pre-patterned substrate, and PbI_2 "seeds" were generated in each hydrophilic region precisely. After exposure to MAI gas under 120 °C, PbI_2 microplates could successfully converted into the $MAPbI_3$ perovskite crystal, as shown in Fig. 5c and d.[95]

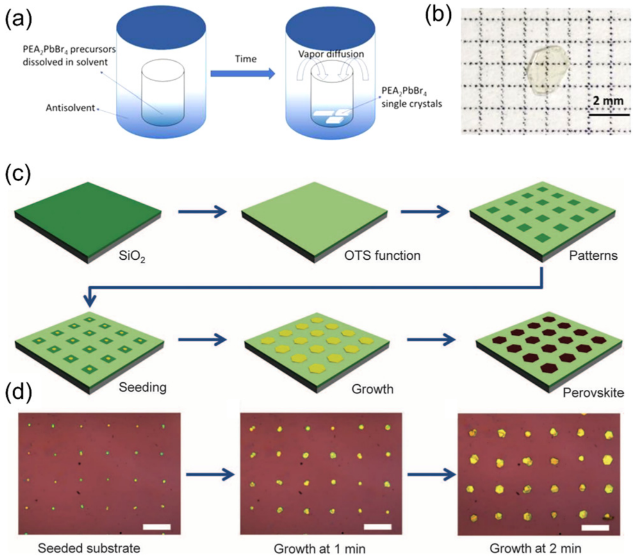

Fig. 5 (a) Schematic illustration of the growth progress of the 2D $(PEA)_2PbBr_4$ perovskite single crystals. (b) Photograph of an as-synthesized transparent, 2 mm $(PEA)_2PbBr_4$ single crystal. Reproduced with permission.[94] Copyright © 2017, American Chemical Society. (c) Schematic illustration of the patterned growth of regular arrays of perovskite crystals. (d) Optical images of PbI_2 seed arrays after the flow seeding process. The scale bars are 40 mm. Reproduced with permission.[95] Copyright © 2015, AAAS.

Epitaxial growth. Epitaxial growth is a solution processing method to grow single crystals, which is often considered as the ultimate technique to fabricate high-quality crystalline films.[96] Using a single crystalline substrate acting as a template, the growth process can be highly ordered and controlled.

An appropriate substrate is essential for epitaxial growth. Substrate materials should be carefully chosen by considering the match of the lattice. For instance, the growth of $MAPbI_3$ on III–V semiconductors, alkali halide, and other materials has already been reported. For example, $MAPbI_3$ has a tetragonal phase with a lattice constant of approximately 6.31 Å. In comparison, KCl also adopts a tetragonal phase with a lattice constant of 6.29 Å, which has only little mismatch.[97] The zinc blende GaAs has a lattice constant of 5.65 Å, which are also proper candidates for substrates.[98] Quasi-epitaxial growth is a more convenient approach to obtaining the crystalline film, which can be accomplished simply by spin-coating either perovskite or precursors solution on a proper single crystal substrate.[96,97]

Lei *et al.* developed a novel lithography-assisted epitaxial growth, whereas a bulk crystal was applied as the substrate, and the patterned polymer was used as a growth mask. Individual crystals grew at first until they got out of the mask. Note that the lattice orientations of the epitaxial crystals were the same. Subsequently, the crystals could grow laterally to form a complete and grain boundaries-free single crystal film and be further transferred to the arbitrary substrate.[99] This work revealed the potential of epitaxial growth in fabricating ultrahigh quality single crystal films.

Bulk crystals are sometimes inapplicable for transistors because of the higher thickness compared to carrier diffusion length.[88] In this case, epitaxial growth has great potential for fabricating ultrahigh performance thin film transistors. Huo *et al.* prepared ultrathin $CsPbBr_3$ platelets using van der Waals epitaxy to fabricate field effect transistors.[100] Analogous method is also promising for preparing organic–inorganic hybrid perovskite thin-film crystals.

3.3. Supplementary methods

Annealing. Solvent-processed perovskite polycrystalline films suffer from widespread crystal defects. The high roughness also harms charge transport between perovskite films and adjacent layers. For optical or electronic devices using perovskite films, annealing is essential to improve the film morphology and further enhance the device performance. Postdeposition annealing, mainly consisting of thermal annealing and solvent annealing, is a common strategy to further coarsen the grain and fix the possible cracks in films to obtain a smoother surface. Thermal annealing is a recrystallization process containing heating and cooling. The annealing temperature should be carefully selected to observe the best film morphology.[101] Solvent annealing is mainly a process where perovskite films are exposed to solvent vapor. During the procedure, perovskites can partially redissolve and be rearranged by the subsequent crystallization, improving grain size and fixing grain boundaries. Moreover, this process also allows chemical reactions to happen, which can partly eliminate residual precursors. Preferential orientation was also found to alter after solvent annealing.[102]

Mechanical exfoliation. Using the mechanical exfoliation method, Li *et al.* prepared $(BA)_2MA_{n-1}Pb_nI_{3n+1}$ (n = 2–5) microplates with 20 nm thickness from perovskite crystals. The as-prepared ultrathin microplates were proved to be with a single n-number perovskite phase. The perovskite microplates were furtherly integrated with hexagonal boron nitride (hBN) thin flakes to fabricate phototransistors.[103] Sun *et al.* obtained RP-phase quasi-2D perovskite $(BA)_2MA_{n-1}Pb_nI_{3n+1}$ (n = 2, 4) while slowly cooling the heated oversaturated solution. After mechanical exfoliation, single-crystalline nanoplates were prepared, and high-performance phototransistors were obtained.[104] However, the low reproducibility of mechanical exfoliation could limit its large-scale application.

4. Applications of HOIPs in transistors

4.1. HOIPs as channel materials in FETs

The field-effect mobility (μ) is the primary parameter to evaluate a field-effect transistor. The mobility can be determined by either saturation or linear regime data.

$$\mu_{\text{sat}} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{\text{DS}}}}{\partial V_{\text{G}}}\right)^2 \tag{4}$$

$$\mu_{\text{lin}} = \frac{L}{WC_{\text{i}}V_{\text{DS}}}\frac{\partial I_{\text{DS}}}{\partial V_{\text{G}}} \tag{5}$$

In the equations above, W and L are the width and length of the channel, C_{i} is the unit area capacitance of the insulating layer, and μ_{sat} and μ_{lin} are field effect mobilities of saturation or linear regime, respectively.

Moreover, on–off ratio ($I_{\text{ON}}/I_{\text{OFF}}$), threshold voltage ($V_{\text{th}}$), and subthreshold swing (SS) are other critical parameters for FETs. The on/off ratio reflects the ability of a transistor to regulate current. The threshold voltage determines the operating voltage of a transistor device. Researchers hope to reduce the threshold voltage to expand the scope of application. In particular, for wearable and implanted electronics, the operating voltage must be under human safety voltage. Subthreshold swing is defined as the derivative of gate voltage with respect to the logarithm of source–drain current. A relatively low SS demonstrates the high sensitivity of output current *versus* gate voltage, which is favorable for fast response. The following equation can calculate SS.

$$\text{SS} = \frac{\mathrm{d}V_{\text{G}}}{\mathrm{d}(\lg I_{\text{DS}})} \tag{6}$$

The most widely investigated three-dimensional HOIP, MAPbX_3, is famous for its balanced ambipolar charge transport. However, not every MAPbI_3-based FET can exhibit ambipolar characteristics. Various factors, such as film morphology and electrode material, can affect the carrier transport process.[105,106] In unipolar FETs, some employ hole-dominating transportation, which exhibits a p-type character. In contrast, others mainly utilize electrons as carriers, which indicates an n-type transistor.

In this section, perovskite transistors utilizing various components and structures in the past 24 years are summarized. We divided perovskites-channel FETs by polarity. Moreover, transistors employing perovskite dielectrics and novel FETs with functional properties are also exhibited.

4.1.1. Ambipolar FETs. Theoretical mobilities of MAPbX_3 were calculated to be over 1000 $\text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$ for both electron and hole, which indicates its excellent ambipolar transport characteristics.[107] However, there are various limitations in practical devices, such as charge trapping, ion migration, and phonon scattering. Due to the limitations, the apparent mobilities of MAPbX_3-based FETs were far lower than the theoretical value, and no field-effect characteristic could be observed. Temperature-dependent and gate bias-dependent characters were also found for perovskites-based electronics. For instance, Chin *et al.* fabricated transistors with MAPbI_3 channels. As tested over 198 K, no gate voltage-modulating character can be seen. N-type transport was observed between 98 and 198 K. The ambipolar characteristic is revealed only if the temperature is lower than 98 K. The transfer and output curves tested at 78 K of the transistor are shown in Fig. 6.[108] Versatile strategies have been developed to obtain better device performance, which are discussed below.

Optimizations of morphologies and grain sizes. Xu *et al.* investigated the film morphology and mobilities of $\text{CH}_3\text{NH}_3\text{PbI}_{3-x}\text{Cl}_x$ transistors under different annealing atmospheres. Annealing in flowing gas was superior to still gas due to the faster crystallization and low roughness. Oxygen might be able to passivate defects on surfaces. Besides, solvent annealing benefits larger grain size, and higher mobilities could be obtained.[109]

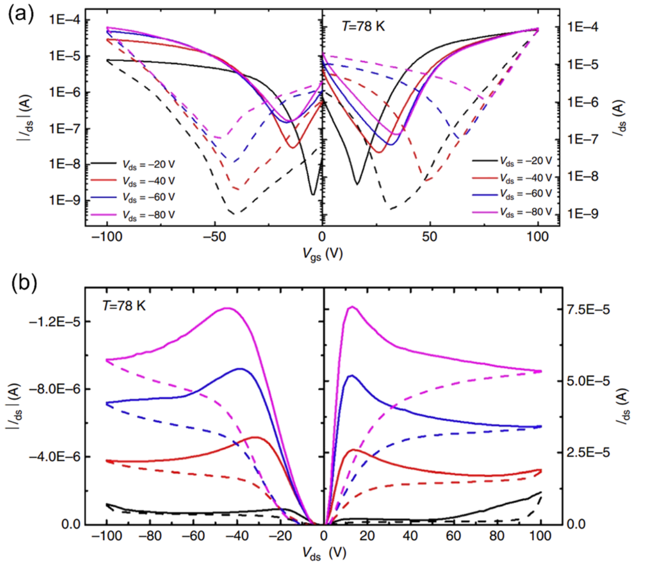

Fig. 6 Ambipolar transport characteristic of the perovskite FET at low temperature. Transfer (a) and output (b) characteristics were tested at 78 K. Solid and dashed curves are measured with forward and backward sweeping, respectively. Reproduced with permission.[108] Copyright © 2015, Xin Yu Chin *et al.*

FETs are particularly sensitive to the semiconductor surface because of the critical role of surface charge accumulation and surface transport procedures. Sirringhaus group used MAI to heal ionic defects on the MAPbI_3 layer. They developed a cleaning–healing–cleaning (C–I–C) process. The first cleaning was to remove weakly-bonded defective species, followed by exposure to MAI solution. This process aimed to eliminate surface organic-halogen defects and vacancies left or introduced by the first cleaning process. Resident ions were left after healing, which needed the final cleaning. Room temperature mobility of 1.8 and 3.0 $\text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$ for p-type and n-type, as well as decreased hysteresis, were observed in the surface-passivated transistor.[110] Zhou *et al.* passivated grain boundaries in MAPbI_3 films using polycaprolactone. Polycaprolactone was found to be confined in grain boundaries. As the polymer ratio increased, the charge transfer characteristic altered from the initial n-type to ambipolar, demonstrating the facilitated hole transfer. Moreover, polycaprolactone could also increase the ion migration activation energy.[106]

Hybrid anion/cation perovskites. Mixed halide perovskites, having the chemical formula of $\text{ABX}_{3-x}\text{X}'_x$, employ more than one kind of halide anion at X-site. Physical properties such as bandgap, exciton binding energy, and carrier diffusion lengths can be tuned more precisely by varying x.[111] For instance, mixed halide perovskites were found to exhibit longer carrier diffusion lengths. Stranks *et al.* found that carrier diffusion lengths for both electrons and holes could reach 1 μm in $\text{MAPbI}_{3-x}\text{Cl}_x$, which was an order of magnitude greater than MAPbI_3 ($\sim$100 nm).[112] By introducing mixed halide perovskite $\text{MAPbI}_{3-x}\text{Cl}_x$, Mei *et al.* fabricated ambipolar FETs with hole and electron mobility of 1.3 and 1.0 $\text{cm}^2\ \text{V}^{-1}\ \text{s}^{-1}$, respectively.[113] Taking advantage of solvent annealing, Zeidell *et al.* successfully optimized the $\text{CH}_3\text{NH}_3\text{PbI}_{3-x}\text{Cl}_x$

film morphology. Highly uniform grain microstructure was observed after solvent annealing. They proved that exposure to solvent vapor could help modify the orientations, increase grain size, and form solvent complexes that could heal the grain boundaries. As a result, compared to the initial μ_h and μ_e of 1.8 and 0.7 $cm^2\ V^{-1}\ s^{-1}$, highly improved and balanced mobilities of holes and electrons of 15.8 and 15.7 $cm^2\ V^{-1}\ s^{-1}$ were measured after solvent annealing, respectively.[102]

Despite applying different anions, a mixed cation strategy can introduce valuable properties to conventional perovskites. To enhance the device's thermal stability, Yusoff *et al.* introduced less volatile Cs^+ into hybrid perovskites to form triple cation $Cs_x(MA_{0.17}FA_{0.83})_{1-x}Pb(Br_{0.17}I_{0.83})_3$. The mobilities for both holes and electrons of $>1\ cm^2\ V^{-1}\ s^{-1}$ could be achieved at room temperature.[114]

Single crystals. However, defect states, grain boundaries, and complex surface morphology in polycrystalline films can inhibit carrier transport for both electrons and holes.[115,116] Applying single crystals is an effective strategy to reduce defects and eliminate grain boundaries, thus improving the overall performance, including carrier diffusion length and carrier lifetime.[117–120]

As described in section 3.2, the Duan group fabricated the FETs array based on $MAPbI_3$ crystal grown on pre-patterned electrodes. The FET exhibited ambipolar transport in which the mobility of dominant n-type transportation is $\sim$2.5 $cm^2\ V^{-1}\ s^{-1}$ of a backward sweep at 77 K.[95]

Unlike bulk single crystals (BSCs), thin single crystals (TSCs) have longer carrier lifetimes and higher mobility.[121] Yu *et al.* grew micrometer-TSCs of $MAPbX_3$ using a spatially confined inverse temperature crystallization method. This approach was developed by Saidaminov *et al.*[122] Unlike conventional cooling crystallization methods, the "inverse temperature" means that the solubility of perovskites in some solvents drops as temperature rises. The schematic illustration of the inverse temperature crystallization, and the as-prepared perovskite crystals are shown in Fig. 7. Thus, crystallization can proceed during heating (*e.g.*, $MAPbBr_3$ in DMF). Besides, the lateral size can be fine-tuned, ranging from micrometers to millimeters. By further applying BGBC device configuration, the mobility of hole and electron could reach 4.7 and 2.9 $cm^2\ V^{-1}\ s^{-1}$, which were superior to those of BGTC devices owing to the reduced distance of the charge pathway to the channel.[123]

Microwires. Gao *et al.* introduced perovskite microwires into FETs to overcome the difficulty of thin single crystal preparation. $MAPbI_3$ microwires were prepared by evaporating water from a needlelike bulk single crystal monohydrate compound. The as-fabricated FETs showed ambipolar transport character of 10^{-3} and 10^{-4} $cm^2\ V^{-1}\ s^{-1}$ for electrons and holes, respectively. However, the mobility and on/off ratio were still far from meeting the practical requirement.[124]

Vertical FETs. Owing to the short channel length and facile layer-by-layer solution fabrication method, the vertical field effect transistor has received attention over the years. Agrawal *et al.* fabricated vertical structured vertical resonant tunnelling field effect transistor using $MAPbI_3$ channel material, where the sharp negative differential resistance (NDR) peaks were observed in both the p and n mode owing to the ambipolar characteristic of $MAPbI_3$.[125] Subsequently, they reported FETs with 120 nm length channel. μ_h and μ_e were calculated to be 1.5 and 0.97 $cm^2\ V^{-1}\ s^{-1}$, respectively. However, the stability of the device still remains to be improved.[126]

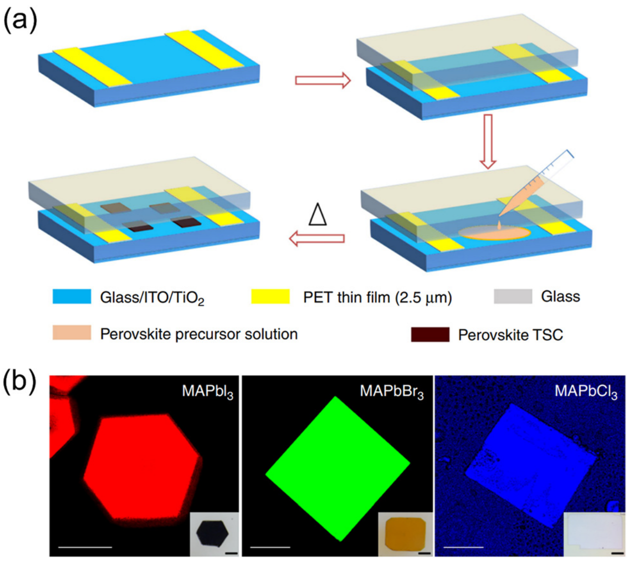

Fig. 7 (a) Schematic illustration of spatially confined inverse temperature crystallization method for producing thin single crystals (TSCs). (b) Fluorescence microscopy images of $MAPbI_3$, $MAPbBr_3$, and $MAPbCl_3$ TSCs, respectively. Reproduced with permission.[123] Copyright © 2018, Weili Yu *et al.*

The reports on perovskites-based ambipolar transistors mentioned in this review are listed in Table 1.

4.1.2 p-Type FETs

3D HOIPs

Mixed perovskites. Different properties can be introduced to the mixed metal or halide perovskites. Senanayak proved that the partial replacement of Sn in lead halide perovskites could modify the electronic structure, reduce the hole effective mass, and minimize the screening effects, which benefited hysteresis-free p-type transport.[127] Ward *et al.* changed the surface energy of the Cytop dielectric by the protein. The hydrophobic surface allowed the solution-processed perovskite film directly on the dielectric and enhanced the mobility from 0.23 to 1.3 $cm^2\ V^{-1}\ s^{-1}$.[128] Zhu *et al.* simultaneously introduced Br and Cl anion into the $MASnI_3$ perovskite. They found that ion migration was not the primary reason for hysteresis in this tin-based perovskite but the deep carrier trap, the vacancies of iodide (V_I). In I/Br/Cl perovskite, Br and Cl atoms could fill in and suppress V_I, which was consistent with the DFT calculations.[129]

Single crystals. Wang *et al.* investigated the electrical reaction that occurs on the interface of Au source/drain electrode and $MAPbBr_3$ single crystal perovskite, which can lead to defects formation. Employing a pentafluorothiophenol (PFBT) buffer layer between Au and perovskite, the maximum hole mobility could reach 15 $cm^2\ V^{-1}\ s^{-1}$ at 80 K, and the on/off ratio improved by four orders of magnitudes.[130]

Heterojunctions. Recently, Jo's group reported a type of high-mobility, low-operating voltage "hybrid" transistor by

Table 1 Properties of ambipolar FETs based on HOIPs channel layer

Channel material	Source/drain	Dielectric	μ_h [cm^2 V^{-1} s^{-1}]	I_{ON}/I_{OFF}	μ_e [cm^2 V^{-1} s^{-1}]	I_{ON}/I_{OFF}	Ref.
$MAPbI_3$[a]	Au, Ni	SiO_2	2.1×10^{-2}	—	7.2×10^{-2}	—	108
$MAPbI_3$[a]	Au	SiO_2	2.5	$\sim 10^6$	—	—	95
$MAPbI_3$	Au	Cytop	1.8	—	3.0	—	110
$MAPbI_{3-x}Cl_x$	Au	SiO_2	7.3×10^{-3}	1×10^4	1×10^{-2}	1.3×10^4	109
$MAPbI_{3-x}Cl_x$	Au	SiO_2	10 ± 2.5	—	10 ± 3.4	—	102
$MAPbI_{3-x}Cl_x$	Au	Cytop	1.3	—	1.0	—	113
$Cs_x(MA_{0.17}FA_{0.83})_{1-x}Pb(Br_{0.17}I_{0.83})_3$	Au	SiO_2	2.02	—	2.39	—	114
$MAPbI_3$	Al	LiF/V_2O_5	—	10^5	—	10^4	125
$MAPbI_3$	Al/ITO	LiF	—	10^4	—	10^4	126
$MAPbI_3$ microwires	Au	SiO_2	7.7×10^{-4}	16.7	1.8×10^{-3}	11.2	124

[a] Tested at 78/77 K.

applying a hybrid channel layer and high-dielectric constant dielectric material. The "hybrid" channel consisted of a bilayer of organic semiconductor and perovskite. Conjugated polymers such as P3HT were used to combine with hybrid perovskites. Nketia-Yawson *et al.* found that compared to the pristine P3HT transistor, the hole mobility could be doubled after injecting an $MAPbI_3$ layer between the P3HT layer and the source/drain electrodes. The enhancement of mobility was attributed to the perovskite-conjugated polymer interactions, such as the passivation of defects on perovskite surfaces.[131] Subsequently, they widen the range of perovskites. Hybrid perovskites such as $FAPbI_3$ and $FA_{0.2}MA_{0.8}PbI_3$ were also applied. XPS confirmed the chemical interaction between perovskite and P3HT. Transistors based on $FAPbI_3$/P3HT heterojunction exhibited an ultrahigh mobility of 24.55 cm^2 V^{-1} s^{-1}, which was a consequence of the interaction between perovskite and P3HT, more efficient hole injection, and optimized contact.[132] Varying the conjugated polymer also had the potential to elevate the device performance. A remarkable mobility of 30.87 cm^2 V^{-1} s^{-1} was observed from a Py1/$MAPbI_3$ FET.[133] Noticeably, the working voltages of these as-described transistors were relatively low ($|V_{th}| < 2$ V), which was the consequence of the high-κ polymer or electrolyte gate dielectrics. These dielectric materials were also responsible for the improved charge densities in the channels and contributed to the high mobilities.

2D HOIPs. Unlike the 3D HOIPs-dominating ambipolar transistors, low-dimensional HOIPs have the potential to be employed in p-type field-effect transistors as well since the first transistor was based on the two-dimensional $(PEA)_2SnI_4$.[18] Compared to the 3D counterparts, 2D HOIPs always exhibit suppressed ion migration, higher ambient and thermal stability, and mostly *p*-type transportation.[77]

Tin-based two-dimensional HOIPs, mainly $(PEA)_2SnI_4$, always work as p-type semiconductors. The first HOIP-based FET was fabricated by Kagan *et al.* in 1999. Spin-coated $(PEA)_2SnI_4$ was selected as the channel layer of the p-type TFT, where heavily *n*-doped silicon wafers with an indium contact and high work function metal were used as gate and source/drain electrodes, respectively. As a result, the p-channel transistor was observed. The field-effect mobility of this organic–inorganic transistor was 0.55 cm^2 V^{-1} s^{-1}, and the on/off ratio was higher than 10^4, as shown in Fig. 8.[18] Employing microcontact printing strategy, transistors with mobility and an on/off ratio of 0.5 cm^2 V^{-1} s^{-1} and 10^5 were subsequently achieved, respectively.[134]

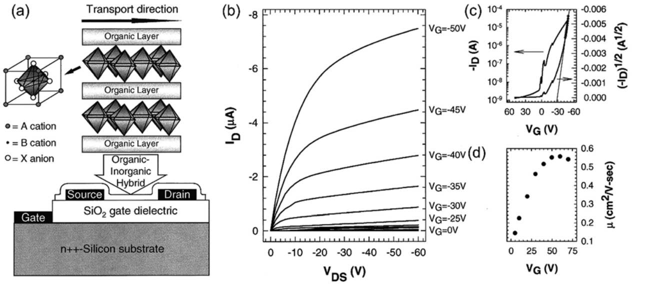

Fig. 8 Structure and properties of the first perovskite-based FET. (a) Schematic illustration of the $(PEA)_2SnI_4$ FET. (b) and (c) Output (b) and transfer (c) curves of the transistor. (d) The variation of mobility *versus* gate voltage. Reproduced with permission.[18] Copyright © 1999, AAAS.

Modifications of cations. Mitzi *et al.* used fluorine-monosubstituted PEA to synthesize the semiconducting $(m\text{-FPEA})_2SnI_4$ (m = 2, 3, or 4). The maximum saturation regime field-effect mobility of 2-FPEA, 3-FPEA, and 4-FPEA devices were 0.24, 0.51, and 0.48 cm^2 V^{-1} s^{-1}, respectively. Notably, the corresponding linear regime mobility was about 1 to 2 orders of magnitude lower than the saturation-regime mobilities, which were only 0.003, 0.06, and 0.06 cm^2 V^{-1} s^{-1}, respectively.[135] The V_G-dependent mobility was observed in both $(PEA)_2SnI_4$ and $(m\text{-FPEA})_2SnI_4$. Thus, higher mobility was always measured under higher V_G. This phenomenon was also observed in other channel materials, such as a-Si and organic semiconductors. The gate-voltage dependent mobility could be explained by the more filled traps and/or the higher carrier density under higher V_G.[136,137] Methoxy could also be modified in $(PEA)_2SnI_4$. The relatively low melting point of the HOIP enabled the melt-processed method. For $(4\text{-MeOPEA})_2SnI_4$ and $(4\text{-MeOPEA})_2SnI_4$, the saturation and linear regime mobility were 2.6 and 1.7 cm^2 V^{-1} s^{-1}, respectively, with a high on/off ratio up to 10^6. The improved grain structure associated with the melting process might contribute to enhanced mobility, both in the saturation and linear regime. Note that the μ_{lin} was only slightly inferior to the corresponding μ_{sat}, which might benefit from the reduced trap density in the melt-processed device.[22]

Butylammonium (BA) is a classical cation used to research the properties of low-dimensional HOIPs. However, there have been rare reports about BA-based HOIP transistors. Liu *et al.*

fabricated transistors with polycrystalline BA_2SnI_4 and investigated methods to optimize the film morphology. The highest mobility they observed was 0.03 $cm^2\ V^{-1}\ s^{-1}$.[138] This work demonstrates the potential of aliphatic ligands in charge transport perovskites, but the mobility must be improved to meet the practical acquirement.

Conjugated ligands. Compared to 3D counterparts, low dimensional perovskites weaken the limitations of structural tolerance factors, providing a platform for diverse organic ligands. For instance, people tried to modify PEA to gain better performance. Previous studies have demonstrated the potential of π-conjugated organic cations to alter the band alignment and promote exciton separation in 2D perovskites.[139,140] Dou's group first introduced conjugated cation perovskites into transistors by changing the conventional organic cation PEA^+ to the highly conjugated cation $4Tm^+$, where $4Tm^+$ was a derivative of the thiophene oligomer. The enhanced mobility of the $4Tm_2SnI_4$ transistor is attributed to three aspects: the higher crystallinity and degree of order, larger grains and tolerance of high annealing temperature, and less hole injection barrier from Au electrodes. Surprisingly, not only electrical properties but also stability in conjugated cation perovskites was found to be superior. They suggested that ionic bonding and nonbonded interaction were stronger in $4Tm_2SnI_4$. Their formation energy was calculated to be more negative, which indicated the higher stability.[141] A series of conjugated organic ligands was developed, And they are all thiophene-containing groups. The maximum mobility and on/off ratio approached 10 $cm^2\ V^{-1}\ s^{-1}$ and 10^6, respectively. The structure and transfer curves of the 2D conjugated ligand perovskite and transistors based on them are shown in Fig. 9.[142] Subsequently, they modified $4Tm^+$ by changing one of the thiophenes rings to the Se-containing selenophen (STM^+). However, $(STm)_2SnI_4$ had smaller grain sizes than $(4Tm)_2SnI_4$, which was not beneficial for high mobility but was suitable for high-efficiency LED devices.[143]

Optimizations of morphologies and grain sizes. Recently, Wang *et al.* substituted the phenyl in the PEA^+ with thienyl to form a novel cation TEA^+. The as-prepared $(TEA)_2SnI_4$ films were annealed at different temperatures in the range from room temperature to 160 °C. The authors found that 120 °C was the optimal casting temperature due to the largest grain size. The mobility of the 120 °C casted FET of 1.08 $cm^2\ V^{-1}\ s^{-1}$ is four times higher than the film fabricated at room temperature.[76] Subsequently, pentanoic acid was employed to improve the $(TEA)_2SnI_4$ film morphology. A small concentration of pentanoic acid in the precursor solution could alter the nucleation process and suppress tin oxidation.[144]

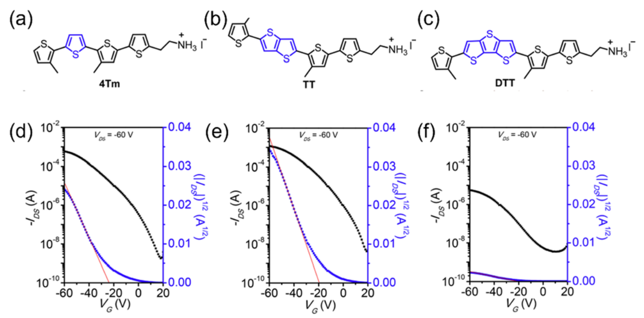

Fig. 9 Structures and properties of 2D halide perovskites with conjugated ligands. (a)–(c) Chemical structures of the (a) 4Tm, (b) TT, and (c) DTT organic cations. (d)–(f) Transfer curves of FETs based on (d) $(4Tm)_2SnI_4$, (e) $(TT)_2SnI_4$, and (f) $(DTT)_2SnI_4$. Reproduced with permission.[142] Copyright © 2021, American Chemical Society.

Additives in precursor solutions can influence the morphology of the deposited films. Lewis bases were demonstrated to be responsible for controlling the grain size and morphology of perovskite films. In the precursor solution, the electron pairs in the Lewis bases could share with the 5d orbital of lead in PbI_2 and form a coordinated compound, hence reducing the Gibbs' free energy of crystallization to slow the process and further modulate the film morphology.[145] Consequently, passivated grain boundaries and larger grain sizes could be formed.[146] Zhu *et al.* found that a 2% volume ratio of urea as an additive of the precursor solution could significantly improve the transistor's mobility and on/off ratio. However, the excess amount of nonversatile urea could harm the device performance.[147] Because PbI_2 is also the precursor of $MAPbI_3$, Jana found that this strategy was also appropriate for altering $MAPbI_3$ deposition. The addition of diethyl sulfide elevated the $MAPbI_3$ mobility to a surprising 21.41 $cm^2\ V^{-1}\ s^{-1}$.[145]

Zhu *et al.* systematically investigated strategies to optimize $(PEA)_2SnI_4$ transistors, especially by improving the film morphology. Excess precursor PEAI was found to be responsible for the self-passivation of carrier traps, and Lewis bases were introduced to enlarge the grain size. Oxygen is usually thought to be fatal to Sn-based perovskites because of the easy oxidation from Sn^{2+} to Sn^{4+}. Remarkably, the authors also demonstrated that a trace amount of oxygen (∼1 ppm) could enhance the mobility by the p-doping effect.[148] Antisolvent strategy was also applied to modulate the film morphology. Unlike the conventional procedure of dripping antisolvent during spin-coating, Zhu *et al.* directly added antisolvent into the precursor solution, which was also effective but more facile.[149]

Chao *et al.* used PEAI/FPEAI (PEA iodide and its fluoro-substituted derivative) to passivate surface defects on $(PEA)_2SnI_4$ transistors. The p-doping effect of passivation promoted hole injection. Notably, in FPEAI-passivated devices, F atoms not only elevated the mobility by interacting with perovskites but also could block moisture, significantly enhancing the device stability. Notably, due to the light-harvesting nature of $(PEA)_2SnI_4$, the transistor also had the potential for phototransistors. The passivated phototransistors exhibited better photoresponse because of the reduced defects.[71]

Device architectures. Li *et al.* fabricated a $(PEA)_2SnI_4$ transistor with low operating voltage employing high-dielectric-constant fluorinated copolymer PVDF-TrFE. In the fabrication process, the $(PEA)_2SnI_4$ film was directly deposited onto the dielectric layer. However, the solvent used to dissolve the perovskite (DMF) could harm the PVDF-TrFE layer. A 10 nm PTFE buffer layer was introduced to protect PVDF-TrFE from DMF corrosion. Nonetheless, PTFE is a nonpolar polymer, so the polar solvent DMF was hard to disperse on it finely. The perovskite film could possess better morphology if a 20 nm-thick polar CL-PVP layer were prepared on the PVDF-TrFE/PTFE bilayer. CL-PVP (cross-linking poly(4-vinylphenol)) is a hydroxyl-rich polymer demonstrated to modify the surface energy and buffer solvent erosion. The contact angles and film morphology of different dielectric layers are shown in Fig. 10a–f.[150] Compared to perovskites on PVDF-TrFE/PTFE, the perovskite films on the trilayer dielectric exhibited enhanced uniformity, as shown in Fig. 10g–j. Although the dielectric constant of PVDF-TrFE/PTFE or PVDF-TrFE/PTFE/CL-PVP was lower than that of pristine PVDF-TrFE, the operating gate voltages of the two devices were still in the low range (−20 to 20 V). However, the improved hysteresis caused by interface charge trapping and a relatively low on/off ratio ($\sim$190) still needs further study (Fig. 10k and l).[151]

Employing the MoO_x hole-injection layer (HIL) and top-gate structure can promote hole injection and reduce the trap density. As a result, the HIL-containing FET exhibited hole mobility up to 15 $cm^2\ V^{-1}\ s^{-1}$ at room temperature.[152] Also, using TG/TC and MoO_x HIL, Matsushima and coworkers promoted the hole mobility to 26 $cm^2\ V^{-1}\ s^{-1}$ by increasing the channel length, which might reduce the relative negative effect of contact resistance between the semiconductor and source/drain electrodes. N-Channel FETs were also fabricated by replacing HIL with a C_{60} electron-injection layer (EIL). Moreover, they found that the surface pretreatment of the substrate with a self-assembled monolayer containing ammonium iodide terminal groups (NH_3I–SAM) could induce better perovskite formation during spin-coating.[153] MoO_x HIL is also applicable for 3D $MAPbI_3$. Tang *et al.* improved the mobility of the $MAPbI_3$ transistor from 3.55 to 7.47 $cm^2\ V^{-1}\ s^{-1}$ by inserting the MoO_3 layer.[154] MoO_x was also demonstrated to be compatible with $MAPbI_3$.[83]

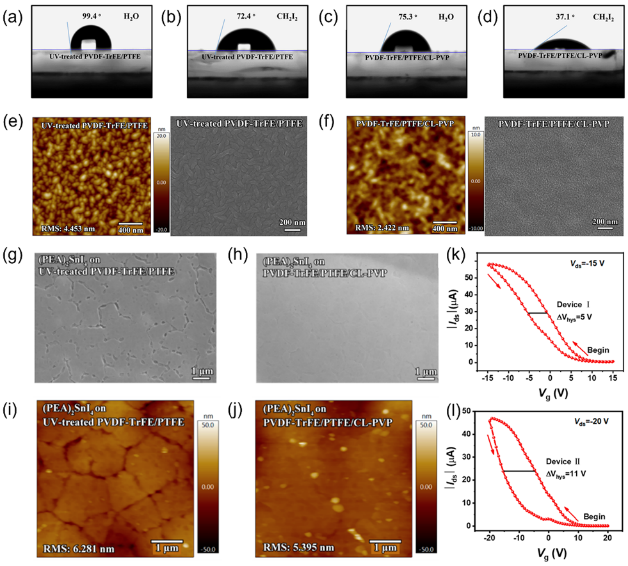

Fig. 10 (a)–(d) Water and CH_2I_2 contact angles of the UV-ozone treated PVDF-TrFE/PTFE bilayer ((a) and (b)) and PVDF/TrFE/PTFE/CL-PVP trilayer. ((c)–(f)) AFM height and SEM images of the (e) UV-treated PVDF-TrFE/PTFE bilayer and (f) PVDF-TrFE/PTFE/CL-PVP trilayer. (g) and (h) SEM images of the $(PEA)_2SnI_4$ thin film on the (g) PVDF-TrFE/PTFE double dielectric layers and (h) PVDF-TrFE/PTFE/CL-PVP triple dielectric layers. (i) and (j) AFM height images of the $(PEA)_2SnI_4$ thin film on the (i) PVDF-TrFE/PTFE bilayer and (j) PVDF-TrFE/PTFE/CL-PVP trilayer. (k) and (l) Transfer curves for the $(PEA)_2SnI_4$ FETs with the (k) PVDF-TrFE/PTFE bilayer and (l) PVDF-TrFE/PTFE/CL-PVP trilayer. Reproduced with permission.[151] Copyright © 2023, American Chemical Society.

The electron harvesting MoO_x can also be applied as a p-dopant. Reo *et al.* doped $(PEA)_2SnI_4$ with MoO_3 and TCNQ, respectively. They found that p-doping enhanced the overall hole concentration in perovskite films. Hence, hole traps could be filled, and the excess holes could participate in charge transport.[155]

Improvements of stability. Lowering the perovskite dimension effectively can bring a significant advance by reducing ion migration due to the confinement effect and thus inhibits the hysteresis. Nonetheless, the hysteresis phenomenon could still be observed in low-dimensional perovskites. Cho *et al.* passivated iodide vacancies (V_I) in $(PEA)_2SnI_4$ with S^{2-}, and hysteresis was slightly declined by 10 V. The similar ionic radii of iodide and sulfur ensured the likely access of the latter into V_I.[156] However, the instability of the tin-based HOIPs in the ambient atmosphere limits its application, mainly because of the easy oxidation from Sn^{2+} to Sn^{4+} (p-type doping).[157,158] Matsushima *et al.* systematically investigated the degradation of $(PEA)_2SnI_4$, where harmful gaps first form between grains. Optimizing spin-coating solvents and annealing temperature could reduce grain boundary density and therefore slow the degradation.[159] Zhang *et al.* blended $(PEA)_2SnI_4$ with aromatic polymer additive poly(4-vinylphenol) (PVP). Hence the morphology, crystallization, stability, and electrical properties were improved due to the interaction between PVP and perovskite.[160]

Single crystals. After removing the residue layer having rough surfaces of the solution-grown $(PEA)_2SnI_4$ single crystal, better contact of electrode and perovskite was obtained by Matsushima *et al.*, and it was necessary to obtain high mobility of 40 and higher. However, the low fabrication yield and bad crystal-substrate contact should be further resolved.[58] Shen *et al.* designed and grew a novel, mixed cation perovskite $(PEA)_2CsSn_2I_7$ crystals with millimeter size. The introduction of cesium cation was thought to benefit enhanced stability. The single crystal transistor exhibited unipolar p-type transportation, which had a mobility of 33 $cm^2\ V^{-1}\ s^{-1}$ at 77 K.[161]

Heterojunctions. Blending 3D perovskites with low dimensional perovskites to form a 2D/3D hybrid is an effective strategy to enhance device performance because 2D parts could regulate the growth of 3D perovskites with improved orientation and crystallinity. Shao added a small amount of quasi-2D $(PEA)_2FA_{n-1}Sn_nI_{3n+1}$ to $FASnI_3$; consequently, the p-doping levels were reduced, and the crystal quality of $FASnI_3$ was improved. Thus, the mobility was significantly enhanced.[162] Yang *et al.* blended 3D perovskites into 2D perovskites to form a 2D/3D hybrid. Noticeably, the antisolvent dripping strategy was applied to control the growth and crystallinity of the perovskite. The fabricated transistors optimally exhibited hole mobility exceeding 10 $cm^2\ V^{-1}\ s^{-1}$ and negligible hysteresis.[163]

Table 2 summarizes HOIP-based p-type transistors with different components.

Table 2 Properties of p-type FETs based on the HOIPs channel layer

Channel material	Source/drain	Dielectric	μ_h [cm^2 V^{-1} s^{-1}]	V_{th} [V]	I_{ON}/I_{OFF}	SS [V dec^{-1}]	Ref.
$(PEA)_2SnI_4$	Pd, Pt, or Au	SiO_2	0.62	—	$>10^4$	—	18
$(4\text{-}FPEA)_2SnI_4$	Pd	SiO_2	0.48	−70	$\sim10^5$	—	135
$(3\text{-}MEOPEA)_2SnI_4$ or $(4\text{-}MEOPEA)_2SnI_4$	Au	SiO_2/polyimide	2.6	—	$\sim10^6$	—	22
$MAPbI_3$	Ag	SiO_2	566	−3.501	2.3×10^3	0.4035	82
$MAPbI_3$	Au	Cytop	1.3	—	—	—	128
$MASn(I/Br/Cl)_3$	Au	HfO_2	19.6	0	3×10^7	—	129
$MAPbI_3$/P3HT	Au	P(VDF-TrFE)	5.01	0.74 ± 1.18	—	−10.76 ± 2.37	131
$FAPbI_3$/P3HT	Au	Electrolyte	24.55	−0.77 ± 0.09	$>10^2$	—	132
$MAPbI_3$/Py1	Au	Electrolyte	30.87	−1.31 ± 0.08	$>10^4$	—	133
TEA_2SnI_4[a]	Au	SiO_2	1.8	6.6	$>10^4$	4.05	76
TEA_2SnI_4[a]	Au	SiO_2	2.3	9	6.1×10^4	2.9	144
$MAPbI_3$	Ti/Au	SiO_2	23.2	−0.57	2.5×10^4	0.14	145
$(PEA)_2SnI_4$	Au	SiO_2	0.67	—	$\sim10^5$	0.8	148
$(PEA)_2SnI_4$	Au	SiO_2	3.7	20 ± 1	6.7×10^5	1.9 ± 0.2	147
$(PEA)_2SnI_4$	Au	SiO_2	3.8 ± 0.6	34 ± 3	$\sim10^6$	2.1 ± 0.2	149
$(PEA)_2SnI_4$	Au	SiO_2	2.96	—	$(2.69 \pm 1.6) \times 10^4$	−27.5 ± 4.4	71
$(PEA)_2SnI_4$	Au	SiO_2	0.78 ± 0.24	−1.7 ± 0.3	$(4.4 \pm 3.5) \times 10^5$	—	86
$(PEA)_2SnI_4$	Au	Cytop	12 ± 1	−22 ± 2	$(1.9 \pm 2.1) \times 10^6$	0.8 ± 0.1	164
$(PEA)_2SnI_4$	Al/MoO_x	Cytop	26	~15	$>10^6$	~1	153
$MAPbI_3$	Au/MoO_x	SiO_2	7.47	0.608	2.4×10^5	0.46	154
$MAPbI_3$	Au/MoO_x	Al_2O_3	21.41	—	10^4	0.49	83
Doped $(PEA)_2SnI_4$[b]	Ni/Au	SiO_2	100	—	—	—	155
$(PEA)_2SnI_4$	Au/MoO_x	Cytop	7.9 ± 2.3	−54 ± 13	$(2.8 \pm 14) \times 10^5$	5.4 ± 3.1	159
$(PEA)_2SnI_4$	Au	PVA/CL-PVP	0.24 ± 0.05	30 ± 6	$\sim5 \times 10^3$	8.6 ± 5.0	160
$MAPbBr_3$ crystal[b]	PFBT-modified Au	SiO_2	15	—	10^6	—	130
$MAPbCl_3$ thin crystal	Au	SiO_2	3.8	1.45	1.45×10^5	2.1	123
$MAPbBr_3$ thin crystal	Au	SiO_2	3.6	1.15	3.37×10^5	1.9	123
$MAPbI_3$ thin crystal	Au	SiO_2	4.7	0.16	8.78×10^4	0.6	123
$(PEA)_2SnI_4$ crystal	Au/MoO_x	SiO_2	42.1	−26.8	3.6×10^6	—	58
$(PEA)_2CsSn_2I_7$ crystal[c]	Cr/Au	SiO_2	34	—	—	—	161
$(PEA)_2FASn_2I_7/FASnI_3$	Au	SiO_2	0.21	2.8	10^4	—	162
$(4\text{-}FPEA)_2SnI_4/FASnI_3$	Au	HfO_2	11.8	—	$>10^8$	0.09	163
$(PEA)_2SnI_4$	Au	PVDF-TrFE/PTFE/CL-PVP	0.42 ± 0.14	9.4 ± 2.9	~180	5.6 1.8	151
$(PEA)_2SnI_4$	Au	SiO_2	1.45 ± 0.15	11.3 ± 1.3	2.9×10^5	2.6 ± 0.7	156
$BDASnI_4$	Au	PVA/CL-PVP	0.48 ± 0.05	6.60 ± 1.09	1.9×10^4	6.0	165
$4Tm_2SnI_4$	Au	SiO_2	2.32	−20 to −30	10^5 to 10^6	~10	141
TT_2SnI_4	Au	SiO_2	9.35	−10 to −20	10^5 to 10^6	~5.4	142
BA_2SnI_4	Au	PVA/CL-PVP	$(1.52 \pm 0.63) \times 10^{-2}$	23.6 ± 8.3	~150	22 ± 4.7	138

[a] Tested at 100 K. [b] Tested at 80 K. [c] Tested at 77 K.

4.1.3. N-Type FETs. N-Type FETs utilize electrons as dominating charge carriers. N-channel transistors are essential for fabricating complementary circuits by integrating with p-type transistors. However, the number of reports on perovskite-based n-type FETs is relatively lower than their p-type and ambipolar counterparts.

3D HOIPs. Ngai *et al.* fabricated $MAPbI_3$ films directly on various gate dielectrics. They found that the surface energy of dielectrics could inversely influence the HOIP crystal sizes and adhesion between the layers. They demonstrated that the larger grains favored growth on a more hydrophobic surface, such as PiPMA and PiBMA. However, perovskites grown on PiPMA and PiBMA also exhibited relatively poor uniformity and adhesion, as shown in Fig. 11. The magnitude of the electron mobility was enhanced by an order of magnitude by optimizing the dielectric material.[166] Mativenga *et al.* observed the abnormal phenomenon that the $MAPbI_3$ film deposited in ambient air had higher mobility than that prepared in the N_2 glove box. Before that, moisture was already found to have a possible enhancement to the film morphology by partially dissolving the reactant species during film formation.[8] Moreover, oxygen was also responsible for reducing the grain boundaries.[167] Works on perovskite films prepared in ambient conditions give us hope to simplify fabrication.

By introducing the $MAPbI_3$-ITO Schottky junction, Yu *et al.* fabricated vertical FETs with an on/off ratio of 10^4 at room temperature. However, the field-effect mobility was only 0.02 cm^2 V^{-1} s^{-1}.[168] Hoang *et al.* found that doping $MAPbI_3$ with cesium ion could decrease the film roughness and enhance the crystallinity. An electron mobility of 0.04 cm^2 V^{-1} s^{-1} was observed in this mixed-cation perovskite $Cs_xMA_{1-x}PbI_3$.[169]

2D HOIPs. N-Type charge transport has been hardly observed in $(PEA)_2SnI_4$, partly because of the huge electron injection

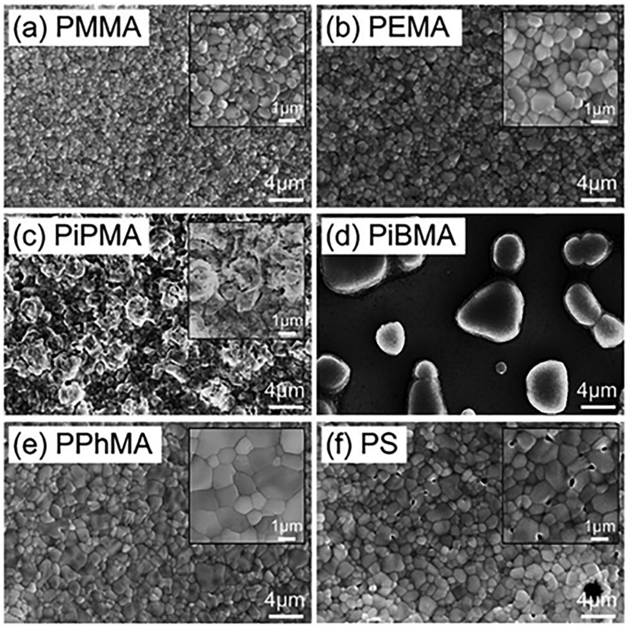

Fig. 11 SEM images of various perovskite films synthesized on various polymer substrates: (a) PMMA; (b) PEMA; (c) PiPMA; (d) PiBMA; (e) PPhMA; and (f) PS.[166] Copyright © 2017, Royal Society of Chemistry.

barrier between the frequently used Au electrode and $(PEA)_2SnI_4$ (1.11 eV). Matsushima *et al.* employed low work function electrode material (Al and Ag) and C_{60} electron injection layer and successfully fabricated n-channel transistors with the highest electron mobility of 2.1 $cm^2\ V^{-1}\ s^{-1}$.[170]

Single crystals. Li *et al.* investigated the effect of n in the RP phase perovskite $(BA)_2MA_{n-1}Pb_nI_{3n+1}$. Transistors were fabricated using single-crystal flakes exfoliated form crystals prepared by the SECT technique.[89] All transistors exhibited n-type conduction when n = 1, 2, and 3. Considering the existence of hysteresis, the field-effect mobilities were calculated to be 1.1×10^{-3}, 7×10^{-2}, and 9.5×10^{-1} $cm^2\ V^{-1}\ s^{-1}$, respectively, for n = 1, 2, and 3 using the data of backward sweeping direction at 77 K, which proved that mobilities could be enhanced by increasing the n.[49] Liu *et al.* also studied transistors based on the $BA_2MA_{n-1}Pb_nI_{3n+1}$ crystal. They supposed that the device was a Schottky-barrier type FET with an n-channel. The conduction band would bend when the gate voltage increased, and electrons had enhanced charge injection. The device showed a mobility of 0.087 $cm^2\ V^{-1}\ s^{-1}$ under 150 K. However, the reason why the mobility of the $BA_2MA_{n-1}Pb_nI_{3n+1}$ single crystal was in the low range even at low temperatures was still unclear.[171]

Different types of n-type perovskite FETs are listed in Table 3.

4.2. HOIPs applied in functional FETs

In this section, four types of functional FETs are presented, which are phototransistors, memory transistors, artificial synapses, and light-emitting transistors. In functional field-effect transistors, hybrid perovskites can play multiple roles, such as carrier transport, light absorbing, and charge trapping. HOIPs can also combine with other materials with versatile properties to integrate the merits of both the components.

4.2.1. Phototransistors. Photodetectors are light-sensing devices that convert photosignals to electrical signals. Beyond hot photovoltaics, light-harvesting HOIPs are also potential candidates for photodetectors owing to their long carrier diffusion length, low carrier recombination rate, tunable properties, and facile solution-based processing.[172] Three main types of photodetector configurations are photodiodes, photoconductors, and phototransistors (PTs).[173,174] Among them, PTs exhibit the unique signal amplification effect, which leads to the high photocurrent and photoresponsivity. Compared to the conventional FET, a PT usually contain an additional light-absorbing layer to generate light-induced carriers. Two operation modes of PTs are photovoltaic mode and photoconductive mode, respectively. In the former mode, the accumulation of photogenerated carriers promotes charge injection and shifts the threshold voltage, while the latter mode represents the linear relationship between the output current and incident light intensity in depletion mode.[175] Responsivity (R) and normalized detectivity (D^*) are key parameters to evaluate the performances of PTs. R reflects the conversion capability from light to electrical signals, defined as the ratio of the photogenerated current in phototransistors to the incident light power of the unit area.

$$R = \frac{\Delta I}{P_{\text{In}}A} = \frac{I_{\text{Photo}} - I_{\text{Dark}}}{P_{\text{In}}A} \tag{7}$$

In the above equation, I_{Photo} and I_{Dark} are drain currents under light illumination and in the dark, respectively. P_{In} is the total power of incident light, and A represents the device area.

D^* has a linear dependence on A and bandwidth (Δf) and is inversely related to the noise equivalent power (NEP). D^* represents

Table 3 Properties of n-type FETs based on HOIPs channel layer

Channel material	Source/drain	Dielectric	μ_e [$cm^2\ V^{-1}\ s^{-1}$]	V_{th} [V]	I_{ON}/I_{OFF}	SS [V dec^{-1}]	Ref.
$MAPbI_3$	Au	PPhMA	0.4	34.3	5.1×10^5	—	166
$MAPbI_3$	IZO	AlO_x	0.2	—	—	0.04	167
$MAPbI_3$	ITO/Al	HfO_2	—	—	10^4	1.1	168
$Cs_xMA_{1-x}PbI_3$	IZO	AlO_x	0.04	8.5	—	0.03	169
$(PEA)_2SnI_4$	Al/C_{60}	Cytop	2.1	47 ± 4	$(2.4 \pm 6.4) \times 10^4$	1.1 ± 0.2	170
$(PEA)_2SnI_4$	Al/C_{60}	Cytop	4.7	∼15	$>10^4$	∼1	153
$(PEA)_2SnI_4$ crystals	Al/C_{60}	SiO_2	121	30.8	6.3×10^6	0.38	58
$BA_2MA_{n-1}Pb_nI_{3n+1}$ single crystal[a]	Au	SiO_2	0.087	—	10^6	—	171

[a] Tested at 150 K.

the detect ability of low-intensity incident light, which refers to the minimum detectable light intensity. In cases of shot noise limit, D^* can be calculated by the following equation:

$$D^* = \frac{A\Delta f}{\mathrm{NEP}} = R\sqrt{\frac{A}{2eI_{\mathrm{Dark}}}} \tag{8}$$

In phototransistors, the incident light can regulate the output current like the typical gate bias, which is called the photogating effect. In other words, light serves as the additional gate voltage. Hybrid organic–inorganic perovskites are semiconductors with direct and tunable bandgap, where Wannier excitons with small binding energy generate. Those merits make HOIPs appropriate as the light-absorbing layer in PTs.

HOIPs can serve the function of light absorption, exciton separation, and charge transport simultaneously. That leads to the possibility of phototransistors with single perovskite active layers. Li *et al.* early fabricated $\mathrm{MAPbI_3}$ and $\mathrm{MAPbI_{3-x}Cl_x}$-based PTs applying bottom-gate top-contact (BGTC) configuration (Fig. 12a). The devices exhibited balanced ambipolar transportation, excellent photoresponsivity, and high response speed. As shown in Fig. 12b, the dark currents of this device approached 0 V even under high gate and source–drain voltages. However, I_{DS} could fast switch to high value after exposure to light. The R values of 320 and 47 A W^{-1} were calculated for PTs based on $\mathrm{MAPbI_3}$ and $\mathrm{MAPbI_{3-x}Cl_x}$, respectively. The relatively lower responsivity was attributed to higher dark currents in mixed halide perovskites. In addition, another vital parameter, the photoconductive gain (G), which represents the number of charge carriers induced by a single incident photon, was estimated as 10–100 of the PTs.[172]

Facile preparation is a prominent advantage for HOIPs-based PTs compared to conventional devices applying inorganic semiconductors. The HOIP light-absorbing layer can be easily solution-processed, even in the ambient atmosphere.[176] He *et al.* demonstrated the all-solution-processed PTs using sol–gel $\mathrm{SiO_2}$ gate dielectric. The dielectric layer was also responsible for protecting the active layer.[177]

2D HOIPs contain highly hydrophobic organic spacers, thus have enhanced air and moisture stability compared to their 3D counterparts. Chen *et al.* first fabricated 2D HOIP $\mathrm{(PEA)_2SnI_4}$-based PTs with an ultrahigh photoresponse of 1.9 × 10^4 A W^{-1}.[178] Wang and coworkers introduced ferroelectric polymer poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) as dielectric material in $\mathrm{(PEA)_2SnI_4}$ PTs. Charge traps were suppressed by the special dielectric layer, which led to inhibited hysteresis. Particularly, the ferroelectric polymer could exhibit different states under different gate biases. Holes could accumulate in the channel layer, causing a higher drain current at the "down" state and *vice versa*.[179] Recently, 3D/2D layer heterojunction was demonstrated to combine the advantages of both components. This strategy could effectively improve the ambient stability of 3D perovskite without sacrificing its photoelectric properties.[180] PTs with different device architecture has also been investigated. Xie *et al.* vertical FETs using MXene ($\mathrm{Ti_3C_2T_x}$) nanosheets as the source electrode. The detectivity was relatively high (7.84 × 10^{15} Jones), indicating the potential of vertical architecture and MXene electrode in phototransistors.[181] Nonetheless, intrinsic Sn vacancies, the oxidation from $\mathrm{Sn^{2+}}$ to $\mathrm{Sn^{4+}}$ (*i.e.*, self p-doping), and unipolar p-type transportation character may limit the development of low-dimensional, tin-based perovskite phototransistors.

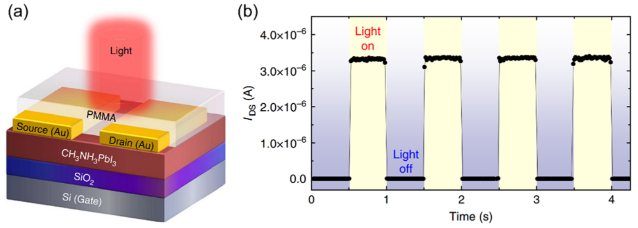

Fig. 12 (a) Schematic structure illustration of the phototransistor with an $\mathrm{MAPbI_3}$ channel. (b) Photocurrent responses of the phototransistors on light illumination, showing time-dependent photosensitivity with a time interval of 0.5 s at V_{GS} = −30 V and V_{DS} = −30 V. Reproduced with permission.[172] Copyright © 2015, Feng Li *et al.*

HOIPs exhibit excellent light-absorption properties, however, compared to inorganic semiconductors, the mobilities and gate modulation of pristine HOIPs-based PTs are still relatively low, which limits their overall performances, including R and response speed.[6] To enhance carrier mobilities of PTs, a heterojunction structure was introduced by combining perovskites with high mobility materials (*e.g.*, graphene[182,183] or carbon nanotubes[184,185]), and the overall photodetecting performance could be elevated.[186] By fine-tuning the band alignment, the junction configuration can promote the exciton separation and charge transport processes. In such devices, HOIPs mainly played a light-absorbing role, and conventional materials dominated carrier transportation.

Layer heterojunctions. Lee *et al.* designed enhanced performance hybrid PTs consisting of $\mathrm{MAPbI_3}$-graphene bilayer.[182] Ultrahigh R and D^* were obtained by sequentially introducing the vapor deposition of graphene and $\mathrm{MAPbI_3}$.[183] Du *et al.* fabricated PTs-containing $\mathrm{MAPbI_3}$ capping indium gallium zinc oxide (IGZO) channel layer. IGZO was thought to be an attractive channel material having an n-type mobility of 12.4 cm^2 V^{-1} s^{-1}. The perovskite-capped IGZO PTs showed an undescended mobility of 12.9 cm^2 V^{-1} s^{-1}, as well as a fair R of 10^6 A W^{-1} and D^* of 9.5 × 10^9 Jones.[187] For low-dimensional perovskites with enhanced stability, Shao demonstrated RP phase $\mathrm{(BA)_2MA_{n-1}Pb_nI_{3n+1}}$ with either faster response or enhanced stability.[188] The layer heterojunction structures combined high mobility and excellent light absorption property of different materials. In addition, Li *et al.* demonstrated that a 40 nm thick $\mathrm{PbI_2}$ layer between the perovskite layer and adjacent dielectric layer could effectively reduce the charge recombination at the interface, mainly because the $\mathrm{PbI_2}$ simultaneously acted as the barrier of holes and electrons in the perovskite.[189]

Bulk heterojunctions. Li and coworkers fabricated PTs using the single-wall carbon nanotubes (SWCNTs)-embedded $\mathrm{MAPbI_{3-x}Cl_x}$ film, which exhibited ultrahigh field-effect mobilities of 595.3 and 108.7 cm^2 V^{-1} s^{-1} for holes and electrons under light illumination, respectively. The record-high mobilities led to a high responsivity of 1 × 10^4 A W^{-1} and G over

8×10^3.[185] In some device structures, HOIPs were not continuous. For instance, in the work by Wang *et al.*, perovskite "islands" were grown onto graphene, and ultrahigh R and G of approximately 6.0×10^5 A W^{-1} and 2.01×10^9 were achieved because of the photogating effect, respectively. Specifically, after the separation of excitons at the interface between perovskite islands and graphene, trapped electrons in the perovskites caused the photogating effect while holes were free to transfer to graphene.[190] In PTs demonstrated by Xu and coworkers, $MAPbI_3$ nanoparticles (NPs) were induced to the surfaces of organic semiconductor 2,7-dioctyl[1]-benzothieno[3,2-*b*][1]benzothiophene (C8-BTBT) single crystal array to broaden the spectral response. High G was estimated to be 9×10^4 for their phototransistors. The integration of two kinds of semiconductors gave the PT dual-band detectivity, in which excitons are generated in $MAPbI_3$ NPs under visible light and in C8-BTBT under UV irritation. In both situations, electrons were trapped in C8-BTBT, and holes made a contribution to the enhanced photocurrent.[191] Zhu *et al.* prepared $(PEA)_2SnI_4$/conjugated polymer-wrapped semiconducting carbon nanotubes (semi-CNTs) blend as the active layer. They observed that film pinholes, gaps, and charge traps were lower in the mixed film, indicating a great blend of perovskites and semi-CNTs. The mobility enhancement was due to the improved morphology and addition of highly conductive CNTs.[192] Chen *et al.* prepared $MAPbI_3$ nanowires using a silicon nanowire template. The as-synthesized nanowires were combined with organic semiconductors (p-type PDVT-10 or n-type N2200) to form heterojunctions.[193] In short, the integration of perovskites and conventional semiconductors can combine the merits of both components: the effective photoresponse of perovskites and gate modulation of semiconductors. However, introducing charge-transporting materials inevitably increased the preparation difficulties and total costs.

Notably, the performances of some perovskites-based PTs can be significantly influenced by gate bias. Liu and coworkers demonstrated that in their 2D perovskites-based Schottky-barrier PT, R could alter from 0.0053 A W^{-1} at $V_G = 0$ V to 1.29 A W^{-1} at $V_G = 100$ V, which increased by over two orders of magnitude. This phenomenon could be explained by the working principle that at low gate voltage under threshold voltage ($V_G < 40$ V), the Schottky barrier dominated the device current, and the photogenerated carriers could not only improve the channel carrier concentration but also promote charge injection. In this case, the photocurrent had a linear relationship with light intensity, *i.e.*, R remained constant. But at a high V_G of > 60 V, photoinduced charges could only influence channel conductivity, and the relation between I_D and P_{In} became nonlinear.[171]

The properties of various HOIPs-based phototransistors are listed in Table 4. Note that some of the PTs are ambipolar transistors, and their mobilities for holes and electrons are exhibited as μ_h/μ_e.

4.2.2. Memory transistors. The emerging new generation memory devices exhibiting high memory capacity, considerable processing speed, and low energy consumption are expected to break the limit of the conventional Si-based memory hardware. Generally, memory devices include capacitor-type,[195] resistor-type,[196,197] and transistor-type electronics.[198,199] Notably, "memory transistors" are distinct from "memristors". A memory transistor is a particular type of memristor. The latter is usually a two-terminal device adopting an electrode-insulator-electrode sandwich structure. Merits such as facile charge-transfer modulation, multibit storage, and facile integration with circuits benefited from the additional gate electrode of memory transistors.[198,200] In addition, the diversity of functional materials provides a versatile platform to achieve memory FETs with universal properties.

Generally, memory transistors include ferroelectric type transistors and charge-trapping type transistors.[198,201] In ferroelectric-type FETs (FeFETs), ferroelectric materials are used as gate insulators to modulate the channel charge

Table 4 Active materials and vital parameters of HOIPs-based phototransistors

Active materials	R [A W^{-1}]	D^* [Jones]	μ_{FE} [cm^2 V^{-1} s^{-1}]	Ref.
$MAPbI_3$	320	—	0.18/0.17	172
$MAPbI_{3-x}Cl_x$	47	—	1.24/1.01	172
$MAPbI_3$	8.95	2.9×10^{12}	—	194
$MAPbI_3$	10.72	6.2×10^{13}	—	177
$MAPbI_3$	0.62	6.87×10^{15}	$(5 \pm 4) \times 10^{-4}/(4 \pm 3) \times 10^{-2}$	176
$MAPbI_3$	1.4×10^{-2}	—	1.7	6
$MAPbI_{3-x}Cl_x$	32	8.94×10^{11}	2.32/1.18	101
$(PEA)_2SnI_4$	1.9×10^4	—	0.76–1.2	178
$(PEA)_2SnI_4$	14.57	1.74×10^{12}	0.04	179
$(PEA)_2SnI_4$	8.8×10^5	1.5×10^{17}	3.7	147
$(PEA)_2SnI_4$	2.1×10^3	7.84×10^{15}	—	181
$MAPbI_3$-graphene bilayer	1.73×10^7	2×10^{15}	212/141	183
$MAPbI_3$-IGZO bilayer	2.5×10^{-2}	9.5×10^8	12.9	187
$(BA)_2MA_{n-1}Pb_nI_{3n+1}$-graphene bilayer	10^5	3.3×10^{10}	—	188
$(FAPbI_3)_{1-x}(MAPbBr_3)_x/PbI_2$	1302	—	21.36/49.32	189
$(PEA)_2MA_2Pb_3I_8$-SWCNTs bilayer	2.0×10^6	7.1×10^{14}	9.7	184
SWCNTs-embedded $MAPbI_{3-x}Cl_x$	1×10^4	3.7×10^{14}	595.3/108.7	185
$MAPbI_3$-coated C8-BTBT single crystal	$> 1.72 \times 10^4$	2.09×10^{12}	1.13	191
$(PEA)_2SnI_4$/semi-CNTs	6.3×10^4	1.12×10^{17}	1.51	192
$MAPbI_3$ nanowire/PDVT-10	169	6.7×10^{11}	0.18	193
$MAPbI_3$ nanowire/N2200	18	3.5×10^{11}	0.21	193

concentration under gate voltages. The ferroelectricity of perovskite-structured materials such as $BaTiO_3$, $PbZr_xTi_{1-x}O_3$, and $SrBi_2Ta_2O_9$ were discovered in the early years. Mathews and coworkers first demonstrated ferroelectric memory transistors based on inorganic perovskites in 1997. In their FeFETs, $La_{0.2}Ca_{0.3}MnO_3$ and $PbZr_{0.2}Ti_{0.8}O_3$ were used as channel and gate dielectric, respectively.[202] However, the thickness of the perovskite films should be downscaled to match the demand of high memory windows, but it is challenging, especially in commercial fields. Moreover, the high dielectric constants of perovskite materials also lead to unreliable polarization.[203,204] As a result, the emerging HOIPs-based memory transistors have been more likely to based on the charge-trapping mechanism. In charge-trapping transistors, charge carriers will be captured powerfully under programming gate bias. For instance, in the widely-investigated floating-gate transistor (a type of charge-trapping transistor), a floating-gate layer is sandwiched between two dielectric layers, namely, tunnelling and blocking layers.[195,199] When a significant enough programming bias is applied, charges in the channel layer can transfer across the tunnelling dielectric and be captured by the floating-gate layer. Charges trapped in the floating-gate layer are not able to return to the channel layer even if the bias is cancelled due to the existence of the barrier. This causes a shift in the threshold voltage, which can be read repeatedly to realize the nonvoltaic memory. In the erasing process, the opposite bias is applied. Thus, the trapped carriers can be released, and the threshold voltage can return. The additional evaluation parameters of a memory transistor *versus* an ordinary FET include the memory window, retention time, and write-read-erase-read (WRER) endurance. The difference between the initial state (OFF state) and programmed state (ON state) is defined as the memory window (ΔV_{th}). A large ΔV_{th} is responsible for the distinct difference between working states and potential multilevel memory. The retention time describes the device ability to maintain an ON state after programming. WRER cycles reflect the device stability during the repeating working process. Obviously, the longer retention time and immense WRER endurance are more desirable for high-performance memory devices.

Floating-gate memory transistors can be simply fabricated by inserting the required layers into normal FET structures. Vasilpoulou *et al.* achieved transistor flash memory by adding a nanofloating-gate layer between the perovskite semiconductor layer and gate insulator. The nanofloating-gate consisted of a star-shaped copolymer composed of styrene and fluorene (termed as $P(S–F)_4$) and fullerene derivative $PC_{61}BM$. The insulating styrene acted as a tunnelling dielectric, while the fluorene and $PC_{61}BM$ acted as the floating-gate. $PC_{61}BM$ could effectively capture electrons during the writing process. The trapped electrons generated an internal electric field to help holes accumulate in the perovskite channel, hence reducing the threshold voltage. This flash memory transistor exhibited a short programming/erasing time of 50 ms, a satisfactory memory window of 30 V, and a long retention time of 10^6 s.[205]

HOIPs themselves are potential candidates for charge-trapping materials due to their abundant trap states and unique energy band structure. In particular, 2D HOIPs have a unique quantum-well structure, which benefits the charge-trapping process. Gedda *et al.* fabricated memory transistors based on the $(PEA)_2SnI_4$-C8-BTBT blend. In the negative biasing condition, holes were injected into the $PbBr_4$ quantum well and unable to escape unless adequate positive gate voltage was applied. In such a device, the perovskite layer acted as a floating-gate. Surprisingly, the mix of organic semiconductors and perovskites could regulate the crystallization of perovskites.[206]

Jiang *et al.* first demonstrated perovskite nanocrystals (NCs)-based transistor memory. $MAPbBr_3$ NCs-decorated CdS nanoribbons (NRs) were applied to fabricate the nanofloating-gate transistor (Fig. 13a). Fig. 13b shows memory windows under different gate bias ranges. A larger memory window was achieved under a larger gate voltage, indicating the charge-trapping mechanism. At positive erasing bias, the electron density was elevated in the CdS NR channel, followed by the injection into $MAPbBr_3$ NCs *via* Fowler–Nordheim tunnelling. This erasing process could turn the transistor into an OFF state. On the contrary, the positive V_G could release the trapped electrons and "turn on" the device. Fig. 13c shows the band alignment of different modes for the transistor. This nanofloating-gate memory transistor exhibited excellent memory performance, including a memory window of 77.4 V, high on/off ratio of $>7 \times 10^7$, long retention time of 12000 s, and ambient stability of 50 days.[207]

Benefiting from the hysteresis caused by an ionic defect and ion migration, metal halide perovskites have the potential to be the single active material in memory devices.[197,208,209] Park and Lee first introduced Dion–Jacobson (DJ)-phase HOIPs into memory transistors. 3AMP)PbI_4 (3AMP = 3-(aminomethyl)piperidinium)) was chosen as the active layer material. The authors found that the ratio of DMF and DMSO in the spin-coat solution could affect the grain sizes of perovskites, and the larger grain sizes benefited from an enhanced on/off ratio. Consequently, the as-described memory FETs exhibited reliable resistive switching behavior with data retention (10^3 s) and WRER

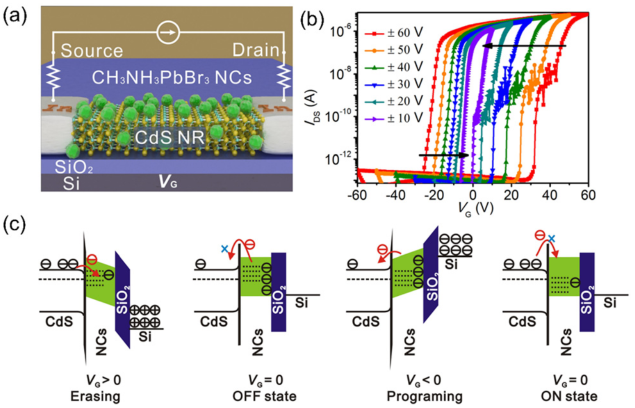

Fig. 13 (a) Schematic device structure of $MAPbBr_3$ NCs/CdS NR memory transistor. (b) Electrical transfer characteristics at V_{DS} = 1 V of the device recorded after every sweeping cycle. (c) Energy band diagrams of the device during the charge storage process. Reproduced with permission.[207] Copyright © 2019, American Chemical Society.

endurance (10^3 cycles). Moreover, DJ-phase HOIPs have enhanced stability compared to RP-phase counterparts because there are no van der Waals gaps between adjacent layers, which is vital for memory devices.[208] Haque and Mativenga realized the $MAPbI_3$ memory transistor and carefully investigated the ion migration in the perovskite. The ion migration (mostly the migration of I^-) by the drive of source–drain voltage caused the ions' dynamic redistribution and the switching from a high resistance state (HRS) to a low resistance state (LRS). The retention time and endurance were tested to be $>10^4$ s and $>10^3$ cycles, respectively.[209] These works inspire us that although, in most cases, the hysteresis phenomenon is harmful to perovskites' application in FETs, it can also be exploited to exhibit unique properties.

Photomemory FETs. Benefiting from the admirable light-absorbing capacity and intrinsic charge-trapping ability, HOIPs are promising for fabricating photomemory transistors, which have the dual function of photodetection and memory. Chen's group systematically investigated a specific device architecture similar to floating-gate transistors, which is an additional hybrid layer consisting of perovskites and polymer matrix inserted between the channel layer and gate dielectric, which plays the role of light-absorption and floating-gate simultaneously, as shown in Fig. 14a. They fabricated a multilayered phototransistor with a pentacene channel layer and a light-sensitive composite layer composed of a polystyrene (PS) matrix with dispersed $MAPbBr_3$ nanoparticles (NCs). In the photoprogramming process, electrons in pentacene would transfer to perovskite NCs to fill the vacancies resulting from exciton formation and got trapped until the erasing voltage was applied. The proposed device mechanism is schematically illustrated in Fig. 14b. This device could maintain reliable memory for more than three months and had an on/off ratio of $>10^4$.[210] Furthermore, the impact of altering the matrix polymer was investigated by Ercan *et al.*, who revealed that different polymers could cause different sizes of perovskite NPs and film morphology due to the coordination between oxygen atoms of polymer and lead atoms of perovskites. In this study, the PS matrix was found to be superior to poly(4-vinylphenol) (PVPh), PMMA, and PMAA.[200] This work confirmed that the aggregation of perovskite NPs was detrimental to memory performance, which was in agreement with the previous work.[210] However, further study demonstrated that changing PS to poly(2-vinylpyridine) (P2VP) could help boost the device performance. The P2VP-based photomemory transistors exhibited an enhanced on/off ratio (10^5) and lower light illumination requirement.[211]

Self-assembled block copolymers can exhibit natural phase separation and form well-organized microstructures. The block copolymer polystyrene-*block*-poly(ethylene oxide) (PS-*b*-PEO) was blended with $MAPbBr_3$, and solution-processed light-absorbing polymer P3HT was introduced as a channel layer to broaden the device absorption spectra by Chen's group. In the device, excitons could form in either P3HT (under red light illumination) or perovskite (under green or blue light illumination). These two situations had the same consequence to electrons trapped in perovskites (Fig. 15a–f).[212] PS-*b*-PEO could also combine with quasi-2D and 2D perovskites. Interestingly, by adding a small amount of PEABr into the $FAPbBr_3$ solution, the 3D perovskite would turn into a quasi-2D phase, and the crystal orientation could be significantly improved.[213] Recently, biphenylmethylammonium lead bromide ($(BPMA)_2PbBr_4$) with room temperature phosphorescence (RTP) was introduced to this type of device by Chen and coworkers. Compared to PEA, BPMA had a larger conjugated system and thus smaller triplet exciton energy. As a result, triplet–triplet Dexter energy transfer (TTDET) was allowed in $(BPMA)_2PbBr_4$ but inhibited in $(PEA)_2PbBr_4$. The formation of triplet excitons with longer lifetimes enabled high photoresponsivity and low power consumption (Fig. 15g and h).[214]

The integration of HOIPs and other semiconductors can broaden the overall absorption spectrum of the device, thus widening the detection range. This property is also well-matched with the multibit memory characteristic. Yang *et al.* selected the photosensitive n-type semiconductor BPE-PTCDI

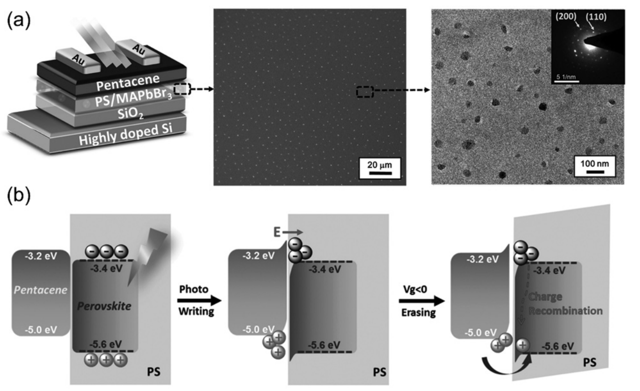

Fig. 14 (a) Schematic device configuration of the PS with dispersed $MAPbBr_3$ NCs photomemory with the SEM and TEM images of the $MAPbBr_3$/PS composite film. (b) The operating mechanism of the non-volatile perovskite-based photomemory. Reproduced with permission.[210] Copyright © 2017, John Wiley & Sons.

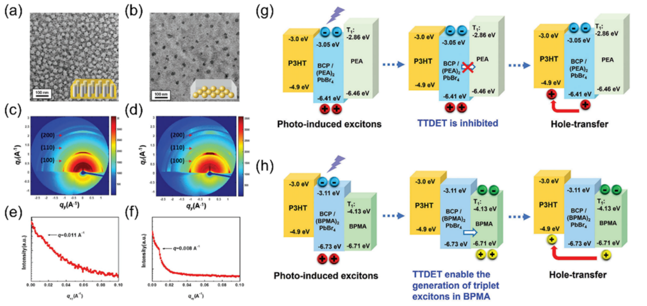

Fig. 15 (a) and (b) TEM images of (a) BCP-1/$MAPbBr_3$ and (b) BCP-2/$MAPbBr_3$ composite films after annealing for 17 h in benzene vapor. (c) and (d) GIWAXS 2D pattern of (c) BCP-1/$MAPbBr_3$ and (d) BCP-2/$MAPbBr_3$ composite films. (e) and (f) The GISAXS profiles of (e) BCP-1/$MAPbBr_3$ and (f) BCP-2/$MAPbBr_3$ composite films. Reproduced with permission.[212] Copyright © 2020 John Wiley & Sons. (g) and (h) The schematic diagram of the operating mechanism of (g) BCP/$(PEA)_2PbBr_4$ and (h) BCP/$(BPMA)_2PbBr_4$-derived photomemory. Reproduced with permission.[214] Copyright © 2023 Jian-Cheng Chen *et al.* Advanced Science published by Wiley-VCH GmbH.

as the channel material, which had complementary absorption spectra with perovskites. The device could be photowritten under light with three wavelengths of 650, 530, and 405 nm. Interestingly, the memory could be erased under 254 nm UV irritation without gate bias.[215] Lai and coworkers investigated photomemory FETs based on MoS_2/hBN/$(BA)_2MAPb_4I_7$ nanosheets van der Waals heterojunctions, in which MoS_2, hBN, and perovskites were channel, tunnelling dielectric, and floating-gate materials, respectively. The high-quality perovskite nanosheets exfoliated from single crystals also played the role of light-absorption. Specifically, MoS_2 had absorption peaks at 627 and 680 nm, whereas perovskites had 570 nm absorption. The device exhibited no memory behavior in dark but controllable memory windows (with the highest value of 94 V) under light illumination.[216] In their subsequent work, the perovskite $(BA)_2MAPb_4I_7$ was demonstrated to have the p-type doping effect, which changed the polarity of MoS_2 from n-type to p-type. Moreover, the MoS_2/perovskite heterojunction had a broadband absorption and thus high-performance (with a memory window of 104 V as well as fast writing speed of 20 μs), multibit (100 states, >6 bits) optoelectronic memory with a wide range operating wavelength of 405–1550 nm could be realized.[217] In conclusion, photomemory transistor combines the advantages of different materials (*e.g.*, perovskites, organic semiconductors, and polymers), and the properties can be promoted by optimizing the components, device architecture, and film morphology.

4.2.3. Artificial synapses. A human brain contains approximately 10^{11} neurons connected by 10^{15} synapses. Synapses delivering electrical or chemical signals between neurons exhibit merits of low power consumption, parallelism, and fault tolerance.[218–220] Inspired by the nervous system, neuromorphic circuits have the potential to break the confronting von Neumann bottleneck. In the past decade, neuromorphic circuits have received considerable attention for their low energy consumption during data transport and the potential ability in new-generation computers and even the field of emerging artificial intelligence (AI).[221,222] Artificial synapses in neuromorphic circuits can mimic synapse functions, including signal processing and transmission, and serve as connectors between pre- and post-"neurons".

Due to the versatile characteristics of artificial synapses, the synaptic plasticity is vital for application. To understand plasticity, we should first comprehend the postsynaptic current (PSC). PSC is the output current of a synapse after stimulation. The changing behavior of PSC after stimuli is called plasticity. Plasticity includes short-term plasticity (STP) and long-term plasticity (LTP). STP occurs when a single pulse is applied to the device, and the output current will not return to the initial value suddenly after the pulse. However, this phenomenon usually maintains only about a few minutes or seconds. Interestingly, under periodicity-repeated stimuli, the later pulse will cause a larger current than the previous one. The ratio of the two currents is defined as paired-pulse facilitation (PPF). STP may convert to LTP by enough repeated stimuli and can last for a more extended period of time. This process is also called "consolidation".

Artificial visual systems converting and remembering light signals have broad applications in image identification, the Internet of Things (IoTs), and robots.[223] Over the past few years, different device architectures were developed to mimic animal visual synapses, mainly including two-terminal photoconductors and three-terminal phototransistors,[218,224] in which phototransistors with signal amplification and ionic-to-electronic transduction properties were regarded as the promising device structure.[220] Metal halide perovskites, including inorganic perovskites and HOIPs, are suitable materials for artificial synapses owing to their excellent optoelectronic properties and facile fabrication process. Moreover, HOIPs exhibit the intrinsic hysteresis phenomenon because of ion migration, charge trapping, and ferroelectric polarization, which is appropriate to stimulate the STP and LTP behavior.[219] Notably, perovskites usually play the light-absorbing role rather than charge transport in photosensitive synaptic transistors.

Qian *et al.* revealed that the charge trapping mechanism could explain the STP and LTP character of the $(PEA)_2SnI_4$-based transistor-structured artificial synapses, where the deep-trapped electrons generated by previous light illumination could induce more holes at the second pulse. Specifically, the dominating electron traps were Sn vacancies.[225] Sun and coworkers fabricated perovskite artificial synapses employing $(PEA)_2SnI_4$ as the single active material. STP, as well as LTP, were successfully observed, as shown in Fig. 16, which shows a typical STP behavior, where the PSC quickly returned to the initial state after a few seconds. Fig. 16d and e demonstrate that continuous stimuli with a frequency of 1 Hz were not able to convert STP to LTP, but the conversion could be achieved when the frequency was enhanced to 20 Hz. It is obvious that the declining speed of STM was much higher than that of LTM. The plasticity was attributed to abundant traps in or onto the

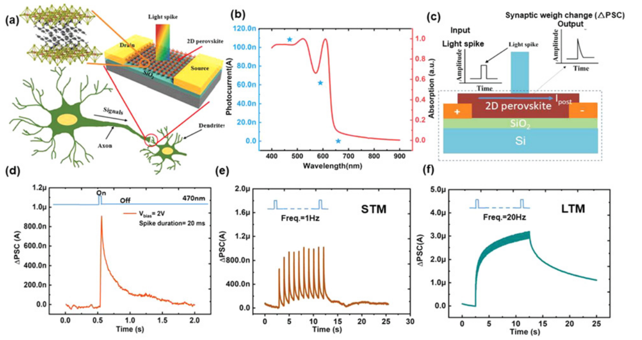

Fig. 16 (a) Schematic illustration of a biological synapse and the signal transmission process. The top right corner is an illustration of a synaptic transistor. (b) The UV-vis absorption spectrum of a $(PEA)_2SnI_4$ film (red line) and photocurrents of the $(PEA)_2SnI_4$-based photoconductor under 470, 590, and 660 nm illumination at the same intensity of 5 μW cm^{-2} (blue stars). (c) Cross-sectional illustration of the artificial synaptic transistor. The insets are examples of the input light pulses and PSC. (d) ΔPSC triggered by a light pulse under a gate bias (V_G) of 2 V, which is the STP behavior. (e) STP (duration = 20 ms, frequency = 1 Hz) and (f) LTP (duration = 20 ms, frequency = 20 Hz) behaviors triggered by light pulses.[219] Copyright © 2019, John Wiley & Sons.

perovskite films. The more the pulses applied to the device, the more opportunities the carriers had to be captured by deeper traps, which needed a longer time to release.[219] Although single-component perovskite transistors could successfully exhibit synaptic characters, however, the device performance can be further improved and fine-tuned employing heterojunction structures.[226]

Layer heterojunctions. Park *et al.* demonstrated the bilayer structure of transparent inorganic semiconductor indium zinc tin oxide (IGTO) and the HOIP $(BA)_2PbBr_4$, which significantly enhanced the retention time of plasticity compared to pristine $(BA)_2PbBr_4$. It can be inferred that 2D perovskites may be more favorable in artificial visual synapses because the BA-based 2D perovskite has deeper level defects compared to its 3D counterparts, leading to a longer retention time.[227] Huang *et al.* combined $(PEA)_2SnI_4$ and Y6 with complementary absorption spectra to broaden the detection range. Owing to the ambipolar transporting behavior of the $(PEA)_2SnI_4$/Y6 hybrid film, the device could distinguish different colors by different ΔPSC (negative ΔPSC for visible and positive ΔPSC for NIR light). As a result, the heterojunction device had the ability to recognize and remember different colors varying from visible to NIR light.[223]

The 3D $MAPbI_3$ is also an appropriate material in visual synapses due to its outstanding light-harvesting property. Hsu *et al.* demonstrated a red-light-stimulated synapse transistor with the P3HT channel layer and the polystyrene-*block*-poly(ethylene oxide) (BCP)/$MAPbBr_3$ heterojunction light-harvesting and floating-gate layer. However, limited by the exciton length, the thickness of the P3HT layer was strictly limited. The device performance was significantly influenced by the thickness of the P3HT layer controlled by rotation speed while spin coating.[228] For lead-based 3D perovskites, the high toxicity of lead is not suitable for broad applications. Recently, aiming to reduce the toxicity of lead-based perovskites, Jeon *et al.* fabricated artificial synapses using a novel mixed-metal perovskite, where 90% of the lead ions were substituted by manganese ions. This work demonstrated the potential of ecofriendly perovskites in optoelectronic devices.[229]

Bulk heterojunctions. A bulk heterojunction structure was introduced to solve the issue of short carrier diffusion lengths. Yin *et al.* fabricated synapses with the $MAPbI_3$-Si nanomembrane (NM) heterostructure. The Si NM trapped holes under light illumination, and therefore, the synaptic character was observed. The authors also found that the device exhibited better performance at negative gate bias due to the more serious bending energy bands of Si NM.[230] Chen *et al.* fabricated a synapse transistor using P3HT/perovskites quantum dots (PQDs) bulk heterojunction film. The $FAPbBr_3$ PQDs exhibited the fastest photoresponse due to the low-lying HOMO compared to $CsPbBr_3$ and $FA_{0.5}Cs_{0.5}PbBr_3$, which benefited the quick hole transfer from PQDs to P3HT.[231] Nevertheless, the microstructures of bulk heterojunctions are more challenging to control and engineer, leading to relatively low reproducibility.

4.2.4. Light-emitting transistors. Light-emitting transistors (LETs), integrating the bias-regulating function of FETs and the light-emitting property of LEDs, were first fabricated using a tetracene channel layer.[232] LETs have attracted considerable research interest due to their gate-assisted luminescence and higher charge carrier densities compared to LEDs.[233] In LETs, holes and electrons injected from different electrodes recombine in the channel layers to form excitons and emit light. Similar to ordinary FETs, LETs can also be divided into unipolar and ambipolar moieties. In unipolar LETs, light emission can only occur near one of two electrodes. Meanwhile, the unbalanced hole and electron injection and strong exciton quenching near the channel-electrode interface critically limit the efficiency of unipolar LETs.[234] In comparison, the balanced carrier injection is more likely to be obtained in ambipolar LETs, and excitons form near the middle of the channel, which can reduce the quenching phenomenon.[108,235] Metal halide perovskites are promising candidates for channels of LETs owing to their balanced ambipolar mobility, long carrier diffusion lengths, and excellent radiative properties. Besides, compared to the group III–V semiconductor analogue, perovskites are more affordable and easier to process.

Soci's group first employed HOIPs in light-emitting transistors. Using $MAPbI_3$ as a channel material, an ambipolar transportation character was obtained but only at low temperatures (78–178 K) due to the screening effect. The perovskite LETs exhibited bright electroluminescence (EL) emission under proper bias. Notably, the operating gate voltage should be carefully selected to accumulate holes and electrons in the channels simultaneously.[108] Subsequently, the co-evaporation method was employed for the film deposition. Thanks to the improvement of the $MAPbI_3$ film morphology, the FETs could exhibit excellent ambipolar transfer characteristics and light emission at room temperature.[236] Recently, a novel approach of metasurfaces was employed in LETs by Soci's group. A metasurface is a nanopatterned surface after rational engineering and exhibits extraordinary phenomena. The chiral photoluminescence was generated and amplified in a LET containing the triangle metasurface. The periodic triangular array on the metasurface broke the in-plane inversion symmetry, which resulted in the optical Rashba effect.[237] The focused ion beam (FIB) technology was used to realize the nanopatterning of active layers. Periodic nanobeams were oriented parallel to the Au electrodes on the metasurface, which served as optical cavities, as shown in Fig. 17. Thanks to the unique microstructure, the charge carrier distribution could be controlled by altering the V_{DS}, and the electroluminescence could be effectively enhanced by polarization. The polaritonic emission was found to be much stronger than the conventional excitonic emission.[233,238]

Further investigation demonstrated that LETs might have better performance under alternating current (AC) compared to direct current (DC) owing to the suppressed ion migration and cation polarization.[239] This concept was also confirmed by a $CsPbI_3$ LET.[240]

However, the carrier mobilities of the as-described perovskite LETs were still in a relatively low range (10^{-3}–10^{-1} $cm^2\ V^{-1}\ s^{-1}$), which should be further improved to enhance the light-emission efficiency.

4.3. HOIPs as gate dielectrics in FETs

Besides the charge-transporting and light-absorbing properties, HOIPs also have dielectricity with large dielectric constant due

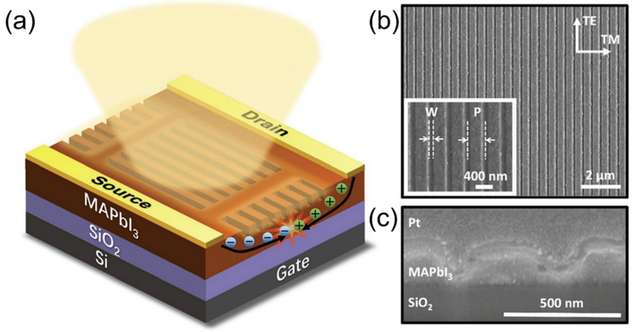

Fig. 17 (a) Schematic illustration of a perovskite LET with a metasurface. (b) Top-view and (c) cross-sectional SEM images of a MAPbI$_3$ perovskite metasurface film. The inset picture in (b) shows the geometrical parameters of the metasurface structure, including the groove width (*W*) and nanograting period (*P*). Reproduced with permission.[233] Copyright © 2022 John Wiley & Sons.

to their componential and structural versatility, which can be employed as the gate dielectric in transistors. Daus group first demonstrated transistors using MAPbI$_3$ dielectric. Although the bandgap of MAPbI$_3$ is narrow, the well-organized band offset between MAPbI$_3$ and channel material could efficiently block charge carriers. The dielectric constant is found to be V_G frequency-dependent, which declined while the frequency increased. This phenomenon was due to the ion migration in MAPbI$_3$. At low V_G frequency (0.05 Hz, Fig. 18a and c), the ions could have enough time to transfer to the interface, causing electrode polarization, thus exhibiting a slow-increasing drain current in a single cycle. In the fast-switching mode (20 kHz, Fig. 18b and d), ions do not have enough time to accumulate, and a much lower I_D was observed.[241]

Kalthoum *et al.* applied novel cadmium-based HOIPs (MACdCl$_3$ and (CH$_3$)$_2$NH$_2$CdCl$_3$) as gate dielectrics in FETs. The Cd-based dielectric exhibited higher capacitance than that for MAPbI$_3$ and frequency-dependent characteristics as well.[242] The facile-fabricated HOIP dielectric is expected to apply in high-performance and low-operating voltage field-effect transistors, especially in low operating frequency.

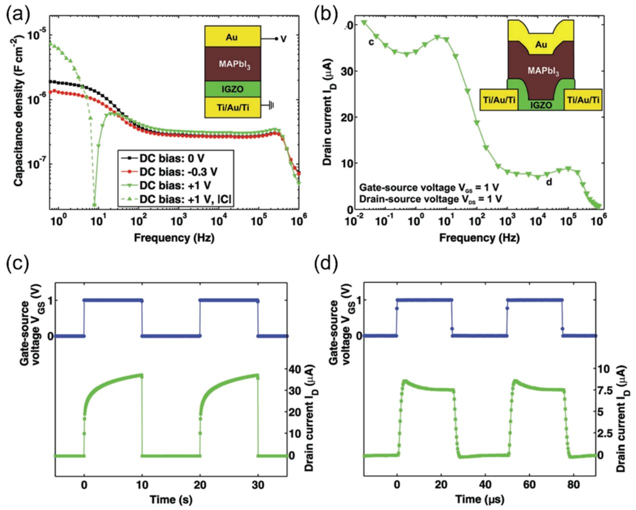

Fig. 18 (a) Capacitance densities at different DC operating conditions. (b) I_D as a function of the V_{GS} frequency. (c) and (d) I_D response at V_{GS} frequency of (c) 0.05 Hz and (d) 20 kHz. Reproduced with permission.[241] Copyright © 2018, John Wiley & Sons.

Functional FETs can be realized by applying functional dielectrics. For instance, Tian *et al.* demonstrated flexible optoelectronic memory transistors using (PEA)$_2$SnI$_4$/Al$_2$O$_3$ heterostructure gate dielectric. The light-sensitive (PEA)$_2$SnI$_4$ enabled the FET to exhibit multilevel photoresponse as well as photomemory properties.[243]

5. Conclusion and outlook

In the past two decades, field-effect transistors based on HOIPs have made tremendous progress due to the versatile and tunable properties of HOIPs, as well as the advancement of people's understanding of their nature, which is advantageous for their application in different types of FETs. Three-dimensional lead halide perovskites can transport electrons and holes, making them applicable in the ambipolar, p-type, and n-type transistors. In comparison, low-dimensional tin-based perovskites containing bulky organic ligands with elevated stoichiometry freedom often exhibit p-type dominating nature. So far, ultrahigh mobilities have been successfully achieved by HOIPs-based FETs. Despite the carrier transport ability, HOIPs also possess diverse remarkable characteristics such as light-harvesting, charge-trapping, and light-emitting, providing them a versatile platform in different types of functional FETs, including phototransistors, memory transistors, artificial synapses, and light-emitting diodes. However, the relatively poor stability compared with conventional semiconductors and severe hysteresis critically block the development of HOIPs-based FETs. In some cases, the apparent mobilities of those TFTs are still not able to match the theoretical value, especially at room temperature. Therefore, HOIPs have been integrated with additional materials, such as graphene or organic semiconductors, to enhance the devices' overall performance. Moreover, it is worth investigating how to transform the intrinsic "disadvantages" of HOIPs. For instance, hysteresis caused by ion migration, charge-trapping, and polarization is usually considered harmful to their application. From another point of view, hysteresis also enables perovskites to fabricate memory transistors with simple device structures.

Compared with the well-established silicon or III–V semiconductors, HOIPs mainly exhibit four outstanding advantages: the large-scale, low-temperature solution-processing ability making them facile; low-cost fabrication and intrinsic flexibility enabling them to fabricate wearable devices; tunable bandgaps ensure their applicability in various conditions, and unique optoelectric physical properties making them promising candidates in functional FETs. However, there also exist some drawbacks that limit their commercialization. To fully release HOIPs' potential in FETs, the challenging issues listed below still need further investigation. (1) The weakening of gate voltage-dependent device character and hysteresis phenomenon. This issue acquires a deeper understanding of processes occurring during charge transport, such as severe ion migration. The reduced hysteresis is also responsible for elevating the FET mobility at high temperatures. Inspired by the published HOIPs-based FETs with delightful mobilities, strategies can be applied to overcome the issue including but not limited to those summarized in this review. (2) The improvement of moisture, oxygen, and thermal stability. The poor stability is a tough issue for both FETs and solar cells, which significantly hinders their further industrial application. Moreover, the Pb-containing and water-sensitive HOIPs may release toxic lead ions when exposed to moisture, which requires further sustainable management. (3) The connection between film morphology and fabrication methods. It is no doubt that the larger grain size, passivated grain boundaries, and smoother film surfaces benefit the overall performances. Although various methods have been used to realize the target, a universal strategy is acquired to guide future investigations and assist us in understanding the process of crystallization. In short, beyond the emerging photovoltaics, HOIPs with chemical and structural diversity are also appropriate for fabricating high-performance FETs. However, it remains crucial, and an important research direction for the fundamental relationship between their structure and properties is required. We believe that hybrid organic–inorganic perovskites have potential in next-generation field-effect transistors, especially functional transistors.

Author contributions

All authors give discussion and write this paper.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

This work is supported by grants from the National Key R&D Program of China (grant no. 2021YFB3200701), the National Natural Science Foundation of China (No. U22A6002, 91833304, 91833306, 21922511, and 51873216), the Strategic Priority Research Program of the Chinese Academy of Sciences (No. XDB30000000), the CAS Project for Young Scientists in Basic Research (No. YSBR-053), the CAS-Croucher Scheme for Joint Laboratories, and the CAS Cooperation Project (No. 121111KYSB20200036).

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