Nanoscale

COMMUNICATION

View Article Online
View Journal | View Issue

Cite this: *Nanoscale*, 2023, **15**, 17335

Received 14th July 2023,
Accepted 12th October 2023

DOI: 10.1039/d3nr03429a

rsc.li/nanoscale

Integrated 4-terminal single-contact nanoelectromechanical relays implemented in a silicon-on-insulator foundry process†

Yingying Li,[a] Elliott Worsey,[b] Simon J. Bleiker,[a] Pierre Edinger,[a] Mukesh Kumar Kulsreshath,[b] Qi Tang,[b] Alain Yuji Takabayashi,[c] Niels Quack,[c]‡ Peter Verheyen,[d] Wim Bogaerts,[d,e] Kristinn B. Gylfason,[a] Dinesh Pamunuwa[b] and Frank Niklaus[a]*

Integrated nanoelectromechanical (NEM) relays can be used instead of transistors to implement ultra-low power logic circuits, due to their abrupt turn off characteristics and zero off-state leakage. Further, realizing circuits with 4-terminal (4-T) NEM relays enables significant reduction in circuit device count compared to conventional transistor circuits. For practical 4-T NEM circuits, however, the relays need to be miniaturized and integrated with high-density back-end-of-line (BEOL) interconnects, which is challenging and has not been realized to date. Here, we present electrostatically actuated silicon 4-T NEM relays that are integrated with multi-layer BEOL metal interconnects, implemented using a commercial silicon-on-insulator (SOI) foundry process. We demonstrate 4-T switching and the use of body-biasing to reduce pull-in voltage of a relay with a 300 nm airgap, from 15.8 V to 7.8 V, consistent with predictions of the finite-element model. Our 4-T NEM relay technology enables new possibilities for realizing NEM-based circuits for applications demanding harsh environment computation and zero standby power, in industries such as automotive, Internet-of-Things, and aerospace.

Nanoelectromechanical (NEM) relays have attracted considerable interest due to their inherent characteristics such as zero off-state leakage, steep switching transition, and harsh-environment operation capabilities, which make them ideally suited as digital switches for ultra-low power computation.[1–5] 4-Terminal (4-T) NEM relays decouple the signal path across the relay from the on/off actuation control such that the pull-in behaviour is determined by the voltage difference between the gate and body terminals, regardless of the signal voltage.[6] This feature distinguishes 4-T relays from both CMOS transistors and conventional 3-terminal (3-T) NEM relays that share a common source electrode between the two electrical paths.[7,8] In this way, the 4-T relay design enables logic circuits to be constructed with far fewer devices compared to transistor-based and 3-T NEM relay-based logic circuits.[9] Also, the decoupling of the actuation and signal voltages allows the pull-in voltage of 4-T NEM relays to be reduced by employing body-biasing, where the beam or gate has a static voltage bias applied to reduce the voltage swing required for actuation. Although basic NEM relay-based logic functions were introduced over a decade ago,[10–13] reliable miniaturization and integration methods for making NEM relay-based integrated circuits with multi-layer metal interconnect stacks have not been demonstrated. While several 4-T relays have been reported to date,[6–9,14,15] as summarized in Table S1,† these are not integrated,[15] and moreover have either a large footprint[6–9,14] or a high pull-in voltage.[6,7,9] Generally, small relay footprints are desirable to reduce cost, while the energy consumption of 4-T relays reduces inversely with the square of the voltage swing.

To demonstrate that these issues can be overcome, we report for the first time, nanoscale, silicon (Si) 4-T NEM relays that are patterned in front-end-of-line (FEOL) processing and monolithically integrated with back-end-of-line (BEOL) metallic interconnect layers manufactured in a commercial silicon-on-insulator (SOI) foundry platform (iSiPP50G by IMEC[16–19]). The foundry wafers containing the NEM relay structures and interconnects are post-processed to implement the electrical isolation between the control and signal paths of the 4-T NEM relays, the metallization of the contacts of the 4-T NEM relays, and the suspension of the movable sections of the relays. These post-processing steps are fully foundry compatible and can in principle be included into the commercial foundry process flow. This compatibility is critical to lower the threshold for potential commercial use and opens entirely new possibilities for efficient manufacturing of very-large-scale integrated (VLSI) NEM relay-based logic circuits at high yield.

[a]*KTH Royal Institute of Technology, 11428 Stockholm, Sweden. E-mail: frank@kth.se*
[b]*University of Bristol, BS8 1UB Bristol, UK*
[c]*École Polytechnique Fédérale de Lausanne (EPFL), 1015 Lausanne, Switzerland*
[d]*IMEC, 3001 Leuven, Belgium*
[e]*Ghent University, 9052 Gent, Belgium*

†Electronic supplementary information (ESI) available. See DOI: https://doi.org/10.1039/d3nr03429a

‡Present address: University of Sydney, 2006, NSW, Australia.

The concept of our integrated Si 4-T NEM relay is illustrated in Fig. 1a; the relay is structured on the Si device layer with surrounding metal interconnect routings and is suspended within a cavity that is created at the end of the BEOL fabrication by post-processing of the foundry wafers. This integration method enables seamless incorporation of Si NEM relays in an existing foundry platform, without the need for intricate 3D stacking or wafer bonding processes. The relay consists of four terminals: two movable beams, connected to the source (S) and the body (B) terminals, as well as fixed drain (D) and gate (G) terminals. Each terminal of the relay passes through the cavity side walls and is electrically connected to an aluminium (Al) contact pad on the chip surface through several metallization routing layers embedded in the BEOL stack. The dielectric plug (aluminium oxide, AlOx, shown in green in Fig. 1a and b) mechanically connects the two beams but electrically isolates the body and source terminals. The 4-T NEM relay is actuated by applying a voltage between the gate and body terminals, thereby inducing electrostatic attraction between them, and deflecting the mechanically connected beams of the body and source terminals to establish an electrical contact between the source and the drain terminals. A 4-T relay with a similar architecture was demonstrated by Reynolds *et al.*,[9] but their focus was on proof-of-concept of the relay principle and the resulting circuit efficiencies using larger microscale relay prototypes fabricated on an SOI wafer. Recently, we presented the fabrication of a 4-T NEM relay in the Si device layer of SOI substrate without metal interconnects.[15] In contrast, in this work we demonstrate the first nanoscale 4-T NEM relay integrated with multi-layer metal interconnects, featuring a ~10× reduction in critical dimension compared to the relays presented in ref. 9 (from 2 μm down to 200 nm). These advancements in integration and miniaturization are pivotal for the development of large-scale integrated NEM relay-based circuits. To demonstrate the viability of our 4-T NEM relays with integrated metal interconnects, we manufactured and characterized six integrated Si 4-T NEM relays with Au contacts deposited by physical vapor deposition (PVD) (see Fig. 1b for an example). We investigated the actuation behaviour of the relays by applying a voltage ramp V_G from 0 to a maximum of 20 V between the gate and body terminals, while grounding the body (*i.e.*, without body-biasing) and recorded the pull-in voltage (V_{pi}). At the same time, we applied a constant voltage of 5 V to the drain and grounded the source. Fig. 1c displays the $I_{ds} - V_{gb}$ characteristic of a typical relay actuation, measured at room temperature under dry air conditions. For this relay, we observed pull-in at 15.8 V and pull-out (V_{po}) at 12.7 V while ramping V_{gb} up and subsequently down without

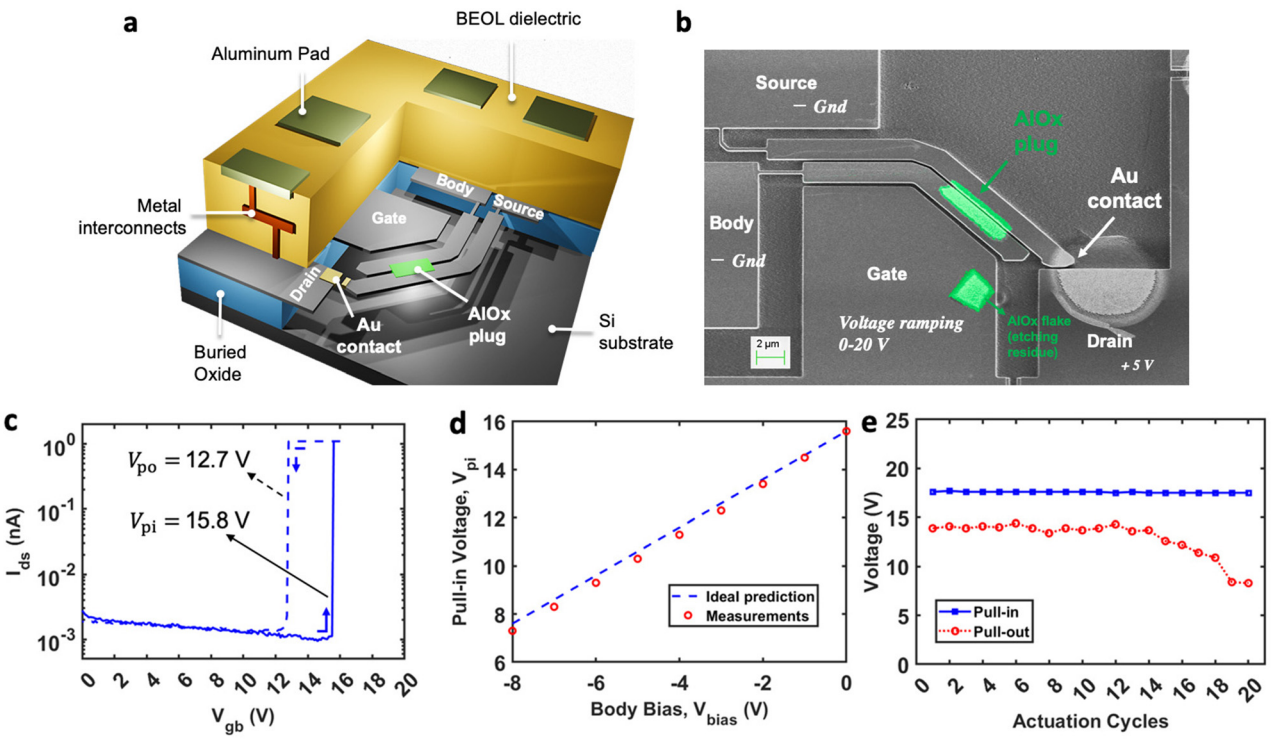

Fig. 1 (a) 3-Dimensional (3D) schematic view of the 4-T NEM relay featuring four independent terminals, integrated with metal interconnect routings in the IMEC ISiPP50G foundry platform. (b) Top-view SEM micrograph of a partially released 4-T NEM relay with an Au coated contact tip featuring an 80 nm thick Au layer on the top surface and an estimated 30–35 nm thick Au layer on the sidewalls. (c) Measured actuation of an integrated 4-T NEM relay. The abrupt drain–source current increase and decrease indicate successful pull-in and pull-out. (d) Reduction of pull-in voltage with body-biasing. (e) Characterization of pull-in and pull-out voltages during 20 hot switching cycles; the unchanging pull-in voltage shows that monocrystalline Si exhibits stable mechanical cycling, while the changing pull-out voltage is indicative of the wear of the metallic contact. In the measurements shown in (c to e), the current limit was set to 1 nA to avoid undesired stiction failures due to the softness of the Au contact.

any current flowing in the body beam, thus demonstrating the electrical isolation between the source and the body terminals effected by the AlOx plug. To further reduce V_{pi}, we then applied a negative bias voltage V_{bias} to the body electrode. As shown in Fig. 1d, when we gradually lowered V_{bias} from 0 V to −8 V in 1 V increments, the pull-in voltage V'_{pi} was reduced from 15.8 V to 7.8 V. This result successfully demonstrates functional body-biasing and matches well with the expected linear relationship in eqn (1).

$$V'_{pi} = V_{pi} + V_{bias} \quad (1)$$

Throughout the actuation process, the currents at the body terminal remained at the noise level (see Fig. S1e†), verifying that the two movable beams remained electrically isolated by the dielectric plug. We then cycled the NEM relay over 20 consecutive hot-switching cycles with a 1 nA current limit and a 5 V drain bias applied and monitored the evolution of V_{pi} and V_{po} without body-biasing. As shown in Fig. 1e, V_{pi} has a variance of ~3 mV during 20 cycles, which indicates stable pull-in behaviour of the Si NEM relay. Nonetheless, it is noteworthy that we observed a significant change of V_{po} with cycling, which most likely is a result of the deterioration of the Au contact.[20] After 20 cycles, the contact resistance of the 4-T relay increased significantly, resulting in a low drain current I_{ds}. In the six devices we measured, V_{pi} was observed to fall within a range of 16 V ± 2 V (measurement data provided in Fig. S1a–d†), which most likely was due to contact variability, requiring a degree of gate overdrive to compensate. In four of the devices the contacts became stuck on the Drain after one cycle, most likely caused by the higher currents used in these measurements, which can cause micro-welding of the Au contact. Contact degradation, manifesting as increasing resistance with cycling, and micro-welding are expected from Au contacts,[20] which was the simplest contact material available in our lab to prove the concept of our miniaturized, integrated 4-T NEM relay. For practical NEM relay utilization in low-power logic circuits, it is critical to achieve good relay contact reliability at the drain–source current of an order of 100 nA (see ESI section 1†). This cannot be easily accomplished with Au contacts,[21] and therefore requires more durable relay contact materials, such as carbon-based coatings,[22,23] hard metals such as Ti, TiN,[24] W[25] or Ru,[26–28] or metal pairs such as Au–Ru.[29] For example, it has been demonstrated that NEM relays with amorphous carbon coated contacts can switch over 100 million cycles at drain–source currents exceeding 1 μA.[22]

To enable the realization of VLSI NEM relay-based logic circuits, integrated 4-T NEM relays have to be manufacturable using high-yield, foundry-compatible processes. We structured our 4-T NEM relays and interconnects in the commercial SOI foundry process iSiPP50G offered by IMEC[18] as depicted in Fig. 2a, with a subsequent post-foundry process as shown in Fig. 2b, to realize the dielectric plugs between the body and source beams, the contact tip metallization, and the suspension of the movable beams of the 4-T NEM relays. First, the 4-T relays were patterned in foundry FEOL processing using stepper lithography on top of an SOI wafer with a 220 nm thick Si device layer and a 2 μm thick layer of buried oxide (BOX) (Fig. 2a, steps i and ii). Then, a conventional 2-layer metal interconnect stack was deposited on top (Fig. 2a, step iii). In the next step, the BEOL oxide layers above the NEM relays were opened to create a cavity and expose the devices (Fig. 2a, step iv). At this stage, the wafers were shipped out

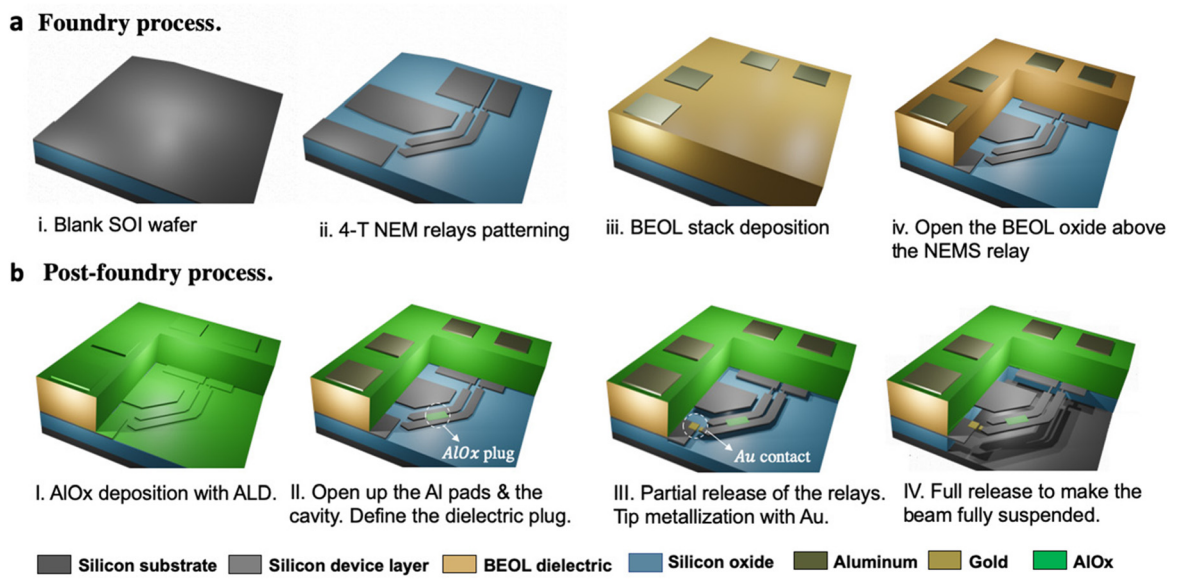

Fig. 2 (a) 3D schematic of the manufacturing process flow for the integrated 4-T NEM relays. (a) Foundry process performed in the IMEC iSiPP50G platform. (i) Blank SOI wafer; (ii) patterning of 4-T NEM relay; (iii) BEOL stack deposition; (iv) opening the BEOL oxide above the relays to define the NEM cavities. (b) Post-foundry process. (I) AlOx passivation. (II) Opening up the Al pads and the NEM cavities, and definition of the dielectric (AlOx) plugs; (III) partial release etch of the NEM relay structures and subsequent relay contact tip metallization with Au; (IV) release etch to fully suspend the source and body terminals of the relays.

from the IMEC foundry and the remaining process steps were carried out in university cleanrooms. One of the critical challenges in 4-T NEM relays is the realization of the dielectric plugs between the Body and Source beams, which we realized in post-processing steps. While the plug formation is more straightforward to establish for out-of-plane relays with layer-by-layer deposition,[2] it has never been realized for in-plane 4-T relays at the nanoscale. Here, we developed a single-lithography process to create an in-plane dielectric plug while also protecting the BEOL stack from the vapor hydrofluoric acid (vHF) that was used for the sacrificial etching to suspend the relay beam. For the dielectric plug we chose AlOx due to its good mechanical performance and electrical isolation, compatibility with existing foundry processes, and excellent resistance to vHF etching. Thus, in the post-foundry process, we first deposited a thin layer (~70 nm) of AlOx on top of the pre-fabricated foundry wafer using atomic layer deposition (ALD) (Fig. 2b, step I). Then, we patterned the AlOx layer with a standard buffered hydrofluoric acid (BHF) etching process using maskless laser lithography, to define the dielectric plug and selectively remove the AlOx in the region inside the cavities (Fig. 2b, step II). As the contact area is a critical parameter that affects surface adhesion forces, and thus V_{po}, we developed a process that allows for full (see Fig. 3a and b) or partial Au metallization (see Fig. 3c and d) of the relay tip contacts. This process uses a single photolithography lift-off process to selectively expose the pre-defined relay contact regions for the subsequent Au deposition and lift-off (Fig. 2b, step III). Finally, the NEM relay beams were fully suspended by etching the BOX below the beams using vHF at a pressure of 14 Torr (Fig. 2b, step IV). Details of the dielectric AlOx plug formation and Au contact metallization processes are provided in ESI, section 2,† and information confirming the AlOx plug integrity is provided in ESI, section 1.†

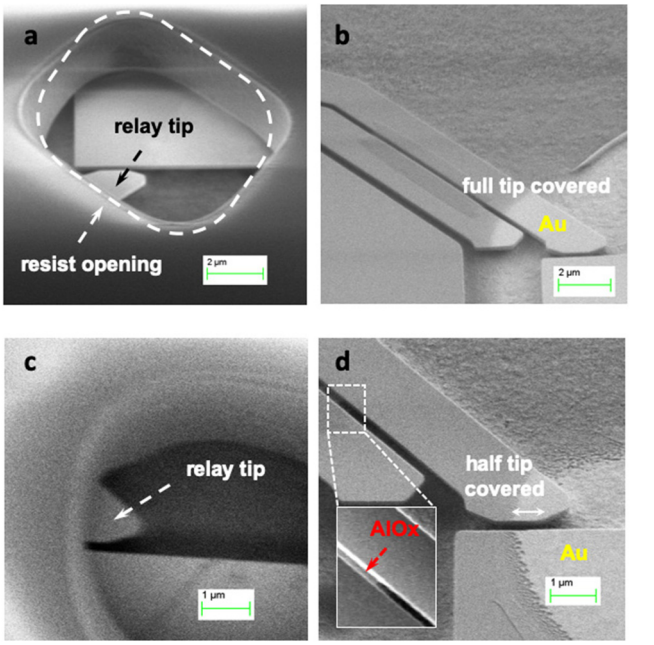

Fig. 3 (a) SEM image of the tip window opening in a photoresist lift-off mask of a relay with full contact tip metallization, implemented using maskless laser lithography. (b) SEM image of the full contact tip Au metallization of a relay after the lift-off and before the full NEM relay release. (c) SEM image of the window opening in a photoresist lift-off mask of a relay with 50% (half) contact tip metallization, implemented using direct laser writing lithography. (d) SEM image of the 50% (half) contact tip metallization of a relay after the lift-off and before the full NEM relay release. The inset shows a close-up view of a part of the AlOx plug connecting the two beams of the relay.

In designing NEM relay tip contacts, an essential parameter that affects the pull-out behaviour is the contact adhesion force (F_{adh}), which is proportional to the effective contact area[30] (A_{eff}). If F_{adh} is larger than the spring restoring force (F_k), the contact will get stuck on the Drain after pull-in, which is a common relay failure mode. To prevent this failure, F_{adh} can be lowered by reducing the effective tip contact area A_{eff}. As a proof-of-concept for this solution, we analysed the pull-in and pull-out behaviour of one of our half-tip 4-T NEM relays, as shown in Fig. 3d. This particular half-tip relay exhibited repeatable pull-in and pull-out, at 17.5 V and 14 V, respectively, measured with a 1 nA current limit (see Fig. S1c, device sw4†). These results show that the adhesion force with half contact tip Au metallization is smaller than the restorative force of the relay hinge. To better understand the impact of the contact adhesion force on the pull-out behaviour, we developed a finite-element model (FEM) of our 4-T NEM relay in Ansys using a coupled field electrostatic simulation (see ESI, section 3† for design principles and relay design parameters). First, we confirmed that the pull-in voltage of the FEM ($V_{pi,sim}$ = 17.8 V) strongly correlates with the measured actuation (V_{pi} = 17.5 V). Next, we simulated the contact adhesion force F_{adh} in the FEM model and extracted the pull-out voltage while varying F_{adh} from 0 to 140 nN, with which we generated a curve illustrating the relationship between V_{po} and F_{adh}, shown in Fig. 4a. For low F_{adh}, the relay exhibits high V_{po} and low hysteresis. However, as F_{adh} increases, V_{po} drops rapidly which leads to high hysteresis. Once the adhesion force surpasses 96 nN, the pull-out voltage drops to zero, suggesting that the relay becomes stuck on the Drain. Thus, this curve provides design insight into how the adhesion force can be optimized to ensure reliable pull-out.

Given that the measured pull-out voltage of the half-tip 4-T NEM relay is 14 V, we infer from the simulated curve that the estimated F_{adh} of this relay is approximately 34 nN. The simulated pull-in and pull-out behaviour of the half-tip NEM relay is shown in Fig. 4b. Considering the linear relationship between F_{adh} and A_{eff}, we estimated that a full-tip 4-T NEM relay should have twice the adhesion force, resulting in 68 nN. Thus, our simulation suggests that the pull-out voltage of the full-tip relay should be around 9.1 V, as shown in Fig. 4c. Finally, this simulation also allows us to extract the point of no pull-out, which is at 96 nN. Above this point the restoring spring force of the relay hinge is insufficient to overcome F_{adh} and the switch gets stuck, which is confirmed in the simulated relay behaviour in Fig. 4d.

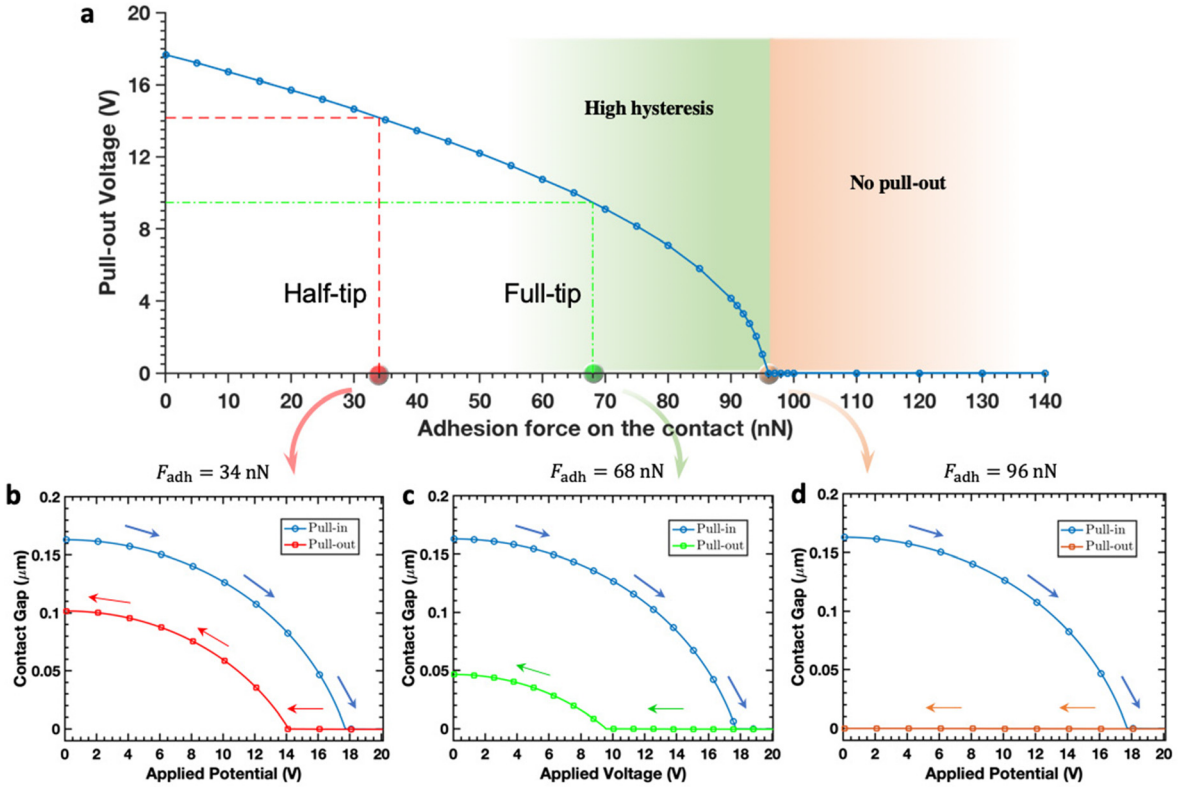

Fig. 4 Finite-element model (FEM) simulations of 4-T NEM relay. (a) Simulation of the relationship between pull-out behaviour and adhesion force. (b) FEM actuation curve of the half-tip 4-T NEM relay, with F_{adh} = 34 nN. (c) FEM actuation curve of the full-tip 4-T NEM relay, with doubled F_{adh} = 68 nN. (d) FEM actuation curve of the 4-T NEM relays in the no pull-out regime.

Thus, our simulations indicate that the 4-T NEM relays with half-tip Au metallization offers reliable pull-in and pull-out behaviour with low hysteresis, which is important for logic devices, as it reduces the noise margin between the discrete logic levels. These findings also suggest that decreasing the effective contact area A_{eff} serves as a viable strategy for reducing the hysteresis in NEM relays and enhancing their reliability. Further, the ability to carry out metallization with variable tip coverage provides an important tool to adjust the effective contact area after fabrication, based on application specific requirements. This is similar to mask-programmable circuits[31] which are prefabricated in batches and customised for different specifications by a few process steps.

Conclusions

We demonstrated the first integrated Si 4-T NEM relays fabricated in a commercial SOI foundry platform, addressing the challenges of miniaturization and integration for practical 4-T NEM circuit applications. Our innovative process for creating an in-plane dielectric plug and partial contact metallization has enabled true 4-T functionality at the nanoscale. The realized 4-T NEM relays exhibited repeatable switching behaviour and functional body-biasing, which allowed for a linear reduction in pull-in voltage. Our NEM relay integration approach allows us to seamlessly incorporate the Si NEM relays into an existing SOI foundry platform, eliminating the need for the more complex wafer bonding and layer transfer processes required for existing heterogeneous 3D integration and stacking solutions. The potential also exists to integrate transistor-based functions in the same plane (*i.e.*, in the Si device layer of the SOI substrate) as the Si NEM relays, which is not easily possible using alternative NEM relay integration approaches, and which could enable very high integration densities of transistor and NEM relay-based circuits. Although the contact reliability of the NEM relays have to be further optimized by investigating alternative contact materials, our results represent a significant milestone in the development of NEM-relay based logic circuits. By leveraging a commercial SOI foundry process and post-foundry steps compatible with wafer-level processing, we have lowered the threshold for commercialization and opened up new possibilities in the development of ultra-low power and highly integrated NEM relay-based logic circuits in the semiconductor industry.

Author contributions

Y. L., S. J. B., and F. N. conceived this work. F. N. and K. B. G. supervised the project. W. B. coordinated the MORPHIC project, built the custom design environment, conceived and

supervised the aggregation of the layouts. P. V. supervised and performed the device fabrication at IMEC. N.Q., F.N. and S. J. B. led, and A. Y. T., Y. L. and P. E. performed the development of the NEM post-processing, and characterization of the NEM devices. E. W. performed the theoretical modelling. S. J. B., E. W., M. K. K, Q. T., and D. P. designed and optimized the NEM structures, the contacts and the dielectric plug. All of the authors discussed and analysed the results. Y. L. and S. J. B. wrote the manuscript with input from all of the authors.

Conflicts of interest

The authors declare no competing financial interest.

Acknowledgements

Support from the European Union's Horizon 2020 research and innovation program under grant agreement No. 780283 (MORPHIC) and No. 871740 (ZeroAMP) is gratefully acknowledged. The authors acknowledge the support of the EPFL Center of MicroNanoTechnology (CMi) for process steps performed at EPFL.

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