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Active-matrix micro-light-emitting diode displays driven by monolithically integrated dual-gate oxide thin-film transistors

A monolithic low-temperature fabrication process was employed to integrate a-IGZO dual-gate thin-film transistor with GaN-based micro-light-emitting diode (micro-LED) to improve its stability. This process exhibited excellent device performance uniformity and reproducibility, showing promise for ultra-high-resolution displays for augmented and virtual realities and biomedical applications.





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1 Introduction

Micro-light-emitting diodes (μ LEDs) are promising as nextgeneration displays for application in augmented reality (AR) owing to their high luminous efficiency, rapid response time, high stability, and low power consumption as compared to liquid crystal and organic LED displays.^{1–7} Furthermore, there is a growing demand for ultra-high-resolution mobile displays for virtual reality (VR) and AR active-matrix μ LEDs to become thinner and more lightweight while maintaining a high pixel density.⁸ Possible driving devices for the active-matrix μ LED array include complementary metal–oxide–semiconductor field-effect transistors (MOSFETs) and thin-film transistors



Junghoon Yang, (1) ‡^a HyunWoo Park, (1) ‡^a Baul Kim, (1) ^b Yong-Hoon Cho (1) *^b and Sang-Hee Ko Park (1) *^a

We demonstrate a reliable monolithic process to fabricate micro-light-emitting diodes (µLEDs) driven by highly stable dual-gate structured amorphous indium gallium zinc oxide (a-IGZO) thin-film transistor (TFT) arrays. In contrast to the conventional µLED integration technologies that require the mass transfer of LEDs, our unique monolithic fabrication of oxide TFTs on the GaN epitaxial layer can be applied for accurate integration compared to the method of mounting discrete µLEDs on a backplane individually. To evaluate the applicability of the method at the wafer level, we introduced an atomic-layer-deposited Al₂O₃ insulator film and a denser oxide semiconductor in a dual-gate structured TFT. The induction of controlled hydrogen diffusion from the gate insulator into the active layer at low temperatures led to the good performance of the dual-gate bottom-contact (DGBC) a-IGZO TFTs under positive bias temperature stress (PBTS), negative bias illumination stress (NBIS), and negative bias temperature illumination stress (NBTIS). Monolithic integration of such μ LEDs and DGBC a-IGZO TFT arrays was achieved using an organic interlayer dielectric at a low temperature below 230 °C. This simple process exhibits excellent TFT manufacturability (stable V_{on} = 0.78 V), stability (ΔV_{on} , PBTS: 0.03 V, NBIS: -1.85 V, and NBTIS: -3.27 V), uniformity, and reproducibility (less than 4% difference in V_{on}). It shows promise for the mass production of µLED displays for flexible and/or ultra-high-resolution displays for augmented and virtual reality and biomedical applications.

(TFTs).^{9–12} Although traditional Si-based MOSFETs have been widely used because of their high package density, high readout speed, and low noise,^{13,14} the high fabrication cost and rigidity limit their application.¹⁵ Conversely, the TFT backplane offers several advantages such as a large-area process, flexibility, excellent performance, and low cost.¹⁶

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Among the various TFT backplanes, low-temperature polycrystalline silicon (LTPS) TFTs have been used in driving highresolution µLEDs. Recently, Kim et al. developed remarkably bright active-matrix µLEDs using the LTPS TFT backplane.¹⁷ A solder bump material was employed for bonding the LTPS backplane to the µLED array. However, this process may cause pressure damage and stress within the µLEDs, which results in a fracture.¹⁸ Others have successfully developed a 12.1 inch 169 ppi full-color µLED display by transferring µLEDs to the LTPS TFT backplane.¹⁹ Despite their careful integration, LTPS TFTs have inherent drawbacks in terms of power consumption and high costs.^{20,21} In contrast, amorphous oxide semiconductor TFTs with high mobility, stability, and uniformity can also drive µLEDs with a high pixel density.^{22,23} Recently, Sun et al. developed a 4 inch full-color µLED display based on indium gallium zinc oxide (IGZO) TFTs.²⁴ The mass transfer was used

^a Department of Materials Science and Engineering, Korea Advanced Institute of Science and Technology (KAIST), 291 Daehak-ro, Yuseong-gu, Daejeon 34141, Republic of Korea. E-mail: shkp@kaist.ac.kr

^b Department of Physics and KI for the NanoCentury, Korea Advanced Institute of Science and Technology (KAIST), 291 Daehak-ro, Yuseong-gu, Daejeon 34141, Republic of Korea. E-mail: yhc@kaist.ac.kr

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[‡] These authors contributed equally.

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to integrate more than 170 000 flip-chip RGB μ LEDs on the IGZO TFT backplane. However, the transfer of LEDs is associated with yield issues, and the mass transfer is not yet commercially viable, particularly for a high-resolution display with a small pixel pitch. Additionally, a lower yield during transfer significantly affects the performance of the μ LED display. Therefore, it is necessary to integrate the TFT array monolithically into the μ LED array.

However, this limits the process temperature for the oxide TFT array because the planarization of the μ LED array is achieved by a photo-patternable organic polymer. Therefore, oxide TFT arrays should be fabricated on top of the μ LED array at a low temperature in order to secure the properties of the planarization material. In general, the defects in the oxide semiconductor and/or the interface between the active layer and the gate insulator (GI) can be minimized by semiconductor densification and defect passivation during the annealing process over 300 °C.^{25–28} Moreover, the instability of oxide TFTs under electrical bias, light, and temperature is a critical hurdle against the commercialization of current driven displays such as μ LEDs. Based on this viewpoint, it is essential to develop a highly reliable oxide TFT on a μ LED array at low temperatures for monolithic integration.

Herein, we describe the first monolithic fabrication of amorphous (a)-IGZO TFTs on a GaN-based µLED array. Our fabrication method could be achieved by introducing an a-IGZO channel with a high film density and atomic-layer-deposited dielectric layers in a dual-gate TFT structure to eliminate the charge trapping defects within the active bulk and/or the interface between the active layer and GI. In addition, the opaque bottom gate of our dual-gate TFT can block the light of top-emission µLEDs, securing the light stability of a-IGZO TFTs during the operation. Through this process, we obtained highly stable a-IGZO TFTs under positive bias temperature stress (PBTS), negative bias illumination stress (NBIS), and negative bias temperature illumination stress (NBTIS) environments. We demonstrated the excellent stability of lowtemperature a-IGZO TFTs and its correlation with defects through various thin-film analyses. On the basis of these characteristics, it has been verified that a multigate transistor is also capable of performing reliable logic and synopsis operations by controlling the gate voltage.²⁹ This unique monolithic fabrication method of the oxide TFT array provides the groundwork for fabricating large-area, high-resolution, and highly stable µLED displays at low cost.

2 Experimental

2.1 Preparation of pixelated µLED arrays

Fig. 1 shows a schematic image of the monolithic dual-gate a-IGZO TFT and materials for each layer. The growth and fabrication of GaN-based blue μ LEDs were conducted as follows: the 1.5 μ m-thick undoped GaN, 2.4 μ m-thick n-type GaN, 250 nm-thick InGaN/GaN superlattice, 50 nm-thick InGaN/GaN multi-quantum well, 30 nm-thick AlGaN electron-blocking

	Top Gate							
Act	/D TGI	Act						
Bottom Gate	BGI	Bottom Gate						
	Buffer oxide							
p-GaN								
Multi Quantum Well								
n-GaN								
Layer	Material	Thickness						
Top Gate	Мо	80 nm						
Top Gate Insulator (TGI)	Al ₂ O ₃	75 nm						
Protection Layer (PL)	Al ₂ O ₃	10 nm						
Active	a-IGZO (In:Ga:Zn = 1:1:2.5)	20 nm						
Source / Drain (S/D)	ITO	150 nm						
Jource / Drain (5/D)								
Bottom-Gate Insulator (BGI)	Al ₂ O ₃	40 nm						
Bottom-Gate Insulator (BGI) Bottom Gate (Light-blocking-layer)	Al ₂ O ₃ Mo	40 nm 80 nm						
Bottom-Gate Insulator (BGI) Bottom Gate (Light-blocking-layer) Buffer oxide	Al ₂ O ₃ Mo Al ₂ O ₃	40 nm 80 nm 20 nm						

Fig. 1 A schematic image of a monolithic dual-gate amorphous indium gallium zinc oxide (a-IGZO) thin-film transistor (TFT) and materials for each layer.

layer, and 250 nm-thick p-GaN were epitaxially grown on sapphire substrates *via* metal–organic chemical vapor deposition. The blue LEDs were pixelated by inductively coupled plasma-reactive ion etching. Next, 100 nm-thick indium-tin oxide (ITO) as the electron spread layer was deposited using an e-beam evaporator and subjected to rapid thermal annealing. The remaining layers were coated with an organic interlayer dielectric (ILD; DW-10; a negative photoresist) to ensure smooth surface morphology and planarization. The organic ILD was patterned to create holes that facilitated the subsequent connection with the a-IGZO TFT arrays.

2.2 Fabrication of the dual-gate bottom-contact (DGBC) a-IGZO TFT array on the planarized µLED arrays

A 20 nm-thick Al₂O₃ buffer oxide layer was deposited via thermal atomic layer deposition (T-ALD) using the tri-methyl aluminum (TMA) precursor and water at 150 °C on the planarization layer to ensure that water and hydrogen from the ILD could not reach a-IGZO TFTs. The bottom gate (80 nm-thick Mo), also acting as a light-blocking layer, was deposited via direct current (DC) sputtering at 5 mTorr and 200 W. The lightblocking layer was photoetched. A 40 nm-thick Al₂O₃ bottomgate insulator (BGI) was deposited via T-ALD using TMA and water at 150 °C. The BGI was then etched (using the buffer oxide etchant, BOE) in order to expose the electrode. Subsequently, a 150 nm-thick ITO source/drain (S/D) electrode was deposited via DC sputtering. Heat treatment at 230 °C for 2 h in vacuo was performed to ensure a uniform clean-etch profile. The ITO film was patterned using a poly-ITO etchant. A 20 nmthick a-IGZO layer was deposited via radiofrequency sputtering

at room temperature (15 to 25 °C), with a partial pressure of 30% $P_{\rm O2}$ and 70% $P_{\rm Ar}$ at 0.075 Pa; the metal cation ratio was 1:1:2.5 (In:Ga:Zn).³⁰ A 10 nm-thick-Al₂O₃ protection layer (PL), which suppresses the formation of defects within the active layer during the patterning process,³¹ was deposited at 150 °C via T-ALD using water as the oxidant. The a-IGZO layer and PL were simultaneously patterned using 49% (v/v) HF diluted in 100:1. The top gate insulator (TGI) of the 75 nmthick Al₂O₃ layer was deposited at 150 °C via T-ALD and patterned using BOE. The 80 nm-thick Mo top gate electrode was deposited via DC sputtering under 5 mTorr of Ar at 200 W. The Mo layer was patterned via wet etching. Finally, the device was heat-treated for 2 h in vacuo at 230 °C. The subpixels of the fabricated monolithic µLEDs were observed via focused ion beam scanning electron microscopy (FIB-SEM; Helios Nanolab 600).

2.3 Electrical characterization

Transfer and output curves were obtained using an HP4156A analyzer; the relevant parameters were extracted from the transfer curves. The measured channel width/length of all TFTs was 20 μ m/20 μ m. The gate voltage sweep range for the transfer curves was -15 to 20 V, in steps of 250 mV. The drain voltages were 0.1 and 10 V, and the drain voltage sweep range for the output curve was -2 V to 20 V, in steps of 500 mV. The gate voltage range was -5 to 20 V, in steps of 5 V. The TFT PBTS transfer curves were obtained at a voltage stress of 1 MV cm⁻¹ and a temperature stress of 60 $^\circ C$ over 10 000 s. The TFT NBIS transfer curves were obtained at a voltage stress of 1 MV cm⁻¹ under a white light stress of 0.5 mW cm^{-2} over 10000 s. The TFT NBTIS transfer curves were obtained at a voltage stress of 1 MV cm⁻¹, a temperature stress of 60 °C, and a white light stress of 0.5 mW cm⁻² over 10 000 s. The device was operated under ambient environmental conditions (27.5 °C, 34% humidity).

3 Results and discussion

In this paper, the performance of a-IGZO TFTs including both top-gate bottom-contact (TGBC) and DGBC architectures was evaluated, in which T-ALD Al₂O₃ and sputtered Mo were adopted as the dielectric and gate layers, respectively. Both structures of TFTs were fabricated on top of the µLED array, which was formed on a sapphire substrate. More importantly, it is essential to minimize the charge trapping defect such as oxygen interstitials (O_i) and maximize the density of the oxide semiconductor film to obtain highly stable a-IGZO TFTs in the low-temperature process.³² In particular, the film density of an active layer significantly changes according to the postannealing process.33 This change in density is mainly attributed to the structural relaxation or rearrangement of the matrix by thermal energy.³⁴ Therefore, we evaluated the morphology and density of the a-IGZO active layers annealed at different temperatures. As shown in Fig. S1 (ESI[†]), atomic force microscopy revealed no significant effect of annealing temperature on the surface roughness of the a-IGZO thin films. For a

detailed analysis, we subjected the samples to X-ray reflectometry (XRR) to explore the density of the thin films. The density of the a-IGZO thin films was obtained from the critical angle (θ_c) of the XRR curve, where reflectivity decreased rapidly. Thus, the difference in the density values was only 0.035 g cm⁻³ between an as-fabricated sample and a 300 °C annealed sample (Fig. S2, ESI†). These results reveal that our a-IGZO films have a sufficient film density without additional heat treatment after the deposition. Because the sputtering pressure was very low at 0.075 Pa during the deposition, we could obtain an a-IGZO thin film with sufficient density and roughness in a pristine state.³⁵ Thus, these a-IGZO films deposited at low pressure can be applied to fabricate a highly stable oxide TFT even at a low temperature.

Subsequently, we investigated the effect of the active layer/ insulator interface on electrical properties. Generally, it is crucial to control the defects within the active layer itself and the interface traps between the active layer and GI for the excellent reliability of oxide TFTs.36,37 We fabricated TGBC TFTs with stack structures similar to those of self-aligned TFTs, which are advantageous for large-sized and high-resolution displays.³⁸ Additionally, we applied the ALD-Al₂O₃ insulator film to both PLs and GIs because of its high quality even when deposited at a low temperature.^{39,40} The details of the fabrication method of TGBC TFTs are described in the ESI.† To identify the optimized characteristics of TFTs in terms of $V_{\rm op}$, mobility, and stability, we fabricated TGBC a-IGZO TFTs by applying two different Al₂O₃ deposition methods [T-ALD and plasma-enhanced ALD (PE-ALD)] to the PL and GI. Initially, we fabricated each pair of TGBC TFTs to determine the suitable deposition method for the monolithic TFT fabrication. All four samples were annealed in vacuo at 230 °C for 2 h.

Fig. 2(a-d) show the transfer curves of a-IGZO TGBC TFTs at drain voltages of 0.1 and 10 V prepared using (a) T-ALD/T-ALD, (b) PE-ALD/T-ALD, (c) T-ALD/PE-ALD, and (d) PE-ALD/PE-ALD for PL/GI deposition. We used a thin PL (first GI) to protect the active a-IGZO layer because the 1:1:2.5 ratio of the a-IGZO film is vulnerable to the acid during the etching process.⁴¹ Fig. 2(e)illustrates that the hysteresis of each TFT [(a-d)] is 0.25, 5.75, 0.75, and 16.5 V, and the linear mobilities are 20.31, 4.47, 25.31, and 0.97 cm^2 V⁻¹ s⁻¹, respectively. When PE-ALD PLs were used, the hysteresis was higher and the linear mobility was lower than those of TFTs adopting T-ALD PLs. While the PE-ALD process suppressed the generation of the shallow donor of oxygen vacancies in the active layer, it yielded charge trapping centers in both the active layer and the interface between the active layer and the GI compared with T-ALD.42 These differences are ascribed to two different oxidants: water and oxygen plasma. Oxygen plasma collisions create Oi-related states, which act as electron acceptor-like traps, thereby decreasing the electron mobility and increasing the hysteresis by capturing free electrons in the a-IGZO active layer and/or the interface between the active layer and GI.^{43,44} The transfer characteristics of TFTs using the PE-ALD method represented a higher hysteresis compared to the T-ALD method. Furthermore, the Al₂O₃ film deposited by PEALD did not contain enough H to be



Fig. 2 Transfer curves of a-IGZO TGBC TFTs prepared using (a) T-ALD/T-ALD, (b) PE-ALD/T-ALD, (c) T-ALD/PE-ALD, and (d) PE-ALD/PE-ALD for PL/GI Al₂O₃ deposition. (e) Hysteresis and linear mobility values of various a-IGZO TFTs.

diffused from the active layer into the GI. This can leave the charge trapping centers generated by oxygen plasma incompletely passivated, yielding hysteresis [Fig. 2(b-d)]. Conversely, the device that applied the T-ALD-Al₂O₃ insulator film to both the GI and PL showed the best electrical performance by suppressing the formation of charge trapping centers at the active/ insulator interface [Fig. 2(a)].⁴⁵ Therefore, we concluded that using a T-ALD-Al₂O₃ insulator film is preferable for fabricating highly stable oxide TFTs at low temperatures.

The delicate control of the deposition temperature of GI is a crucial factor in securing the high stability of the metal-oxide transistor.46 For more detailed optimization, we manufactured another TGBC a-IGZO TFT by changing the deposition temperature of GI to 200 °C. Hence, we fabricated a second device (device B, PL: 150 °C and GI: 200 °C) wherein the turn-on voltage was shifted by 1.14 V after the PBTS measurements, which was larger than the shift of the turn-on voltage of device A (0.35 V) [Fig. 3(a)]. According to the secondary-ion mass spectrometry (SIMS) analysis, the amounts of hydrogen and hydroxyl at the PL/GI interface were lower in device B than those in device A [Fig. 3(d and e)]. In general, ALD at a higher growth temperature lowers the amount of residual hydrogen in the films due to the complete removal of the hydroxyl groups during the surface reaction.⁴⁶ However, the amount of hydrogen in the active layer/PL interface was similar for devices A and B. Because ALD-Al₂O₃ is an excellent hydrogen barrier,⁴⁷ the temperature for the GI deposition on the top of the PL does not affect the TFT instability directly. However, in contrast to the structure of thin films for SIMS analysis, in which a-IGZO was

completely covered with the Al_2O_3 PL, the contact between the GI of the TFT and the side edge of the exposed a-IGZO was noticeable despite the presence of the PL. Therefore, hydrogen can diffuse toward the active layer/GI interface *via* these contact areas to affect the reliability. These careful analyses confirmed that the increased hydrogen levels within the PL and GI were associated with improved PBTS stability. Therefore, we selected the structure of device A with good PBTS stability for fabricating monolithic oxide TFTs on the µLED array.

Before fabricating the monolithic µLEDs, we investigated the electrical properties of the a-IGZO TGBC TFTs of device A under various environments (Fig. S3, ESI⁺). Although the subthreshold swing, turn-on voltage, uniformity, and hysteresis values were excellent, the output characteristics showed that the drain current was not saturated at a high drain voltage. As the current saturation characteristics of TFTs have important effects on driving the µLEDs with constant luminance,⁴⁸ the driving TFTs must have a saturation drain current at a specific drain voltage. In addition, the turn-on-voltage shift was -7.07 V during the NBIS stability measurements over 10000 s at -1 MV cm⁻¹ and 0.5 mW cm⁻² white light stress. Because the NBIS measurement environment corresponds to the major operation state of the µLED display,⁴⁹ these unfavorable NBIS characteristics should also be addressed. Generally, the deterioration in NBIS stability originates from hydrogen impurities or ionized oxygen vacancies in metal-oxide semiconductors.47 In addition, the subgap density-of-states caused by the metalhydrogen bonds or non-bridging oxygen hole centers can



Fig. 3 (a) V_{on} shifts according to the GI growth temperature. PBTS stability of TGBC a-IGZO TFTs with GI Al₂O₃ deposited at (b) 150 °C and (c) 200 °C. (d) Hydrogen and (e) hydroxyl group peaks dictated from SIMS analysis.



Fig. 4 (a and e) The transfer curve, (b and f) output curve, (c and g) PBTS stability (60 $^{\circ}$ C, 10 000 s, 1 MV cm⁻¹), and (d and h) schematics of the DGBC a-IGZO TFT in the absence and presence of a ground voltage at the bottom gate, respectively.

degrade the stability of NBIS.^{49,50} In our results, the NBTIS characteristics were poor compared to those of NBIS due to the trapping of the ionized oxygen vacancies into the defects of Al–OH or Si–OH in the gate insulator by light and thermal stress.⁵¹ Hence, to overcome these drawbacks, we inserted opaque light-blocking layers (Mo bottom gate) in the dual-gate structure.⁵²

Fig. 4(a-d) illustrates the results of a DGBC a-IGZO TFT without applying any bottom-gate voltage, while Fig. 4(e-h) shows the corresponding results in the presence of a ground bottom-gate voltage. As shown in Fig. 4, various improved electrical properties were obtained simultaneously after a ground voltage was applied to the bottom gate. First, the ground voltage of the bottom gate rendered the turn-on voltage of the DGBC TFTs consistent regardless of the applied drain voltage [Fig. 4(a and e)]. Second, the saturated drain current was achieved, as identified from the output curves [Fig. 4(b and f)]. Third, the enhanced PBTS characteristics were also obtained; the turn-on-voltage shift during PBTS decreased from 1.16 V to 0.10 V [Fig. 4(c and g)]. These phenomena could be explained by the schematics in Fig. 4(d and h). The Von shift is caused by the electron accumulation or depletion after application of the bottom gate voltage (V_{BG}), in which a negative V_{BG} generates a positive shift and a positive V_{BG} induces a negative shift [Fig. S4, ESI[†]].⁵³ This shift can also be affected by introducing impurities serving as carriers, such as hydrogen. However, T-ALD Al₂O₃ used as the buffer oxide plays as an effective barrier, preventing impurities from entering the active interface layer. Therefore, the impact of these impurities can be effectively reduced.47 In the absence of electrical voltage with the bottom gate, the electric field caused by the drain voltage was transferred to that bottom gate. Thus, a backchannel in the a-IGZO active layer was induced close to the bottom gate. This induced backchannel can shift the turn-on voltage in a negative

direction as the drain voltage increases. Furthermore, because the backchannel current can be increased as the drain voltage increases, it is difficult to gain drain saturation current characteristics in an output curve. Simultaneously, from the viewpoint of electrical stability, this backchannel surface serves as a charge trapping site at the active layer/BGI interface, thereby deteriorating the stability of PBTS.⁵⁴ In contrast, when the ground voltage is applied to the bottom gate, the problems mentioned above are solved as the channel is formed only in the a-IGZO region close to TGI [Fig. 4(d and h)]. Indeed, the DGBC TFTs exhibited outstanding electrical properties, including low hysteresis, hard-saturation characteristics, and good PBTS stability, when a ground voltage was applied.

The PBTS stability of DGBC a-IGZO TFTs was measured over 10000 s at 60 °C and 1 MV cm⁻¹ according to the BGI deposition temperatures (150 °C, 200 °C, and 300 °C) to clarify the effect of the deposition temperature of the BGI on the electrical reliability (Fig. S5, ESI⁺). The amount of hydrogen in the GI can improve the PBTS stability by diffusing to the a-IGZO/GI interface. Similarly, the amount of hydrogen in the BGI positively influences the improvement of PBTS stability, supported by the SIMS data (Fig. S5, ESI[†]). As the deposition temperature of the BGI decreased, more amount of hydrogen was detected in the channel. Consequently, the BGI deposited at low temperatures contained more hydrogen, thereby enhancing the PBTS stability. These results suggest that our BGI films deposited at low temperatures are suitable for fabricating highly stable DGBC TFTs. Thus, high-performance DGBC TFTs can be fabricated using the Al₂O₃ BGI deposited at 150 °C.

To monolithically integrate the optimized DGBC TFTs on the μ LED array, a thick photo-patternable insulating layer is required to planarize the pixelated μ LEDs. Therefore, an organic ILD (a negative photoresist, DW-10) was introduced,



Fig. 5 (a) Transfer curves and mobility parameters, (b) output curves, (c) PBTS stability (60 °C, 10 000 s, 1 MV cm⁻¹), (d) NBIS stability (0.5 mW cm⁻² white light, 10 000 s, -1 MV cm⁻¹), and (e) NBTIS stability (60 °C, 0.5 mW cm⁻² white light, 10 000 s, -1 MV cm⁻¹) of DGBC a-IGZO TFTs with an organic ILD layer between the substrate and the buffer oxide.

which was spin-coated and patterned *via* conventional photolithography. Because the ILD layer can withstand temperatures up to 230 °C, the μ LEDs and oxide TFTs can be sufficiently integrated at this low temperature *via* monolithic fabrication. In order to prevent the diffusion of hydrogen and water vapor from ILD, an extra layer of T-ALD Al₂O₃ buffer oxide was applied.^{47,55} Additional experiments were also conducted to explore the extent to which the ILD will affect the TFT performance; we deliberately omitted the ILD in the DGBC TFT structure.

Fig. S6 (ESI[†]) shows the TFT transfer, output curves, and stability (PBTS, NBIS, and NBTIS) of DGBC a-IGZO TFTs without the ILD layer; Fig. 5 illustrates the corresponding data for the device with the ILD layer. Comparing both results, the ILD did not degrade the TFT performance owing to the excellent barrier properties exhibited by the Al₂O₃ buffer layer.⁴⁷ In addition, Fig. S7-S11 (ESI[†]) depict the uniformity of device performance within a batch and between batches. The performance of devices was found to be highly consistent among testing samples from batch to batch regardless of the device location on the substrate. These results indicate that the monolithic fabrication reported in this article shows great reproducibility and reliability. Finally, we integrated DGBC TFT arrays on µLEDs via monolithic fabrication. Fig. 6(a and b) show the subpixel layouts of the µLED and TFT arrays and the FIB-SEM images of the sub-pixel surface, respectively. Remarkably, the device fabrication proceeded as designed. In



Fig. 6 (a) The subpixel layouts of the μ LED and DGBC TFT arrays. (b) FIB-SEM image of the surface subpixels. (c) Image of the operation of μ LED and DGBC TFT arrays when both of the arrays were turned on.

contrast to the existing inorganic ILD materials, which may contain numerous voids at low temperatures, our organic ILD (DW-10) processed by spin coating provides several merits such Table 1 Main set of achievements including our work and previous studies in the µLED field in terms of optoelectronics and microelectronics

Novelty	Driving devices	Integration method	LED	LED/driving cir- cuit fabrication substrate	TFT structure	Bonding material	TFT process temperature	Year/ ref.
Active-matrix (AM) driving: 8×8	PMOS	Flip-chip	GaN-µLED	Sapphire/silicon	—	Solder bump		2009/ 12
High-brightness (10 ⁶ cd m ⁻²)	CMOS	Flip-chip	GaN-µLED	Sapphire/silicon	—	Bump- bonded (Au)	_	2015/ 9
High-brightness (40 000 cd m ⁻²), AM driving	LTPS TFT	Flip-chip	GaN-µLED	Sapphire/glass	Conventional coplanar	Mo-Au layer	\sim 450 °C	2018/ 17
2D materials (transpar- ent conducting film/ channel)	Graphene FET	Monolithic with the use of the graphene transfer method	GaN-µLED	Sapphire	Bottom-gate bottom- contact	No information	No information	2019/ 11
Large scale (12.1 inches), full-color	LTPS TFT	Mass transfer	µLED with color conversion materials	Glass	No information	No information	\sim 450 °C	2019/ 19
Large scale (4 inches), full-color	a-IGZO TFT	Mass transfer	μLED	Glass	Conventional coplanar	Solder bump	No information	2020/ 24
Real-monolithic, highly-stable TFT (also AM driving)	a-IGZO TFT	Monolithic	GaN-µLED	Sapphire	Dual-gate	Organic inter-layer dielectric	Below 230 °C	This work

as rapid processability, inexpensive production cost, and no requirement for additional planarization.

Fig. 6(c) illustrates an operational image of the µLED driven by DGBC TFT arrays. The scan line was swept from -15 to 20 V to ensure the proper performance of the TFT array; the data line, V_{DD}, and V_{Ground} were 3.5, 5, and 0 V, respectively. As shown in Fig. 6(c), the phrase "KAIST 70 ppi" can be visualized, indicating that our unique methodology can achieve adequate monolithic fabrication of highly stable oxide TFTs on µLEDs under low temperature process conditions, compared to other previous achievements (Table 1). The thickness of the organic ILD on the µLEDs and unetched n-GaN was approximately 1.11 and 2.00 µm, respectively (Fig. S12, ESI⁺). This difference is considered reasonable as the µLED layer thickness is approximately 900 nm.

4 Conclusions

Our present study is the first to report reliable and lowtemperature (below 230 °C) monolithic integration of activematrix-µLED displays. A dual-gate a-IGZO TFT array controls the µLED displays to exhibit excellent electrical stability under the PBTS, NBIS, and NBTIS environments. In addition, this integration has been demonstrated to result in the development of superior TFTs, including reproducibility and reliability, which are crucial characteristics for future mass production in display technology. Comprehensive analyses of the electrical, structural, and chemical properties revealed that the deposited ALD-Al₂O₃ films had crucial roles in terms of high-quality dielectric properties and passivation of defects within the a-IGZO active layer/insulator interface by hydrogen. Our organic ILD ensures reliable interconnections by the excellent gapfilling and planarization properties, even at low temperatures, thus successfully creating the phrase "KAIST 70 ppi" from the active-matrix-µLED array. We believe that our method can be embedded in applications related to VR, AR, and biomedical sensors. Furthermore, in large-area high-resolution µLED displays, our novel monolithic method will be the cornerstone of mass production with low production costs.

Author contributions

Junghoon Yang: conceptualization, data curation, formal analysis, funding acquisition, visualization, validation, writing original draft, and writing - review and editing. HyunWoo Park: investigation, methodology, software, and writing - original draft. Baul Kim: investigation and resources, Yong-Hoon Cho: conceptualization, writing - review and editing, and supervision. Sang-Hee Ko Park: project administration, supervision, and writing - review and editing.

Conflicts of interest

There are no conflicts to declare.

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